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FAIRCHILD SEMICONDUCTOR®

December 2013

FQN1N50C

N-Channel QFET® MOSFET

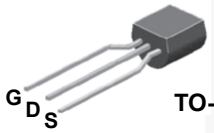
500 V, 0.38 A, 6 Ω

Description

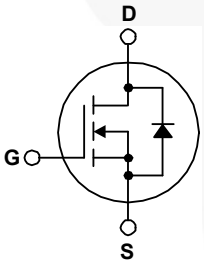
This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

Features

- 0.38 A, 500 V, $R_{DS(on)}$ = 6 Ω (Max.) @ V_{GS} = 10 V, I_D = 0.19 A
- Low Gate Charge (Typ. 4.9 nC)
- Low Crss (Typ. 4.1 pF)
- 100% Avalanche Tested



TO-92



Absolute Maximum Ratings

T_C = 25°C unless otherwise noted.

Symbol	Parameter			FQN1N50CTA	Unit
V_{DSS}	Drain-Source Voltage			500	V
I_D	Drain Current	- Continuous (T_C = 25°C)		0.38	A
		- Continuous (T_C = 100°C)		0.24	A
I_{DM}	Drain Current	- Pulsed	(Note 1)	3.04	A
V_{GSS}	Gate-Source Voltage			± 30	V
E_{AS}	Single Pulsed Avalanche Energy		(Note 2)	44.4	mJ
I_{AR}	Avalanche Current		(Note 1)	0.38	A
E_{AR}	Repetitive Avalanche Energy		(Note 1)	0.21	mJ
dv/dt	Peak Diode Recovery dv/dt		(Note 3)	4.5	V/ns
P_D	Power Dissipation (T_A = 25°C)			0.89	W
	Power Dissipation (T_L = 25°C)			2.08	W
	- Derate above 25°C			0.017	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range			-55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds.			300	°C

Thermal Characteristics

Symbol	Parameter		FQN1N50CTA	Unit
$R_{\theta JL}$	Thermal Resistance, Junction-to-Lead, Max.	(Note 5a)	60	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	(Note 5b)	140	

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Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQN1N50CTA	1N50C	TO-92	AMMO	N/A	N/A	2000 units

Electrical Characteristics T_C = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	500	--	--	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	--	0.5	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 500 V, V_{GS} = 0 V	--	--	50	μA
		V_{DS} = 400 V, T_C = 125°C	--	--	250	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30 V, V_{DS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 0.19 A	--	4.6	6.0	Ω
g_{FS}	Forward Transconductance	V_{DS} = 40 V, I_D = 0.19A	--	0.6	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	150	195	pF
C_{oss}	Output Capacitance		--	28	40	pF
C_{rss}	Reverse Transfer Capacitance		--	4.1	--	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 250 V, I_D = 1.0 A, R_G = 25 Ω (Note 4)	--	10	30	ns
t_r	Turn-On Rise Time		--	10	30	ns
$t_{d(off)}$	Turn-Off Delay Time		--	20	50	ns
t_f	Turn-Off Fall Time		--	15	40	ns
Q_g	Total Gate Charge	V_{DS} = 400 V, I_D = 1.0 A, V_{GS} = 10 V (Note 4)	--	4.9	6.4	nC
Q_{gs}	Gate-Source Charge		--	0.66	--	nC
Q_{gd}	Gate-Drain Charge		--	2.9	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	0.38	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	3.04	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 0.38 A	--	--	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 1.0 A, dI_F / dt = 100 A/μs	--	188	--	ns
Q_{rr}	Reverse Recovery Charge		--	0.55	--	μC

Notes:

1. Repetitive rating : pulse-width limited by maximum junction temperature.
2. L = 80 mH, I_{AS} = 1.0 A, V_{DD} = 50 V, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 0.38 A, di/dt ≤ 200 A/μs, V_{DD} ≤ $BV_{DSS,}$ starting T_J = 25°C.
4. Essentially independent of operating temperature.
5. a) Reference point of the $R_{\theta JL}$ is the drain lead.
   b) When mounted on 3"x4.5" FR-4 PCB without any pad copper in a still air environment
   ($R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance. $R_{\theta CA}$ is determined by the user's board design)

Typical Performance Characteristics

Figure 1. On-Region Characteristics

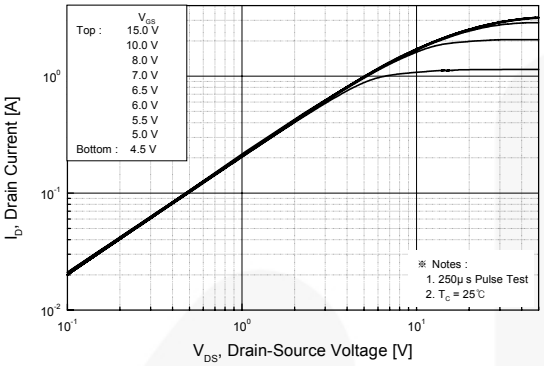


Figure 2. Transfer Characteristics

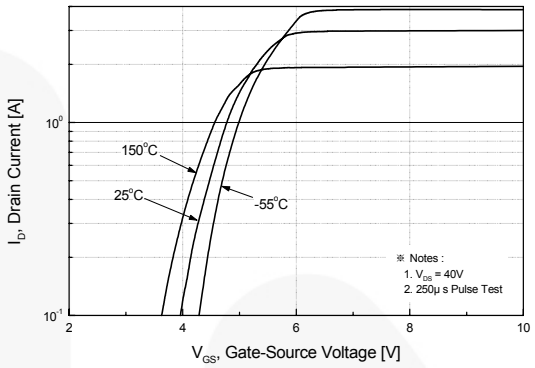


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

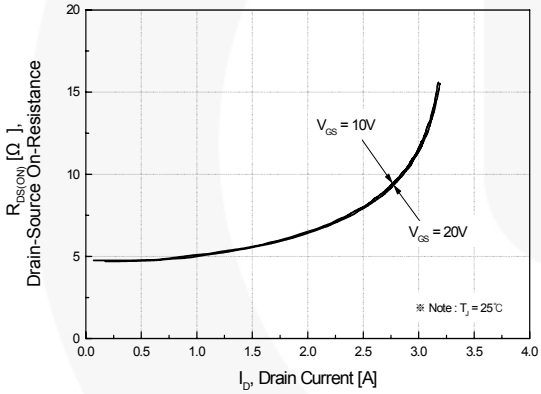


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperatue

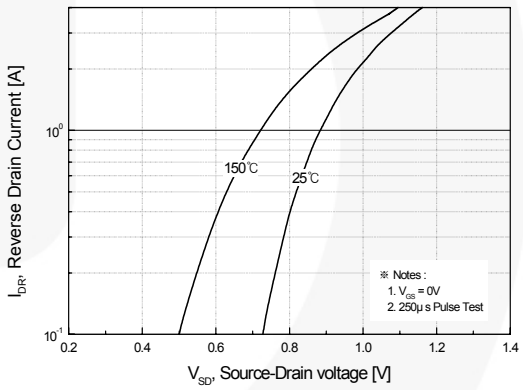


Figure 5. Capacitance Characteristics

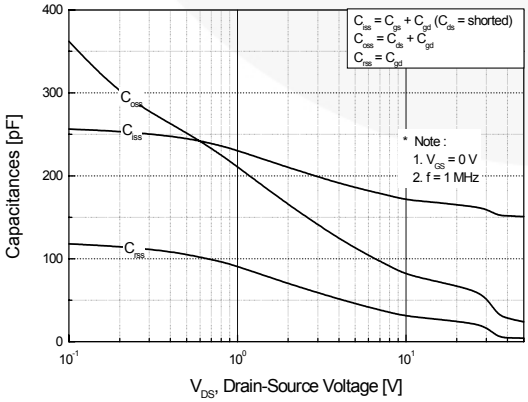
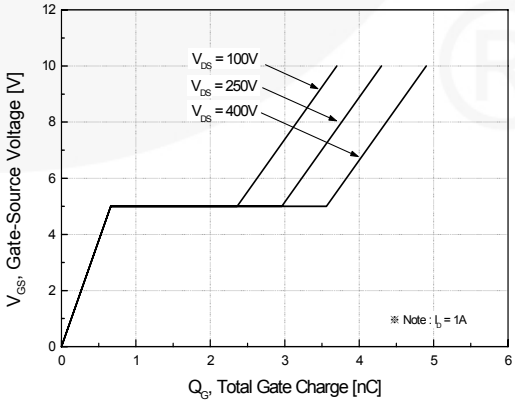


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

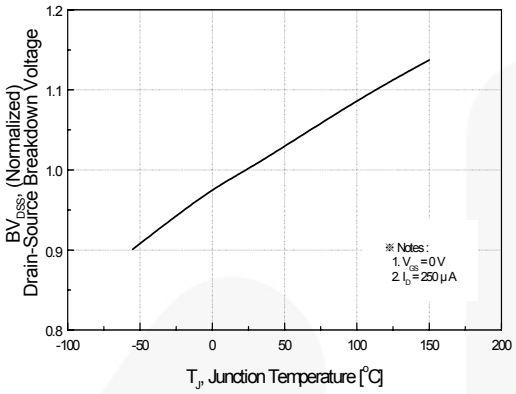


Figure 8. On-Resistance Variation vs. Temperature

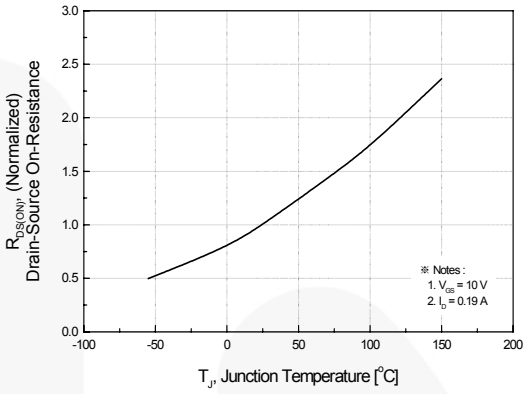


Figure 9. Maximum Safe Operating Area

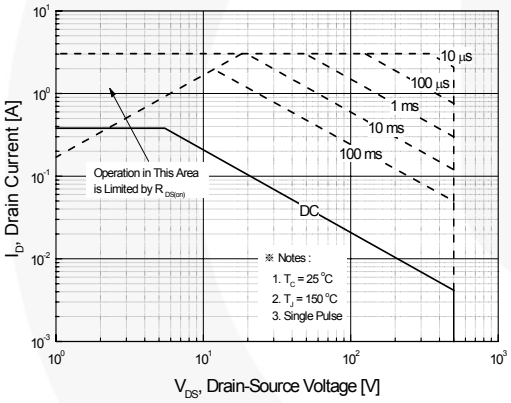


Figure 10. Maximum Drain Current vs. Case Temperature

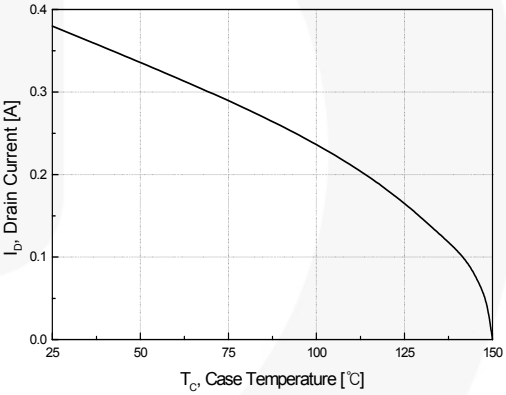
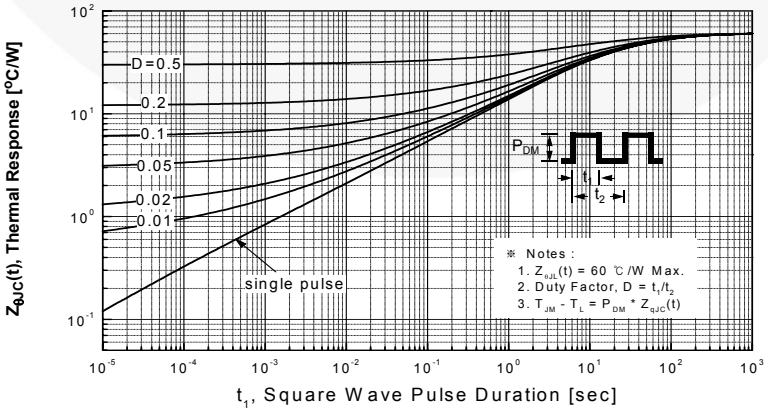


Figure 11. Transient Thermal Response Curve



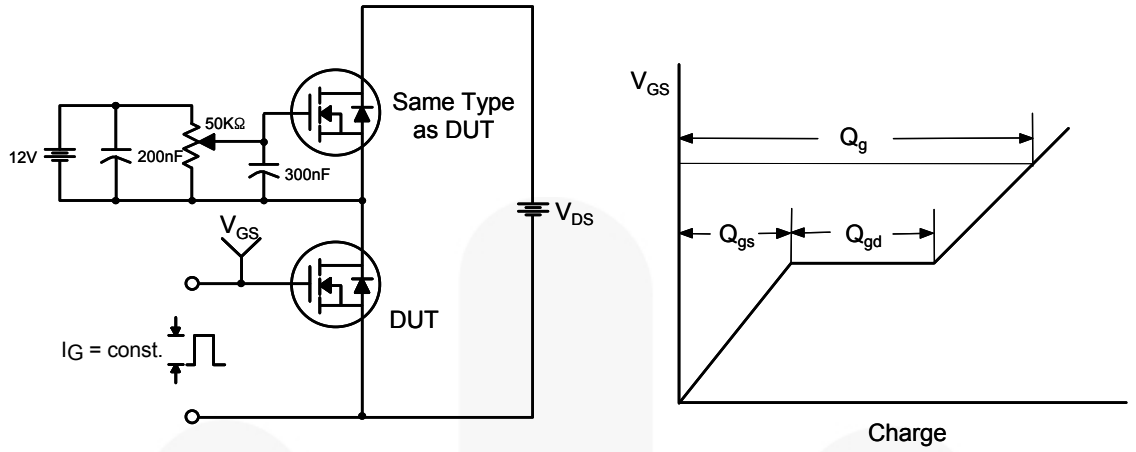


Figure 12. Gate Charge Test Circuit & Waveform

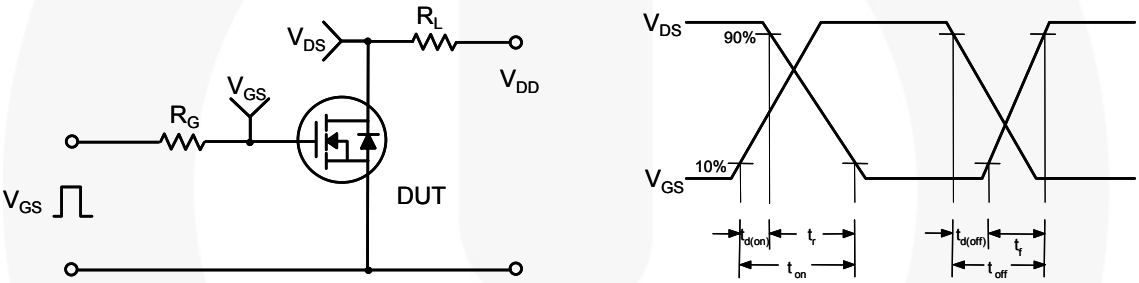


Figure 13. Resistive Switching Test Circuit & Waveforms

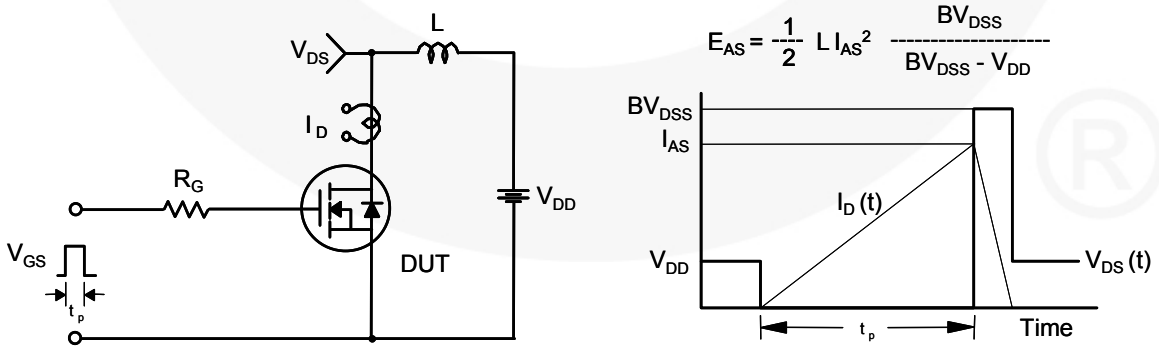


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

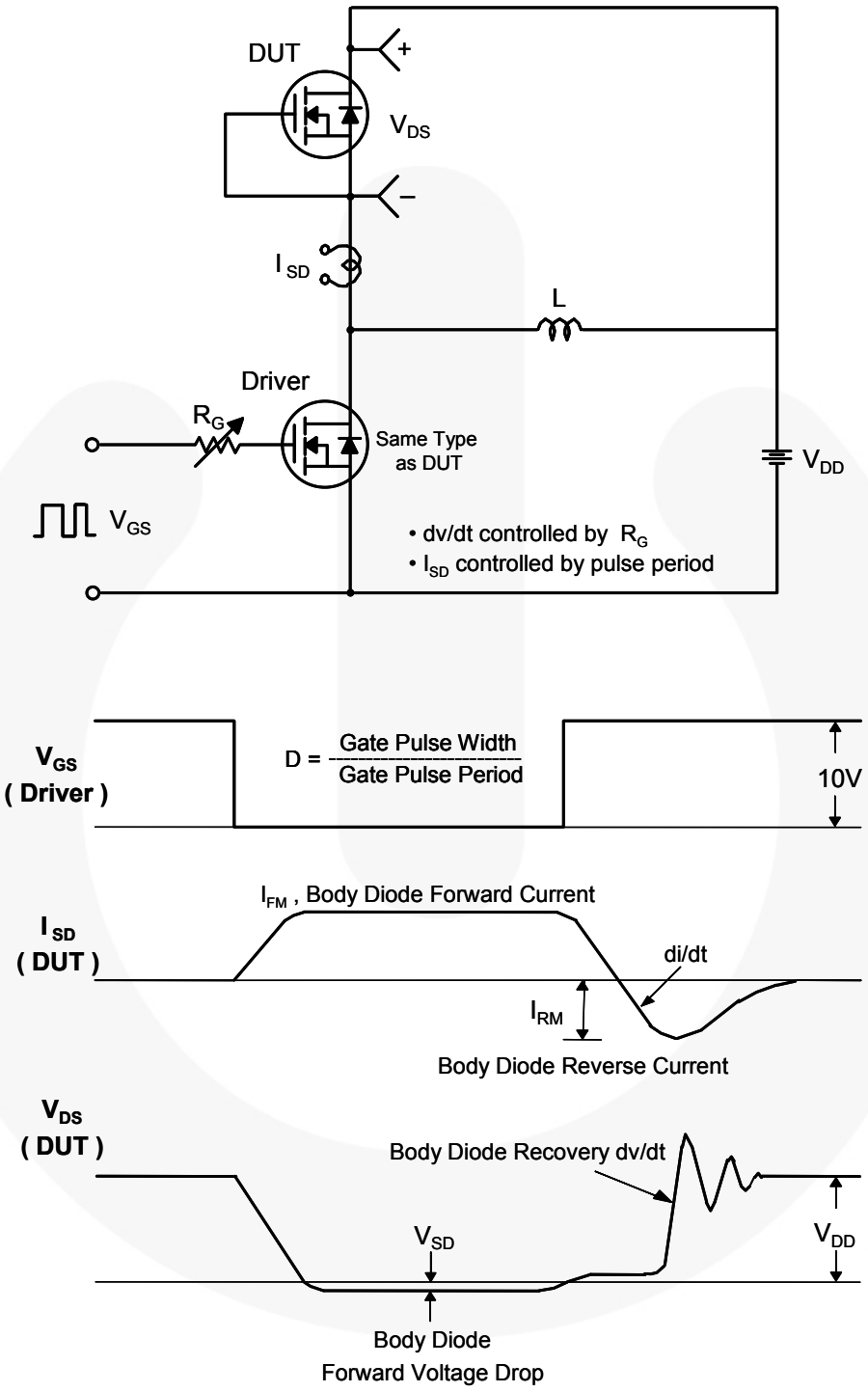


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions

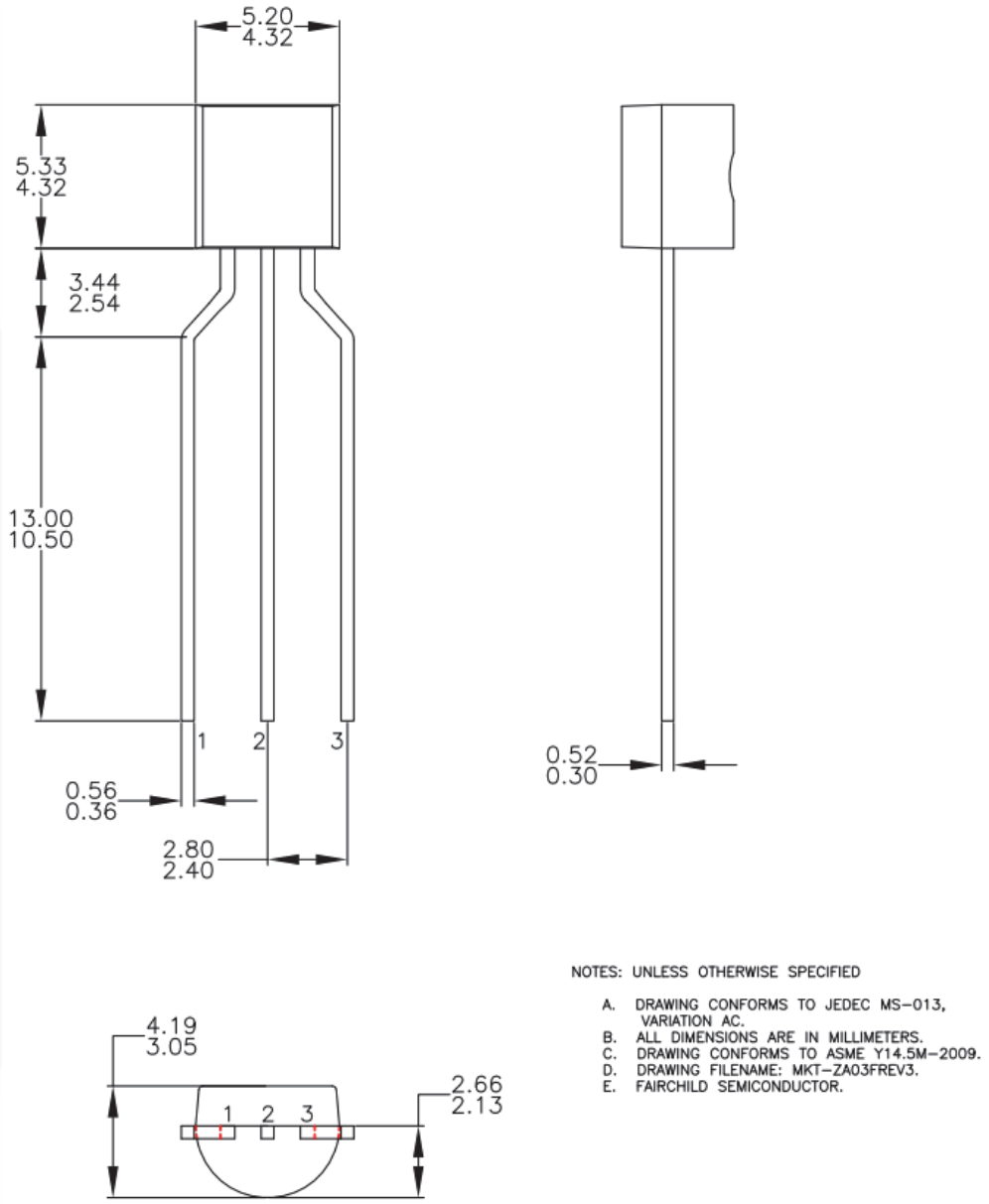


Figure 16. TO92, Molded, 3-Lead, 0.200 In Line Spacing LD Form (J61Z Option)

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