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March 2016

FQB34P10

P-Channel QFET® MOSFET

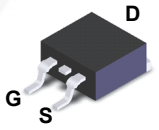
100 V, -33.5 A, 60 mΩ

Description

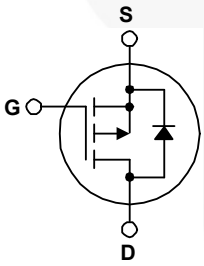
This P-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

Features

- -33.5 A, -100 V, $R_{DS(on)}$ = 60 mΩ (Max.) @ V_{GS} = .10 V, I_D = -16.75 A
- Low Gate Charge (Typ. 85 nC)
- Low Crss (Typ. 170 pF)
- 100% Avalanche Tested
- 175°C Maximum Junction Temperature Rating



D^2-PAK



Absolute Maximum Ratings

T_C = 25°C unless otherwise noted.

Symbol	Parameter		FQB34P10TM	Unit
V_{DSS}	Drain-Source Voltage		-100	V
I_D	Drain Current - Continuous (T_C = 25°C)		-33.5	A
	- Continuous (T_C = 100°C)		-23.5	A
I_{DM}	Drain Current - Pulsed	(Note 1)	-134	A
V_{GSS}	Gate-Source Voltage		± 25	V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	2200	mJ
I_{AR}	Avalanche Current	(Note 1)	-33.5	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	15.5	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	-6.0	V/ns
P_D	Power Dissipation (T_A = 25°C) *		3.75	W
	Power Dissipation (T_C = 25°C)		155	W
	- Derate above 25°C		1.03	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +175	°C
T_L	Maximum lead temperature for soldering, 1/8" from case for 5 seconds		300	°C

Thermal Characteristics

Symbol	Parameter	FQB34P10TM	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.97	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Minimum Pad of 2-oz Copper), Max.	62.5	
	Thermal Resistance, Junction to Ambient (*1 in^2 Pad of 2-oz Copper), Max.	40	

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Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQB34P10TM	FQB34P10	D^2-PAK	Tape and Reel	330 mm	24 mm	800 units

Electrical Characteristics

T_C = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 μA	-100	--	--	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = -250 μA, Referenced to 25°C	--	-0.1	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -100 V, V_{GS} = 0 V	--	--	-1	μA
		V_{DS} = -80 V, T_C = 150°C	--	--	-10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = -25 V, V_{DS} = 0 V	--	--	-100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = 25 V, V_{DS} = 0 V	--	--	100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 μA	-2.0	--	-4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -16.75 A	--	0.049	0.06	Ω
g_{FS}	Forward Transconductance	V_{DS} = -40 V, I_D = -16.75 A	--	23	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = -25 V, V_{GS} = 0 V, f = 1.0 MHz	--	2240	2910	pF
C_{oss}	Output Capacitance		--	730	950	pF
C_{rss}	Reverse Transfer Capacitance		--	170	220	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = -50 V, I_D = -33.5 A, R_G = 25 Ω (Note 4)	--	25	60	ns
t_r	Turn-On Rise Time		--	250	510	ns
$t_{d(off)}$	Turn-Off Delay Time		--	160	330	ns
t_f	Turn-Off Fall Time		--	210	430	ns
Q_g	Total Gate Charge	V_{DS} = -80 V, I_D = -33.5 A, V_{GS} = -10 V (Note 4)	--	85	110	nC
Q_{gs}	Gate-Source Charge		--	15	--	nC
Q_{gd}	Gate-Drain Charge		--	45	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	-33.5	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	-134	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -33.5 A	--	--	-4.0	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = -33.5 A, dI_F / dt = 100 A/μs	--	160	--	ns
Q_{rr}	Reverse Recovery Charge		--	0.88	--	μC

Notes:

1. Repetitive rating : pulse-width limited by maximum junction temperature.
2. L = mH, I_{AS} = -33.5A, V_{DD} = -25 V, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ -33.5 A, di/dt ≤ 300 A/μs , V_{DD} ≤ BV_{DSS}, starting T_J = 25°C.
4. Essentially independent of operating temperature.

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Typical Characteristics

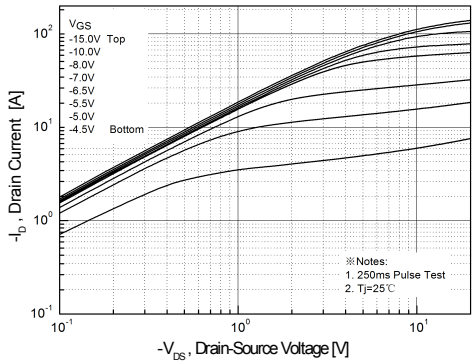


Figure 1. On-Region Characteristics

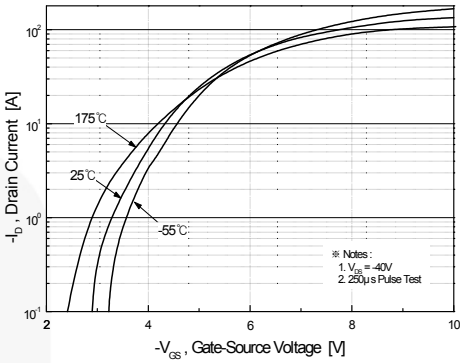


Figure 2. Transfer Characteristics

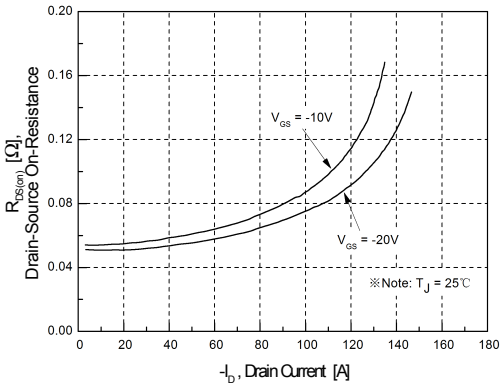


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

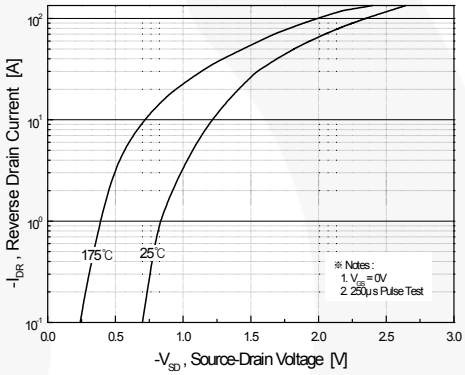


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

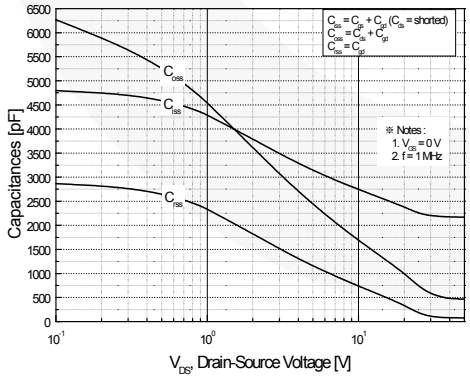


Figure 5. Capacitance Characteristics

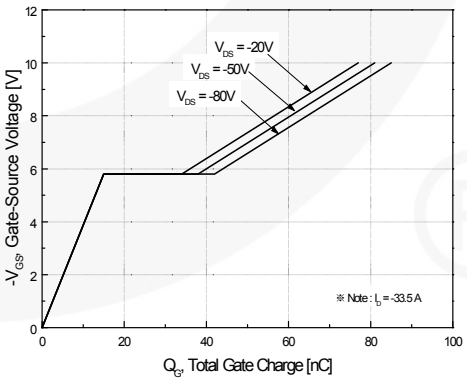


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

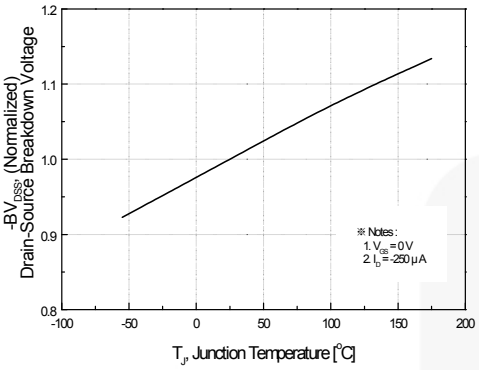


Figure 7. Breakdown Voltage Variation vs. Temperature

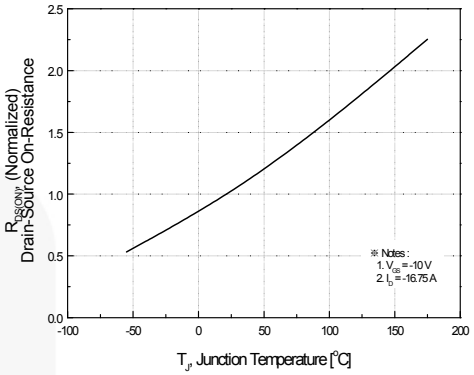


Figure 8. On-Resistance Variation vs. Temperature

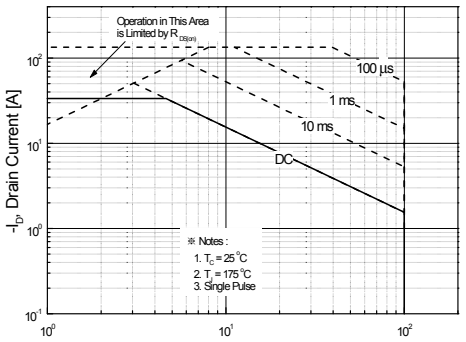


Figure 9. Maximum Safe Operating Area

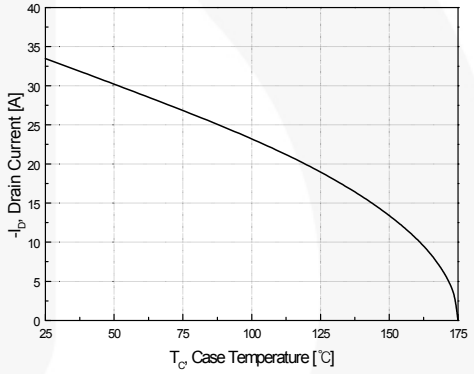


Figure 10. Maximum Drain Current vs. Case Temperature

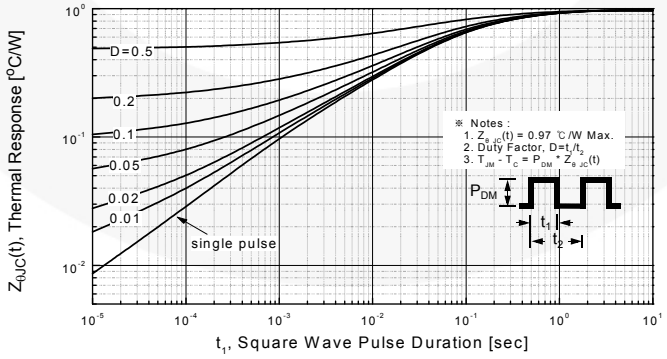


Figure 11. Transient Thermal Response Curve

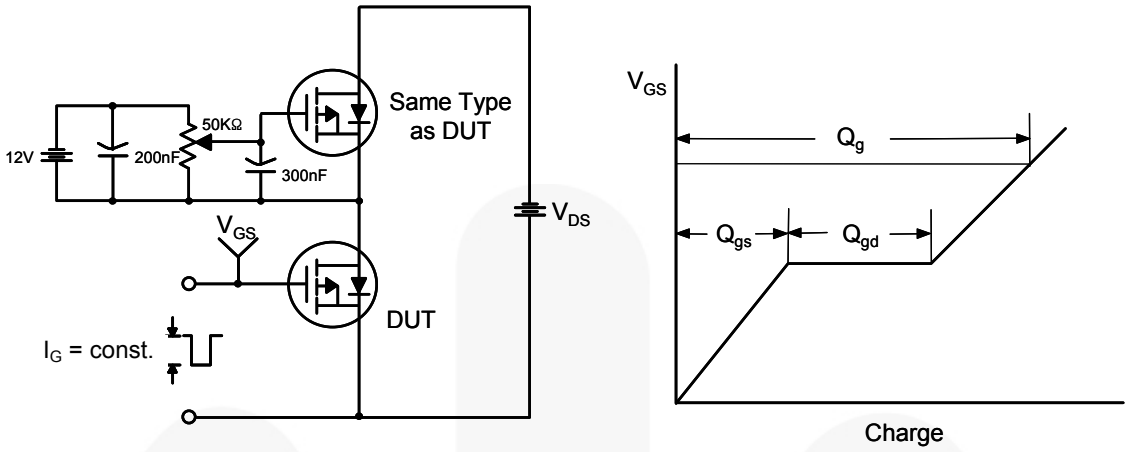


Figure 12. Gate Charge Test Circuit & Waveform

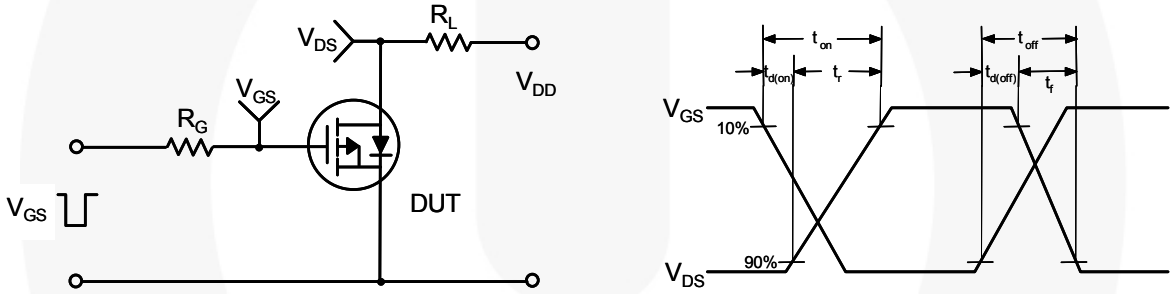


Figure 13. Resistive Switching Test Circuit & Waveforms

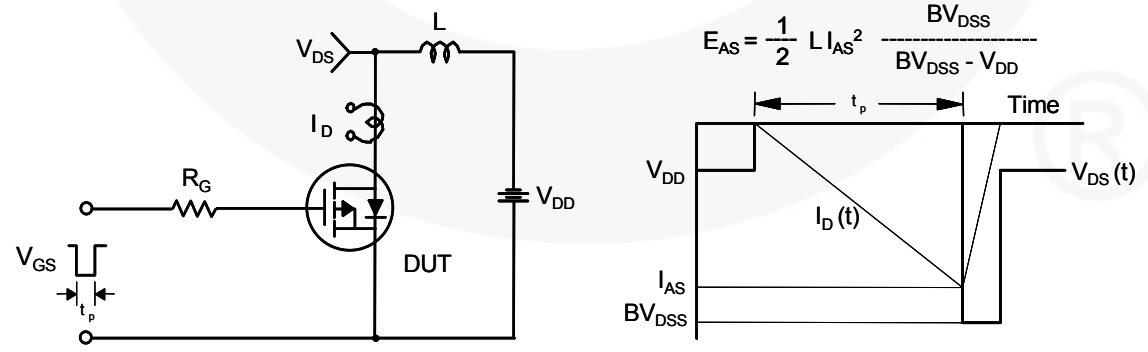


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

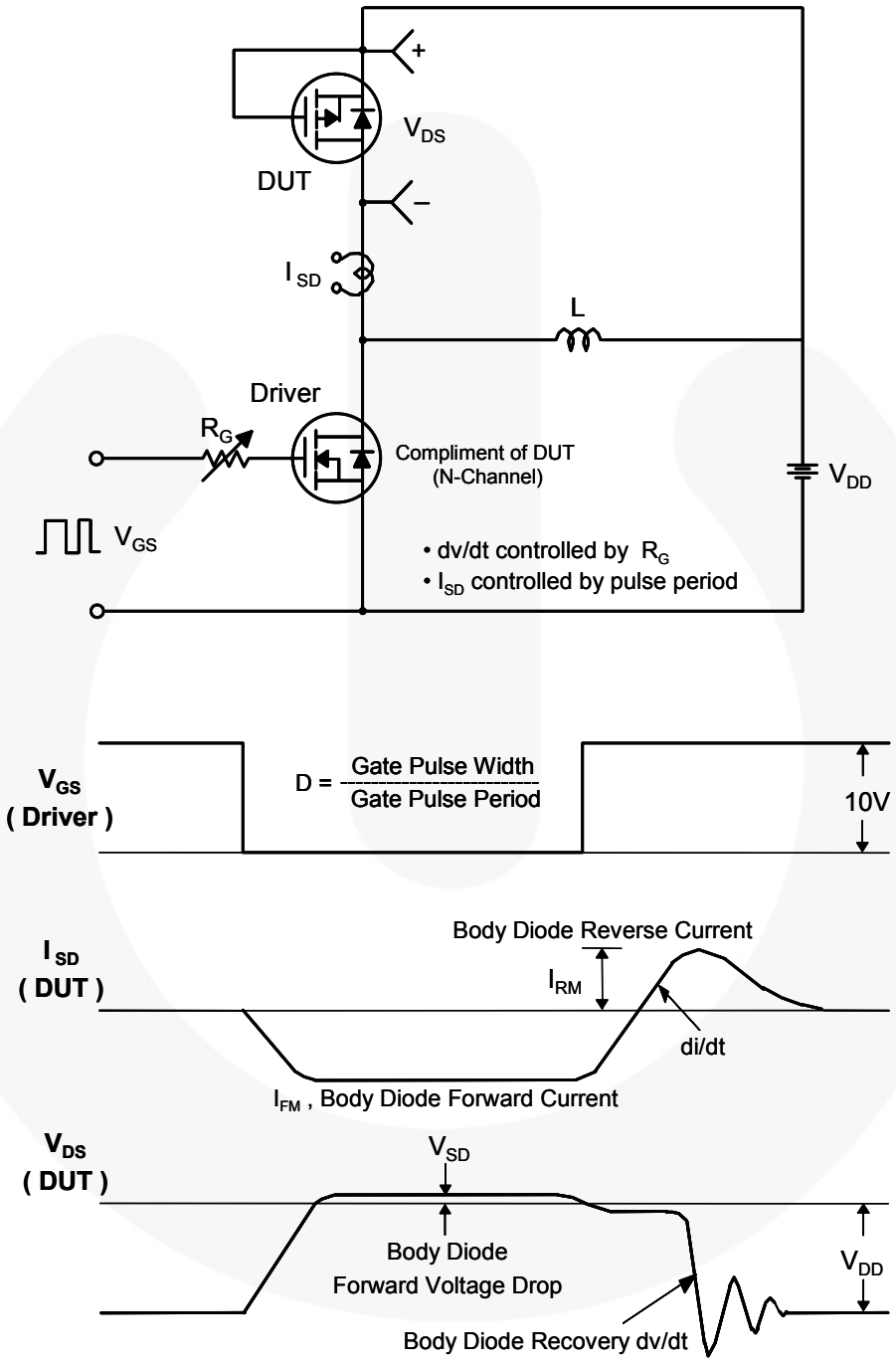
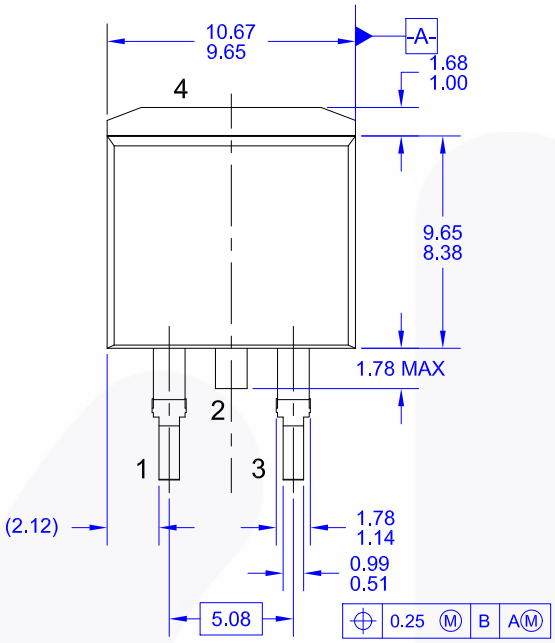
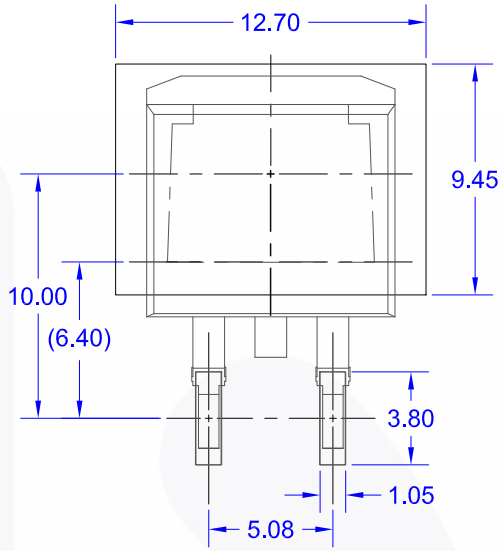


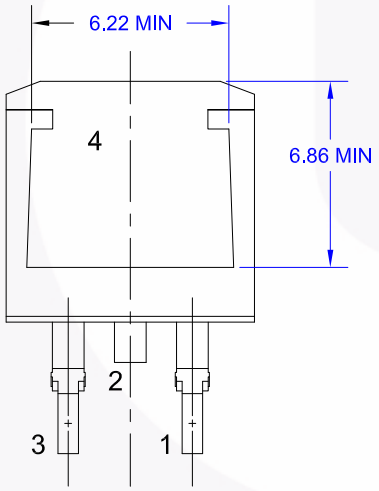
Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

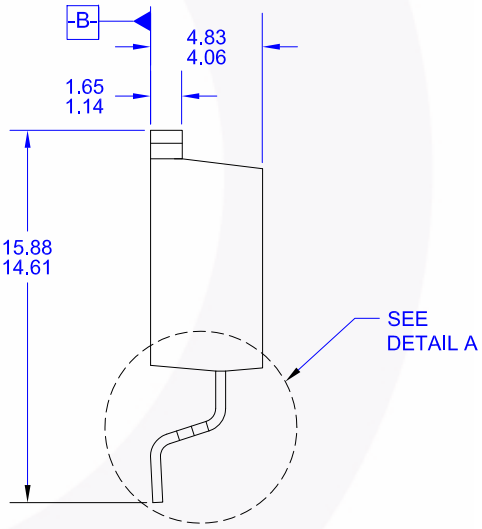
Mechanical Dimensions





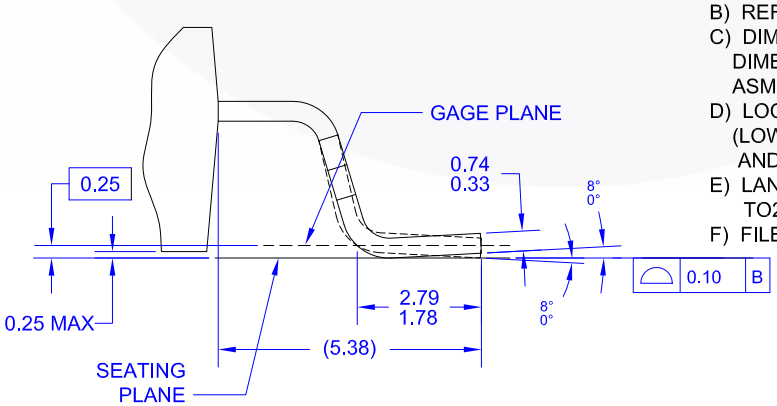
LAND PATTERN RECOMMENDATION
UNLESS NOTED, ALL DIMS TYPICAL





NOTES: UNLESS OTHERWISE SPECIFIED

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D) LOCATION OF THE PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE).
E) LANDPATTERN RECOMMENDATION PER IPC TO254P1524X482-3N
F) FILENAME: TO263A02REV7



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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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