Filtronic

FPD750DFN

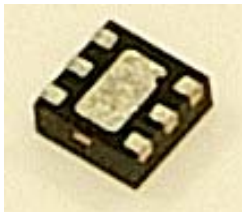
Datasheet v3.0

LOW NOISE HIGH LINEARITY PACKAGED PHEMT

FEATURES (1850MHZ):

- 24 dBm Output Power (P1dB)
- 20 dB Small-Signal Gain (SSG)
- 0.3 dB Noise Figure
- 39 dBm Output IP3 at 50% Bias
- 45% Power-Added Efficiency
- RoHS compliant

PACKAGE:



RoHS

GENERAL DESCRIPTION:

The FPD750DFN is a packaged depletion mode AlGaAs/InGaAs pseudomorphic High Electron Mobility Transistor (pHEMT). It utilizes a 0.25 µm x 750 µm Schottky barrier Gate, defined by high-resolution stepper-based photolithography. The recessed and offset Gate structure minimizes parasitics to optimize performance, with an epitaxial structure designed for improved linearity over a range of bias conditions and input power levels.

TYPICAL APPLICATIONS:

- Drivers or output stages in PCS/Cellular base station transmitter amplifiers
- High intercept-point LNAs
- WLL and WLAN systems, and other types of wireless infrastructure systems.

ELECTRICAL SPECIFICATIONS:

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power at 1dB Gain Compression	P1dB	VDS = 5 V; IDS = 50% IDSS	22.5	24		dBm
Small-Signal Gain	SSG	VDS = 5 V; IDS = 50% IDSS	19	20		dB
Power-Added Efficiency	PAE	VDS = 5 V; IDS = 50% IDSS; POUT = P1dB		45		%
Noise Figure	NF	VDS = 5 V; IDS = 50% IDSS VDS = 5 V; IDS = 25% IDSS		0.7 0.3	1.1 0.9	dB
Output Third-Order Intercept Point (from 15 to 5 dB below P1dB)	IP3	VDS = 5V; IDS = 50% IDSS Matched for optimal power Matched for best IP3		 37 39		dBm
Saturated Drain-Source Current	IDSS	VDS = 1.3 V; VGS = 0 V	180	230	280	mA
Maximum Drain-Source Current	IMAX	VDS = 1.3 V; VGS ≅ +1 V		375		mA
Transconductance	GM	VDS = 1.3 V; VGS = 0 V		200		mS
Gate-Source Leakage Current	IGSO	VGS = -5 V		1	15	µA
Pinch-Off Voltage	|VP|	VDS = 1.3 V; IDS = 0.75 mA	0.7	1.0	1.3	V
Gate-Source Breakdown Voltage	|VBDGS|	IGS = 0.75mA	12	16		V
Gate-Drain Breakdown Voltage	|VBDGD|	IGD = 0.75 mA	12	16		V

Note: $T_{AMBIENT}$ = 22°; RF specification measured at f = 1850 MHz using CW signal (except as noted)

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ABSOLUTE MAXIMUM RATING[1]:

PARAMETER	SYMBOL	TEST CONDITIONS	ABSOLUTE MAXIMUM
Drain-Source Voltage	VDS	-3V < VGS < +0V	8V
Gate-Source Voltage	VGS	0V < VDS < +8V	-3V
Drain-Source Current	IDS	For VDS > 2V	IDss
Gate Current	IG	Forward or reverse current	7.5mA
RF Input Power[2]	PIN	Under any acceptable bias state	175mW
Channel Operating Temperature	TCH	Under any acceptable bias state	175°C
Storage Temperature	TSTG	Non-Operating Storage	-55°C to 150°C
Total Power Dissipation	PTOT	See De-Rating Note below	1.5W
Gain Compression	Comp.	Under any bias conditions	5dB
Simultaneous Combination of Limits[3]		2 or more Max. Limits	

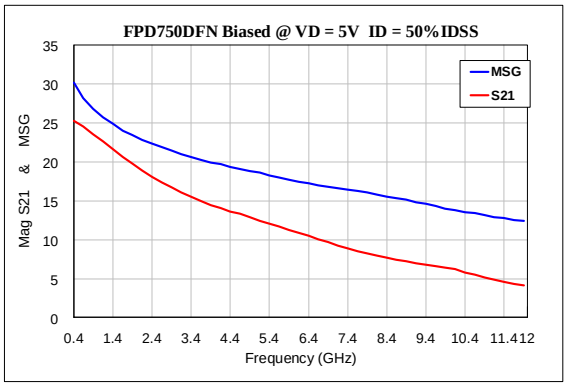
Notes:
[1]$T_{Ambient}$ = 22°C unless otherwise noted; exceeding any one of these absolute maximum ratings may cause permanent damage to the device
[2]Max. RF Input Limit must be further limited if input VSWR > 2.5:1
[3]Users should avoid exceeding 80% of 2 or more Limits simultaneously
[4]Total Power Dissipation defined as: $P_{TOT} \equiv (P_{DC} + P_{IN}) - P_{OUT}$,
where P_{DC}: DC Bias Power, P_{IN}: RF Input Power, P_{OUT}: RF Output Power
Total Power Dissipation to be de-rated as follows above 22°C:
P_{TOT}= 1.5 - (0.011W/°C) x T_{PACK}
where T_{PACK}= source tab lead temperature above 22°C
(coefficient of de-rating formula is the Thermal Conductivity)
Example: For a 65°C carrier temperature: P_{TOT} = 1.5W – (0.011 x (65 – 22)) = 1.03W
[5]The use of a filled via-hole directly beneath the exposed heatsink tab on the bottom of the package is strongly recommended to provide for adequate thermal management. Ideally the bottom of the circuit board is affixed to a heatsink or thermal radiator

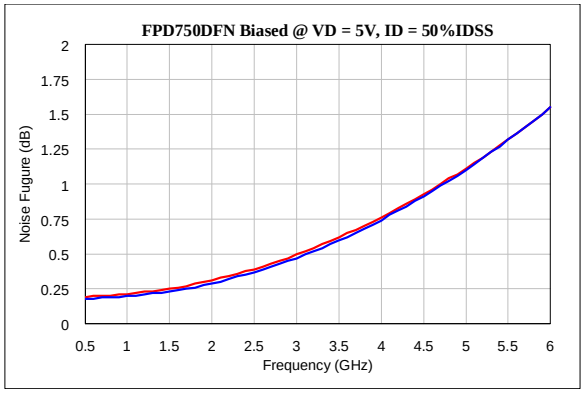
BIASING GUIDELINES:

- Active bias circuits provide good performance stabilisation over variations of operating temperature, but require a larger number of components compared to self-bias or dual-biased. Such circuits should include provisions to ensure that Gate bias is applied before Drain bias, otherwise the pHEMT may be induced to self-oscillate
- Dual-bias circuits are relatively simple to implement, but will require a regulated negative voltage supply for depletion-mode devices.
- For standard Class A operation, a 50% of IDSS bias point is recommended. A small amount of RF gain expansion prior to the onset of compression is normal for this operating point. Note that pHEMTs, since they are “quasi- E/D mode” devices, exhibit Class AB traits when operated at 50% of IDSS. To achieve a larger separation between P1dB and IP3, an operating point in the 25% to 33% of IDSS range is suggested. Such Class AB operation will not degrade the IP3 performance.

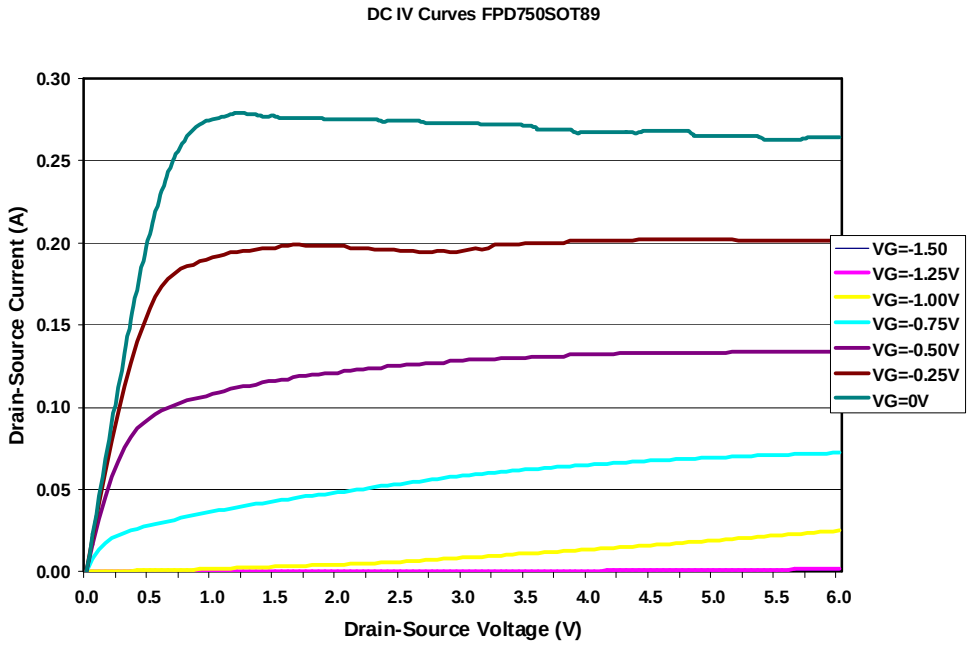
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TYPICAL TUNED RF PERFORMANCE:





TYPICAL I-V CHARACTERISTICS:

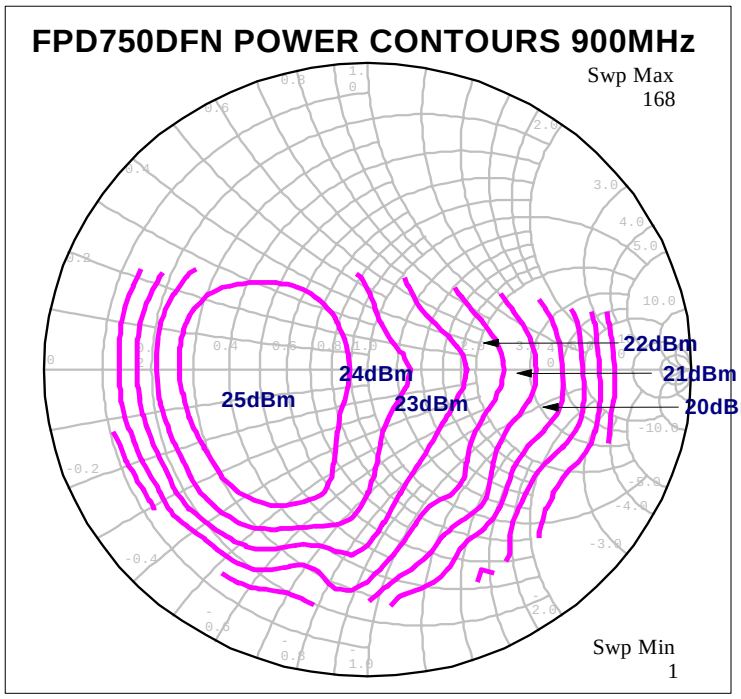


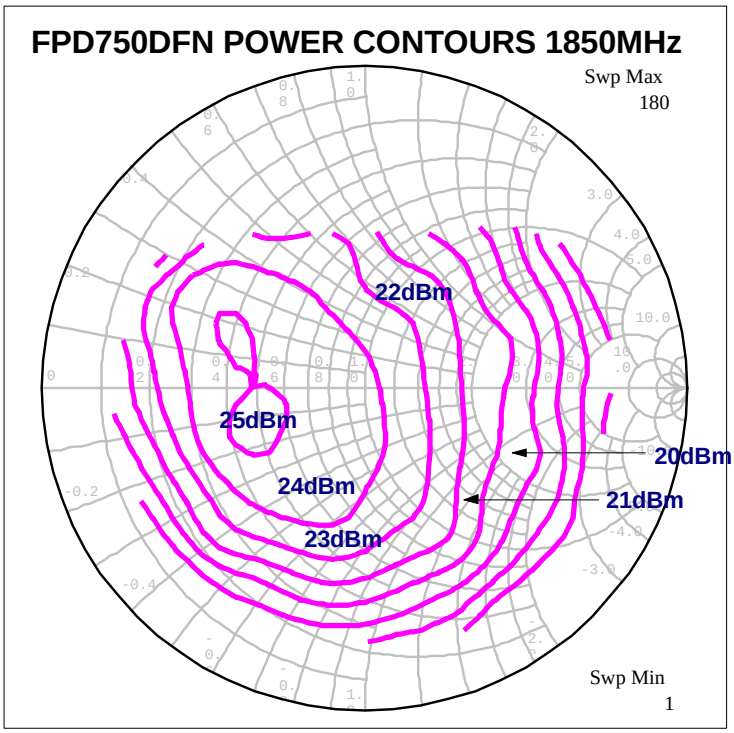
Note: The recommended method for measuring I_{DSS}, or any particular I_{DS}, is to set the Drain-Source voltage (V_{DS}) at 1.3V. This measurement point avoids the onset of spurious self-oscillation which would normally distort the current measurement (this effect has been filtered from the I-V curves presented above). Setting the V_{DS} > 1.3V will generally cause errors in the current measurements, even in stabilised circuits.

Recommendation: Traditionally a device's I_{DSS} rating (I_{DS} at V_{GS} = 0V) was used as a predictor of RF power, and for MESFETs there is a correlation between I_{DSS} and P_{1dB} (power at 1dB gain compression). For pHEMTs it can be shown that there is *no* meaningful statistical correlation between I_{DSS} and P_{1dB}; specifically a linear regression analysis shows $r^2 < 0.7$, and the regression fails the F-statistic test. I_{DSS} is sometimes useful as a guide to circuit tuning, since the S_{22} does vary with the quiescent operating point I_{DS}.

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TYPICAL OUTPUT PLANE CONTOURS (VDS = 5V, IDS = 50%IDSS):





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NOISE PARAMETERS:

Bias 3V, 50%IDSS

Freq (GHz)	Γopt		Rn/50
	Mag	Angle	
0.900	0.509	20.5	0.082
1.800	0.404	52.8	0.074
2.000	0.408	56.5	0.070
2.200	0.402	61.7	0.067
2.400	0.375	70.3	0.064
2.600	0.349	74.1	0.066
2.800	0.302	84.4	0.064
3.000	0.281	96.7	0.060
3.500	0.264	116.1	0.055
4.000	0.244	137.0	0.056
4.500	0.265	162.8	0.051
5.000	0.303	168.7	0.043
5.500	0.312	-176.1	0.049
6.000	0.342	-165.0	0.060

Bias 5V, 25%IDSS

Freq (GHz)	Γopt		Rn/50
	Mag	Angle	
0.900	0.520	16.1	0.079
1.800	0.465	36.4	0.148
2.000	0.471	47.4	0.069
2.200	0.458	52.0	0.068
2.400	0.435	60.0	0.065
2.600	0.423	62.1	0.067
2.800	0.355	71.6	0.064
3.000	0.327	80.7	0.060
3.500	0.298	97.0	0.056
4.000	0.246	116.3	0.057
4.500	0.245	144.0	0.051
5.000	0.271	149.5	0.041
5.500	0.279	171.0	0.042
6.000	0.295	176.4	0.053

Bias 5V, 50%IDSS

Freq (GHz)	Γopt		Rn/50
	Mag	Angle	
0.900	0.512	21.8	0.096
1.800	0.400	52.8	0.084
2.000	0.403	57.5	0.080
2.200	0.385	63.2	0.077
2.400	0.362	72.0	0.074
2.600	0.344	76.1	0.075
2.800	0.299	86.7	0.072
3.000	0.284	98.0	0.068
3.500	0.264	117.5	0.062
4.000	0.236	139.7	0.064
4.500	0.263	163.7	0.058
5.000	0.298	171.9	0.051
5.500	0.323	-165.6	0.062
6.000	0.326	-163.6	0.075

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S-PARAMETERS (BIASED @ 5V, 50%IDSS):

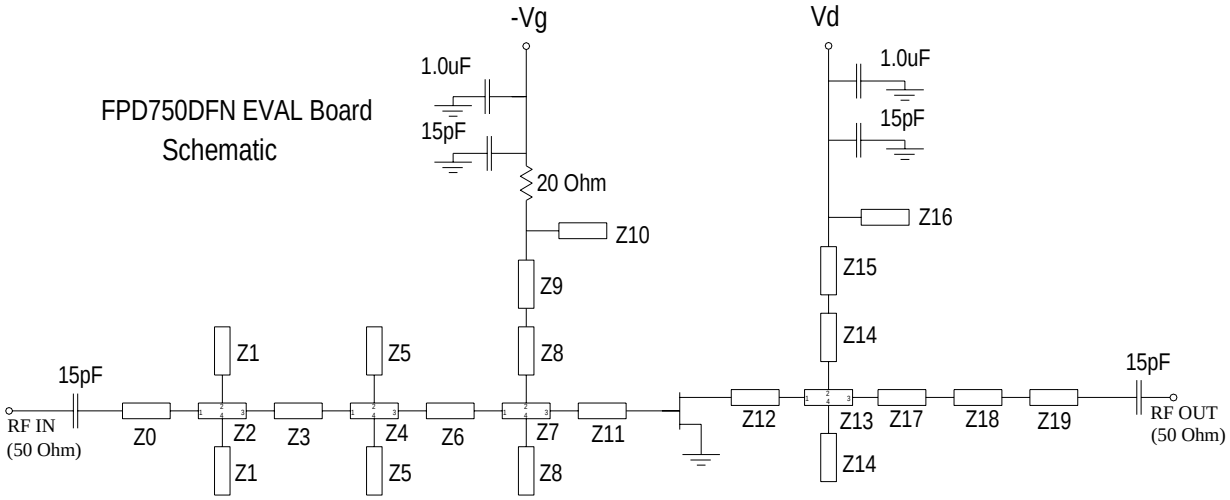
FREQ[GHz]	S11m	S11a	S21m	S21a	S12m	S12a	S22m	S22a
0.400	0.987	-36.5	17.890	156.1	0.017	72.2	0.392	-29.3
0.650	0.906	-58.0	16.489	140.4	0.025	60.3	0.335	-46.1
0.900	0.863	-76.9	14.905	128.5	0.031	51.8	0.311	-60.1
1.150	0.825	-93.8	13.369	118.1	0.036	44.8	0.287	-72.4
1.400	0.794	-108.7	11.976	109.1	0.039	39.4	0.266	-82.9
1.650	0.770	-121.7	10.761	101.1	0.043	35.2	0.246	-91.7
1.900	0.753	-133.2	9.713	94.1	0.044	30.6	0.228	-99.5
2.150	0.741	-143.2	8.828	87.6	0.046	27.7	0.212	-106.8
2.400	0.732	-152.1	8.065	81.9	0.047	24.9	0.198	-113.7
2.650	0.724	-159.8	7.416	76.5	0.048	23.2	0.185	-120.5
2.900	0.720	-166.8	6.864	71.5	0.049	19.9	0.174	-126.8
3.150	0.713	-172.7	6.398	66.8	0.051	18.2	0.166	-133.4
3.400	0.710	-178.4	5.991	62.2	0.052	15.3	0.160	-140.4
3.650	0.700	176.6	5.643	58.0	0.053	13.5	0.152	-145.6
3.900	0.703	171.4	5.308	53.6	0.054	13.2	0.158	-152.6
4.150	0.694	166.9	5.058	49.7	0.054	10.4	0.150	-158.5
4.400	0.703	161.1	4.815	45.1	0.056	10.5	0.154	-161.5
4.650	0.690	156.4	4.649	41.3	0.058	7.8	0.157	-167.5
4.900	0.683	151.2	4.422	35.6	0.058	3.8	0.167	-173.1
5.150	0.687	146.8	4.199	32.0	0.058	4.2	0.158	-179.6
5.400	0.696	141.5	4.033	27.7	0.060	0.8	0.159	177.3
5.650	0.699	136.3	3.855	23.5	0.062	-0.8	0.158	173.8
5.900	0.705	131.1	3.694	19.0	0.062	-3.1	0.162	170.1
6.150	0.709	126.2	3.527	14.8	0.064	-6.4	0.165	164.5
6.400	0.715	121.8	3.367	10.8	0.064	-9.4	0.166	158.7
6.650	0.721	117.6	3.224	6.8	0.064	-11.5	0.167	152.8
6.900	0.726	113.6	3.083	2.7	0.065	-14.1	0.169	146.4
7.150	0.729	110.0	2.933	-1.0	0.064	-16.3	0.173	139.2
7.400	0.731	106.8	2.801	-4.3	0.064	-18.7	0.172	131.7
7.650	0.733	104.0	2.692	-7.5	0.064	-19.0	0.172	125.5
7.900	0.739	100.9	2.601	-10.8	0.064	-20.2	0.177	120.8
8.150	0.743	98.3	2.516	-14.0	0.066	-21.4	0.185	116.1
8.400	0.750	95.3	2.443	-17.4	0.068	-21.9	0.196	111.4
8.650	0.755	92.3	2.373	-20.7	0.069	-22.7	0.209	107.8
8.900	0.761	89.1	2.315	-24.3	0.071	-25.0	0.221	104.8
9.150	0.768	85.7	2.256	-27.8	0.075	-26.4	0.239	102.5
9.400	0.779	81.9	2.205	-31.5	0.077	-28.9	0.257	100.2
9.650	0.782	77.8	2.149	-35.4	0.080	-30.6	0.276	98.4
9.900	0.791	73.9	2.115	-39.4	0.084	-33.7	0.299	96.1
10.150	0.805	69.3	2.066	-44.4	0.086	-37.3	0.320	93.8
10.400	0.804	64.7	1.973	-48.7	0.087	-40.7	0.337	90.6
10.650	0.807	60.7	1.899	-52.5	0.087	-43.2	0.350	88.1
10.900	0.813	57.1	1.833	-56.1	0.089	-45.3	0.361	85.8
11.150	0.821	53.6	1.776	-59.6	0.091	-48.0	0.374	83.2
11.400	0.831	50.3	1.718	-63.2	0.091	-50.4	0.385	80.3
11.650	0.845	47.2	1.669	-66.6	0.093	-52.7	0.394	77.0
11.900	0.858	43.9	1.635	-70.4	0.094	-54.3	0.398	73.2

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REFERENCE DESIGN (5.3 – 5.9GHz):

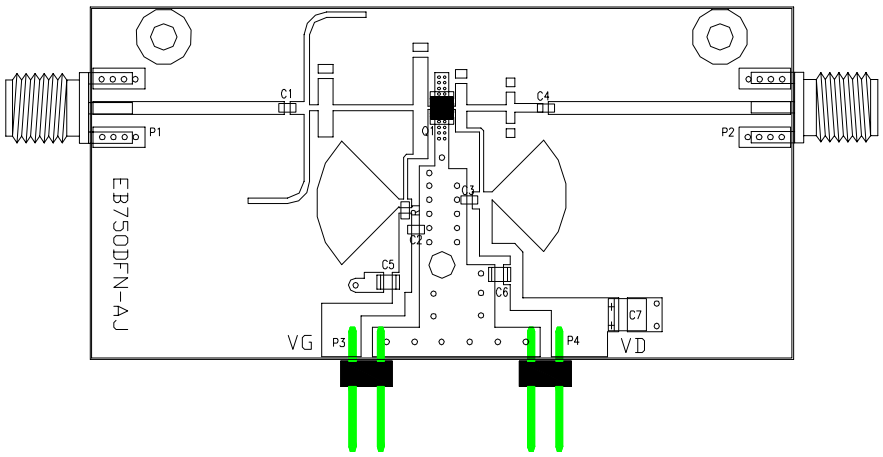


Desc.	Value
Z0	0.045" x 0.050" Microstrip
Z1	0.020" x 0.500" Microstrip
Z2	W1=0.020" W2=0.020" W3=0.020" W4=0.020" Microstrip Cross
Z3	0.020" x 0.030" Microstrip
Z4	W1=0.020" W2=0.052" W3=0.020" W4=0.052" Microstrip Cross
Z5	0.052" x 0.94" Microstrip
Z6	0.020" x 0.285" Microstrip
Z7	W1=0.020" W2=0.054" W3=0.020" W4=0.054" Microstrip Cross
Z8	0.054" x 0.170" Microstrip
Z9	0.015" x 0.162" Microstrip
Z10	0.310" x 90° Microstrip Radial Stub
Z16	0.280" x 90° Microstrip Radial Stub
Z11, Z12	0.012" x 0.037" Microstrip
Z13	W1=0.022" W2=0.040" W3=0.022" W4=0.040" Microstrip Cross
Z14	0.040" x 0.075" Microstrip
Z15	0.015" x 0.257" Microstrip
Z17	0.022" x 0.140" Microstrip
Z18	0.110" x 0.030" Microstrip
Z19	0.030" x 0.100" Microstrip

PARAMETER	UNIT	PERFORMANCE
Frequency	GHz	5.3 to 5.9
Gain	dB	13.5
P1dB	dBm	24
N.F.	dB	1.2
S11	dB	-8
S22	dB	-10
Vd	V	5
Vg	V	-0.4 to -0.7
Id	mA	100

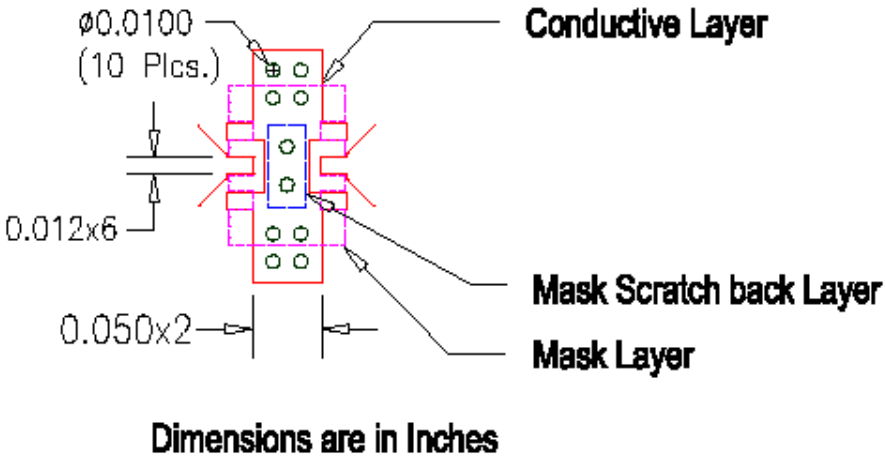
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EVALUATION BOARD:



Component	Description
R1	Resistor 0.06 x 0.03 20Ω 1/4W
C1, C2, C3, C4	Cap. 0.06 x 0.03 15pF
C5, C6	Cap. 0.08 x 0.05 0.01uF
C7	Cap. SMD-B 1.0uF
P1, P2	Edge Mount RF Connecter
P3, P4	2 Pin Header
Q1	FPD750DFN
PCB	EV-SP-000051-002 (R4003, 20mil Thick)
Base Plate	TF-SP-000055-001

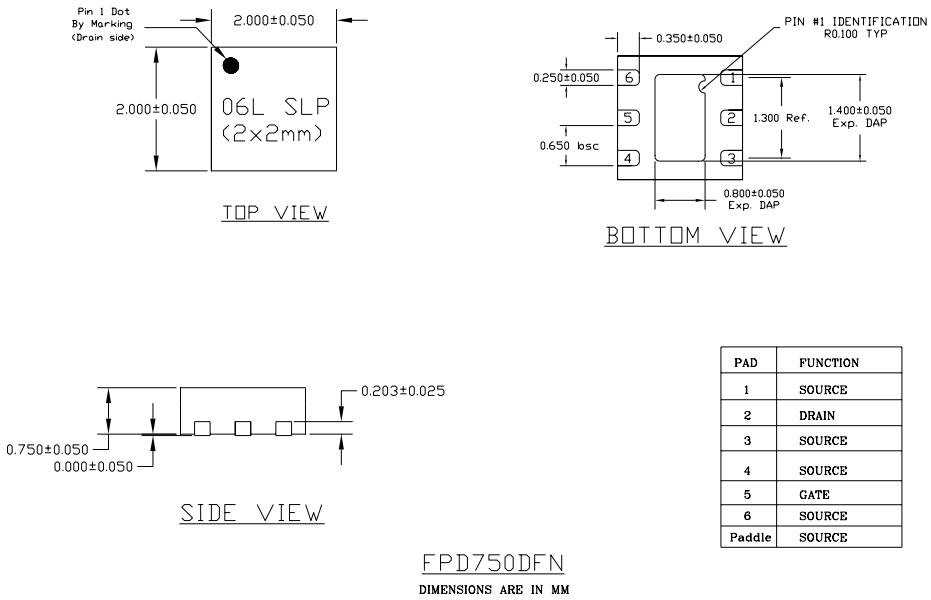
PCB FOOTPRINT:



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PACKAGE OUTLINE:

(dimensions in millimetres – mm)



PAD	FUNCTION
1	SOURCE
2	DRAIN
3	SOURCE
4	SOURCE
5	GATE
6	SOURCE
Paddle	SOURCE

PREFERRED ASSEMBLY INSTRUCTIONS:

Available on request.

HANDLING PRECAUTIONS:



To avoid damage to the devices care should be exercised during handling. Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing. These devices should be treated as Class 0 (0-250 V) as defined in JEDEC Standard No. 22-A114. Further information on ESD control measures can be found in MIL-STD-1686 and MIL-HDBK-263.

APPLICATION NOTES & DESIGN DATA:

Application Notes and design data including S-parameters are available on request.

DISCLAIMERS:

This product is not designed for use in any space based or life sustaining/supporting equipment.

ORDERING INFORMATION:

PART NUMBER	DESCRIPTION
FPD750DFN	Packaged pHEMT
EB750DFN-BB	Packaged pHEMT eval board – 900MHz
EB750DFN-BA	Packaged pHEMT eval board – 1.85GHz
EB750DFN-BC	Packaged pHEMT eval board – 2.0GHz
EB750DFN-BE	Packaged pHEMT eval board – 2.4GHz
EB750DFN-AJ	Packaged pHEMT eval board – 5.3 to 5.75GHz

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