FP2189

1 Watt HFET

The Communications Edge ™

Preliminary Product Information

Product Features

- 50 – 4000 MHz
- Up to +31 dBm P1dB
- Up to +45 dBm Output IP3
- High Drain Efficiency
- 19 dB Gain @ 900 MHz
- MTBF >100 Years
- SOT-89 SMT Package

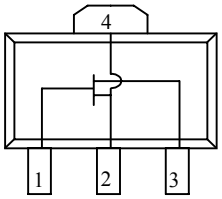
Product Description

The FP2189 is a high performance 1-Watt HFET (Heterostructure FET) in a low-cost SOT-89 surface-mount package. This device works optimally at a drain bias of +8 V and 250 mA to achieve +45 dBm output IP3 performance and an output power of +31 dBm at 1-dB compression.

The device conforms to WJ Communications' long history of producing high reliability and quality components. The FP2189 has an associated MTBF of greater than 100 years at a mounting temperature of 85°C. All devices are 100% RF & DC tested.

The product is targeted for use as driver amplifiers for wireless infrastructure where high performance and high efficiency are required.

Functional Diagram



Function	Pin No.
Input	1
Ground	2
Output/Bias	3
Ground	4

Specifications

DC Electrical Parameter	Units	Min	Typ	Max
Saturated Drain Current[1], I_{dss}	mA		500	
Transconductance, G_m	mS		350	
Pinch Off Voltage[2], V_p	V		-2.0	

Parameters[3]	Units	Min	Typ	Max
Frequency Range	MHz	50		4000
Small Signal Gain, Gss	dB		15	
Output P1dB	dBm		+31	
Output IP3[4]	dBm		+45	
Thermal Resistance	°C/W			30

1. I_{dss} is measured with V_{gs} = 0 V, V_{ds} = 3 V.
2. Pinch-off voltage is measured when I_{ds} = 0.4 mA.
3. Test conditions unless otherwise noted: T = 25ºC, V_{DS} = 8 V, I_{DQ} = 250 mA, frequency = 900 MHz in an application circuit with $Z_L = Z_{LOPT}$, $Z_S = Z_{SOPT}$.
4. 3OIP measured with two tones at an output power of +15 dBm/tone separated by 1 MHz. The suppression on the largest IM3 product is used to calculate the 3OIP using a 2:1 rule.

Typical Parameters[5]

Parameter	Units	Typical		
Frequency	MHz	915	1960	2140
S21	dB	19.1	15.2	13.8
S11	dB	-17	-16	-23
S22	dB	-10	-8	-9
Output P1dB	dBm	+30.3	+30.8	+31.4
Output IP3	dBm	+44.3	+44.2	+45.5
Noise Figure	dB	4.2	3.5	4.5
V_{dd}	V	+8	+8	+8
I_{dq}[6]	mA	250	250	250
I_{dd} at P1dB	mA	260	330	320

5. Typical parameters represent performance in an application circuit.
6. I_{dq} is the quiescent drain current at small signal output levels. The current may increase as the output power is increased near its compression point.

Absolute Maximum Ratings

Parameters	Rating
Operating Case Temperature	-40 to +85 °C
Storage Temperature	-40 to +125 °C
Maximum DC Power	4.0 W
RF Input Power (continuous)	+20 dBm

Operation of this device above any of there parameters may cause permanent damage

Ordering Information

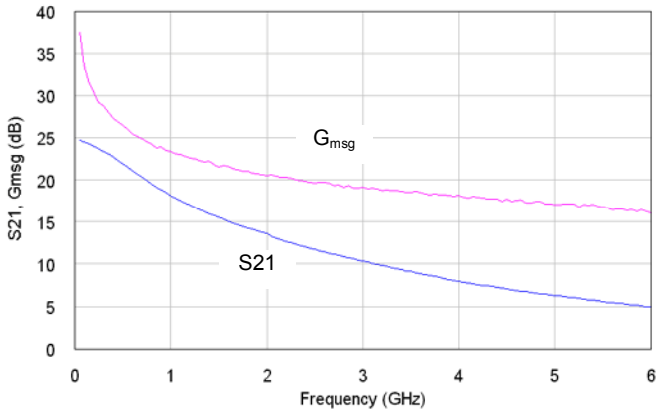
Part No.	Description
FP2189	1-Watt HFET (Available in Tape & Reel)
FP2189-PCB900S	900 MHz Application Circuit
FP2189-PCB1900S	1900 MHz Application Circuit
FP2189-PCB2140S	2140 MHz Application Circuit

This document contains information on a new product.
Specifications and information are subject to change without notice

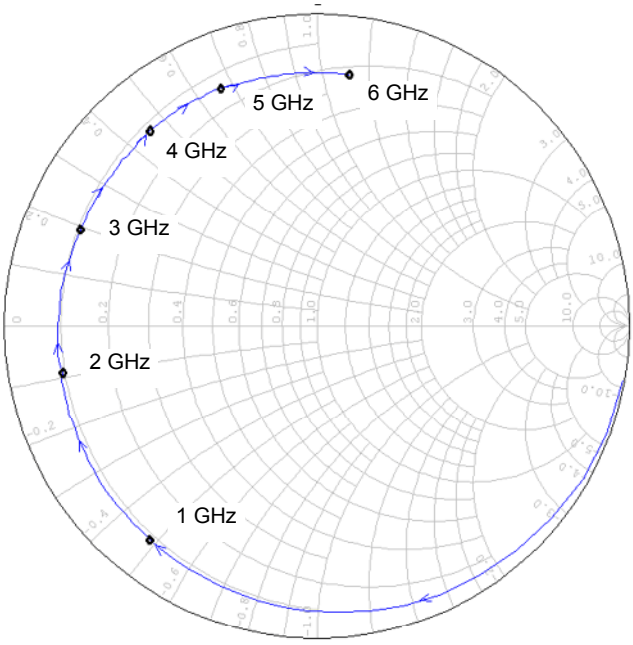
Typical Performance Data

S-Parameters (V_{ds} = 8 V, I_{ds} = 250 mA, 25°C, Unmatched 50 ohm system)

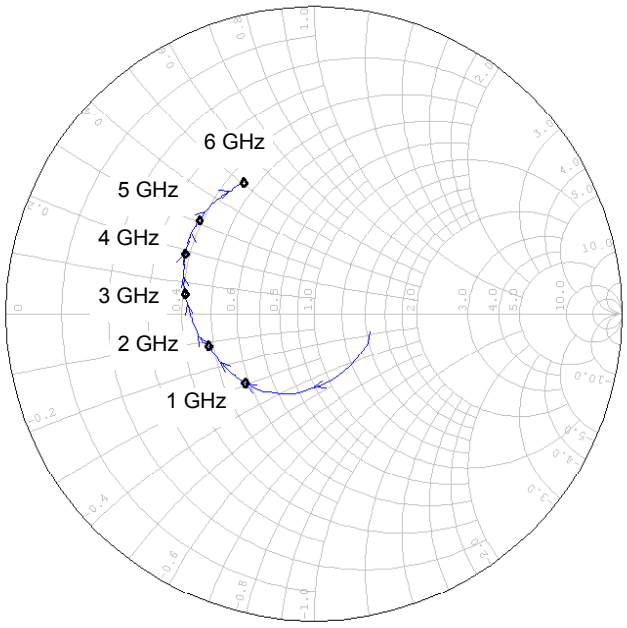
Gain, Maximum Stable Gain vs Frequency



S_{11} vs Frequency



S_{22} vs Frequency



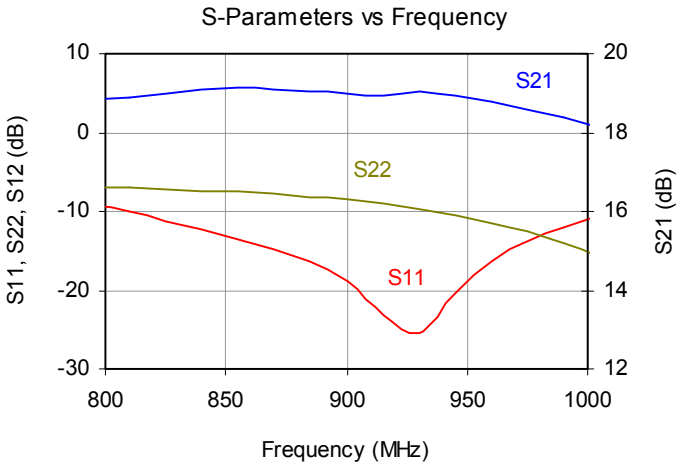
Note:
Measurements were made on the packaged device in a test fixture with 50 ohm input and output lines. The S-parameters that are shown are the de-embedded data down to the device leads and represents typical performance of the device.

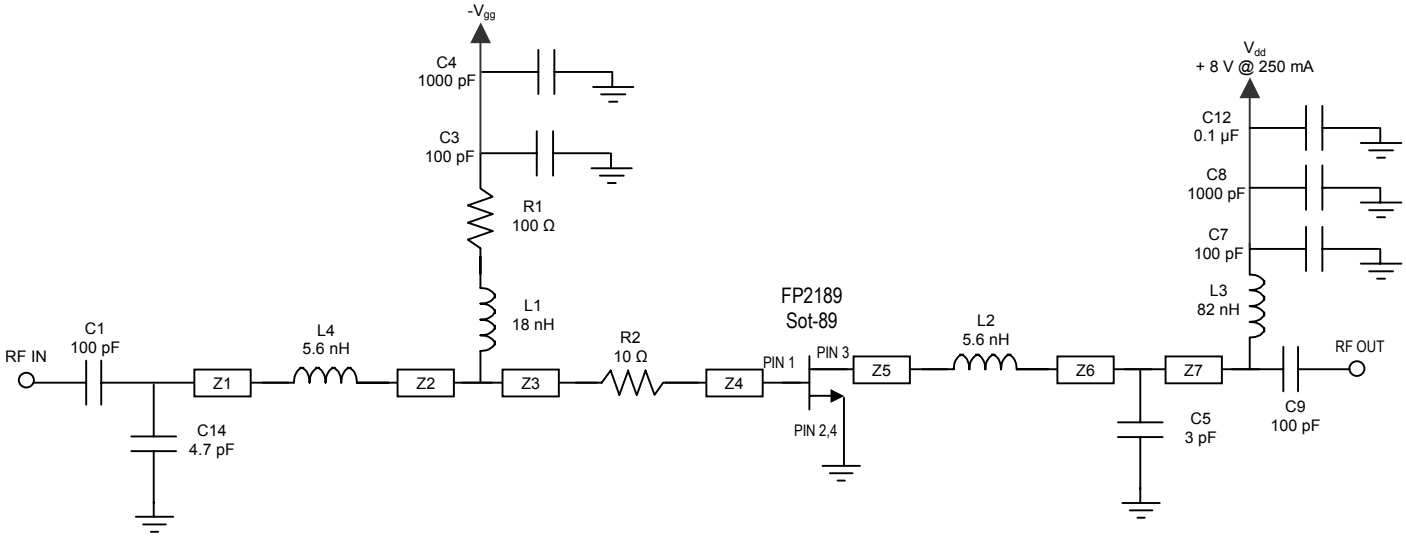
Application Circuit: 870 – 960 MHz

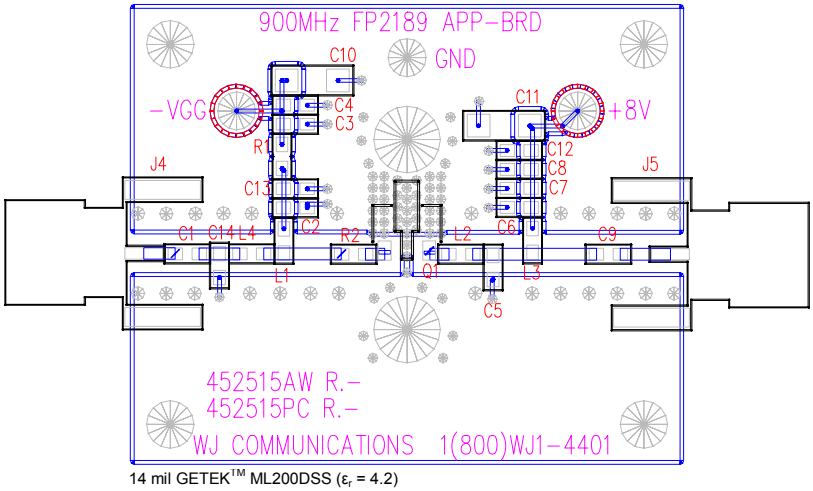
Typical Specifications

Frequency	870	915	960
S21 - Gain	19.1	19.1	19.1
S11 - Input R.L.	-12	-17	-25
S22 - Output R.L.	-9	-10	-12
Output P1dB	+30.4	+30.3	+30.2
Output IP3	+44.4	+44.3	+44.3
Noise Figure	4.2	4.2	4.2
V_{dd}		+ 8 V	
I_{dq} [1]		250 mA	

[1] I_{dq} is the quiescent current at small signal output levels. The current typically increases up to 260 mA at the 1-dB compression point.







14 mil GETEK™ ML200DSS (ε_r = 4.2)
The layout of this circuit can be downloaded from the website.

Ref. Designator	Length on .014" GETEK™ (mil)	Electrical length @ 900 MHz (deg)
Z1	30	1.45
Z2	30	1.45
Z3	135	6.5
Z4	50	2.4
Z5	50	2.4
Z6	42	2.0
Z7	65	3.1

The lengths are measured from the component edge-to-edge.
All microstrip lines have a line impedance of 50 Ω.

Ref. Designator	Value	Part style	Size
C1, C3, C7, C9	100 pF	5% 50V, NPO/COG	0603
C4, C8	1000 pF	5%, 50V, NPO/COG	0603
C5	3 pF	AVX 06031J3R0BAWTR	0603
C11	0.1 µF	10%, 50V, X7R	1206
C14	4.7 pF	AVX 06035J4R7APWTR	0603
R1	100 Ω	1/16 W, 5%	0603
R2	10 Ω	1/16 W, 5%	0603
L1	18 nH	TOKO LL1608-FH18NJ	0603
L2, L4	5.6 nH	TOKO LL1608-FH5N6S	0603
L3	82 nH	TOKO LL1608-FH82NJ	0603

All other parts are No Loads.
Total unique parts count: 10

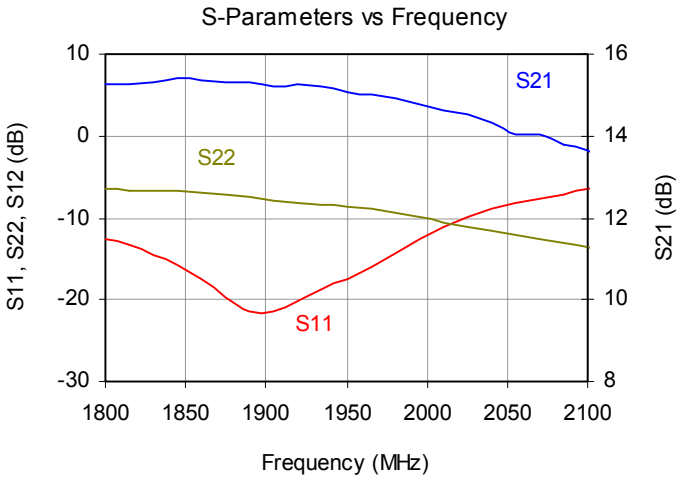
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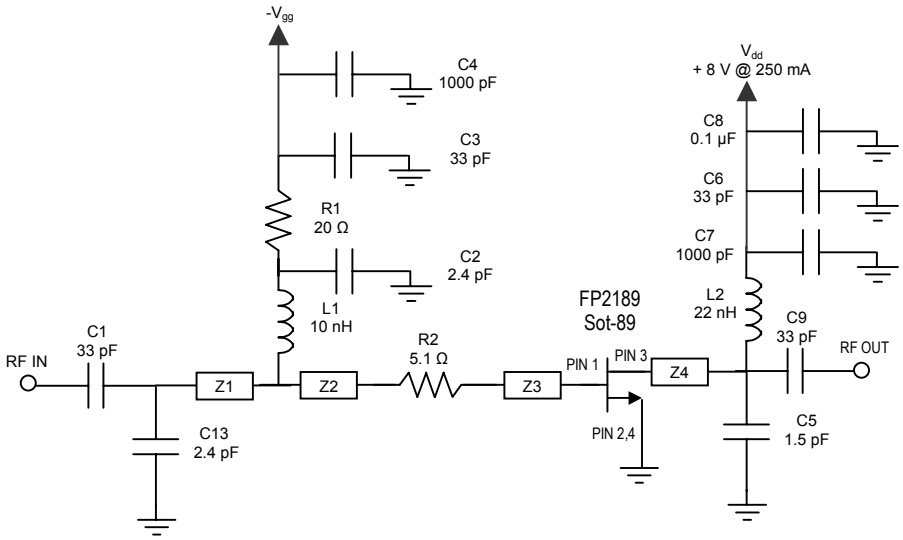
Application Circuit: 1930 – 1990 MHz

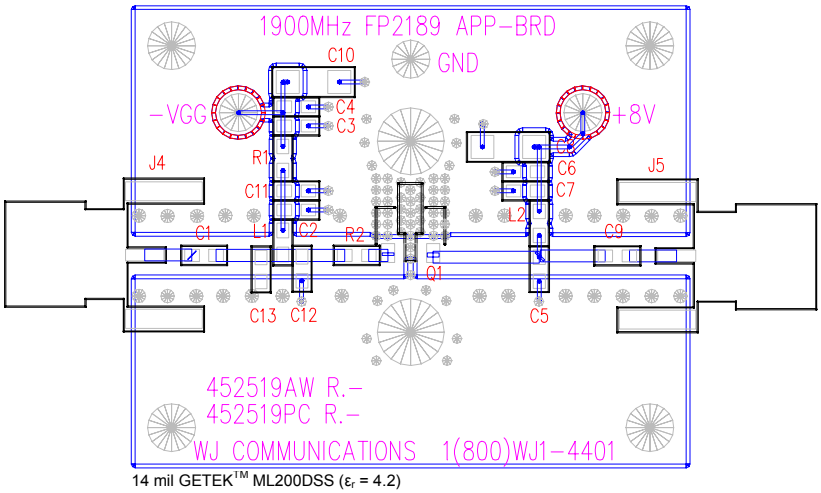
Typical Specifications

Frequency	1930	1960	1990
S21 - Gain	15.3	15.2	15.0
S11 - Input R.L.	-14	-16	-19
S22 - Output R.L.	-8	-8	-9
Output P1dB	+30.8	+30.8	+30.7
Output IP3	+44	+44.2	+44.3
Noise Figure	3.6	3.5	3.5
V_{dd}		+ 8 V	
I_{dq} [1]		250 mA	

[1] I_{dq} is the quiescent current at small signal output levels. The current typically increases up to 330 mA at the 1-dB compression point.







14 mil GETEK™ ML200DSS (ε_r = 4.2)
The layout of this circuit can be downloaded from the website.

Ref. Designator	Length on .014" GETEK™ (mil)	Electrical length @ 1900 MHz (deg)
Z1	30	3.1
Z2	145	14.8
Z3	50	5.1
Z4	255	26.1

The lengths are measured from the component edge-to-edge.
All microstrip lines have a line impedance of 50 Ω.

Ref. Designator	Value	Part style	Size
C1, C3, C6, C9	33 pF	5% 50V, NPO/COG	0603
C2, C13	2.4 pF	AVX 06035J2R4AAWTR	0603
C4, C7	1000 pF	5% 50V, NPO/COG	0603
C5	1.5 pF	AVX 06035J1R5AAWTR	0603
C8	0.1 µF	10%, 50V, X7R	1206
R1	20 Ω	1/16 W, 5%	0603
R2	5.1 Ω	1/16 W, 5%	0603
L1	10 nH	TOKO LL1608-FH10NJ	0603
L2	22 nH	TOKO LL1608-FH22NJ	0603

All other parts are No Loads.
Total unique parts count: 9

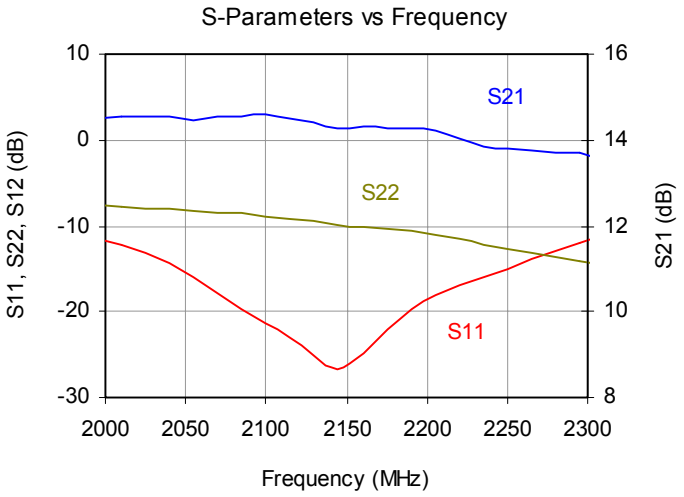
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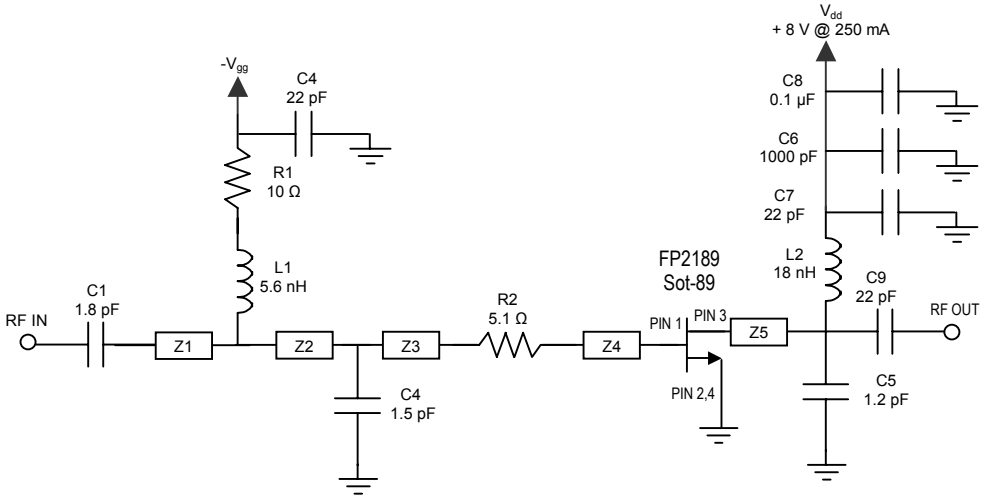
Application Circuit: 2110 – 2170 MHz

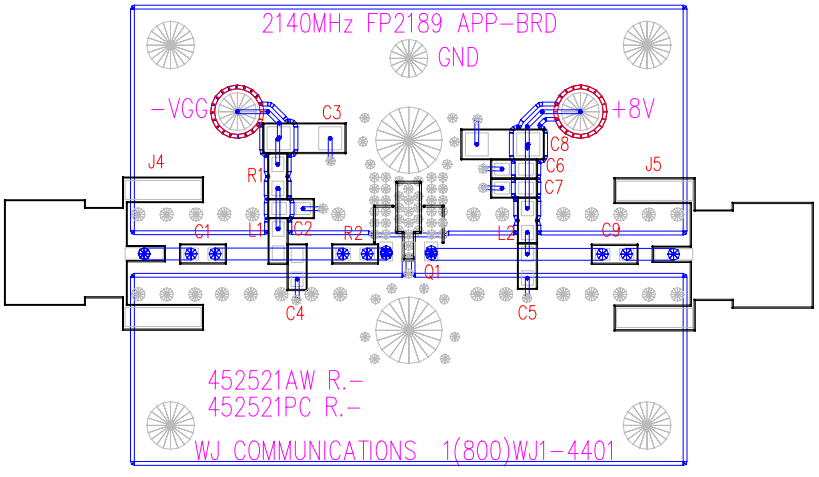
Typical Specifications

Frequency	2110	2140	2170
S21 - Gain	13.9	13.8	13.7
S11 - Input R.L.	-27	-23	-20
S22 - Output R.L.	-8	-9	-10
Output P1dB	+31.4	+31.4	+31.4
Output IP3	+44.5	+45.5	+43.2
Noise Figure	4.5	4.5	4.5
V_{dd}		+ 8 V	
I_{dq} [1]		250 mA	

[1] I_{dq} is the quiescent current at small signal output levels. The current typically increases up to 320 mA at the 1-dB compression point.







14 mil GETEK™ ML200DSS (ε_r = 4.2)
The layout of this circuit can be downloaded from the website.

Ref. Designator	Length on .014" GETEK™ (mil)	Electrical length @ 2140 MHz (deg)
Z1	150	17.3
Z2	15	1.7
Z3	100	11.5
Z4	50	5.8
Z5	225	25.9

The lengths are measured from the component edge-to-edge.
All microstrip lines have a line impedance of 50 Ω.

Ref. Designator	Value	Part style	Size
C1	1.8 pF	AVX 06035J1R8AAWTR	0603
C3, C7, C9	22 pF	5% 50V, NPO/COG	0603
C4	1.5 pF	AVX 06035J1R5AAWTR	0603
C5	1.2 pF	AVX 06035J1R2AAWTR	0603
C6	1000 pF	5% 50V, NPO/COG	0603
C8	0.1 µF	10%, 50V, X7R	1206
R1	10 Ω	1/16 W, 5%	0603
R2	6.2 Ω	1/16 W, 5%	0603
L1	18 nH	TOKO LL1608-FH18NJ	0603
L2	5.6 nH	TOKO LL1608-FH5N6S	0603

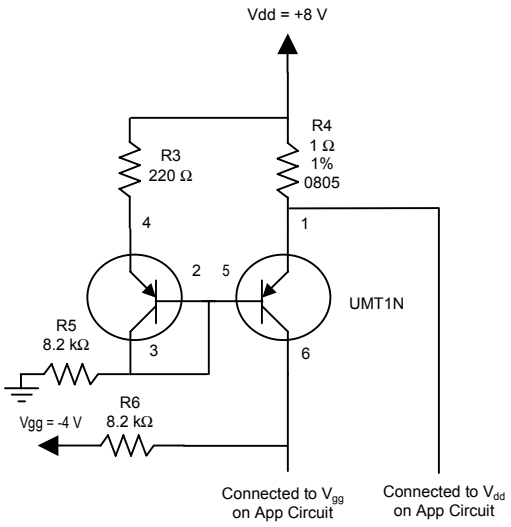
All other parts are No Loads.
Total unique parts count: 10
C3 is of size 0805 on the app board so that it would fit in the 1206 pad.

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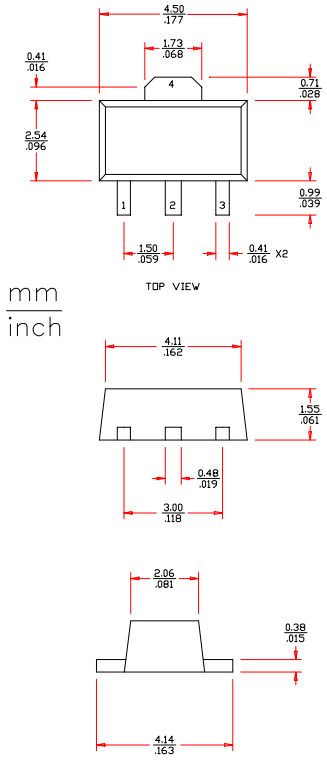
Application Note

Special attention should be taken to properly bias the FP2189. Power supply sequencing is required to prevent the device from operating at 100% I_{dss} for a prolonged period of time and possibly causing damage to the device. It is recommended that for the safest operation, the negative supply be "first on and last off." With a negative gate voltage present, the drain voltage can then be applied to the device. The gate voltage can then be adjusted to have the device be used at the proper quiescent bias condition.

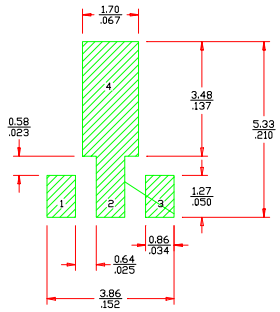
An optional temperature-compensation active-bias circuit is recommended for use with the application circuit, which requires two standard voltage supplies +8V and -4V, and is set for an optimal drain bias of +8V @ 250 mA. The circuit schematic, shown on the right, uses dual PNP transistors to provide a constant drain current into the FP2189 and also eliminates the effects of pinchoff variation. Temperature compensation is achieved by tracking the voltage variation with the temperature of the emitter-to-base junction of the PNP transistors. Thus the transistor emitter voltage adjusts the voltage incident at the gate of the FP2189 so that the device draws a constant current, regardless of the temperature. Two fixed voltage supplies are needed for operation. A Rohm dual transistor, UMT1N, and a dual-chip resistor (8.2 kΩ) are recommended to minimize board space and help decrease the current variability through R4 with the components being matched to one another. The active-bias circuit can directly be attached to the voltage supply ports in the circuit diagram as shown above (V_{dd} and V_{gg}).



Outline Drawing



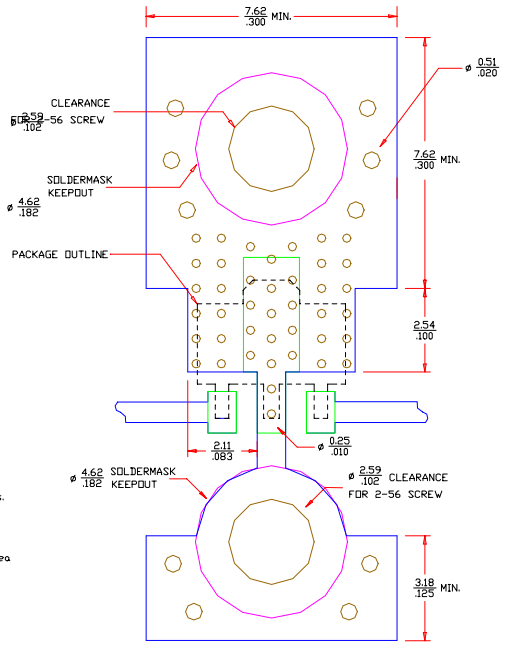
Land Pattern



FUNCTION	PIN NO.
INPUT	1
GROUND	2
OUTPUT (BIAS)	3
GROUND	4

Notes:
1. Ground vias are critical for thermal and RF grounding considerations.
2. Two 2-56 screws with washers should be used for thermal grounding to the main chassis.
3. Ground plane on the backside should extend past the holes for the 2-56 screws as a minimum.
4. No soldermask should be applied to the backside where heat sink area contacts the main chassis.
5. Holes for the 2-56 screws should be plated through.
6. Keepout diameter for the 2-56 screw is to allow good thermal contact for the screw and washer.
7. Trace width depends on PC board.
8. A minimum of 1 oz. / 1 oz. copper should be used.

Mounting Configuration



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