Document Title

1M x 16 bit Super Low Power and Low Voltage Full CMOS RAM

Revision History

Revision No.	History	Draft date	Remark
0.0	Initial Draft	Apr.19th, 2006	Preliminary
0.1	Revised P/N according to the new P/N system	Jun.01st , 2006	Preliminary

1M x 16 bit Super Low Power and Low Voltage Full CMOS RAM

FEATURES

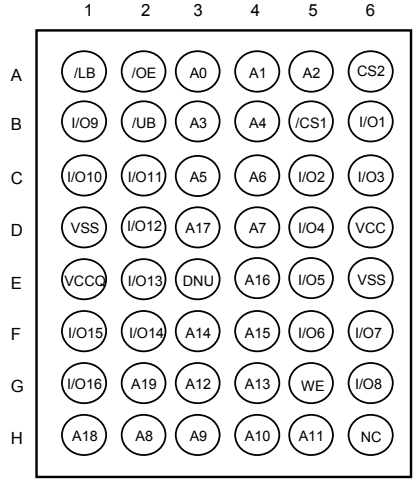
- Process Technology : Full CMOS
- Organization : 1M x 16
- Power Supply Voltage : 1.7~1.95V
- Dual CS & Page Modes
  - FMP1617CC0 : Dual CS
  - FMP1617CC7 : Page mode with Dual CS
- Operating Temperature Ranges:
  - Special (-10'C to +60'C)
  - Commercial (0'C to +70'C)
  - Extended (-25'C to +85'C)
  - Industrial (-40'C to +85'C)
- Three state output and TTL Compatible
- Package Type : 48-FBGA-6.00x8.00 mm²
  - FMP1617CC0(7)-FxxX : Normal
  - FMP1617CC0(7)-GxxX : Pb-Free
  - FMP1617CC0(7)-HxxX : Pb-Free & Halogen Free
- Separated I/O power(VCCQ) & Core Power(VCC)
- Easy memory expansion with /CS1, CS2, and /OE features
- Automatic power-down when deselected

PRODUCT FAMILY

Product Family	Operating Voltage (V)			Speed	Power Dissipation					
					ICC1		ICC2		ISB1 (CMOS Standby Current)	
					f = 1MHz		f = fmax			
	Min.	Typ.	Max.		Typ.	Max.	Typ.	Max.	Typ.	Max.
FMP1617CC0(7)-G60E FMP1617CC0(7)-G70E	1.7	1.8	1.95	70ns 85ns	1.5mA	3mA	15mA 12mA	20mA	**70uA**	**100uA**

1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at Vcc = Vcc (typ) and T_A = 25C.
2. F=FBGA, G=FBGA(Pb-Free), H=FBGA(Pb-Free & Halogen Free), W=WAFER
3. Operating Temperature Range: S (-10'C~60'C), C(0'C~70'C), E(-25'C~85'C), I (-40'C~85'C)

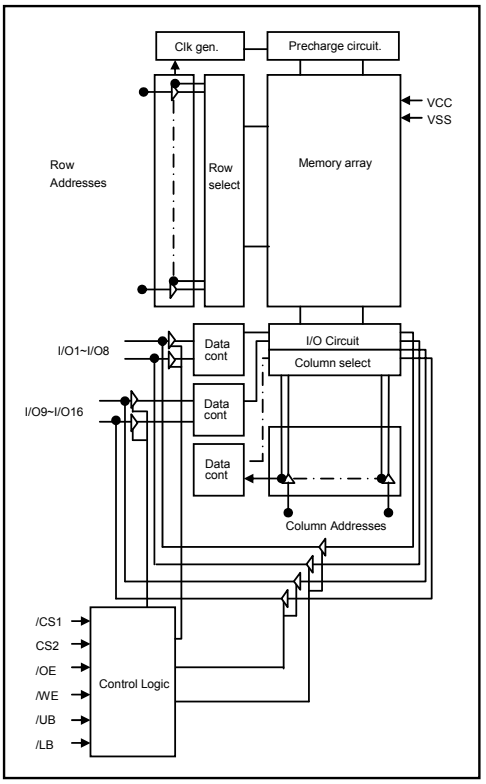
PIN DESCRIPTION



48-FBGA : Top View(Ball Down)

Name	Function	Name	Function
CS2	Chip Select Input	VCC	Core Power
/CS1	Chip Select Input	VCCQ	I/O Power
/OE	Output Enable Input	VSS	Ground
/WE	Write Enable Input	/UB	Upper Byte(I/O9~16)
A0~A19	Address Inputs	/LB	Lower Byte(I/O 1~8)
I/O1~I/O16	Data Inputs/Outputs	DNU	Do Not Use

FUNCTIONAL BLOCK DIAGRAM



PRODUCT LIST

Part Name	Function
FMP1617CC0(7)-G70E	48-FBGA, 70ns, VCC=1.8V, VCCQ=1.8V
FMP1617CC0(7)-G85E	48-FBGA, 85ns, VCC=1.8V, VCCQ=1.8V

1. F=FBGA, G=FBGA(Pb-Free), H=FBGA(Pb-Free & Halogen Free), W=WAFER
2. Operating Temperature Range: S (-10'C~60'C), C(0'C~70'C), E(-25'C~85'C), I (-40'C~85'C)

FUNCTIONAL DESCRIPTION

/CS1	CS2	/OE	/WE	/LB	/UB	I/O1-8	I/O9-16	Mode	Power
H	H	X[1]	X[1]	X[1]	X[1]	High-Z	High-Z	Deselect/Power-down	Standby
X[1]	L	X[1]	X[1]	X[1]	X[1]	High-Z	High-Z	Deselect/Power-down	Standby
X[1]	H	X[1]	X[1]	H	H	High-Z	High-Z	Deselect/Power-down	Standby
L	H	H	H	L	X[1]	High-Z	High-Z	Output Disabled	Active
	H	H	H	X[1]	L	High-Z	High-Z	Output Disabled	Active
L	H	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
				H	L	High-Z	Dout	Upper Byte Read	Active
				L	L	Dout	Dout	Word Read	Active
		X[1]	L	L	H	Din	High-Z	Lower Byte Write	Active
				H	L	High-Z	Din	Upper Byte Write	Active
				L	L	Din	Din	Word Write	Active

1. X means don't care.(Must be low or high state)

ABSOLUTE MAXIMUM RATINGS[1]

Item	Symbol	Ratings	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.2 to Vcc+0.3V	V
Voltage on Vcc supply relative to Vss	Vcc	-0.2 to 3.6	V
Power Dissipation	P_D	1.0	W
Storage temperature	T_{STG}	-65 to 150	'C

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	FMP1617CC		Unit
		Min	Max	
Supply voltage	V_{CC}	1.7	1.95	V
I/O operating voltage (VCCQ ≤ VCC)	V_{CCQ}	1.7	1.95	V
Ground	V_{SS}	0	0	V
Input high voltage	V_{IH}	0.8VCCQ	VCC+0.2[1]	V
Input low voltage	V_{IL}	-0.2[2]	0.2VCCQ	V

Note :
1. Overshoot : Vcc+1.0V in case of pulse width≤20ns.
2. Undershoot : -1.0V in case of pulse width≤20ns.
3. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE[1] (f=1MHz , T_A=25'C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	CIN	VIN=0V	-	8	pF
Input/Output capacitance	CIO	VIO=0V	-	8	pF

1. Capacitance is sampled, not 100% tested.

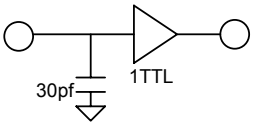
DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Input leakage current	ILI	VIN=VSS to VCC	-1	-	1	uA
Output leakage current	ILO	/CS=VIH, CS2=VIH, /OE=VIH or /WE=VIL, VIO=VSS to VCC	-1	-	1	uA
Average operating current	ICC1	Cycle time=1us, 100%duty, IIO=0mA, /CS≤0.2V, CS2=VIH, VIN≤0.2V or VIN≥VCC-0.2V	-	-	3	mA
	ICC2	Cycle time=Min, IIO=0mA, 100% duty, /CS=VIL, CS2=VIH, VIN=VIL or VIH	-	-	20	mA
Output low voltage	VOL	IOL=0.5mA			0.2VCCQ	V
Output high voltage	VOH	IOH=-0.5mA	0.8VCCQ			V
Standby Current(TTL)	ISB	/CS=VIH, CS2=VIH, Other inputs=VIH or VIL	-	-	0.3	mA
Standby Current(CMOS)	ISB1	/CS≥VCC-0.2V, CS2≤0.2V, Other inputs=0~VCC	-	-	100	uA

Operating Range

Device	Range	Ambient Temperature	V_{DD}	V_{DDQ}
FMP1617CC0(7)-XxxS	Special	-10℃ to +60℃	1.7V to 1.95V	1.7V to 1.95V
FMP1617CC0(7)-XxxC	Commercial	0℃ to +70℃		
FMP1617CC0(7)-XxxE	Extended	-25℃ to +85℃		
FMP1617CC0(7)-XxxI	Industrial	-40℃ to +85℃		

AC OPERATING CONDITIONS



TEST CONDITIONS(Test Load and Input/Output Reference)

Input pulse level : 0.2 to VCC-0.2V
Input rising and falling time : 5ns
Input and output reference voltage : 0.5*VCCQ
Output load(see right) : CL=30pF+1TTL

AC CHARACTERISTICS(VCC=1.7V~1.95V)

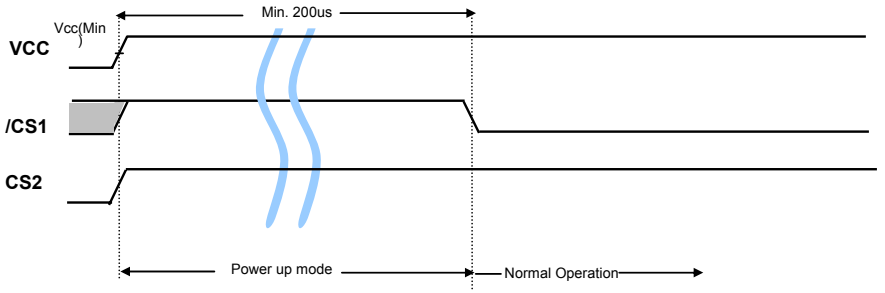
Parameter List		Symbol	Speed Bins				Units
			70ns		85ns		
			Min	Max	Min	Max	
Read	Read Cycle Time	tRC	70	20k	85	20k	ns
	Address Access Time	tAA	-	70	-	85	ns
	Chip Select to Output	tCO	-	70	-	85	ns
	Output Enable to Valid Output	tOE	-	25	-	30	ns
	/UB, /LB Access Time	tBA	-	70	-	85	ns
	Chip Select to Low-Z Output	tLZ	10	-	10	-	ns
	/UB, /LB Enable to Low-Z Output	tBLZ	10	-	10	-	ns
	Output Enable to Low-Z Output	tOLZ	5	-	5	-	ns
	Chip Disable to High- Z Output	tHZ	0	5	0	5	ns
	/UB, /LB Disable to High- Z Output	tBHZ	0	5	0	5	ns
	Output Disable to High- Z Output	tOHZ	0	5	0	5	ns
	Output Hold from Address Change	tOH	5	-	5	-	ns
Write	Write Cycle Time	tWC	70	20k	85	20k	ns
	Chip Select to End of Write	tCW	60	-	70	-	ns
	Address Set-up Time	tAS	0	-	0	-	ns
	Address Valid to End of Write	tAW	60	-	70	-	ns
	/UB, /LB Valid to End of Write	tBW	60	-	70	-	ns
	Write Pulse Width	tWP	50	-	60	-	ns
	Write Recovery Time	tWR	0	-	0	-	ns
	Write to Output High-Z	tWHZ	0	5	0	5	ns
	Data to Write Time Overlap	tDW	20	-	20	-	ns
	Data Hold from Write Time	tDH	0	-	0	-	ns
	End Write to Output Low-Z	tOW	5	-	5	-	ns
Page	Page Mode Cycle Time	tPC	25	-	30	-	ns
	Page Mode Address Access Time	tPAA	-	25	-	30	ns
	Maximum Cycle Time	tMRC	-	20k	-	20k	ns
/CS High Pulse Width		tCP	10	-	10	-	ns

1. /CS High Pulse Width is defined by /CS or (/UB and /LB) because /UB & /LB can make standby mode when /UB=High and /LB=High.

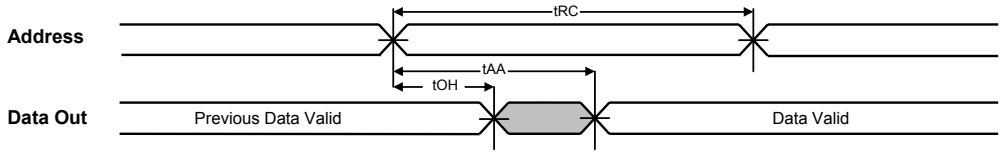
Power Up Sequence

1. Apply Power.
2. Maintain stable power for a minimum of 200us with /CS1=VIH and CS2=VIH.

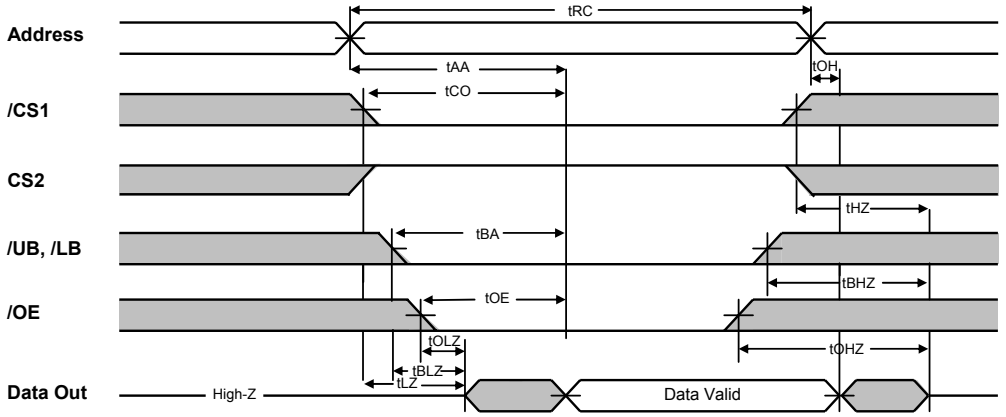
Timing Waveform of Power Up



READ CYCLE (1) (Address controlled,/CS1=/OE=VIL, CS2=/WE=VIH, /UB or/and /LB=VIL)

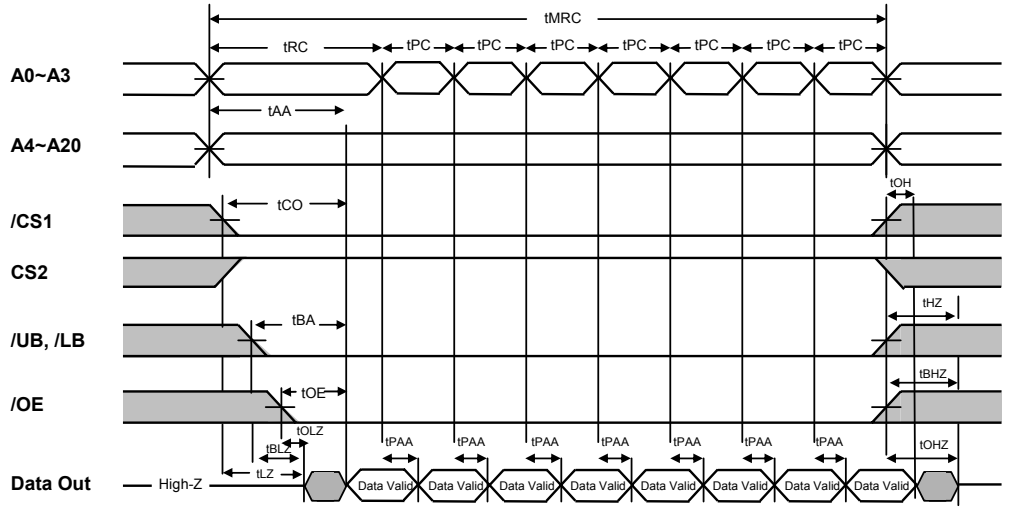


READ CYCLE (2) (CS2=/WE=VIH)



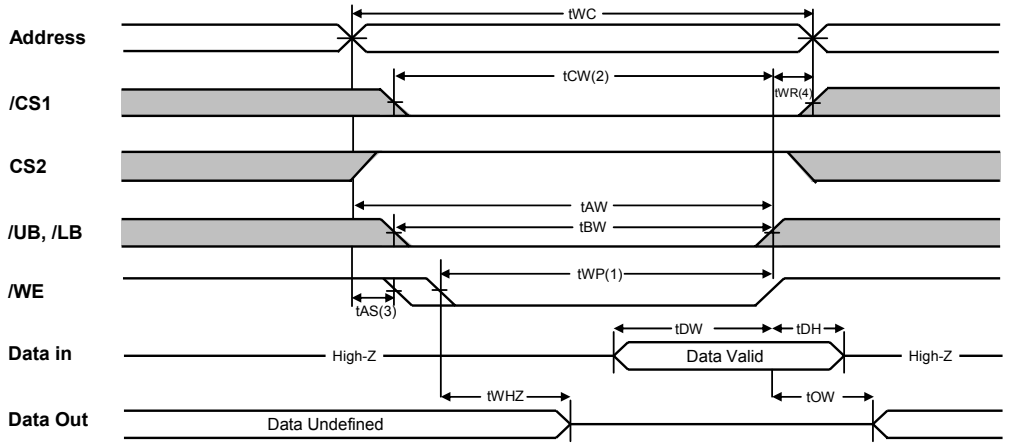
1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, tHZ(Max.) is less than tLZ(Min.) both for a given device and from device to device interconnection.
3. Do not access device with cycle timing shorter than tRC(tWC) for continuous periods > 20us.

PAGE READ CYCLE (CS2=/WE=VIH, 16 words access)

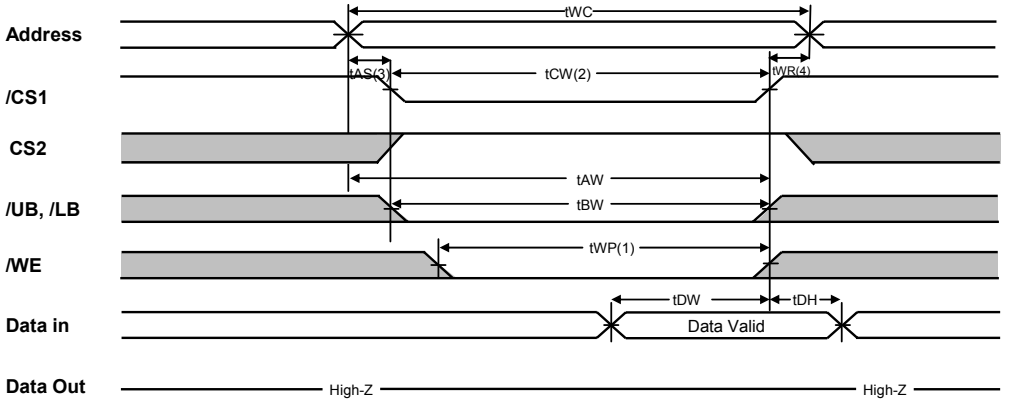


1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, tHZ(Max.) is less than tLZ(Min.) both for a given device and from device to device interconnection.
3. Do not access device with cycle timing shorter than tRC(tWC) for continuous periods > 20us.
4. In case page address skew is over 3ns, tPAA will be out of spec.

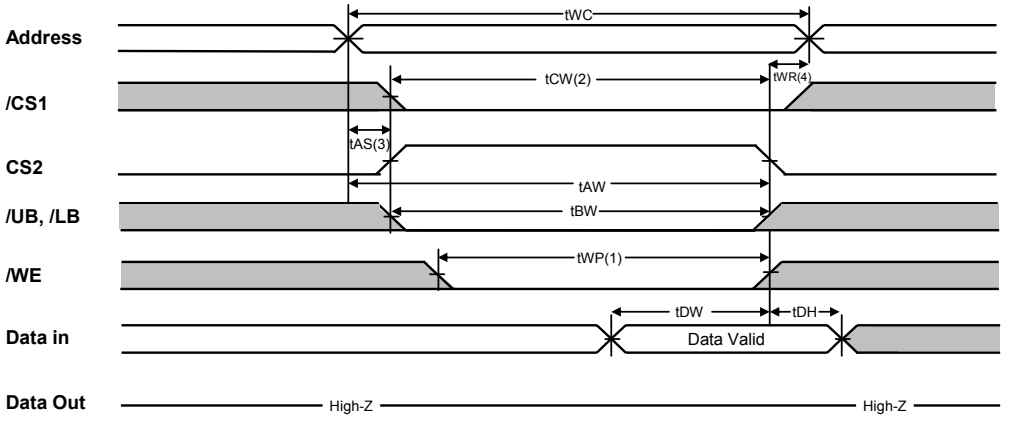
WRITE CYCLE (1) (/WE controlled)



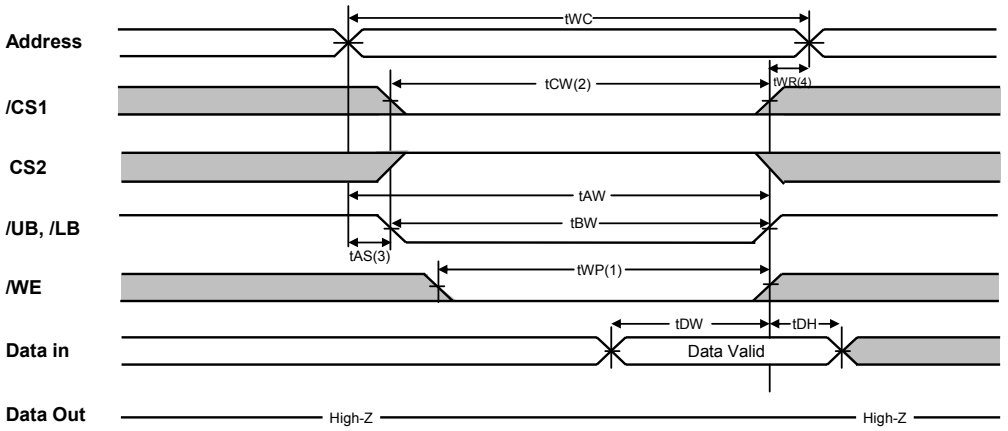
WRITE CYCLE (2) (/CS1 controlled)



WRITE CYCLE (3) (CS2 controlled)

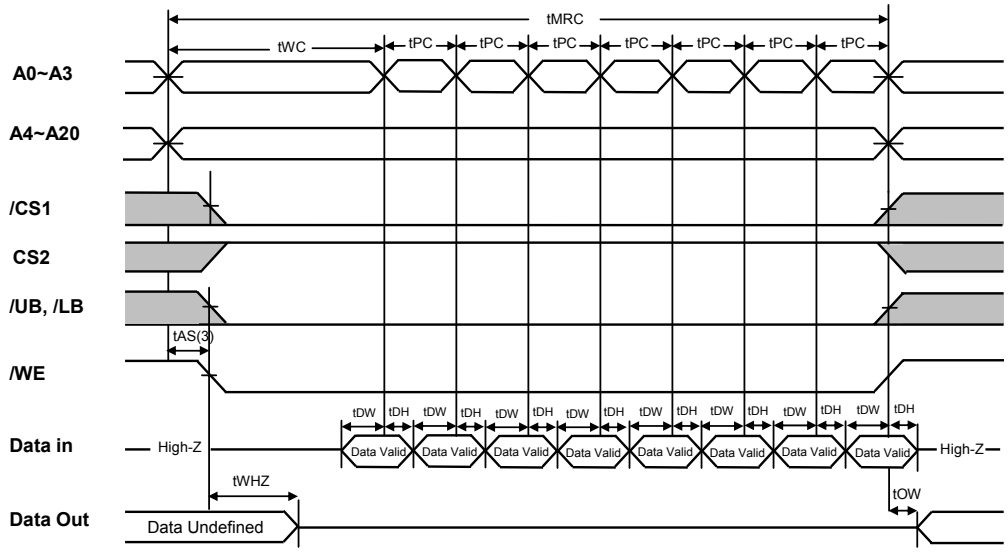


WRITE CYCLE (4) (/UB, /LB controlled)



1. A write occurs during the overlap (tWP) of low /CS and /WE. A write begins when /CS goes low and /WE goes low with asserting /UB or /LB for single byte operation or simultaneously asserting /UB and /LB for double byte operation. A write ends at the earliest transition when /CS goes high and /WE goes high. The tWP is measured from the beginning of write to the end of write.
2. tCW is measured from the /CS going low to end of write.
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tWR applied in case a write ends as /CS or /WE going high.
5. Do not access device with cycle timing shorter than tRC(tWC) for continuous periods > 20us.

PAGE WRITE CYCLE (Address controlled, CS2=VIH)



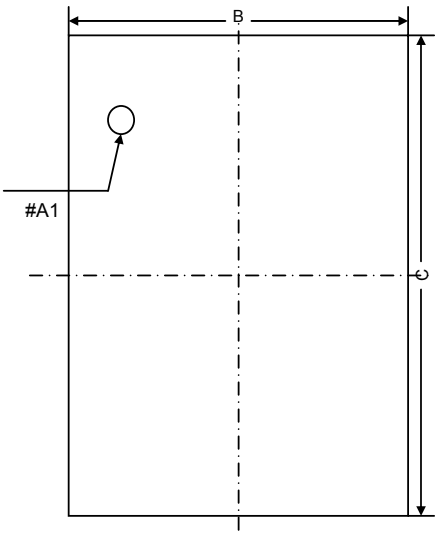
1. A write occurs during the overlap (tWP) of low /CS and /WE. A write begins when /CS goes low and /WE goes low with asserting /UB or /LB for single byte operation or simultaneously asserting /UB and /LB for double byte operation. A write ends at the earliest transition when /CS goes high and /WE goes high. The tWP is measured from the beginning of write to the end of write.
2. tCW is measured from the /CS going low to end of write.
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tWR applied in case a write ends as /CS or /WE going high.
5. Do not access device with cycle timing shorter than tRC(tWC) for continuous periods > 20us.
6. In case page address is over 3ns, write to the invalid address can occur.

PACKAGE DIMENSION

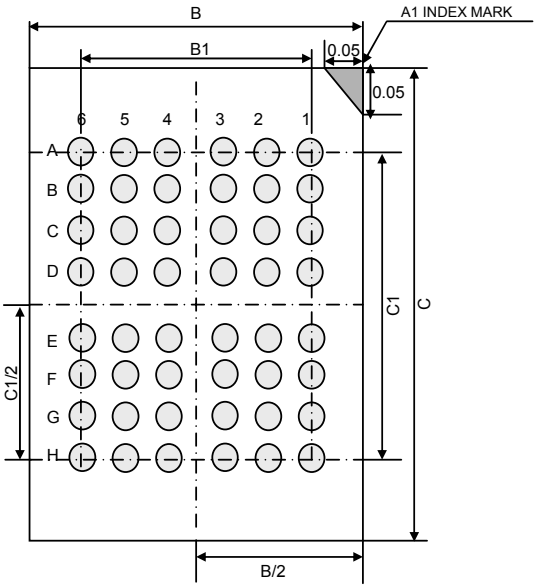
Unit : millimeters

48 BALL FINE PITCH BGA(0.75mm ball pitch)

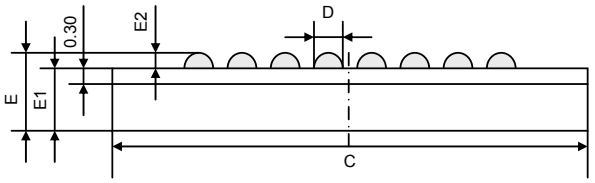
Top View



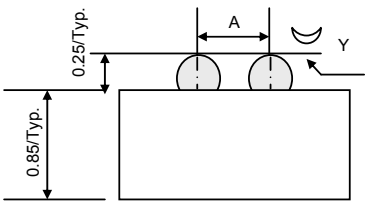
Bottom View



Side View



Detail A



-	Min	Typ	Max
A	-	0.75	-
B	5.90	6.00	6.10
B1	-	3.75	-
C	7.90	8.00	8.10
C1	-	5.25	-
D	0.30	0.35	0.40
E	-	1.10	1.20
E1	-	0.85	-
E2	0.20	0.25	0.30
Y	-	-	0.08

NOTES.

1. Bump counts : 48(8row x 6column)
2. Bump pitch : (x,y)=(0.75 x 0.75)(typ.)
3. All tolerance are +/-0.050 unless otherwise specified.
4. Typ : Typical
5. Y is coplanarity : 0.08(Max)