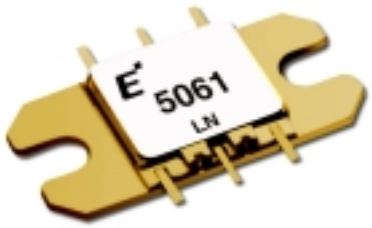
FMM5061VF

X-Band Power Amplifier MMIC

FEATURES

- High Output Power: Pout=33.0dBm (typ.)
- High Linear Gain: GL=27.0dB (typ.)
- Broad Band: 9.5~13.3GHz
- Impedance Matched Zin/Zout=50Ω
- Small Hermetic Metal-Ceramic Package(VF)



DESCRIPTION

The FMM5061VF is a MMIC amplifier that contains a three-stage amplifier, internally matched, for standard communications band in the 9.5 to 13.3GHz frequency range.

Eudyna Devices's stringent Quality Assurance Program assures the highest reliability and consistent performance.

ABSOLUTE MAXIMUM RATING

Item	Symbol	Condition	Rating	Unit
Drain-Source Voltage	V_{DD}		10	V
Gate-Source Voltage	V_{GG}		-7	V
Input Power	P_{in}		26	dBm
Channel Temperature	T_{ch}		+175	°C
Storage Temperature	T_{stg}		-55~125	°C

RECOMMENDED OPERATING CONDITION

Item	Symbol	Condition	Recommend	Unit
Drain-Source Voltage	V_{DD}		6	V
Gate-Source Voltage	V_{GG}		-5	V
Input Power	P_{in}		≤12	dBm
Operating Case Temperature	T_C		-40~+85	°C

ELECTRICAL CHARACTERISTICS (Case Temperature T_C =25°C)

Item	Symbol	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
Frequency Range	f	V_{DD}=6V	9.5	-	13.3	GHz
Output Power at 1dB G.C.P.	P_{1dB}	V_{GG}=-5V	31*1	33*1	-	dBm
		Z_s=Z_l=50ohm	29*2	31*2	-	
Power Gain at 1dB G.C.P.	G_{1dB}	*1:f=9.5~11.7GHz	24*1	26*1	-	dB
		*2:f=11.7~13.3GHz	22*2	24*2	-	
Power-added Efficiency at 1dB G.C.P.	η_{add}		-	21*1	-	%
			-	15*2	-	
Third Order Intermodulation*	IM_3	*3:Δf=10MHz ,	-42*3	-45*3	-	dBc
Drain Current at 1dB G.C.P.	I_{DD}	2-Tone Test,	-	1700*1	2400*1	mA
		P_{out}=19dBm S.C.L.	-	1500*2	2400*2	mA
Gate Current	I_{GG}		-	25	-	mA
Input Return Loss (at Pin=-20dBm)	RL_{in}		-	-8	-	dB
Output Return Loss (at Pin=-20dBm)	RL_{out}		-	-8	-	dB

CASE STYLE: VF

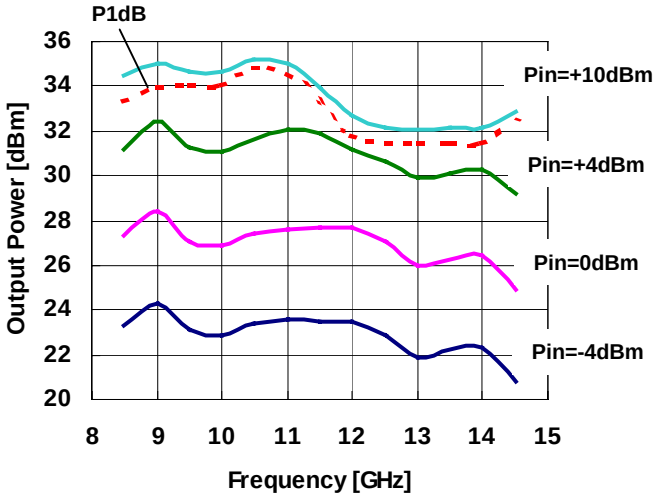
G.C.P.:Gain Compression Point, S.C.L.:Single Carrier Level

ESD	Class 0	~ 199 V

Note : Based on EIAJ ED-4701 C-111A(C=100pF, R=1.5kΩ)

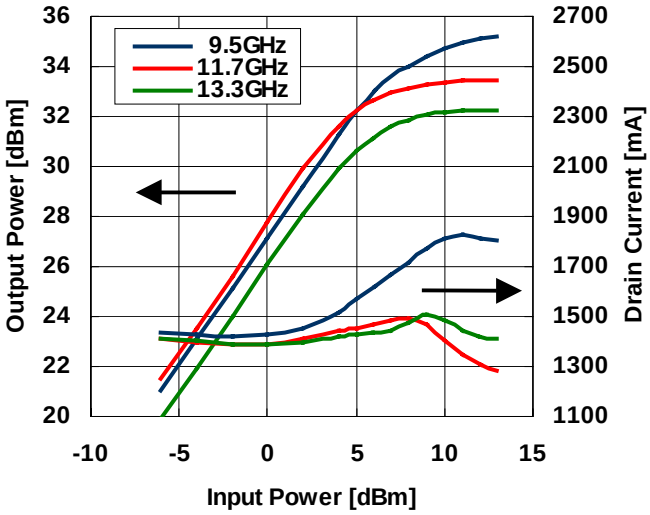
OUTPUT POWER vs. FREQUENCY

VDD=6V, VGG=-5V



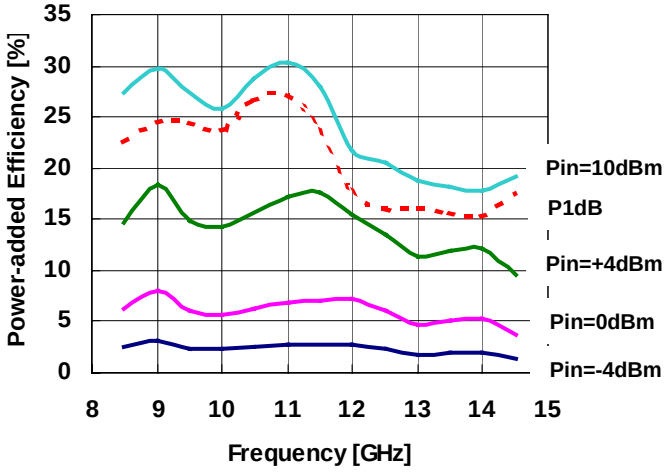
OUTPUT POWER , DRAIN CURRENT vs. INPUT POWER

VDD=6V, VGG=-5V



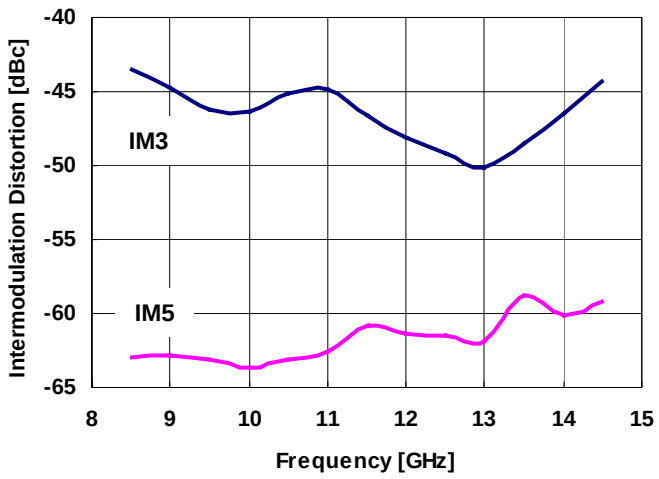
POWER ADDED EFFICIENCY vs FREQUENCY

VDD=6V, VGG=-5V



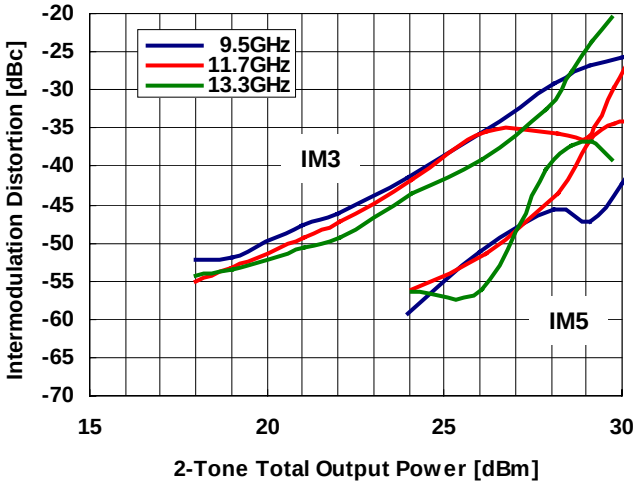
IMD vs. FREQUENCY

VDD=6V, VGG=-5V, Pout=19dBm S.C.L.



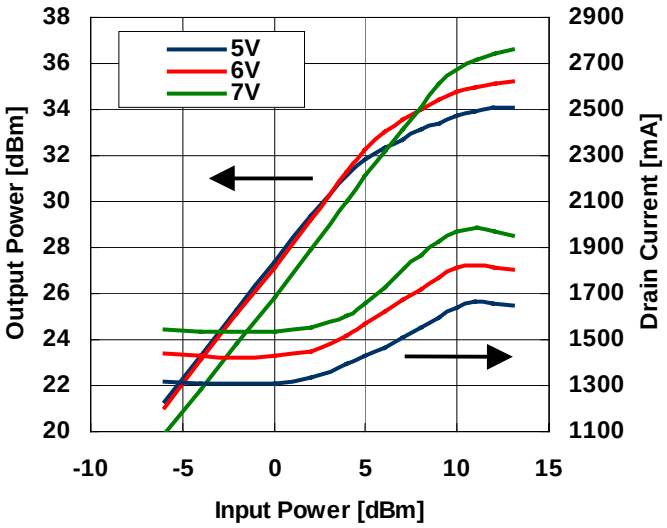
IMD vs OUTPUT POWER

VDD=6V, VGG=-5V



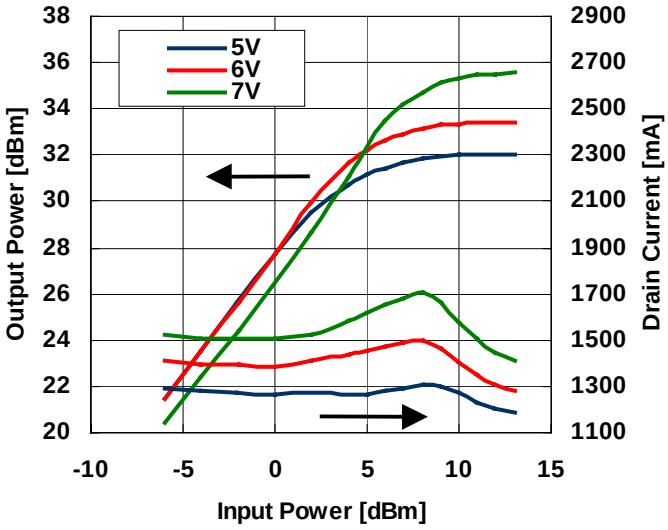
OUTPUT POWER, DRAIN CURRENT vs. INPUT POWER by Drain Voltage

VGG=-5V @9.5GHz



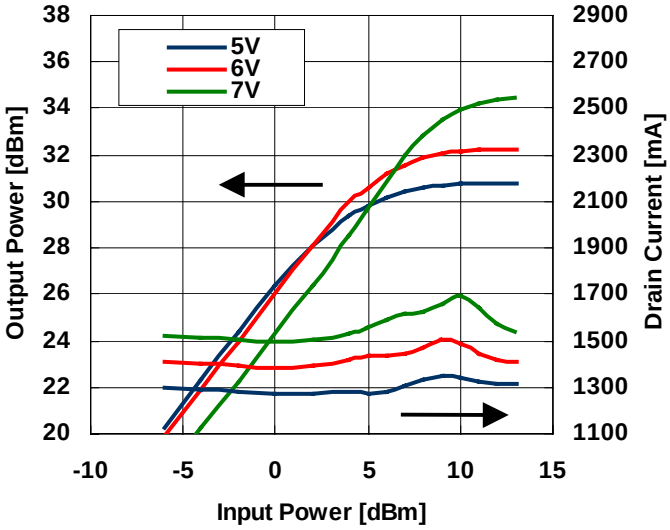
OUTPUT POWER, DRAIN CURRENT vs. INPUT POWER by Drain Voltage

VGG=-5V @11.7GHz



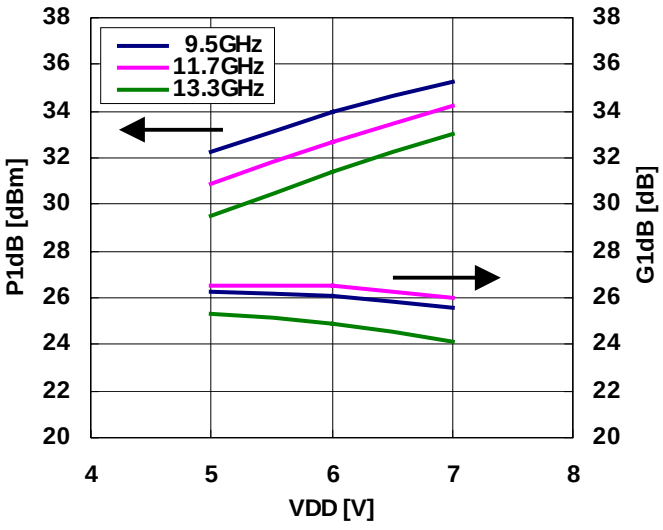
OUTPUT POWER, DRAIN CURRENT vs. INPUT POWER by Drain Voltage

VGG=-5V @13.3GHz



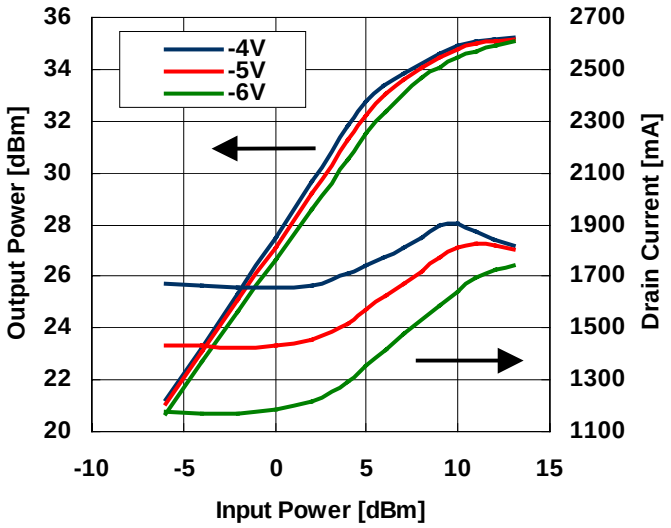
OUTPUT POWER, GAIN vs. DRAIN VOLTAGE

VGG=-5V



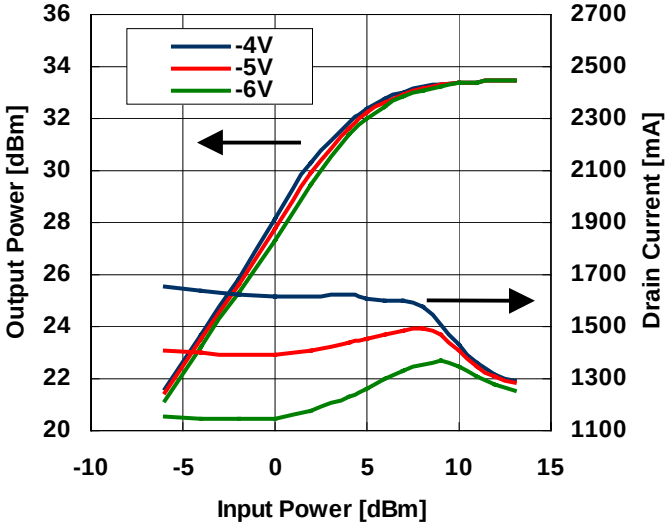
OUTPUT POWER, DRAIN CURRENT vs. INPUT POWER by Gate Voltage

VDD=6V @9.5GHz



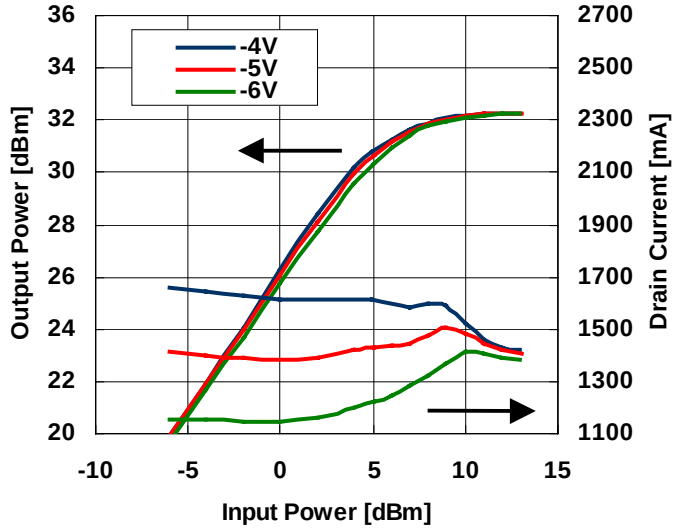
OUTPUT POWER, DRAIN CURRENT vs. INPUT POWER by Gate Voltage

VDD=6V @11.7GHz



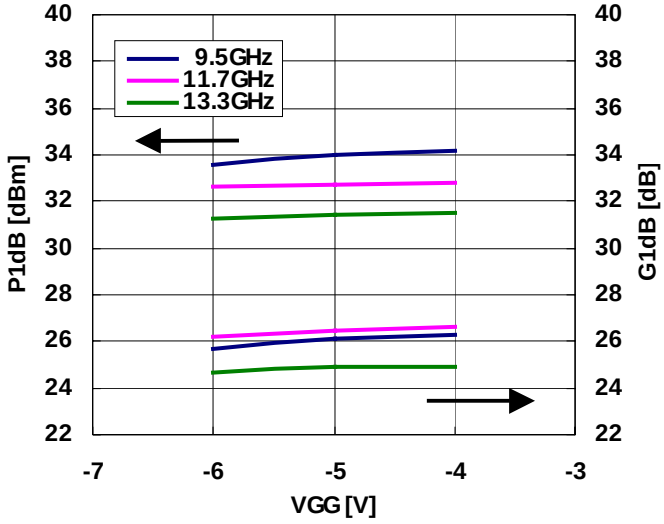
OUTPUT POWER, DRAIN CURRENT vs. INPUT POWER by Gate Voltage

VDD=6V @13.3GHz



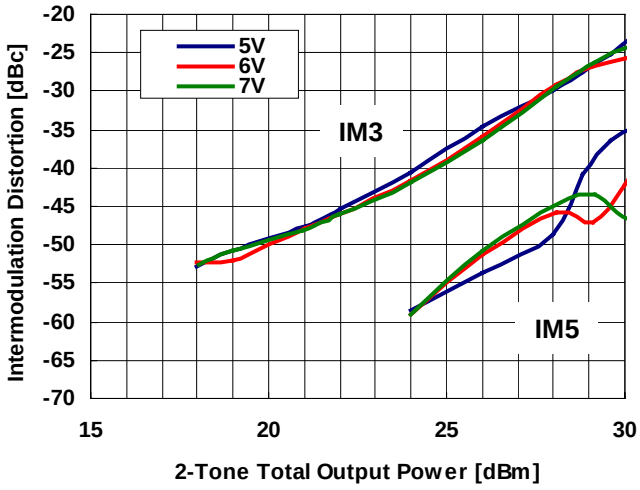
OUTPUT POWER, GAIN vs. GATE VOLTAGE

VDD=6V



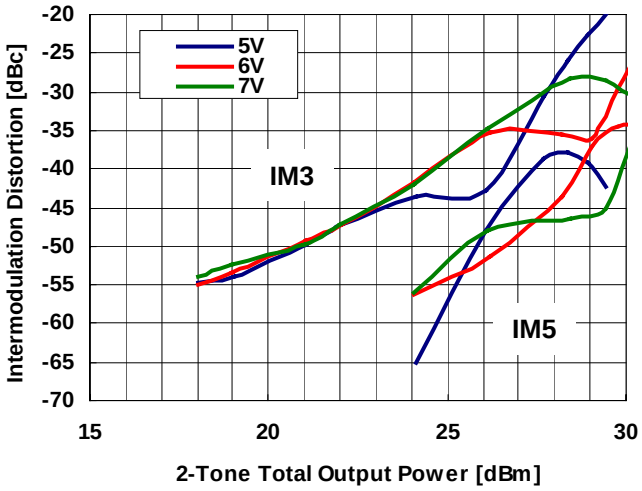
IMD PERFORMANCE vs OUTPUT POWER by Drain Voltage

VGG=-5V @9.5GHz



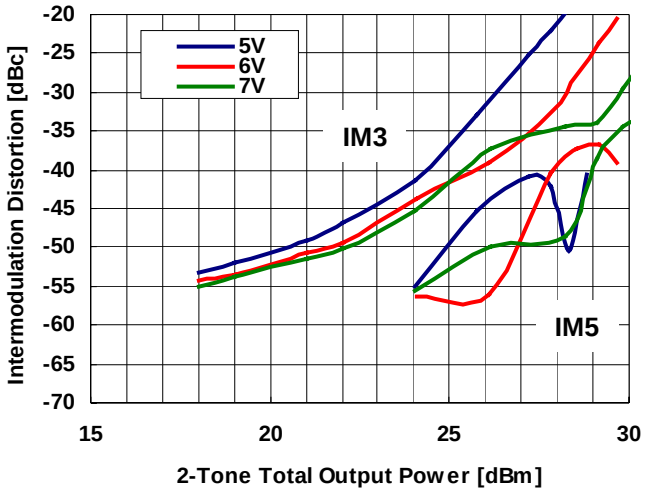
IMD PERFORMANCE vs OUTPUT POWER by Drain Voltage

VGG=-5V @11.7GHz



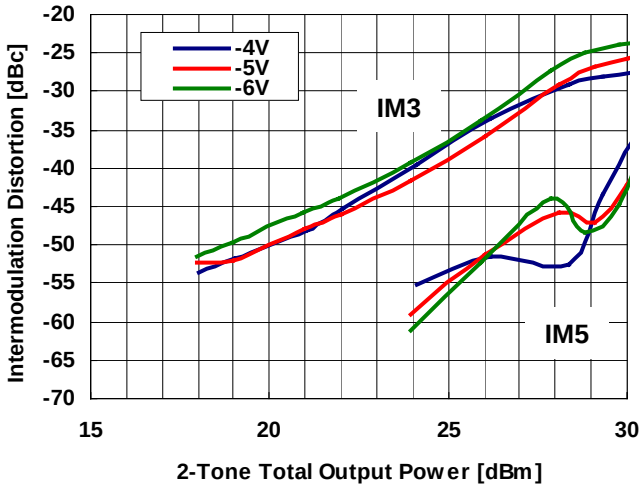
IMD PERFORMANCE vs OUTPUT POWER by Drain Voltage

VGG=-5V @13.3GHz



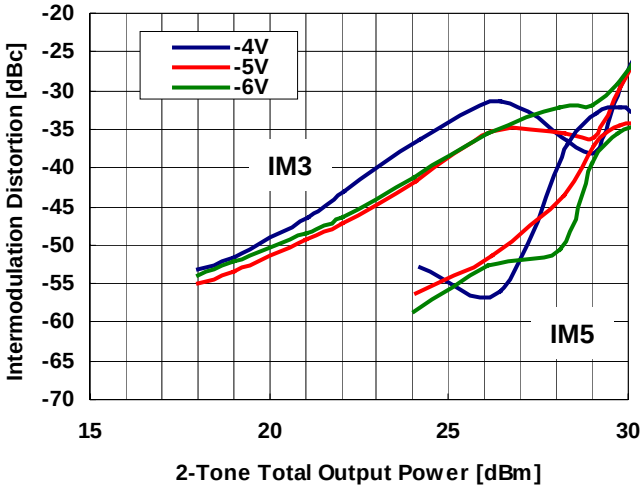
IMD PERFORMANCE vs OUTPUT POWER by Gate Voltage

VDD=6V @9.5GHz



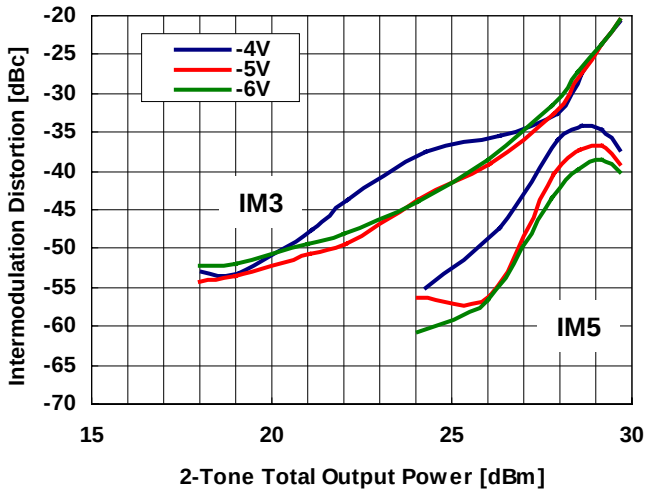
IMD PERFORMANCE vs OUTPUT POWER by Gate Voltage

VDD=6V @11.7GHz



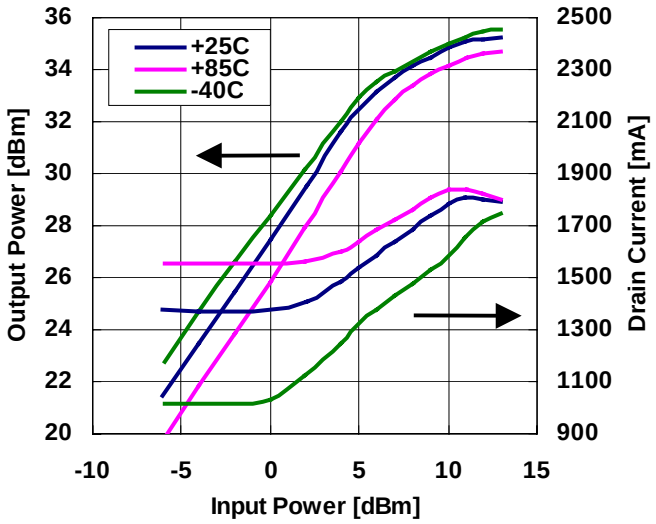
IMD PERFORMANCE vs OUTPUT POWER by Gate Voltage

VDD=6V @13.3GHz



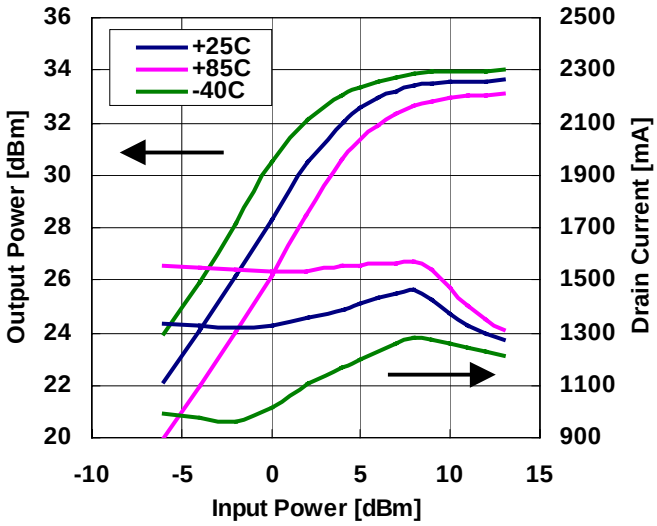
OUTPUT POWER, DRAIN CURRENT vs. INPUT POWER by Temperature

VDD=6V, VGG=-5V @9.5GHz



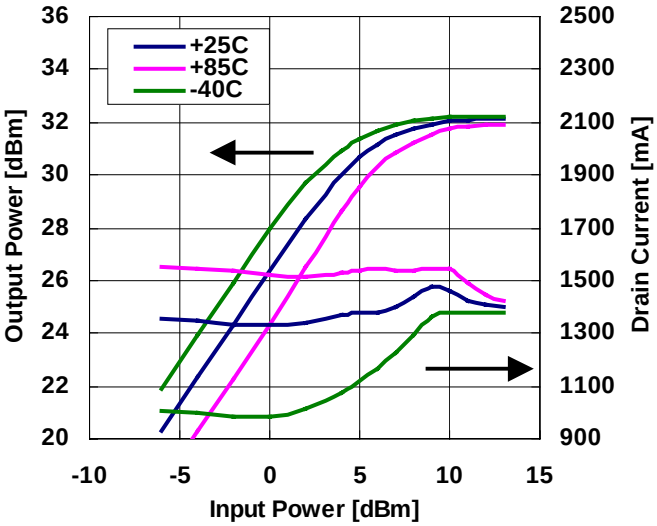
OUTPUT POWER, DRAIN CURRENT vs. INPUT POWER by Temperature

VDD=6V, VGG=-5V @11.7GHz



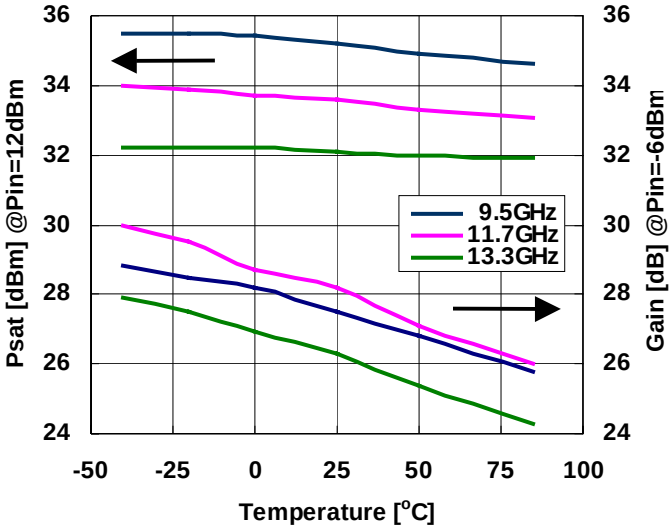
OUTPUT POWER, DRAIN CURRENT vs. INPUT POWER by Temperature

VDD=6V, VGG=-5V @13.3GHz

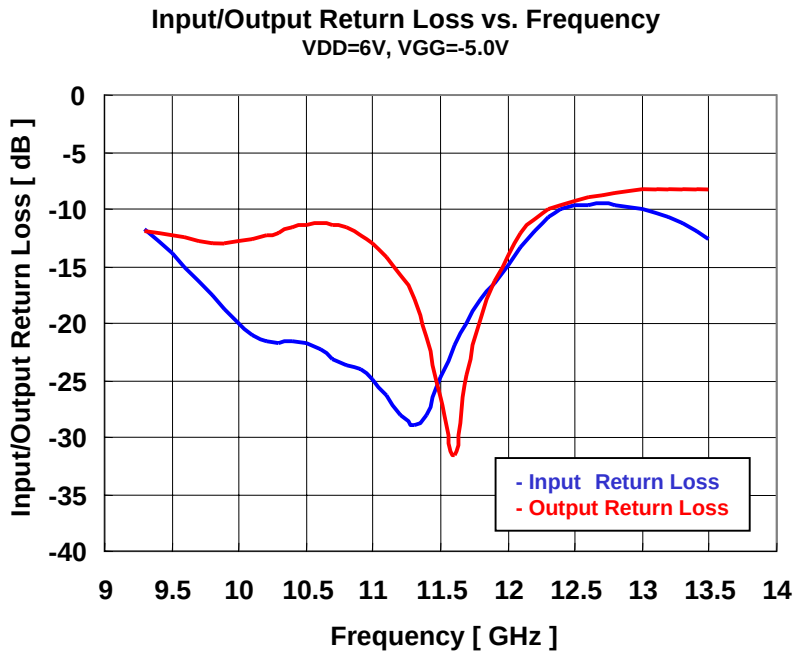


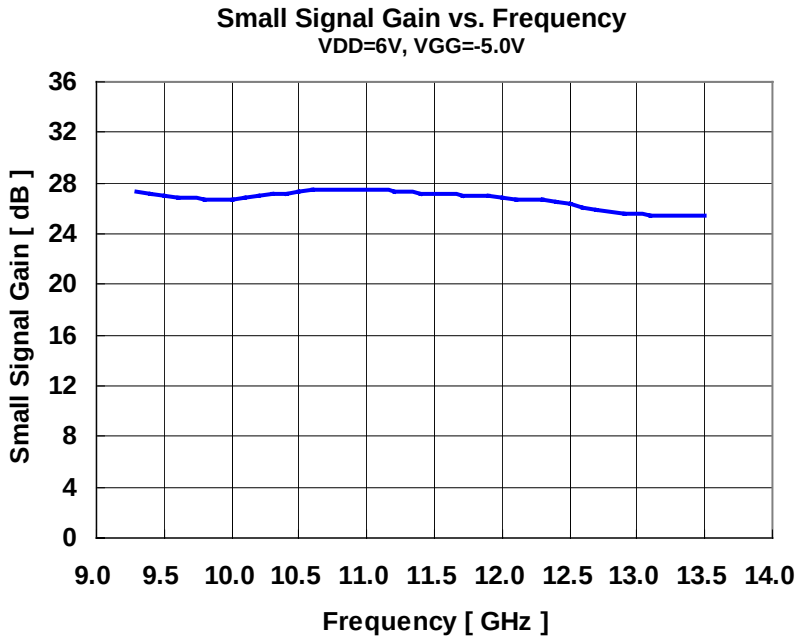
OUTPUT POWER, GAIN vs. TEMPERATURE

VDD=6V, VGG=-5V



■ S-PARAMETER


Input/Output Return Loss vs. Frequency
VDD=6V, VGG=-5.0V
Input/Output Return Loss [dB]
0
-5
-10
-15
-20
-25
-30
-35
-40
9
9.5
10
10.5
11
11.5
12
12.5
13
13.5
14
Frequency [GHz]
- Input Return Loss
- Output Return Loss


Small Signal Gain vs. Frequency
VDD=6V, VGG=-5.0V
Small Signal Gain [dB]
36
32
28
24
20
16
12
8
4
0
9.0
9.5
10.0
10.5
11.0
11.5
12.0
12.5
13.0
13.5
14.0
Frequency [GHz]

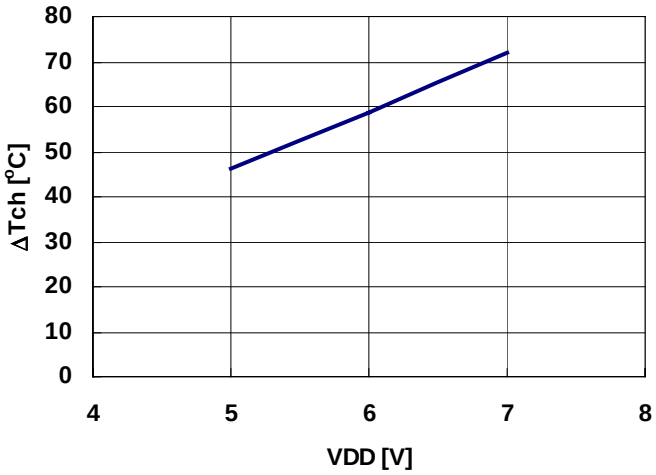
■ S-PARAMETER

VDD=6.0V, VGG=-5.0V

Frequency	S11		S21		S12		S22	
[GHz]	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
9.30	0.261	-99.9	23.106	-71.0	0.003	-155.4	0.252	-41.8
9.40	0.231	-104.9	22.787	-85.3	0.003	-162.6	0.250	-46.1
9.50	0.204	-107.9	22.461	-99.3	0.003	-166.3	0.243	-50.7
9.60	0.177	-111.0	22.034	-113.0	0.003	-169.3	0.236	-53.9
9.70	0.154	-114.3	21.842	-126.2	0.003	-168.3	0.228	-56.2
9.80	0.133	-116.1	21.705	-139.2	0.003	-170.0	0.225	-57.6
9.90	0.116	-114.8	21.602	-151.7	0.003	-175.1	0.225	-58.1
10.00	0.100	-112.4	21.781	-164.4	0.003	-179.7	0.228	-58.8
10.10	0.089	-108.2	21.916	-177.4	0.003	-179.4	0.232	-59.6
10.20	0.083	-103.6	22.244	169.8	0.003	178.1	0.241	-60.6
10.30	0.082	-98.8	22.665	156.8	0.003	174.8	0.250	-62.4
10.40	0.084	-96.7	22.982	143.4	0.003	169.9	0.261	-64.6
10.50	0.083	-97.2	23.362	129.3	0.003	168.6	0.272	-68.4
10.60	0.077	-97.2	23.583	115.3	0.003	171.2	0.275	-73.6
10.70	0.070	-97.8	23.710	101.3	0.002	172.9	0.271	-79.1
10.80	0.066	-96.7	23.685	87.6	0.003	176.6	0.261	-84.3
10.90	0.063	-95.5	23.626	73.4	0.003	174.2	0.244	-89.7
11.00	0.057	-93.2	23.536	59.2	0.003	173.1	0.223	-95.1
11.10	0.048	-86.6	23.513	46.0	0.003	172.1	0.196	-99.9
11.20	0.040	-74.5	23.249	32.3	0.003	176.4	0.163	-104.3
11.30	0.036	-52.8	23.074	18.8	0.003	173.4	0.128	-108.0
11.40	0.040	-30.0	22.920	4.9	0.003	171.7	0.087	-108.7
11.50	0.057	-19.9	22.825	-8.5	0.003	168.7	0.048	-99.7
11.60	0.080	-10.9	22.875	-22.0	0.003	167.8	0.027	-35.6
11.70	0.100	-11.2	22.517	-35.9	0.003	165.0	0.059	9.9
11.80	0.128	-12.8	22.305	-49.7	0.004	161.1	0.105	15.3
11.90	0.151	-14.1	22.229	-63.5	0.004	153.6	0.153	13.6
12.00	0.180	-18.9	21.987	-76.9	0.004	146.3	0.201	9.4
12.10	0.217	-22.2	21.654	-90.7	0.004	135.0	0.248	3.4
12.20	0.253	-27.9	21.530	-104.2	0.004	123.8	0.287	-3.3
12.30	0.294	-36.0	21.516	-118.9	0.003	110.5	0.315	-10.3
12.40	0.314	-45.8	21.151	-133.1	0.002	105.4	0.329	-15.4
12.50	0.328	-54.8	20.750	-146.8	0.002	107.4	0.342	-19.2
12.60	0.330	-62.1	19.987	-160.7	0.002	111.3	0.354	-22.1
12.70	0.334	-69.4	19.742	-174.6	0.002	113.0	0.364	-25.0
12.80	0.329	-75.1	19.461	172.1	0.002	117.2	0.374	-27.6
12.90	0.321	-82.9	19.175	158.9	0.002	112.3	0.380	-30.0
13.00	0.317	-88.7	18.916	145.3	0.001	111.7	0.386	-32.4
13.10	0.302	-95.8	18.807	131.9	0.001	114.6	0.389	-34.4
13.20	0.294	-102.4	18.700	117.4	0.001	110.7	0.390	-36.1
13.30	0.272	-109.3	18.763	104.0	0.001	104.2	0.390	-38.1
13.40	0.256	-118.4	18.833	89.6	0.001	110.1	0.389	-39.4
13.50	0.234	-125.4	18.766	74.6	0.001	108.7	0.387	-40.6

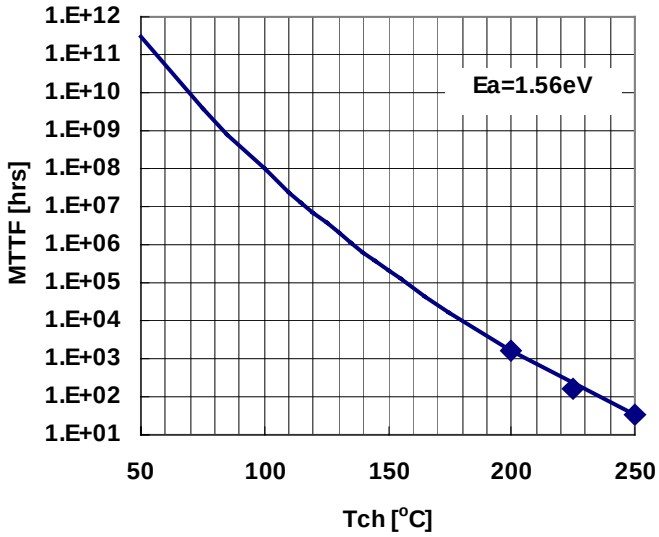
ΔTch vs. DRAIN VOLTAGE
(Reference Data)

VGG=-5V



Note : ΔTch : Case to Channel Temperature Rise

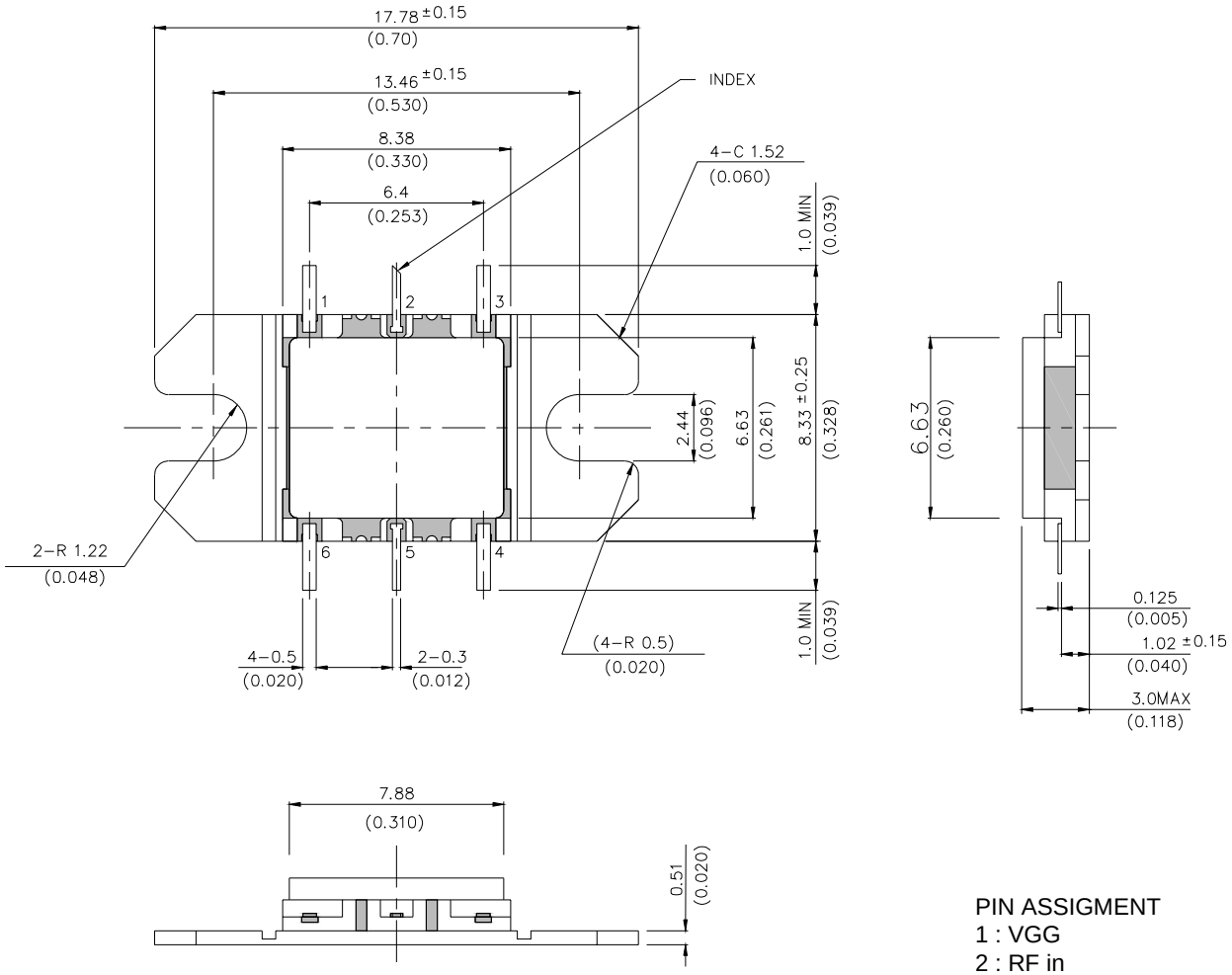
MTTF vs. Tch



FMM5061VF

X-band Power Amplifier MMIC

■ Package Out Line



PIN ASSIGMENT
1 : VGG
2 : RF in
3 : N.C.
4 : VDD
5 : RF out
6 : VDD

■ Mounting Instructions for VF Package

1. Screw Mounting

(1) The flange of package may be attached using screws. Torque conditions are shown in table 1.

Table 1. Recommended and Maximum Torque for Screw Mounting

Package	Recommended screw	Recommended Torque	Maximum Torque
VF	M2.0	10 N-cm (0.9 lb-in)	15 N-cm (1.3 lb-in)

(2) First, tighten the screws with a torque driver set to 5 N-cm.

(3) The surface finish of the heat sink should be better than 0.8 μm, and the surface flatness must be better than 10 μm.

(4) Silicon based heat sink compounds should not be used for thermal conductive grease. They cause poor grounding of the source flange, contamination and long term degradation of thermal resistance between the FET package and heat sink.

2. Solder Mounting

(1) Recommended solder are Tin-Lead solder (63Sn/37Pb), Lead-Free solder (Sn-3.0Ag-0.5Cu)*[1] or equivalent.

(2) For soldering, Tin-Lead solder (63Sn/37Pb) or Lead-Free solder (Sn-3.0Ag-0.5Cu)*[1] shall be used. (*1: The figure displays with weight %. A predominantly tin-rich alloy with 3.0% silver and 0.5% copper.)

(3) Recommended Flux is Rosin type with chlorine content: 0.2% or less and a low halogen content. After soldering, the flux residue should be removed by appropriate cleaning methods.

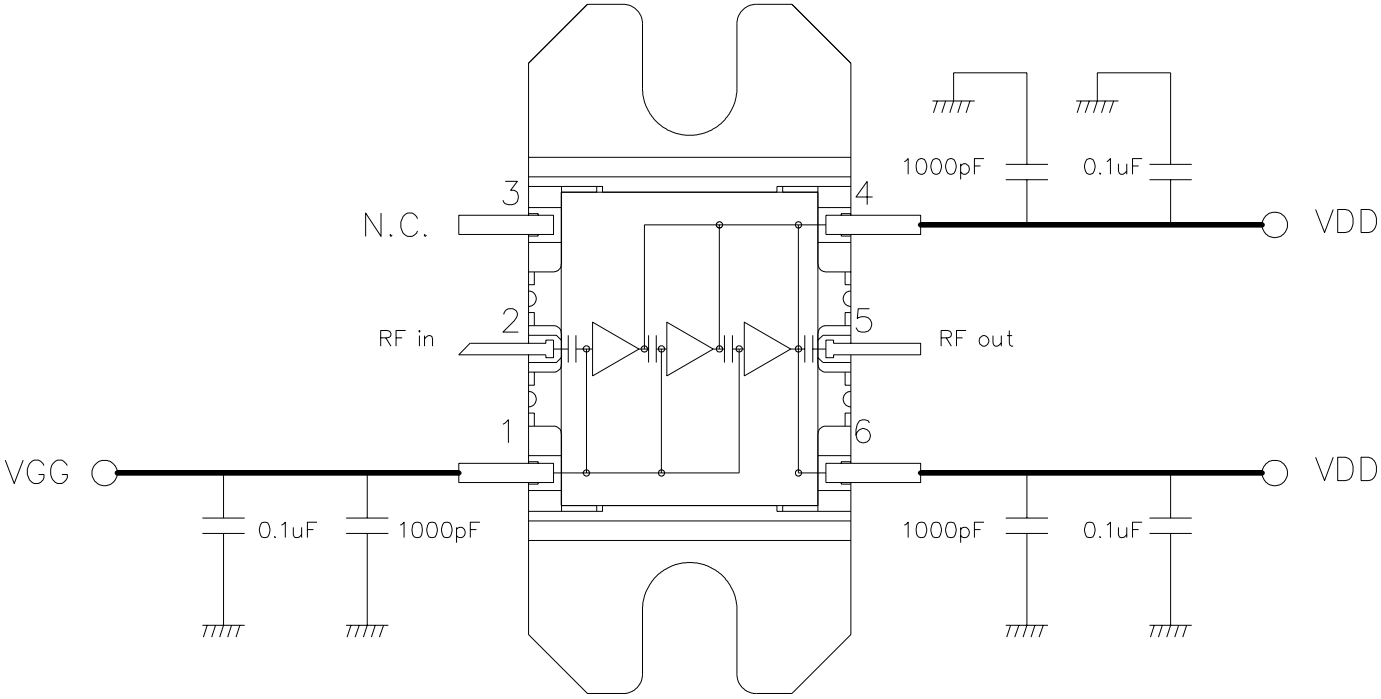
(4) The recommended soldering conditions are as follows:

Partial heating method (soldering iron, spot laser/air)

Product terminal temperature: 260 deg-C, max. 10 s./terminal

or 400 deg-C, max. 3 s./terminal

■ **Recommended board layout**



PIN ASSIGMENT
1 : VGG
2 : RF in
3 : N.C.
4 : VDD
5 : RF out
6 : VDD

Note 1: The capacitors are recommended on the bias supply line, close to the package, in order to prevent video oscillations which could damage the module.
Note 2: Two pins named VDD are internally connected.

Eudyna Devices USA Inc.
2355 Zanker Rd.
San Jose, CA 95131-1138, U.S.A.
TEL: (408) 232-9500
FAX: (408) 428-9111
www.us.eudyna.com

Eudyna Devices Europe Ltd.
Network House
Norreys Drive
Maidenhead, Berkshire SL6 4FJ
United Kingdom
TEL: +44 (0) 1628 504800
FAX: +44 (0) 1628 504888

Eudyna Devices Asia Pte. Ltd.
Hong Kong Branch
Rm.1101,Ocean Centre, 5 Canton Road
Tsim Sha Tsui, Kowloon, Hong Kong
TEL: +852-2377-0227
FAX: +852-2377-3921

Eudyna Devices Inc.
1000 Kamisukiahara, showa-cho
Nakakomagun, Yamanashi
409-3883, Japan
(Kokubo Industrial Park)
TEL +81-55-275-4411
FAX +81-55-275-9461
Sales Division
1, Kanai-cho, Sakae-ku
Yokohama, 244-0845, Japan
TEL +81-45-853-8156
FAX +81-45-853-8170

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