FMC XM104 Connectivity Card User Guide

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/07/09	1.0	Initial Xilinx release.
09/24/10	1.1	Updated note about FMC cards in Table 1-1.

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About This Guide

This document describes the FPGA Mezzanine Card (FMC) XM104 connectivity card, referred to as the *XM104* in this guide. Xilinx® supported evaluation (carrier) boards are referred to simply as *boards* in this guide.

Guide Contents

This manual contains the following chapter:

- Chapter 1, XM104.

Additional Documentation

Prior to using the XM104, users should be familiar with Xilinx resources. See the following locations for additional documentation on Xilinx tools and solutions:

- ISE® Design Suite: www.xilinx.com/ise
- Answer Browser: www.xilinx.com/support
- Intellectual Property: www.xilinx.com/ipcenter

The XM104 can be used with Xilinx FMC high pin count (HPC) boards and, with limited functionality, FMC low pin count (LPC) boards. Board documentation, schematics and PCB design files are available at www.xilinx.com/fmc.

Additional Support Resources

To find additional documentation, see the Xilinx website at:

www.xilinx.com/support/documentation/index.htm

To search the Answer Database of silicon, software, and IP questions and answers, or to create a technical support WebCase, see the Xilinx website at:

www.xilinx.com/support/mysupport.htm

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Chapter 1

XM104

Overview

This document describes the FPGA Mezzanine Card (FMC) XM104 connectivity module, referred to as the *XM104* in this guide. A Quick Start section and Board Technical Description are combined within this document.

Quick Start

System Requirements

Hardware

Table 1-1 details the board validated to support the XM104. The ML605 board provides one FMC high pin count (HPC) (J64) and one FMC low pin count (LPC) (J63) connector interface. The XM104 connector must be installed on the HPC J64 connector of the ML605 board to have full functionality, as shown in Figure 1-1, page 9.

Table 1-1: **FMC Supported Boards**

Xilinx Platform	Part Number	FMC HPC Connector	FMC LPC Connector
Virtex-6 FPGA ML605 Evaluation Kit	EK-V6-ML605-G	J64	J63

Notes:

While every effort has been made to comply with the *FPGA Mezzanine Card Specification*, Xilinx cannot claim nor assume full compliance with the FMC/VITA-57-1 specification. Consequently, Xilinx cannot claim nor support the usage of the XM104 on any other FMC (VITA-57.1) board.

Xilinx FMC cards are generally designed to implement expanded functionality for supported Xilinx evaluation boards (SP601, SP605, or ML605) and thus might exceed the FMC card outline dimensions discussed in the Single Width FMC Module Mechanical section of the FMC/VITA-57-1 specification. Therefore, Xilinx FMC cards might not physically fit in a non-Xilinx evaluation board environment.

The XM104 can work on LPC FMC interfaces, but with limited functionality. Xilinx boards containing LPC connectors are supported as follows:

- SP601 - Si5368 clock source only
- SP605 - Si5368 clock source and Data Port 0 (DP0) channel
- ML605 LPC (J63) - Si5368 and DP0 channel
- ML623 - Si5368 clock source only
- SP623 - Si5368 clock source only

Software

Example designs that use this hardware are not provided at this time.

Package Contents

The following items are included in the XM104 shipment:

- XM104 card
- Four (4) mounting screws
- Two (2) standoffs
- Four (4) SMA-P to SMA-P cables
- Serial ATA loopback cable
- Serial ATA cable
- Welcome letter

Necessary Equipment

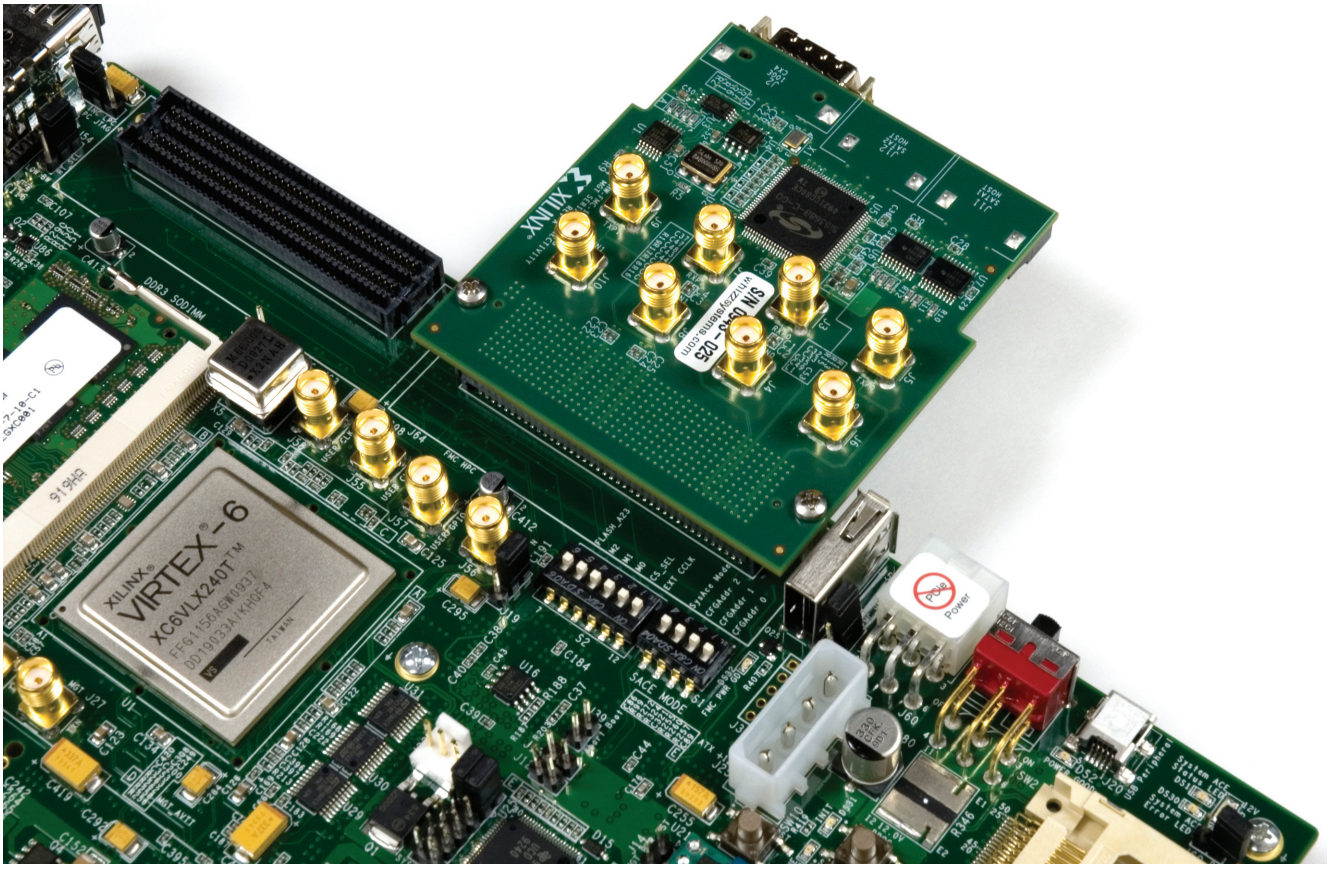
- Small Phillips screwdriver to secure the XM104 to the board
- PC with Internet access to download documentation, board files, and schematics

System Setup

Complete the following steps to install the XM104 to a Xilinx board. For additional information on Xilinx boards, refer to the board's user guide. See Additional Documentation, page 5.

1. Turn off the DC power switch and disconnect the input power source from the board.
2. Remove the XM104 from the electrostatic device (ESD) bag.
3. Using a small Phillips screwdriver, remove the two screws from the bottom side of the two standoffs on the XM104. These screws will be used to attach the board to the standoffs attached to the XM104.
4. Install the XM104 to the ML605 FMC HPC connector J64. The XM104 hangs off the edge of the board as shown in Figure 1-1, page 9.
5. Turn the attached board and XM104 such that the FPGA is facing the table. Install two screws from the bottom side of board's FMC mounting holes into the two standoffs attached to the XM104. Hand tighten the two mounting screws to the bottom of the board.
6. Turn the attached board and XM104 unit over such that the Xilinx FPGA is visible.
7. Connect the input power source to the board. Turn the board power input switch to ON.

The system is now ready for use.



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Figure 1-1: **Installation of XM104 to Board FMC HPC Connector**

Technical Support

Xilinx offers technical support for this product *only* when used in conjunction with boards listed in Table 1-1. For assistance with the XM104 and Xilinx boards, contact Xilinx for technical support at www.xilinx.com/support.

Board Technical Description

The XM104 provides a number of connectors which break out the FPGA multi-gigabit transceiver (MGT) interface signals to and from the board interface. Figure 1-2 shows a block diagram of the XM104. Each MGT data port interface consists of two differential pairs of MGT signals, one pair for the transmitter and one pair for the receiver. MGT Data Ports 0 and 1 are each wired to four SMA connectors. MGT Data Ports 2 and 3 are each wired to host Serial ATA connectors J11 and J12 respectively. MGT Data Ports 4 through 7 are wired to a 10GE Base-CX4 connector supporting a XAUI application interface. MGT transmitter Data Ports 8 and 9 are electrically looped back to the board receiver ports 8 and 9 respectively. The ML605 does not support Data Port 8 and 9 interfaces.

Silicon Laboratories Si570 serial IIC bus reprogrammable LVDS clock source and a Si5368 any-rate precision clock multiplier and jitter attenuator integrated circuits provide a variety of programmable differential clock sources to the board's FGPA. The Si5368 integrated circuit receives three differential LVDS clock inputs from the board and outputs five LVDS differential clock outputs to the FPGA.

A 2 Kb serial IIC EEPROM is also connected to the IIC interface of the board providing non-volatile storage. The serial IIC interface also connects to the Si570 and Si5368 integrated circuits enabling the board's FPGA to program the clock circuitry on the XM104.

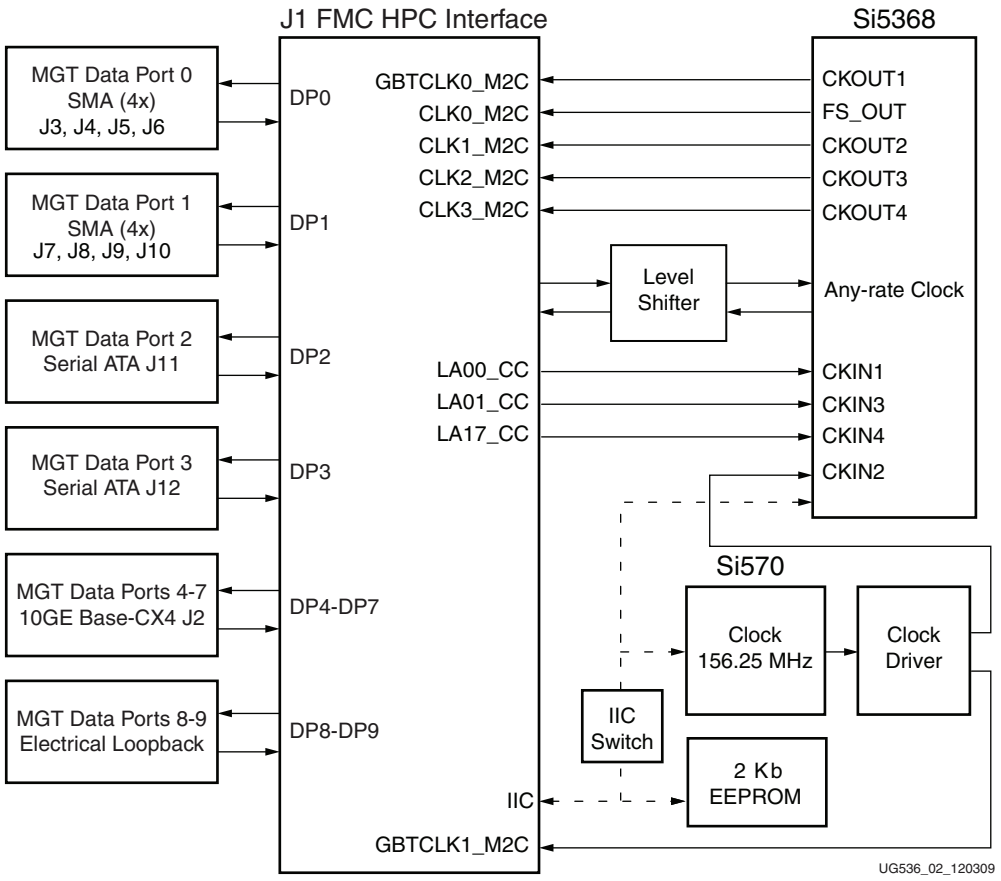
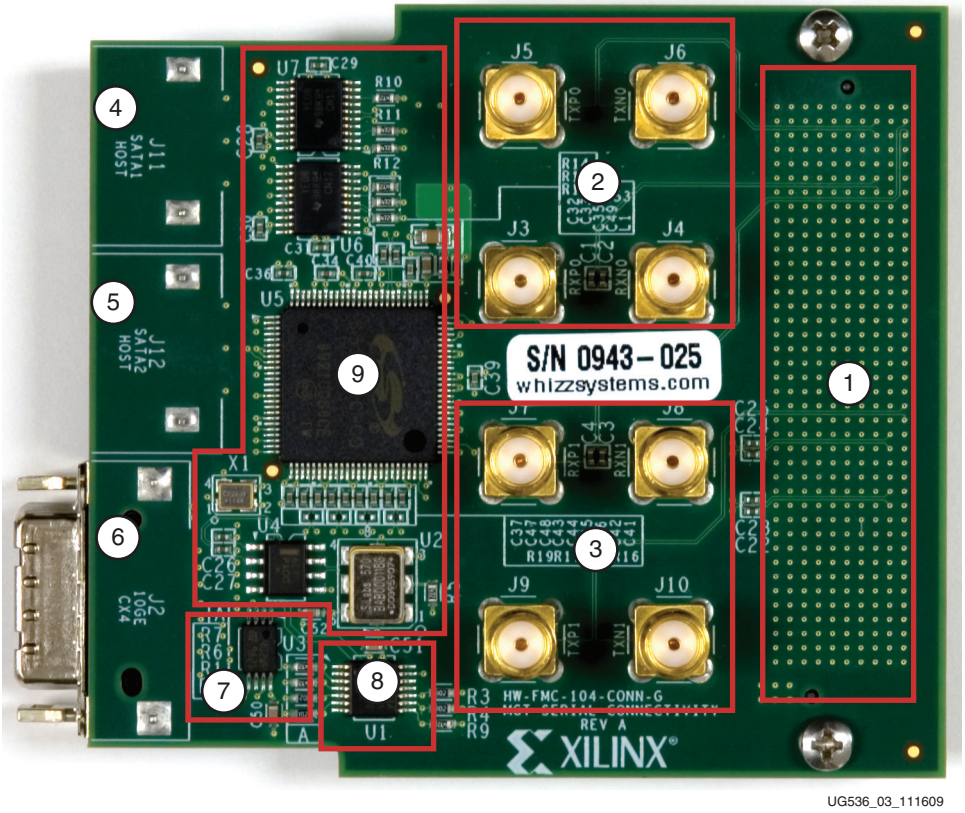


Figure 1-2: **XM104 Block Diagram**

Detailed Description

The numbered features in Figure 1-3 correlate to the features and notes listed in Table 1-2, page 12. For full functionality, the XM104 must be installed on a board FMC connector supporting high pin count interfaces.



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Figure 1-3: **XM104 Features**

Table 1-2: **XM104 Features**

Number	Feature	Notes	Schematic Page
1	VITA 57.1 FMC HPC connector	**J1:** Ten sets of FPGA multi-gigabit transceiver data port signals, a small number of FPGA single ended control signals from the board, clocks and power. The connector is mounted on the bottom side of the card.	2-5
2	MGT Data Port 0: Four SMA connectors	FPGA multi-gigabit transceiver data port 0 on SMA connectors **J3**, **J4**, **J5**, **J6**.	6
3	MGT Data Port 1: Four SMA connectors	FPGA multi-gigabit transceiver data port 1 on SMA connectors **J7**, **J8**, **J9**, **J10**.	6
4	MGT Data Port 2: Serial ATA Port 1	FPGA multi-gigabit transceiver data port 2 on Serial ATA host connector **J11**. The connector is mounted on the bottom side of the XM104. This connector is mounted on the bottom side of the card.	6
5	MGT Data Port 3: Serial ATA Port 2	FPGA multi-gigabit transceiver data port 3 on Serial ATA host connector **J12**. The connector is mounted on the bottom side of the XM104.	6
6	MGT Quad Data Port: 10GE Base-CX4 receptacle	FPGA multi-gigabit transceiver data ports 4 through 7 on 10GE Base-CX4 receptacle **J2**. The connector is mounted on the bottom side of the card.	6
7	2K bit EEPROM	IIC compatible electrically erasable programmable memory (EEPROM) with 2 Kb (256 bytes) of non-volatile storage.	7
8	PCA9543 IIC Switch	IIC bus switch to isolate the fixed address SI570 and Si5368 devices.	7
9	Clocking circuits	Silicon Labs Si570 IIC serial bus re-programmable clock source and Silicon Labs Si5368 any-rate precision clock multiplier and clock jitter attenuator clock source integrated circuits.	7-8

Notes:

1. VITA 57.1 FMC HPC Connector J1.

1. VITA 57.1 FMC HPC Connector J1

This connector interfaces to the board containing the Xilinx FPGA and mating FMC connector. The XM104 uses Samtec FMC HPC connector part number ASP-134488-01. The XM104 connector mates with an FMC connector.

See Xilinx board user guides and schematics for a description of features provided by HPC interfaces contained on the board, including power supply specifications, FPGA banking connectivity, and FPGA pin assignments.

- For ML605 LPC and HPC interfaces, see UG534 *ML605 Hardware User Guide*

See the *VITA57.1 Specification* at www.vita.com/fmc.html for additional information on FMC.

2. Multi-Gigabit Transceiver Data Port 0

Board FPGA multi-gigabit transceiver Data Port 0 signals are wired to SMA connectors on the XM104. Data Port 0 connections between the XM104 FMC HPC connector and four SMA connectors are defined in Table 1-3.

Table 1-3: **FPGA Multi-Gigabit Transceiver Data Port 0 Connectivity**

FMC HPC Connector J1 Pin	Signal Name	SMA Connector
C6	DP0_M2C_P(1)	J3
C7	DP0_M2C_N(1)	J4
C2	DP0_C2M_P	J5
C3	DP0_C2M_N	J6

Notes:

1. AC coupled using a series 0.1 uF capacitor

3 Multi-Gigabit Transceiver Data Port 1

Board FPGA multi-gigabit transceiver Data Port 1 signals are wired to SMA connectors on the XM104. Data Port 1 connections between the XM104 FMC HPC connector and four SMA connectors are defined in Table 1-4.

Table 1-4: **FPGA Multi-Gigabit Transceiver Data Port 1 Connectivity**

FMC HPC Connector J1 Pin	Signal Name	SMA Connector
A2	DP1_M2C_P(1)	J7
A3	DP1_M2C_N(1)	J8
A22	DP1_C2M_P	J9
A23	DP1_C2M_N	J10

Notes:

1. AC coupled using a series 0.1 uF capacitor

4. Multi-Gigabit Transceiver Data Port 2 - J11 SATA1

Board FPGA multi-gigabit transceiver Data Port 2 signals are wired to Serial ATA host connector J11 on the XM104. Data Port 2 connections between the XM104 FMC HPC connector and Serial ATA connector J11 are defined in Table 1-5.

Table 1-5: **FPGA Multi-Gigabit Transceiver Data Port 2 Connectivity**

FMC HPC Connector J1 Pin	Signal Name	Serial ATA Connector J11
A26	DP2_C2M_P(1)	2
A27	DP2_C2M_N(1)	3
A7	DP2_M2C_N(1)	5
A6	DP2_M2C_P(1)	6

Notes:

1. AC coupled using a series 0.1 uF capacitor

5. Multi-Gigabit Transceiver Data Port 3 - J12 SATA2

Board FPGA multi-gigabit transceiver Data Port 3 signals are wired to a Serial ATA host connector J12 on the XM104. Data Port 3 connections on the XM104 FMC HPC connector and Serial ATA connector J12 are defined in Table 1-6.

Table 1-6: **FPGA Multi-Gigabit Transceiver Data Port 3 Connectivity**

FMC HPC Connector J1 Pin	Signal Name	Serial ATA Connector J12
A30	DP3_C2M_P(1)	2
A31	DP3_C2M_N(1)	3
A11	DP3_M2C_N(1)	5
A10	DP3_M2C_P(1)	6

Notes:

1. AC coupled using a series 0.1 uF capacitor

6. Multi-Gigabit Transceiver Data Ports [4:7] - J2 10GE Base-CX4 Connector

Board FPGA multi-gigabit transceiver Data Ports 4 through 7 are wired to a 10GE Base-CX4 connector J2 on the XM104. The four data port connections between the XM104 FMC HPC connector and the 10G Base-CX4 connector J2 are defined in Table 1-7.

Table 1-7: **FPGA Multi-Gigabit Transceiver Data Ports 4 - 7 Connectivity**

FMC HPC Connector J1 Pin	Signal Name	J2 Connector Pin (Receiver)	FMC HPC Connector J1 Pin	Signal Name	J2 Connector Pin (Transmitter)
A14	DP4_M2C_P (1)	S1	B33	DP7_C2M_N	S9
A15	DP4_M2C_N (1)	S2	B32	DP7_C2M_P	S10
A18	DP5_M2C_P (1)	S3	B37	DP6_C2M_N	S11
A19	DP5_M2C_N (1)	S4	B36	DP6_C2M_P	S12
B16	DP6_M2C_P (1)	S5	A39	DP5_C2M_N	S13
B17	DP6_M2C_N (1)	S6	A38	DP5_C2M_P	S14
B12	DP7_M2C_P (1)	S7	A35	DP4_C2M_N	S15
B13	DP7_M2C_N (1)	S8	A34	DP4_C2M_P	S16

Notes:

1. All receiver signals are AC coupled using 0.1 uF series capacitors

7. 2 Kb EEPROM

An STMicroelectronics M24C02 2 Kb serial IIC bus EEPROM component provides a small amount of non-volatile memory storage on the XM104. The IIC interface is connected directly to the board's IIC interface as shown in Figure 1-2, page 10.

The IIC address of this component is controlled by a combination of the board's interface and chip enable connections to the component inputs on the XM104. Signals GA0 and GA1 from the board are connected to the chip enable inputs of the M24C02 component enables E0 and E1. Xilinx boards provide GA0 and GA1 signal strapping to 3.3V and GND signals creating different E0 and E1 chip enable decodes on the E1 and E0 inputs of the EEPROM.

The IIC memory addressing protocol requires a bus master to initiate communication to a peripheral device using a start condition followed by a device select code. The device select code consists of a 4 bit Device Type Identifier and a 3-bit Chip Enable Address (E2, E1 and E0). Bit 0 is used to indicate read/write. The Device Type Identifier for the EEPROM is 1010 binary. Table 1-8 defines the generic EEPROM Device Select Code as well as specific Device Code Select addresses of the EEPROM when the XM104 is connected to a Xilinx board defined in Table 1-1, page 7.

Table 1-8: **EEPROM IIC Device Select Code**

Bit 7:4 Device Type Identifier	Bit 3	Bit 2	Bit 1	Bit 0 LSB	Description
1010	0	GA0	GA1	Read/$\overline{\text{Write}}$	Connected to mezzanine FMC HPC interface

The M24C02 component data sheet is available online at www.st.com.

8. PCA9543 IIC Switch

The board's serial IIC bus is wired to an EEPROM and a two-channel NXP (formerly Philips Semiconductor) PCA9543 IIC bus switch on the XM104 (as shown in Figure 1-2, page 10). The IIC bus switch provides bidirectional bus isolation and isolates the fixed address Si570 and Si5368 devices from the main IIC bus of the board. The upstream side of the switch connects to the FMC HPC connector. Only one of the two downstream ports is utilized and it uses 3.3V signal levels. The downstream switch port interfaces to the two Silicon Laboratories clock integrated circuits.

The PCA9543 is a bidirectional translating switch, controlled by the upstream board side IIC bus. The PCA9543 must be initialized *prior to* attempting to communicate with the two clock circuits, Si570 and Si5368, on the downstream IIC bus. The PCA9543 component data sheet contains detailed application information and is available online at www.nxp.com.

The IIC address of this component is controlled by a combination of the board interface and chip enable connections to the component inputs on the XM104. Signals GA0 and GA1 from the board are connected to the two address inputs A1 and A0 of the PCA9543 component. Xilinx boards provide GA0 and GA1 signal strapping to 3.3V and GND signals creating different A0 and A1 address decodes on the PCA9543.

The IIC memory addressing protocol requires a bus master to initiate communication to a peripheral device using a start condition followed by a device select code. The device select code consists of a 4 bit Device Type Identifier and a 3-bit Address (A2, A1 and A0). A2 is internally grounded inside the PCA9543. Bit 0 is used to indicate read/write. The Device Type Identifier for the PCA9543 is 1110 binary. Table 1-9 defines the generic PCA9543 Device Select Code as well as specific Device Code Select address when the XM104 is connected to a Xilinx board as defined in Table 1-1, page 7.

Table 1-9: **PCA9543 IIC Switch Device Select Code**

Bit 7:4 Device Type Identifier	Bit 3	Bit 2	Bit 1	Bit 0 LSB	Description
1110	0	GA0	GA1	Read/$\overline{\text{Write}}$	Connected to mezzanine FMC HPC interface

The PCA9543 has a Control register which must be initialized by the IIC bus master to enable the channel 0 downstream IIC port. Channel 0 must be enabled prior to attempting to communicate with the two downstream programmable clock devices on the XM104. After the IIC bus master enables PCA9543 channel 0 downstream IIC bus, the bus master can communicate directly with the Si570 component or the Si5368 component without further interaction with the Control register. The Control Register can be read by the IIC bus master. Table 11 defines the PCA9543 Control Register.

Table 1-10: **PCA9543 Control Register**

Bit 7:4	Bit 3:2	Bit 1	Bit 0
XXXX	XX	Channel 1 Enable(1)	Channel 0 Enable(2)

Notes:

1. Channel 1 is not connected on the XM104.
2. Channel 0 must be set to a logic 1 state by the IIC bus master prior to attempting to communicate with the Si570 or the Si5368 components on the downstream IIC bus.

The two downstream IIC devices connected to the PCA9543 are at the following IIC addresses:

- Si570 IIC address is at 0x5D
- Si5368 IIC address is at 0x68

9. Clocking Circuits

Two programmable clock circuits are provided on the XM104:

- Silicon Labs Si570
- Silicon Labs Si5368

A Silicon Labs Si570 serial IIC bus re-programmable clock source provides a low-jitter clock with a user-programmable output frequency from 10 to 810 MHz. The Si570 is located at IIC address 0x5D. The Si570 clock output (shown in Figure 1-2, page 10) is wired to a NB6L11 clock driver integrated circuit. One differential output of the NB6L11 clock driver is AC coupled, with 0.1 uF capacitors, and wired to the FMC HPC connector signal GBTCLK1_M2C. The second output of the NB6L11 clock driver is connected one of the Si5368 differential clock inputs. The default clock frequency is 156.25 MHz. Connections to the FMC HPC connector are defined in Table 1-11.

Table 1-11: **Si570 Clock Source Routed to XM104 FMC HPC J1 Connector**

FMC HPC Connector J1 Pin	Signal Name	Source
B20	GBTCLK1_M2C_P(1)	Si570
B21	GBTCLK1_M2C_N(1)	Si570

Notes:

1. Signals are AC coupled using 0.1 uF series capacitors

The component installed on the XM104 is factory programmed with parameters in Table 1-12.

Table 1-12: **Characteristics of Si570 Component**

Si570 Characteristic	XM104
Output Format	LVDS
Output Enable Polarity	High
Temperature Stability	50 ppm
Frequency Range	10–810 MHz
Six-Digit Startup Frequency	156.250 MHz
Power Supply	3.3V
IIC Address	x5D

For additional information on this component, including reprogramming the clock frequency through the IIC serial bus interface, consult the manufacturer's data sheet at: www.silabs.com.

Silicon Labs Si5368

A Silicon Labs Si5368 any-rate precision clock multiplier/jitter attenuator integrated circuit provides a wide range of clocking applications for the Xilinx board and XM104 combination. Table 1-13 shows the connections of the SI5368 differential clock outputs to the XM104 FMC HPC connector. Table 1-13 also shows connections of the clock outputs from the board to the inputs of the SI5368.

Table 1-13: **Si5368 Clock I/O Connections to FMC HPC Connector J1**

FMC Connector J1 Pin	Signal Name	I/O Standard	Si5368 In/Out	Si5368
H4	CLK0_M2C_P	LVDS	Output	CKOUT5/FS_OUT_P
H5	CLK0_M2C_N	LVDS		CKOUT5/FS_OUT_N
G2	CLK1_M2C_P	LVDS	Output	CKOUT2_P
G3	CLK1_M2C_N	LVDS		CKOUT2_N
K4	CLK2_M2C_P	LVDS	Output	CKOUT3_P
K5	CLK2_M2C_N	LVDS		CKOUT3_N
J2	CLK3_M2C_P	LVDS	Output	CKOUT4_P
J3	CLK3_M2C_N	LVDS		CKOUT4_N
D4	GBTCLK0_M2C_P	LVDS	Output	CKOUT1_P
D5	GBTCLK0_M2C_N	LVDS		CKOUT1_N
G6	LA00_CC_P	LVDS	Input	CKIN1_P
G8	LA00_CC_N	LVDS		CKIN1_N
-	CLK_SI570_P	LVDS	Input	CKIN2_P
-	CLK_SI570_N	LVDS		CKIN2_N
D8	LA01_CC_P	LVDS	Input	CKIN3_P
D9	LA01_CC_N	LVDS		CKIN3_N
D20	LA17_CC_P	LVDS	Input	CKIN4_P
D21	LA17_CC_N	LVDS		CKIN4_N
G13	LA08_N	LVCMOS_Vadj	Input	C2A
G12	LA08_P	LVCMOS_Vadj	Input	C1A
H14	LA07_N	LVCMOS_Vadj	I/O	CS1_C4A(1)
H13	LA07_P	LVCMOS_Vadj	Input	INC
C11	LA06_N	LVCMOS_Vadj	Input	DEC
C10	LA06_P	LVCMOS_Vadj	Output	LOL
D11	LA05_P	LVCMOS_Vadj	Input	FS_ALIGN
H12	LA04_N	LVCMOS_Vadj	I/O	CS0_C3A(1)
H10	LA04_P	LVCMOS_Vadj	Output	INT_ALM

Table 1-13: **Si5368 Clock I/O Connections to FMC HPC Connector J1 *(Cont'd)***

FMC Connector J1 Pin	Signal Name	I/O Standard	Si5368 In/Out	Si5368
G10	LA03_N	LVCMOS_Vadj	Output	C3B
G9	LA03_P	LVCMOS_Vadj	Output	C2B
H8	LA02_N	LVCMOS_Vadj	Output	C1B
H7	LA02_P	LVCMOS_Vadj	Input	RESET_B

Notes:

1. These signals are either inputs or outputs to the Si5368 depending upon the state of an internal Si5368 register.

The Si5368 does not provide any clock outputs to the board without first going through internal register initialization via the serial IIC bus interface from the bus master. Asserting the reset input also requires re-initialization of the Si5368 registers to re-establish clock outputs. The Si5368 is located at IIC address 0x68.

For additional application information on the Si5368 component see the manufacturer's data sheet at www.silabs.com.