FAIRCHILD
SEMICONDUCTOR™

June 2000

FM24C256
256 KBit 2-Wire Bus Interface Serial EEPROM with Write Protect

General Description

The FM24C256/C256L/C256LZ devices are 256 Kbits CMOS nonvolatile electrically erasable memory. These devices offer the designer different low voltage and low power options. They conform to all requirements in the Extended IIC 2-wire protocol. Furthermore, they are designed to minimize device pin count and simplify PC board layout requirements.

The entire memory array can be write disabled (Write Protection) by connecting the WP pin to V_{CC}.

Functional address lines allow up to eight devices on the same bus, for up to a total of 2 Mbit address space.

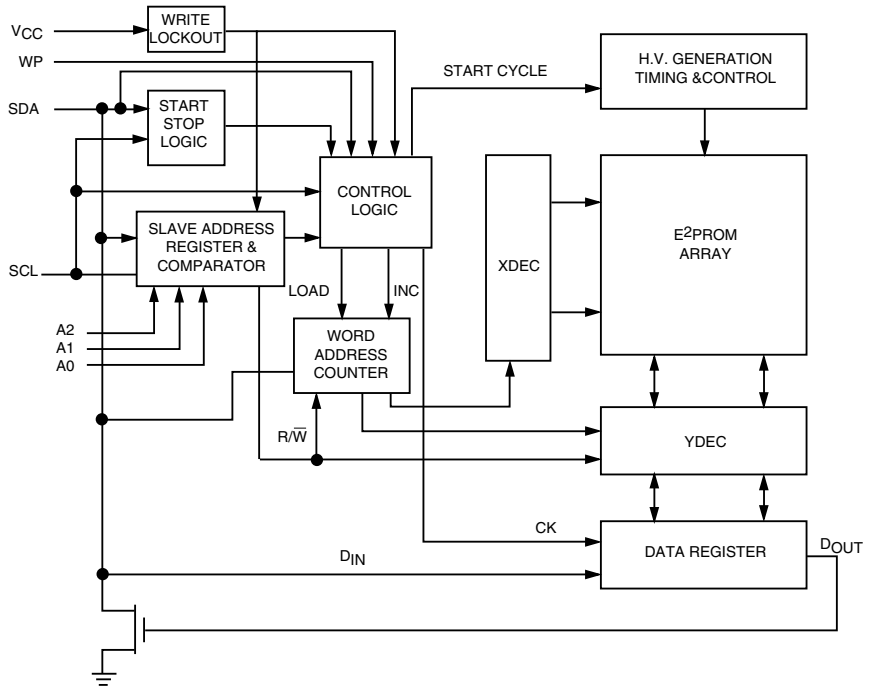
The IIC communication protocol uses CLOCK (SCL) and DATA I/O (SDA) lines to synchronously clock data between the master (for example a microprocessor) and the slave EEPROM device(s).

Fairchild EEPROMs are designed and tested for applications requiring high endurance, high reliability, and low power consumption.

Features

- Extended Operating Voltages
  - — C256: 4.5V - 5.5V
  - — C256L: 2.7V - 5.5V
  - — C256LZ: 2.7V - 5.5V
- Low Power CMOS
  - — 1mA active current typical
  - — C256/C256L: 10μA standby current typical
  - — C256LZ: less than 1μA standby current
- 2-wire IIC serial interface
- 64 byte page write mode
- Max write cycle time of 6ms byte/page
- 40 years data retention
- Endurance: 100,000 data changes
- Hardware write protect for entire array
- Schmitt trigger inputs for noise suppression
- Electrostatic discharge protection > 4000V
- 8-pin DIP and 8-pin SO (150 mil) packages. Contact factory for CSP package availability

Block Diagram

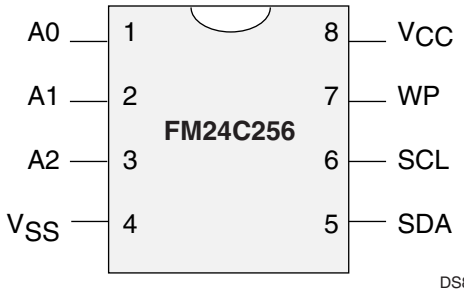


DS800023-1

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Connection Diagram

Dual-In-Line Package (N)
and 8-Pin SO Package (M8)



DS800023-2

Top View
See Package Number N08E and M08A

Pin Names

A0, A1, A2	Device Address Input
V_{SS}	Ground
SDA	Data I/O
SCL	Clock Input
WP	Write Protect
V_{CC}	Power Supply

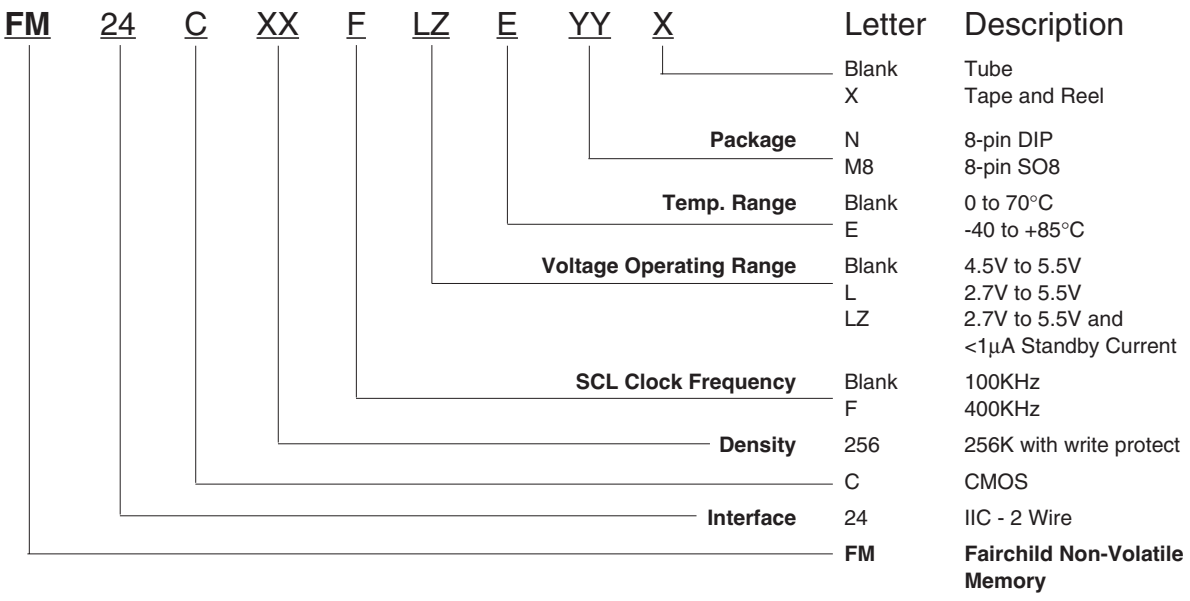
Ordering Information

Commercial Temperature Range: 0° to +70°C

Part Number	Clock Frequency	V_{CC}	Standby Current
FM24C256YYX	100KHz	4.5V - 5.5V	10μA typical
FM24C256LYYX		2.7V - 5.5V	
FM24C256LZYYX			1μA max
FM24C256FYYX	400KHz	4.5V - 5.5V	10μA typical
FM24C256FLYYX		2.7V - 5.5V	
FM24C256FLZYYX			1μA max

Industrial Temperature Range: -40° to +85°C

Part Number	Clock Frequency	V_{CC}	Standby Current
FM24C256EYYX	100KHz	4.5V - 5.5V	10μA typical
FM24C256LEYYX		2.7V - 5.5V	
FM24C256LZEYYX			1μA max
FM24C256FEYYX	400KHz	4.5V - 5.5V	10μA typical
FM24C256FLEYYX		2.7V - 5.5V	
FM24C256FLZEYYX			1μA max



Letter	Description
Package	
Blank	Tube
X	Tape and Reel
N	8-pin DIP
M8	8-pin SO8
Temp. Range	
Blank	0 to 70°C
E	-40 to +85°C
Voltage Operating Range	
Blank	4.5V to 5.5V
L	2.7V to 5.5V
LZ	2.7V to 5.5V and <1μA Standby Current
SCL Clock Frequency	
Blank	100KHz
F	400KHz
Density	
256	256K with write protect
C	CMOS
Interface	
24	IIC - 2 Wire
FM	**Fairchild Non-Volatile Memory**

Absolute Maximum Ratings

Ambient Storage Temperature	–65°C to +150°C
All Input or Output Voltages with Respect to Ground	6.5V to –0.3V
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD Rating	4000V min.

Operating Conditions

Ambient Operating Temperature	
FM24C256/L/LZ	0°C to +70°C
FM24C256F/FL/FLZ	0°C to +70°C
FM24C256E/LE/LZE	-40°C to +85°C
FM24C256FE/FLE/FLZE	-40°C to +85°C
Positive Power Supply	
FM24C256/E	4.5V to 5.5V
FM24C256F/FE	4.5V to 5.5V
FM24C256L/LZ	2.7V to 5.5V
FM24C256FL/FLZ	2.7V to 5.5V
FM24C256LE/LZE	2.7V to 5.5V
FM24C256FLE/FLZE	2.7V to 4.5V

Standard V_{CC} (4.5V to 5.5V) DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 100 kHz f_{SCL} = 400 kHz		0.5	1.0	mA
I_{SB}	Standby Current	V_{IN} = GND or V_{CC}		10	50	µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		0.1	1	µA
V_{IL}	Input Low Voltage		–0.3		V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V

Low V_{CC} (2.7V to 5.5V) DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 100 kHz f_{SCL} = 400 kHz		0.5	1.0	mA
I_{SB} (Note 1)	Standby Current for L	V_{IN} = GND or V_{CC} = 4.5V - 5.5V V_{IN} = GND or V_{CC} = 2.7V - 4.5V		10 1	50 10	µA
	Standby Current for LZ	V_{IN} = GND or V_{CC} = 4.5V - 5.5V V_{IN} = GND or V_{CC} = 2.7V - 4.5V		10 0.1	50 1	
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		0.1	1	µA
V_{IL}	Input Low Voltage		–0.3		V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V

Capacitance T_A = +25°C, f = 100/400 KHz, V_{CC} = 5V

Symbol	Test	Conditions	Max	Units
$C_{I/O}$	Input/Output Capacitance (SDA)	$V_{I/O}$ = 0V	8	pF
C_{IN}	Input Capacitance (A0, A1, A2, SCL)	V_{IN} = 0V	6	pF

Note 1: Typical values are for T_A = 25°C and nominal supply voltage (5V).

AC Conditions of Test

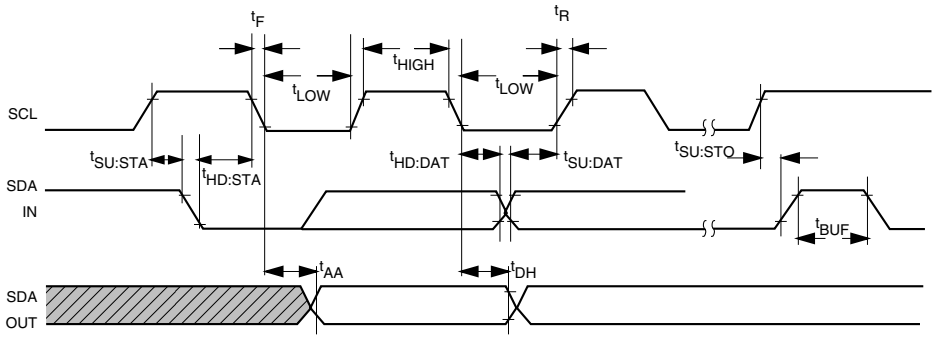
Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10 ns
Input & Output Timing Levels	V_{CC} x 0.5
Output Load	1 TTL Gate and C_L = 100 pF

Read and Write Cycle Limits (Standard and Low V_{CC} Range - 2.7V-5.5V)

Symbol	Parameter	100 kHz		400 kHz		Units
		Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency		100		400	kHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs (Minimum V_{IN} Pulse width)		100		50	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	0.3	1.2	µs
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	4.7		1.3		µs
$t_{HD:STA}$	Start Condition Hold Time	4.0		0.6		µs
t_{LOW}	Clock Low Period	4.7		1.5		µs
t_{HIGH}	Clock High Period	4.0		0.6		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		0.6		µs
$t_{HD:DAT}$	Data in Hold Time	0		0		µs
$t_{SU:DAT}$	Data in Setup Time	250		100		ns
t_R	SDA and SCL Rise Time		1		0.3	µs
t_F	SDA and SCL Fall Time		300		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		0.6		µs
t_{DH}	Data Out Hold Time	100		100		ns
t_{WR} (Note 2)	Write Cycle Time		6		6	ms

Note 2: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the FM24C256 bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address

Bus Timing



Note 3: SCL = Serial Clock Data
SDA = Serial Data I/O

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BACKGROUND INFORMATION (IIC Bus)

The IIC bus allows synchronous bidirectional communication between Transmitter/Receiver using the SCL (clock) and SDA (Data I/O) lines. All communication must be started with a valid START condition, concluded with a STOP condition and acknowledged by the Receiver with an ACKNOWLEDGE condition.

In addition, since the IIC bus is designed to support other devices such as RAM, EPROM, etc., the device type identifier string, or control byte, must follow the START condition. For EEPROMs, the first 4-bit of the control byte is 1010 binary for READ and WRITE operations. This is then followed by the device selection bits A2, A1 and A0, and acts as the three most significant bits of the word address.The final bit in the control byte determines the type of operation performed (READ/WRITE). A "1" signifies a READ while a "0" signifies a WRITE. The control byte is then followed by two bytes that define the word address, which is then followed by the data byte.

The EEPROMs on the IIC bus may be configured in any manner required, providing the total memory addressed does not exceed 512K bits (64K bytes). EEPROM memory addressing is controlled by hardware configuring the A2, A1, and A0 pins (Device Address pins) with pull-up or pull-down resistors. ALL UNUSED PINS MUST BE GROUNDED (tied to V_{SS}).

Addressing an EEPROM memory location involves sending a command string with the following information:

[DEVICE TYPE]-[DEVICE ADDRESS]-[PAGE BLOCK ADDRESS]-[BYTE ADDRESS]

Pin Description

SERIAL CLOCK (SCL)

	Definitions
Word	8 bits (byte) of data
Page	64 sequential addresses (one byte each) that may be programmed during a "Page Write" programming cycle.
Master	Any IIC device CONTROLLING the transfer of data (such as a microcontroller).
Slave	Device being controlled (EEPROMS are always considered Slaves).
Transmitter	Device currently SENDING data on the bus (may be either a Master or Slave).
Receiver	Device currently receiving data on the bus (Master or Slave).

The SCL input is used to clock all data into and out of the device.

SERIAL DATA (SDA)

SDA is a bidirectional pin used to transfer data to and from the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

Device Address Inputs (A0, A1, A2)

Device address pins A0, A1, and A2 are connected to V_{CC} or V_{SS} to configure the EEPROM address for multiple device configuration. A total of eight different devices can be attached to the same SDA bus.

Write Protection (WP)

If WP is tied to V_{CC}, program WRITE operations onto the entire array of the memory will not be executed. READ operations are always available.

If WP is tied to V_{SS} or left floating (unconnected), normal memory operation is enabled for READ/WRITE over the entire 256K bit memory array.

This feature allows the user to assign the entire array of the memory as ROM, which can be protected against accidental programming writes. When WRITE is disabled, slave address and word address will be acknowledged but data will not be acknowledged.

Device Operation

The FM24C256xxx supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving devices as the receiver. The device controlling the transfer is the master and the device that is controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the FM24C256xxx is considered a slave in all applications.

CLOCK AND DATA CONVENTIONS

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH and are reserved for indication of start and stop conditions. *Refer to Figures 1 and 2.*

START CONDITION

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The FM24C256xxx continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

STOP CONDITION

All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the FM24C256xxx to place the device in the standby power mode.

Write Cycle Timing

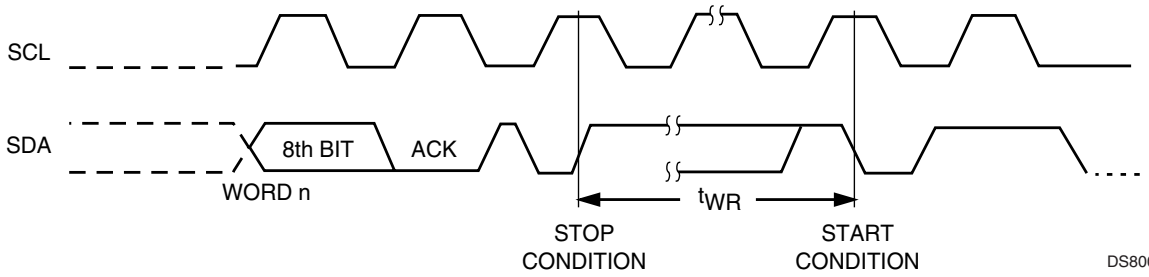
ACKNOWLEDGE

ACK (acknowledge) is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to *Figure 3*.

The FM24C256xxx device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a WRITE operation have been selected, the FM24C256xxx will respond with an acknowledge after the receipt of each subsequent eight bit word.

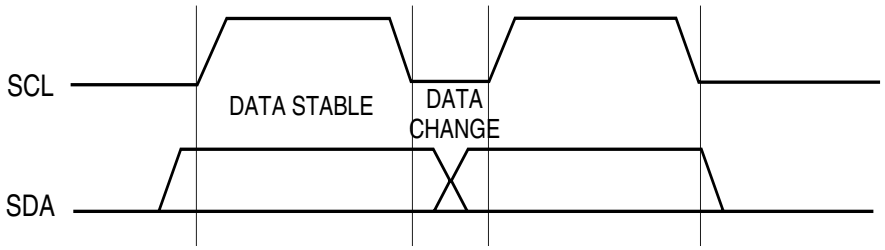
In the READ mode the FM24C256xxx slave will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to the standby power mode.

Write Cycle Timing:



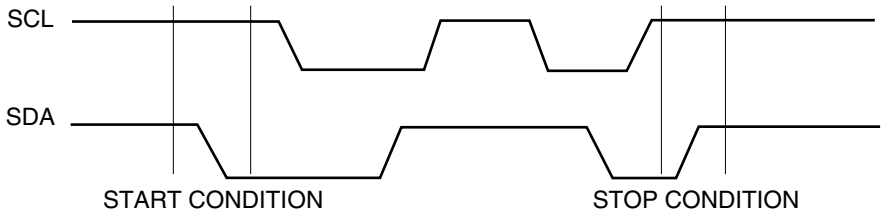
DS800023-4

Data Validity (Figure 1)



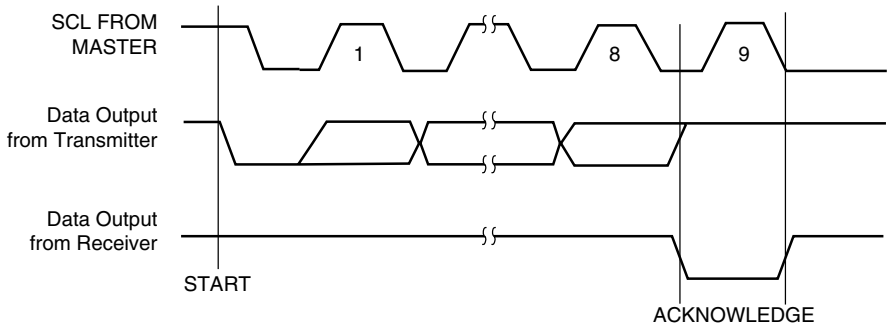
DS800023-5

Definition of Start and Stop (Figure 2)



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Acknowledge Response from Receiver (Figure 3)



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DEVICE ADDRESSING

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are those of the device type identifier. This is fixed as 1010 for all different FM24C256xxx devices.

The next three bits identify the device address. Address from 000 to 111 are acceptable thus allowing up to eight devices to be connected to the IIC bus.

The last bit of the slave address defines whether a write or read condition is requested by the master. A "1" indicates that a READ operation is to be executed and a "0" initiates the WRITE mode.

A simple review: After the FM24C256xxx recognizes the start condition, the device interfaced to the IIC bus waits for a slave address to be transmitted over the SDA line. If the transmitted slave address matches an address of one of the devices, the designated slave pulls the SDA line LOW with an acknowledge signal and awaits further transmissions.

Write Operations

BYTE WRITE

For a WRITE operation, two additional address fields are required after the control byte acknowledge. These are the word addresses and comprise fifteen bits to provide access to any one of the 32K words. The first byte indicates the high-order byte of the word address. Only the seven least signicant bits can be changed, the most significant bit is pre-assigned the value "0". Following the acknowledgement from the first word address, the next byte indicates the low-order byte of the word address. Upon receipt of the word address, the FM24C256xxx responds with another acknowledge and waits for the next eight bits of data, again, responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the FM24C256xxx begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress, the device's inputs are disabled and the device will not respond to any requests from the master. Refer to *Figure 5* for the address, acknowledge and data transfer sequence.

PAGE WRITE

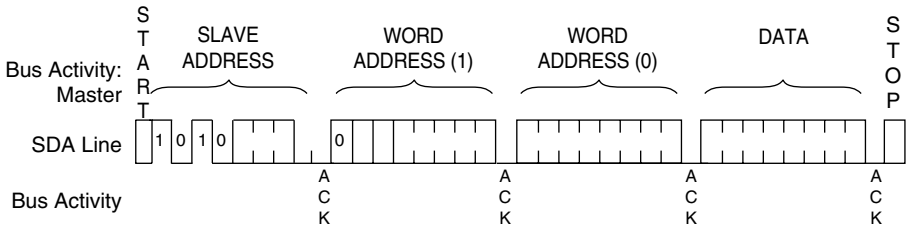
The FM24C256xxx is capable of 64 byte page write operation. It is initiated in the same manner as the byte write operation; but instead of terminating the write cycle after the first data word is transferred, the master can transmit up to 63 more words. After the receipt of each word, the device responds with an acknowledge.

After the receipt of each word, the internal address counter increments to the next address and the next SDA data is accepted. If the master should transmit more than 64 words prior to generating the stop condition, the address counter will "roll over" and the previous written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to *Figure 6* for the address, acknowledge and data transfer sequence.

Acknowledge Polling

Once the stop condition is isssued to indicate the end of the host's write operation, the FM24C256xxx initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the FM24C256xxx is still busy with the write operation, no ACK will be returned. If the device has completed the write operation, an ACK will be returned and the host can then proceed with the next read or write operation.

Byte Write (Figure 5)



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Write Protection

Programming of the memory array will not take place if the WP pin is connected to V_{CC}. The device will accept control and word addresses; but if the memory accessed is write protected by the WP pin, the FM24C256xxx will not generate an acknowledge after the first byte of data has been received, and thus the program cycle will not be started when the stop condition is asserted.

Read Operation

Read operations are initiated in the same manner as write operations, with the exception that the R/W bit of the slave address is set to "1". There are three basic read operations: current address read, random read and sequential read.

CURRENT ADDRESS READ

Internally the FM24C256xxx contains an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n+1. Upon receipt of the slave address with R/W set to "1," the FM24C256xxx issues an acknowledge and transmits the eight bit word. The master will not acknowledge the transfer but does generate a stop condition, and therefore discontinues transmission. Refer to *Figure 7* for the sequence of address, acknowledge and data transfer.

RANDOM READ

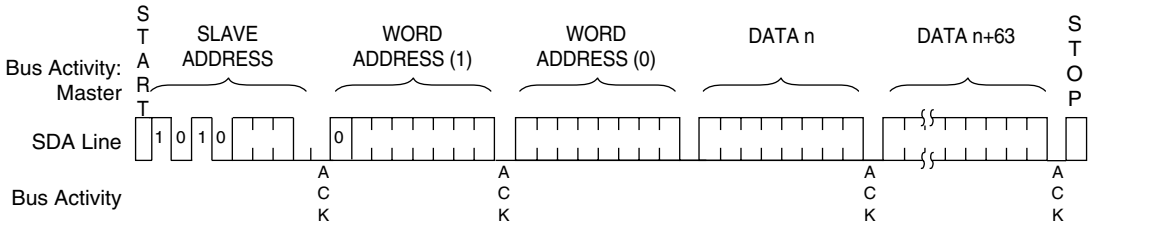
Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/W bit set to "1", the master must first perform a "dummy" write operation. The master issues a start condition, a slave address, and then the word address to be read. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the R/W bit set to "1". This will be followed by an acknowledge from the FM24C256xxx and then by the eight bit word. The master will not acknowledge the transfer but does generate the stop condition, and therefore the FM24C256xxx discontinues transmission. Refer to *Figure 8* for the address, acknowledge, and data transfer sequence.

SEQUENTIAL READ

Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted in the same manner as the other read modes; however, the master now responds with an acknowledge, indicating it requires additional data. The FM24C256xxx continues to output data for each acknowledge received. The read operation is terminated by the master not responding with an acknowledge or by generating a stop condition.

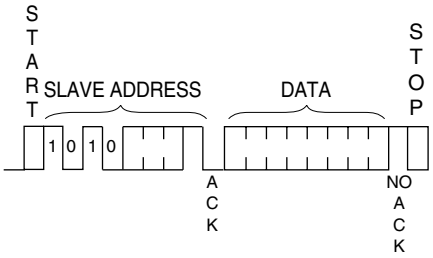
The data output is sequential, with the data from address n, followed by the data n+1. The address counter for read operations increments all word address bits, allowing the entire memory contents to be serially read during one operation. After the entire memory has been read, the counter "rolls over" and the FM24C256xxx continues to output data for each acknowledge received. Refer to *Figure 9* for the address, acknowledge, and data transfer sequence.

Page Write (Figure 6)



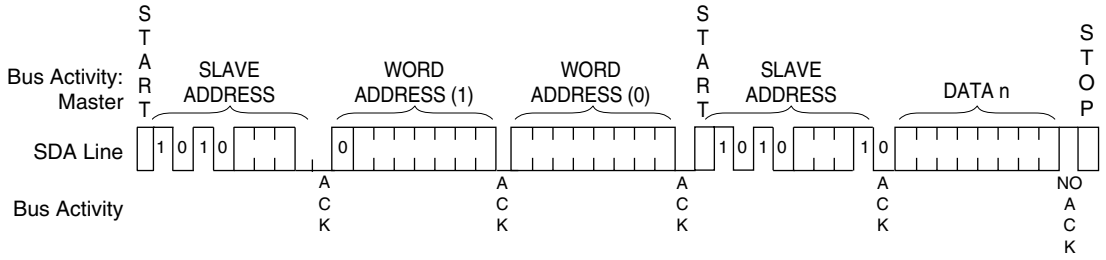
DS800023-9

Current Address Read (Figure 7)



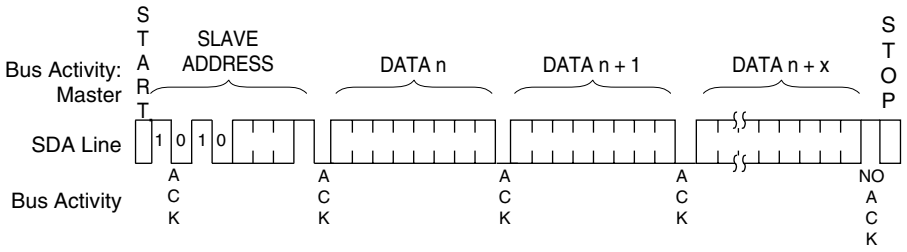
DS800023-10

Random Read (Figure 8)



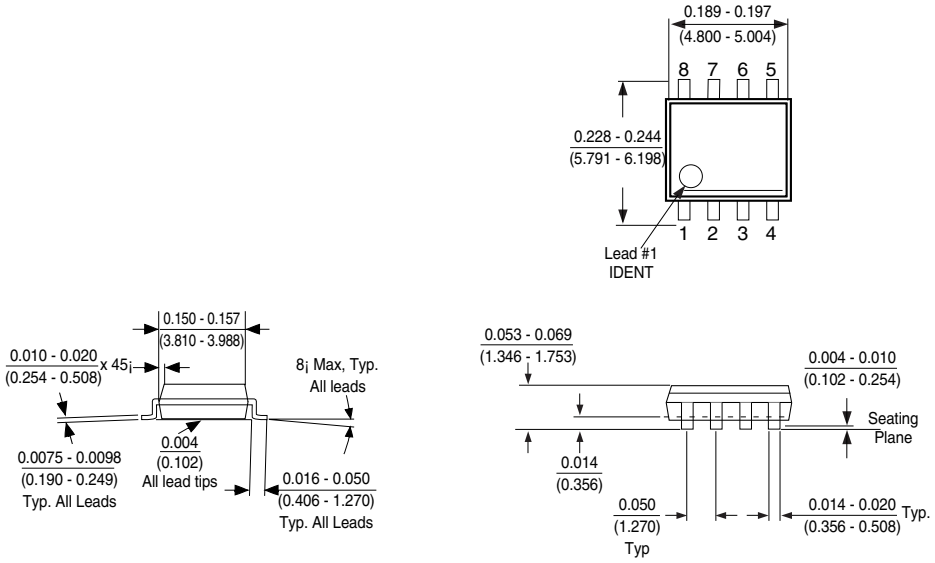
DS800023-11

Sequential Read (Figure 9)



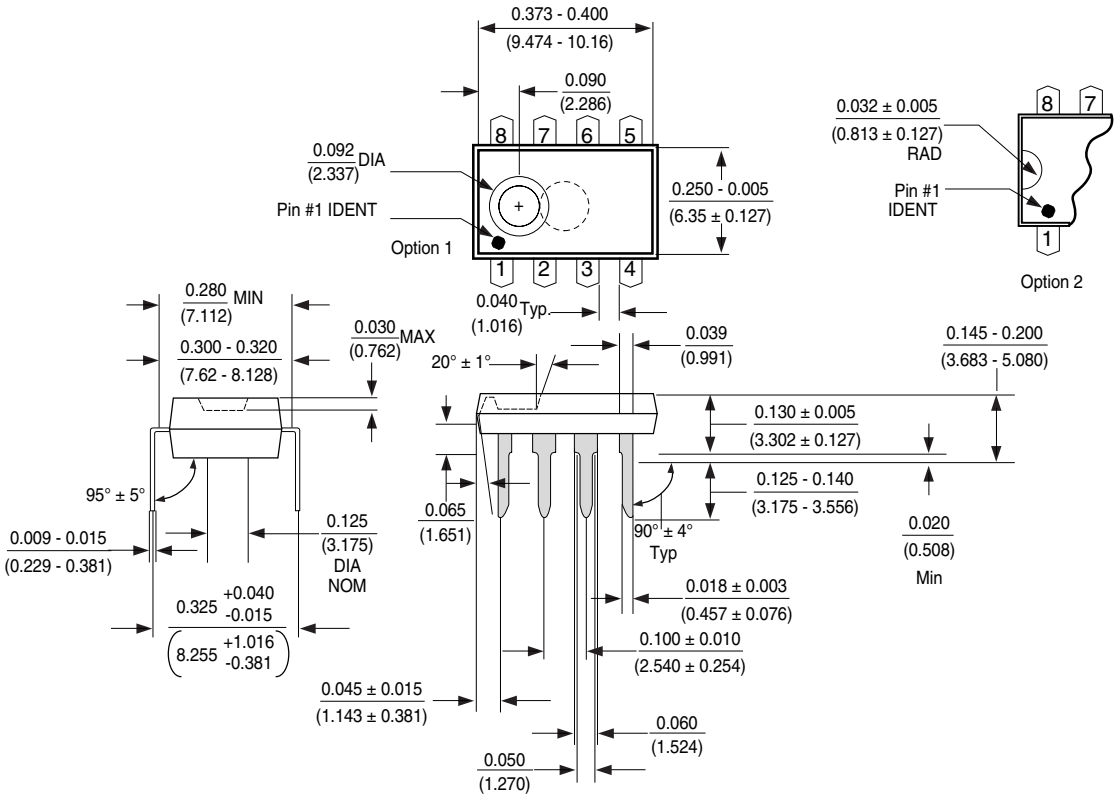
DS800023-12

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Small Out-Line Package (M8)
Order Number FM24C256xxxM8 or FM24C256xxxEM8
Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Dual-In-Line Package (N)
Order Number FM24C256xxxN or FM24C256xxxEN
Package Number N08E

Life Support Policy

Fairchild's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Fairchild Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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