FM18L08

256Kb 2.7-3.6V Bytewide FRAM Memory

Features

256K bit Ferroelectric Nonvolatile RAM
- Organized as 32,768 x 8 bits
- 10 year data retention at 85° C
- Unlimited read/write cycles
- NoDelay™ write
- Advanced high-reliability ferroelectric process

Superior to Battery-backed SRAM
- No battery concerns
- Monolithic reliability
- True surface mount solution, no rework steps
- Superior for moisture, shock, and vibration
- Resistant to negative voltage undershoots

SRAM & EEPROM Compatible
- JEDEC 32Kx8 SRAM & EEPROM pinout
- 70 ns access time
- 130 ns cycle time
- Equal access & cycle time for reads and writes

Low Power Operation
- 2.7V to 3.6V operation
- 15 mA active current
- 15 µA standby current

Industry Standard Configuration
- Industrial temperature -40° C to +85° C
- 28-pin SOP or DIP

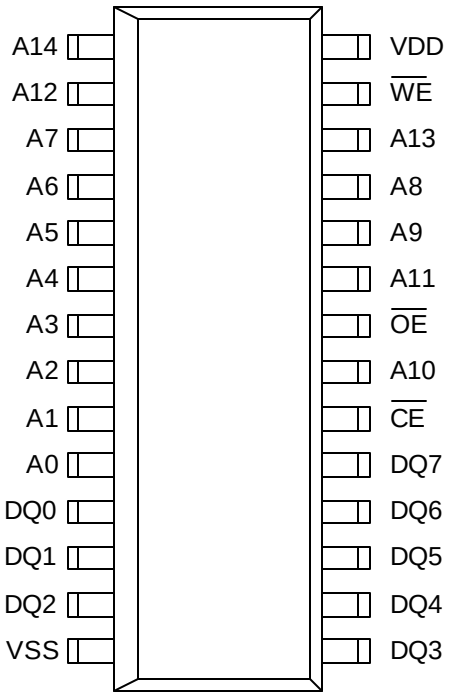
Description

The FM18L08 is a 256-kilobit nonvolatile memory employing an advanced ferroelectric process. A ferroelectric random access memory or FRAM is nonvolatile but operates in other respects as a RAM. It provides data retention for 10 years while eliminating the reliability concerns, functional disadvantages and system design complexities of battery-backed SRAM. Fast-write time and practically unlimited read/write endurance make it superior to other types of nonvolatile memory and a good substitute for ordinary SRAM.

In-system operation of the FM18L08 is very similar to other RAM based devices. Memory read- and write-cycles require equal times. The FRAM memory, however, is nonvolatile due to its unique ferroelectric memory process. Unlike BBSRAM, the FM18L08 is a truly monolithic nonvolatile memory. It provides the same functional benefits of a fast write without the serious disadvantages associated with modules and batteries or hybrid memory solutions.

These capabilities make the FM18L08 ideal for nonvolatile memory applications requiring frequent or rapid writes in a bytewide environment. The availability of a true surface-mount package improves the manufacturability of new designs, while the DIP package facilitates simple design retrofits. The FM18L08 offers guaranteed operation over an industrial temperature range of -40°C to +85°C.

Pin Configuration

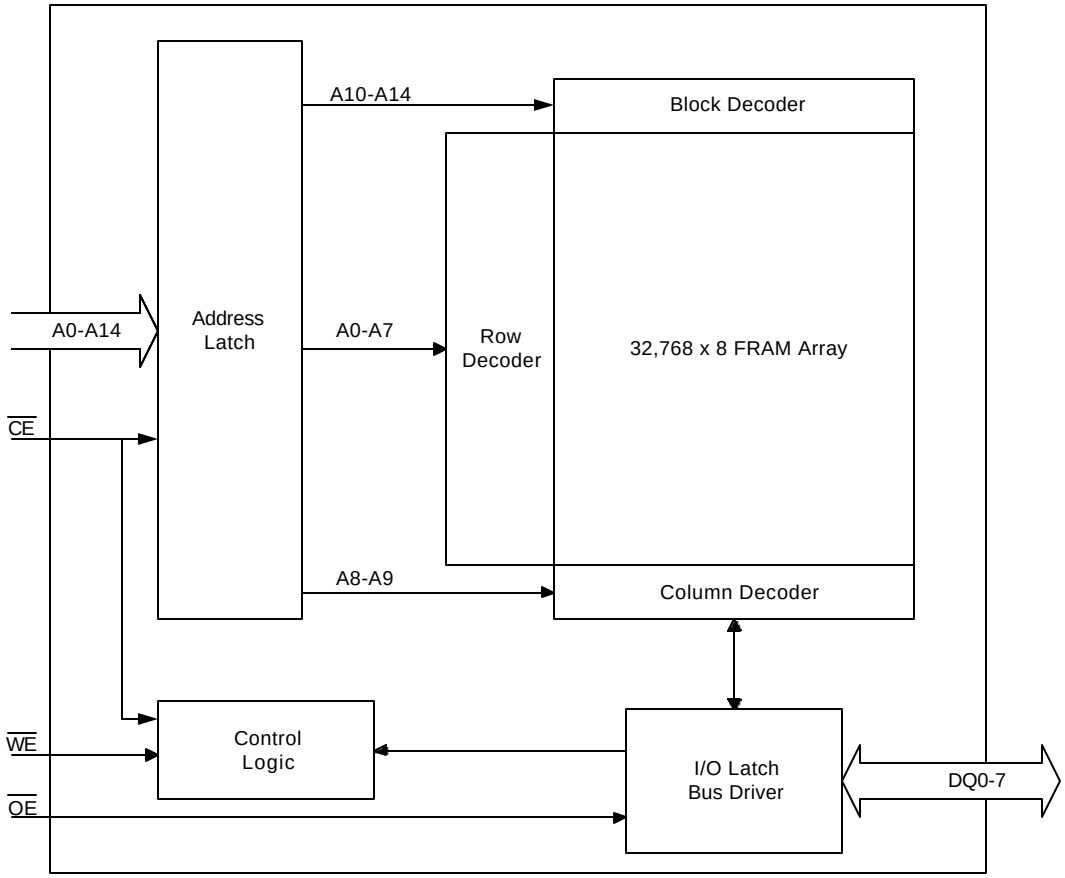


Ordering Information	
FM18L08-70-S	70 ns access, 28-pin SOP
FM18L08-70-P	70 ns access, 28-pin DIP

This data sheet contains specifications for a product under development.
Characterization is not complete; specifications may change without notice.

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Figure 1. Block Diagram



Pin Description

Pin Name	Pin Number	I/O	Pin Description
A0-A14	1-10, 21, 23-26	I	Address. The 15 address lines select one of 32,768 bytes in the FRAM array. The address value will be latched on the falling edge of /CE.
DQ0-7	11-13, 15-19	I/O	Data. 8-bit bi-directional data bus for accessing the FRAM array.
/CE	20	I	Chip Enable. /CE selects the device when low. The falling edge of /CE causes the address to be latched internally. Address changes that occur after /CE goes low will be ignored until the next falling edge occurs.
/OE	22	I	Output Enable. When /OE is low the FM18L08 drives the data bus when valid data is available. Taking /OE high causes the DQ pins to be tri-stated.
/WE	27	I	Write Enable. Taking /WE low causes the FM18L08 to write the contents of the data bus to the address location latched by the falling edge of /CE.
VDD	28	I	Supply Voltage.
VSS	14	I	Ground.

Functional Truth Table

/CE	/WE	/OE	Function
H	X	X	Standby/Precharge
↘	X	X	Latch Address
L	H	L	Read
L	L	X	Write

Overview

The FM18L08 is a bytewide FRAM logically organized as 32,768 x 8. It is accessed using an industry standard parallel interface. The FM18L08 is inherently nonvolatile via its unique ferroelectric process. All data written to the part is immediately nonvolatile with no delay. Functional operation of the FRAM memory is similar to SRAM type devices. The major operating difference between the FM18L08 and an SRAM (besides nonvolatile storage) is that the FM18L08 latches the address on the falling edge of /CE.

Memory Operation

Users access 32,768 memory locations each with 8 data bits through a parallel interface. The access and cycle time are the same for read and write memory operations. Writes occur immediately at the end of the access with no delay. Unlike an EEPROM, it is not necessary to poll the device for a ready condition since writes occur at bus speed. A pre-charge operation, where /CE goes inactive, is a part of every memory cycle. Thus unlike SRAM, the access and cycle times are not equal.

Note that the FM18L08 contains a limited low voltage write protection circuit. This will prevent access when VDD is much lower than the specified operating range. It is still the user's responsibility to ensure that VDD is within data sheet tolerances to prevent incorrect operation.

The FM18L08 is designed to operate in a manner very similar to other bytewide memory products. For users familiar with SRAM, the performance is comparable but the bytewide interface operates in a slightly different manner as described below. For users familiar with EEPROM, the obvious differences result from the higher write performance of FRAM technology including NoDelay writes and from unlimited write endurance.

Read Operation

A read operation begins on the falling edge of /CE. At this time, the address bits are latched and a memory cycle is initiated. Once started, a full memory cycle must be completed internally regardless of the state of /CE. Data becomes available on the bus after the access time has been satisfied.

After the address has been latched, the address value may be changed upon satisfying the hold time parameter. Unlike an SRAM, changing address values will have no effect on the memory operation after the address is latched.

The FM18L08 will drive the data bus when /OE is asserted to a low state. If /OE is asserted after the memory access time has been satisfied, the data bus will be driven with valid data. If /OE is asserted prior to completion of the memory access, the data bus will be driven when valid data is available. This feature minimizes supply current in the system by eliminating transients due to invalid data. When /OE is inactive the data bus will remain tri-stated.

Write Operation

Writes operations require the same time as reads. The FM18L08 supports both /CE- and /WE-controlled write cycles. In all cases, the address is latched on the falling edge of /CE.

In a /CE-controlled write, the /WE signal is asserted prior to beginning the memory cycle. That is, /WE is low when /CE falls. In this case, the device begins the memory cycle as a write. The FM18L08 will not drive the data bus regardless of the state of /OE.

In a /WE-controlled write, the memory cycle begins on the falling edge of /CE. The /WE signal falls after the falling edge of /CE. Therefore, the memory cycle begins as a read. The data bus will be driven according to the state of /OE until /WE falls. The timing of both /CE- and /WE-controlled write cycles is shown in the electrical specifications.

Write access to the array begins asynchronously after the memory cycle is initiated. The write access terminates on the rising edge of /WE or /CE, whichever is first. Data set-up time, as shown in the electrical specifications, indicates the interval during which data cannot change prior to the end of the write access.

Unlike other truly nonvolatile memory technologies, there is no write delay with FRAM. Since the read and write access times of the underlying memory are the same, the user experiences no delay through the bus. The entire memory operation occurs in a single bus cycle. Therefore, any operation including read or write can occur immediately following a write. Data polling, a technique used with EEPROMs to determine if a write is complete, is unnecessary.

Pre-charge Operation

The pre-charge operation is an internal condition where the state of the memory is prepared for a new

access. All memory cycles consist of a memory access and a pre-charge. The pre-charge is user initiated by taking the /CE signal high or inactive. It must remain high for at least the minimum pre-charge timing specification.

The user dictates the beginning of this operation since a pre-charge will not begin until /CE rises. However, the device has a maximum /CE low time specification that must be satisfied.

Applications

As a true nonvolatile RAM, the FM18L08 fits into many diverse applications. Clearly, its monolithic nature and high performance make it superior to battery-backed SRAM in most every application. Unlimited endurance allows the FM18L08 to be used in applications that could not take advantage of the previous generation of RAM products. This applications guide is intended to facilitate the transition from BBSRAM to FRAM. It is divided into two parts. First is a treatment of the advantages of FRAM memory compared with battery-backed SRAM. Second is a design guide, which highlights the simple design considerations that should be reviewed in both retrofit and new design situations.

FRAM Advantages

Although battery-backed SRAM is a mature and established solution, it has numerous weaknesses. These stem directly or indirectly from the presence of the battery. FRAM uses an inherently nonvolatile storage mechanism that requires no battery. It therefore eliminates these weaknesses. The major considerations in upgrading to FRAM are as follows.

Construction Issues

1. Cost

The cost of both the component and the manufacturing overhead of battery-backed SRAM is high. FRAM with its monolithic construction is inherently a lower cost solution. In addition, there is no 'built-in' rework step required for battery attachment when using surface mount parts. Therefore assembly is streamlined and more cost effective. In the case of DIP battery-backed modules, the user is constrained to through-hole assembly techniques and a board wash using no water.

2. Humidity

A typical battery-backed SRAM module is qualified at 60º C, 90% Rh, no bias, and no pressure. This is because the multi-component assemblies are vulnerable to moisture, not to mention dirt. FRAM is qualified using HAST – highly accelerated stress test. This requires 120º C at 85% Rh, 24.4 psia at VDD.

3. System reliability

Data integrity must be in question when using a battery-backed SRAM. They are inherently vulnerable to shock and vibration. If the battery contact comes loose, data will be lost. In addition a negative voltage, even a momentary undershoot, on any pin of a battery-backed SRAM can cause data loss. The negative voltage causes current to be drawn directly from the battery. These momentary short circuits can greatly weaken a battery and reduce its capacity over time. In general, there is no way to monitor the lost battery capacity. Should an undershoot occur in a battery backed system during a power down, data can be lost immediately.

4. Space

Certain disadvantages of battery-backed SRAM, such as susceptibility to shock, can be reduced by using the old fashioned DIP module. However, this alternative takes up board space, height, and dictates through-hole assembly. FRAM offers a true surface-mount solution that uses 25% of the board space.

No multi-piece assemblies, no connectors, and no modules. A real nonvolatile RAM is finally available!

Direct Battery Issues

5. Field maintenance

Batteries, no matter how mature, are a built-in maintenance problem. They eventually must be replaced. Despite long life projections, it is impossible to know if any individual battery will last considering all of the factors that can degrade them.

6. Environmental

Lithium batteries are widely regarded as an environmental problem. They are a potential fire hazard and proper disposal can be a burden. In addition, shipping of lithium batteries may be restricted.

7. Style!

Backing up an SRAM with a battery is an old-fashioned approach. In many cases, such modules are the only through-hole component in sight. FRAM is the latest memory technology and it is changing the way systems are designed.

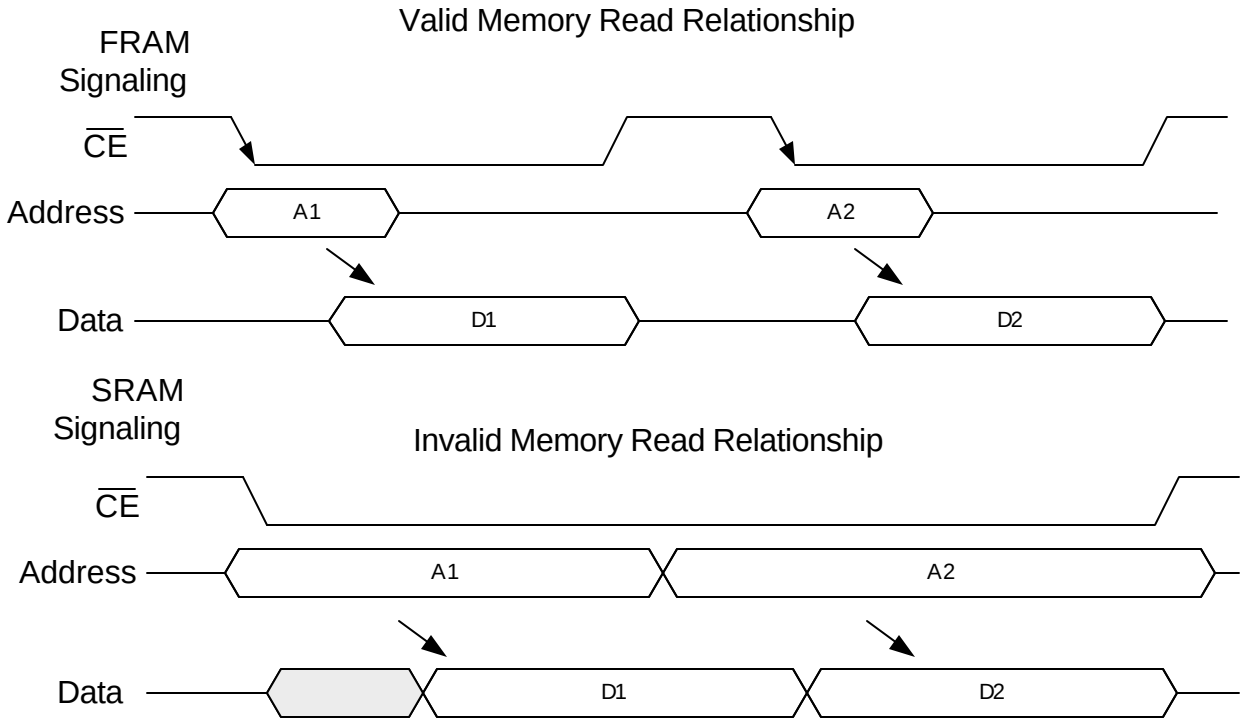
FRAM Design Considerations

When designing with FRAM for the first time, users of SRAM will recognize a few minor differences. First, bytewide FRAM memories latch each address on the falling edge of chip enable. This allows the address bus to change after starting the memory access. Since every access latches the memory address on the falling edge of /CE, users should not ground it as they might with SRAM.

Users that are modifying existing designs to use FRAM should examine the hardware address decoders. Decoders should be modified to qualify addresses with an address valid signal if they do not already. In many cases, this is the only change required. Systems that drive chip enable active, then inactive for each valid address may need no modifications. An example of the target signal relationships are shown in Figure 2. Also shown is a common SRAM signal relationship that will not work for the FM18L08.

The main design issue is to create a decoder scheme that will drive /CE active, then inactive for each address. This accomplishes the two goals of latching the new address and creating the precharge period.

Figure 2. Memory Address Relationships



Electrical Specifications

Absolute Maximum Ratings

Description	*Ratings*
Ambient storage or operating temperature	-40°C to + 85°C
Voltage on any pin with respect to ground	-1.0V to +5.0V
Lead temperature (Soldering, 10 seconds)	300° C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and the functional operation of the device at these or any other conditions above those listed in the operational section of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability

DC Operating Conditions TA = -40° C to + 85° C, VDD = 2.7V to 3.65V unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Units	Notes
VDD	Power Supply	2.7		3.65	V	1
IDD	VDD Supply Current - Active		5	15	mA	2
ISB	Standby Current - TTL			400	µA	3
ISB	Standby Current - CMOS		7	15	µA	4
ILI	Input Leakage Current			10	µA	5
ILO	Output Leakage Current			10	µA	5
VIL	Input Low Voltage	-1.0		0.8	V	1
VIH	Input High Voltage	2.0		VDD + 1.0	V	1
VOL	Output Low Voltage			0.4	V	1,6
VOH	Output High Voltage	2.4V			V	1,7

Notes

1. Referenced to VSS.
2. VDD = 3.65V, /CE cycling at minimum cycle time. All inputs at CMOS levels, all outputs unloaded.
3. VDD = 3.65V, /CE at VIH, All inputs at TTL levels, all outputs unloaded.
4. VDD = 3.65V, /CE at VDD, All inputs at CMOS levels, all outputs unloaded.
5. VIN, VOUT between VDD and VSS.
6. IOL = 3.2 mA
7. IOH = -1.0 mA

Read Cycle AC Parameters TA = -40° C to + 85° C, VDD = 2.7V to 3.65V unless otherwise specified

Symbol	Parameter	Min	Max	Units	Notes
tCE	Chip Enable Access Time (to data valid)		70	ns	
tCA	Chip Enable Active Time	70	10,000	ns	
tRC	Read Cycle Time	130		ns	
tPC	Precharge Time	60		ns	
tAS	Address Setup Time	0		ns	
tAH	Address Hold Time	10		ns	
tOE	Output Enable Access Time		10	ns	
tHZ	Chip Enable to Output High-Z		15	ns	1
tOHZ	Output Enable to Output High-Z		15	ns	1

Write Cycle AC Parameters TA = -40° C to + 85° C, VDD = 2.7V to 3.65V unless otherwise specified

Symbol	Parameter	Min	Max	Units	Notes
tCA	Chip Enable Active Time	70	10,000	ns	
tCW	Chip Enable to Write High	70		ns	
tWC	Write Cycle Time	130		ns	
tPC	Precharge Time	60		ns	
tAS	Address Setup Time	0		ns	
tAH	Address Hold Time	10		ns	
tWP	Write Enable Pulse Width	40		ns	
tDS	Data Setup	40		ns	
tDH	Data Hold	0		ns	
tWZ	Write Enable Low to Output High Z		15	ns	1
tWX	Write Enable High to Output Driven	10		ns	1
tHZ	Chip Enable to Output High-Z		15	ns	1
tWS	Write Setup	0		ns	2
tWH	Write Hold	0		ns	2

Notes

1 This parameter is periodically sampled and not 100% tested.

2 The relationship between /CE and /WE determines if a /CE- or /WE-controlled write occurs. There is no timing specification associated with this relationship.

Data Retention TA = -40° C to + 85° C, VDD = 2.7V to 3.65V unless otherwise specified

Parameter	Min	Units	Notes
Data Retention	10	Years	1
Endurance	1E16	Cycles	2

Notes

1. Data retention is specified at 85° C.
2. Endurance is the guaranteed number of read- or write-cycles per address that can be performed while maintaining the specified data retention. It should be impossible to reach this limit for most applications.

Power Cycle Timing TA = -40° C to + 85° C, VDD = 2.7V to 3.65V unless otherwise specified

Symbol	Parameter	Min	Units	Notes
tPU	VDD Min to First Access Start	1	µS	
tPD	Last Access Complete to VDD Min	0	µS	

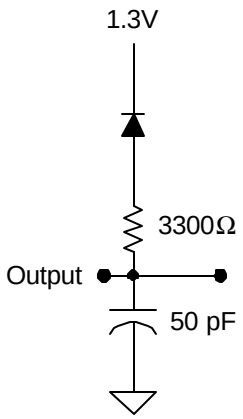
Capacitance TA = 25° C , f=1.0 MHz, VDD = 3V

Symbol	Parameter	Max	Units	Notes
CI/O	Input Output Capacitance	8	pF	
CIN	Input Capacitance	6	pF	

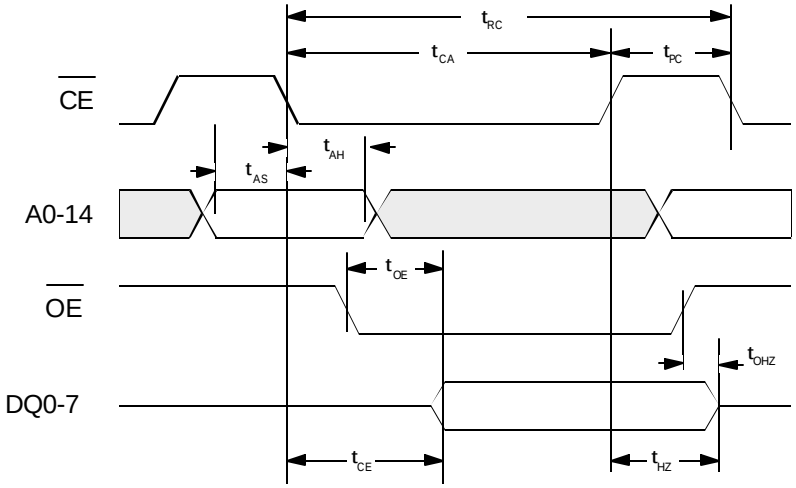
AC Test Conditions

Input Pulse Levels	0.1 VDD to 0.9 VDD
Input rise and fall times	5 ns
Input and output timing levels	1.5V

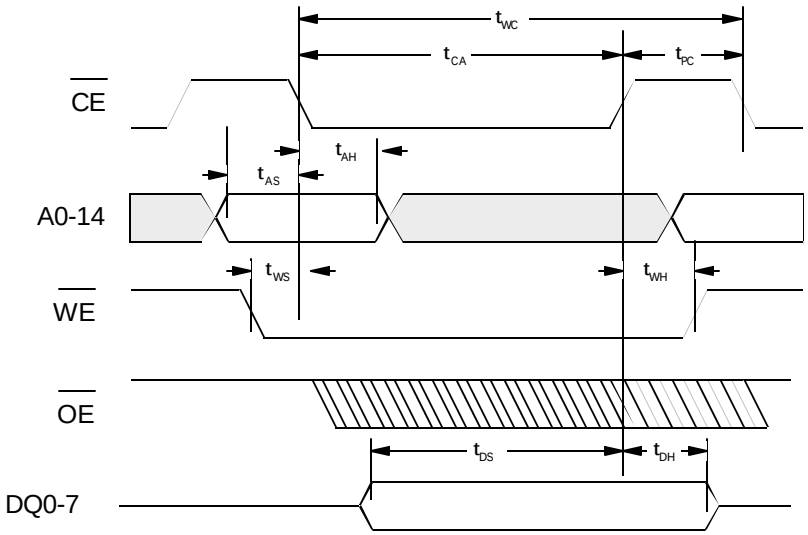
Equivalent AC Load Circuit



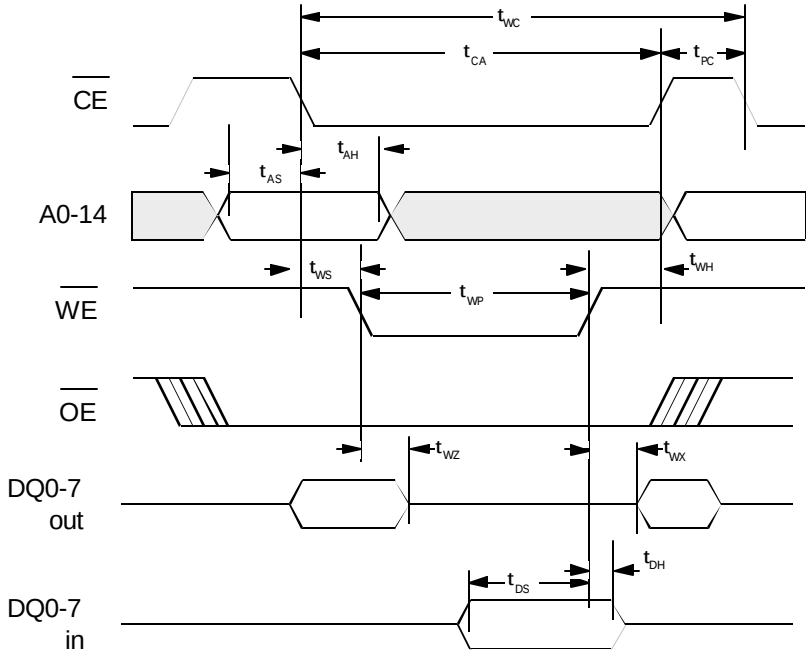
Read Cycle Timing



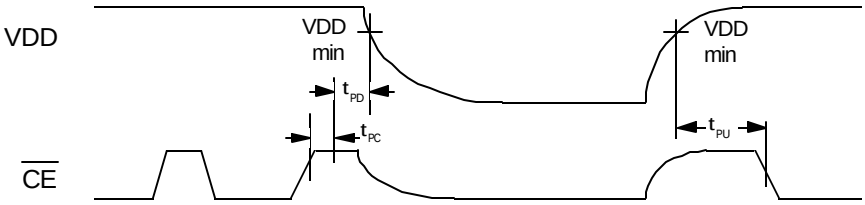
Write Cycle Timing - /CE Controlled Timing



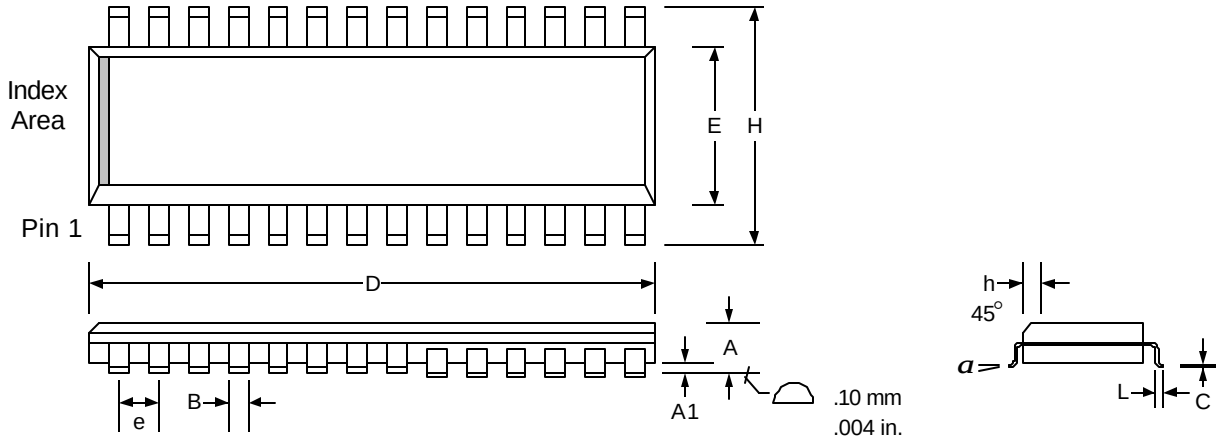
Write Cycle Timing - /WE Controlled Timing



Power Cycle Timing



28-pin SOP JEDEC MS-013

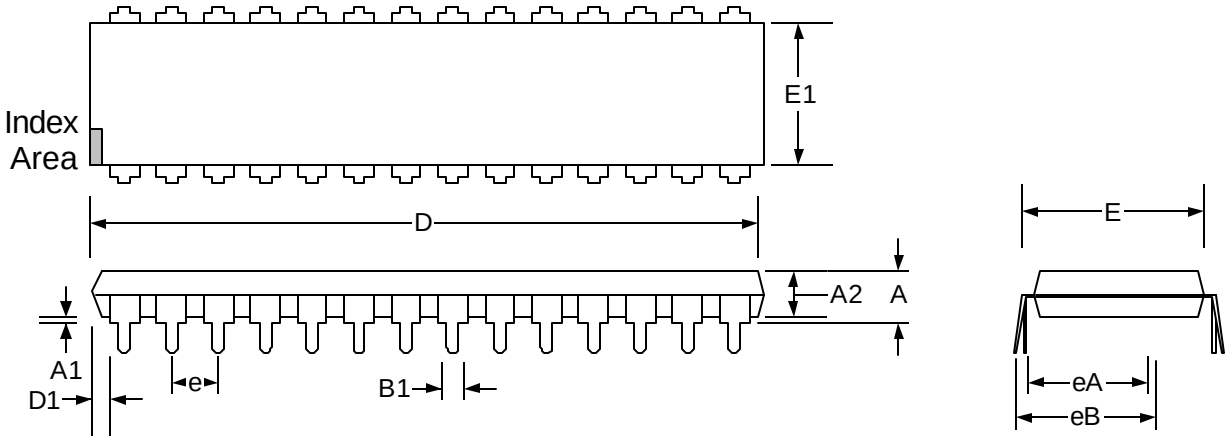


Selected Dimensions

For complete dimensions and notes, refer to JEDEC MS-013
Controlling dimensions is in millimeters. Conversions to inches are not exact.

Symbol	Dim	Min	Nom.	Max
A	mm in.	2.35 0.0926		2.65 0.1043
A1	mm in.	0.10 0.004		0.30 0.0118
B	mm in.	0.33 0.013		0.51 0.020
C	mm in.	0.23 0.0091		0.32 0.0125
D	mm in.	17.70 0.6969		18.10 0.7125
E	mm in.	7.40 0.2914		7.60 0.2992
e	mm in.		1.27 BSC 0.050 BSC	
H	mm in.	10.00 0.394		10.65 0.419
h	mm in.	0.25 0.010		0.75 0.029
L	mm in.	.40 0.016		1.27 0.050
α		0°		8°

28-pin 600-mil DIP



Selected Dimensions

For complete dimensions and notes, refer to JEDEC MS-011
Controlling dimensions is in inches. Conversions to millimeters are not exact.

Symbol	Dim	Min	Nom.	Max
A	in. mm			0.250 6.35
A1	in. mm	0.015 0.39		
A2	in. mm	0.125 3.18		0.195 4.95
B	in. mm	0.014 0.356		0.022 0.558
B1	in. mm	0.030 0.77		0.070 1.77
D	in. mm	1.380 35.1		1.565 39.7
D1	in. mm	0.005 0.13		
E	in. mm	0.600 15.24		0.625 15.87
E1	in. mm	0.485 12.32		0.580 14.73
e	in. mm		0.100 BSC 2.54 BSC	
eA	in. mm		0.600 BSC 15.24 BSC	
eB	in. mm			0.700 17.78