FDWS86068-F085

N-Channel POWERTRENCH® MOSFET

100 V, 80 A, 6.4 mΩ

ON Semiconductor®

www.onsemi.com

V_{DSS}	I_D MAX	$R_{DS(on)}$ MAX
100 V	80 A	6.4 mΩ

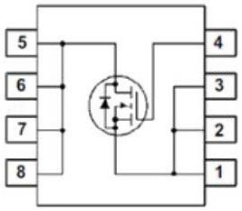
Features

- Typ $R_{DS(on)}$ = 5.2 mΩ at V_{GS} = 10 V, I_D = 80 A
- Typ $Q_{g(tot)}$ = 31 nC at V_{GS} = 10 V, I_D = 80 A
- UIS Capability
- Qualified to AEC Q101
- Wettable flanks for automatic optical inspection (AOI)
- These Devices are Pb−Free and are RoHS Compliant

Applications

- Automotive Engine Control
- Powertrain Management
- Solenoid and Motor Drivers
- Electronic Steering

ELECTRICAL CONNECTION



N-Channel MOSFET

MOSFET MAXIMUM RATINGS (T_A = 25°C, Unless otherwise specified)

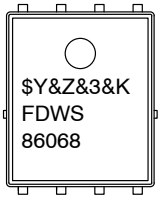
Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain to Source Voltage	100	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current (T_C = 25°C) Continuous (V_{GS} = 10 V) (Note 1) Pulsed	 80 (see Fig. 4)	A
E_{AS}	Single Pulse Avalanche Energy (Note 2)	36	mJ
P_D	Power Dissipation Derate above 25°C	214 1.43	W W/°C
T_J, T_{STG}	Operating and Storage Temperature	−55 to +150	°C
$R_{\theta JC}$	Thermal Resistance (Junction to case)	0.7	°C/W
$R_{\theta JA}$	Maximum Thermal Resistance (Junction to Ambient) (Note 3)	50	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Top View Bottom View

Power 56
(DFN8)
CASE 506DW

MARKING DIAGRAM



$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
FDWS86068	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDWS86068	FDWS86068−F085	Power 56	13″	12 mm	3,000 Units

NOTES:
1. Current is limited by wirebond configuration.
2. Starting T_J = 25°C, L = 20 μH, I_{AS} = 60 A, V_{DD} = 80 V during inductor charging and V_{DD} = 0 V during time in avalanche.
3. $R_{\theta JA}$ is the sum of the junction−to−case and case−to−ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design. The maximum rating presented here is based on mounting on a 1 in2 pad of 2oz copper.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
B_{VDSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	100	–	–	V
I_{DSS}	Drain to Source Leakage Current	V_{DS} = 100 V, V_{GS} = 0 V (T_J = 25°C) (T_J = 175°C) (Note 4)	 – –	 – –	 1 1	 μA mA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V	–	–	±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	2	3	4	V
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 10 V, I_D = 80 A (T_J = 25°C) (T_J = 175°C) (Note 4)	 – –	 5.2 11.4	 6.4 14	 mΩ
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHZ	–	2220	–	pF
C_{oss}	Output Capacitance		–	1350	–	pF
C_{rss}	Reverse Transfer Capacitance		–	19	–	pF
R_g	Gate Resistance	V_{GS} = 0.5 V, f = 1 MHz	–	0.3	–	Ω
$Q_{g(tot)}$	Total Gate Charge	V_{GS} = 0 to 10 V, V_{DD} = 50 V, I_D = 80 A	–	31	43	nC
$Q_{g(th)}$	Threshold Gate Charge	V_{GS} = 0 to 2 V, V_{DD} = 50 V, I_D = 80 A	–	4	–	nC
Q_{gs}	Gate to Source Gate Charge	V_{DD} = 50 V, I_D = 80 A	–	12	–	nC
Q_{gd}	Gate to Drain "Miller" Charge		–	7	–	nC
SWITCHING CHARACTERISTICS						
t_{on}	Turn-On Time	V_{DD} = 50 V, I_D = 80 A, V_{GS} = 10 V, R_{GEN} = 6 Ω	–	–	30	ns
$t_{d(on)}$	Turn-On Delay Time		–	15	–	ns
t_r	Turn-On Rise Time		–	6	–	ns
$t_{d(off)}$	Turn-Off Delay Time		–	24	–	ns
t_f	Turn-Off Fall Time		–	7	–	ns
t_{off}	Turn-Off Time		–	–	48	ns
DRAIN-SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Forward Voltage	I_{SD} = 80 A, V_{GS} = 0 V	–	0.95	1.3	V
		I_{SD} = 40 A, V_{GS} = 0 V	–	0.87	1.2	V
T_{rr}	Reverse Recovery Time	I_F = 80 A, dI_{SD}/dt = 100 A/μs	–	61	80	ns
Q_{rr}	Reverse Recovery Charge		–	56	84	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
4. The maximum value is specified by design at T_J = 175°C. Product is not tested to this condition in production

TYPICAL CHARACTERISTICS

(T_J = 25°C unless otherwise noted)

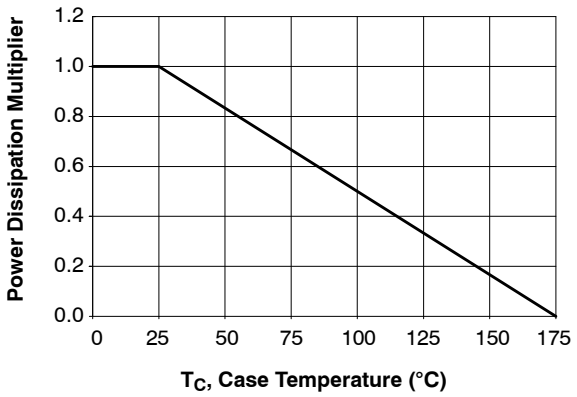


Figure 1. Normalized Power Dissipation vs. Case Temperature

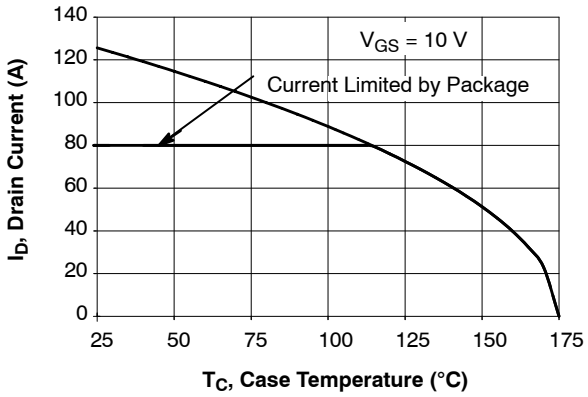


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

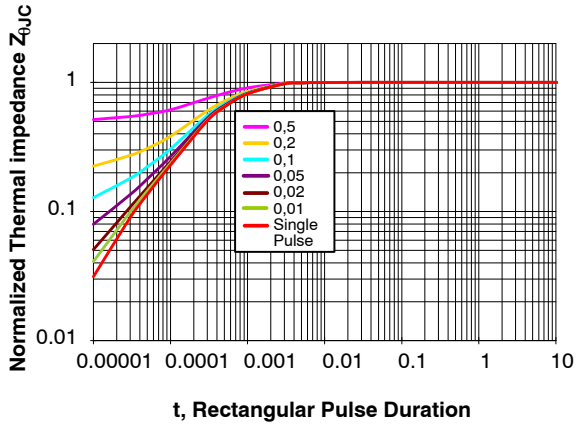


Figure 3. Normalized Maximum Transient Thermal Impedance

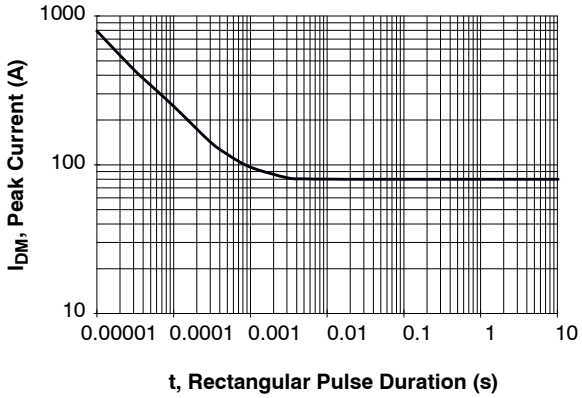


Figure 4. Peak Current Capability

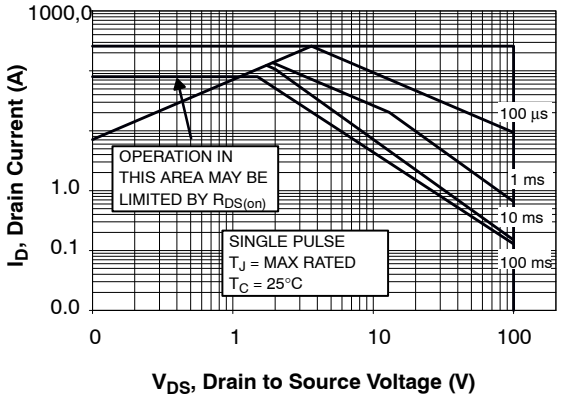
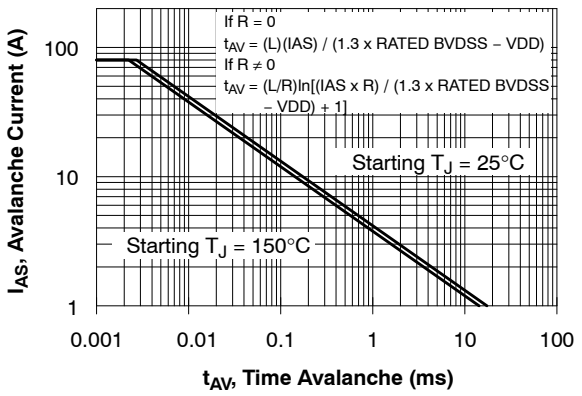


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to On Semiconductor Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

TYPICAL CHARACTERISTICS

(T_J = 25°C unless otherwise noted)

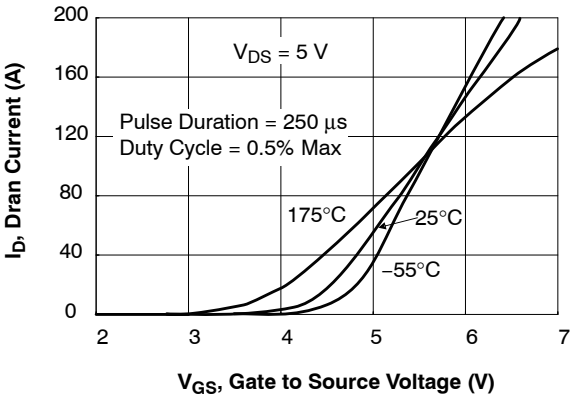


Figure 7. Transfer Characteristic

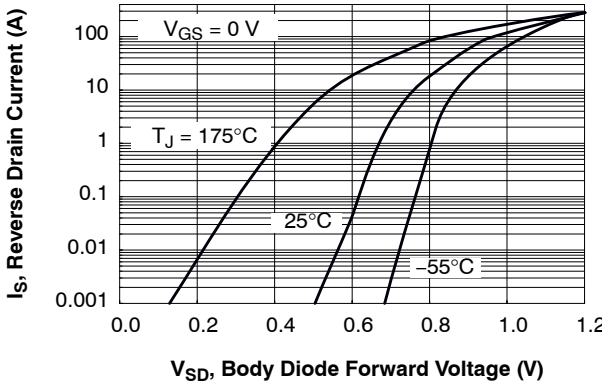


Figure 8. Forward Diode Characteristics

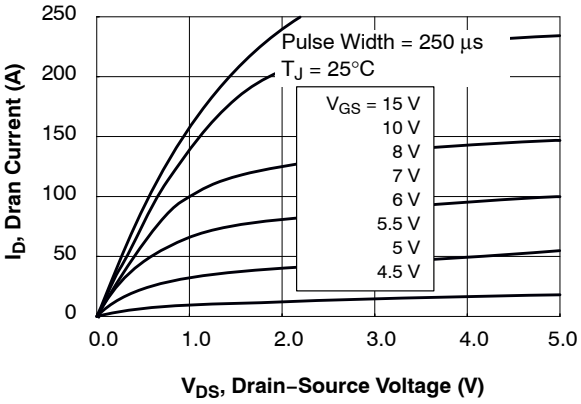


Figure 9.

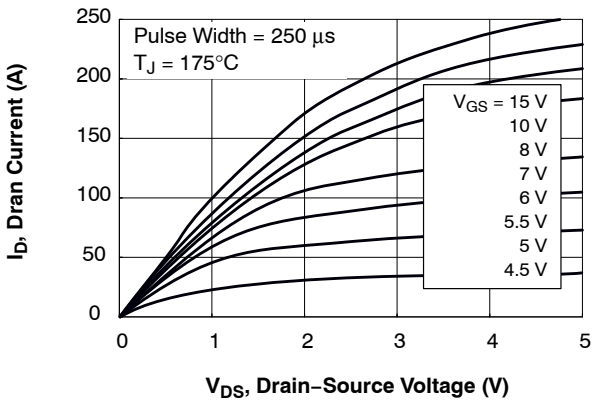


Figure 10. Peak Current Capability

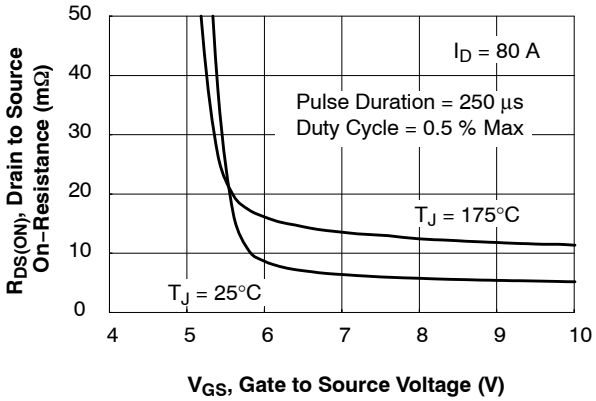


Figure 11. R_{DSON} vs. Gate Voltage

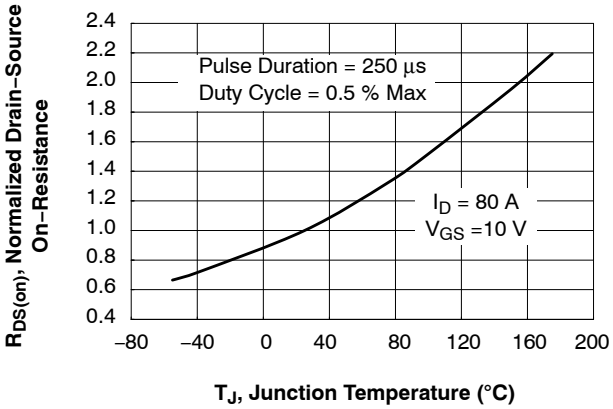


Figure 12. Normalized R_{DSON} vs. Junction Temperature

TYPICAL CHARACTERISTICS

(T_J = 25°C unless otherwise noted)

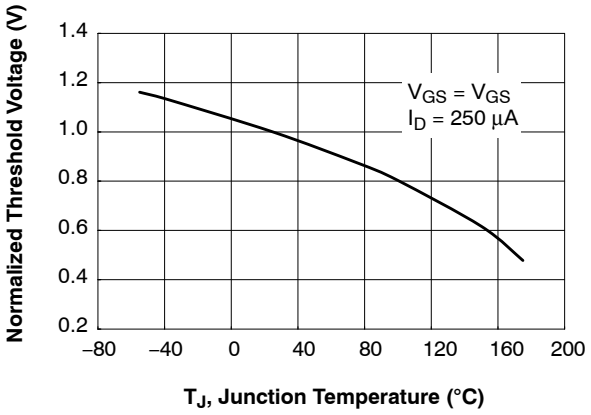


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

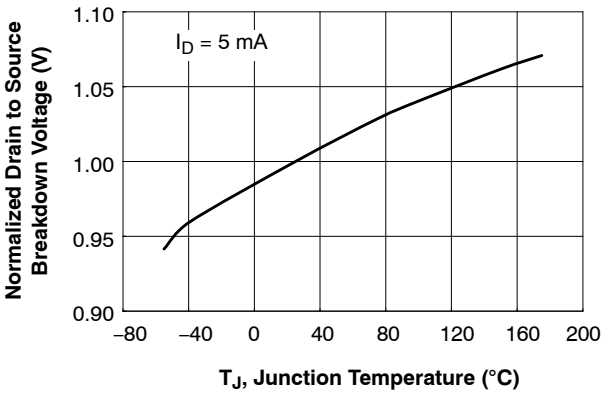


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

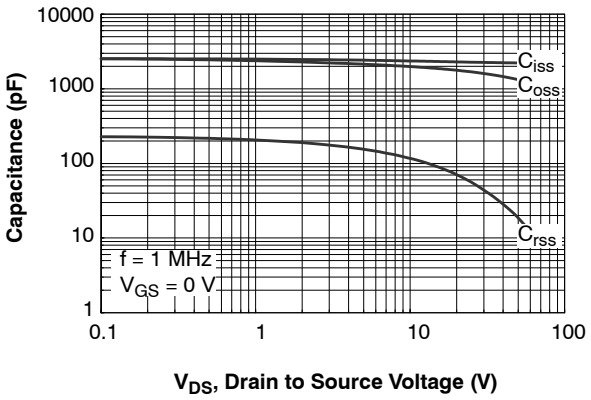


Figure 15. Capacitance vs. Drain to Source Voltage

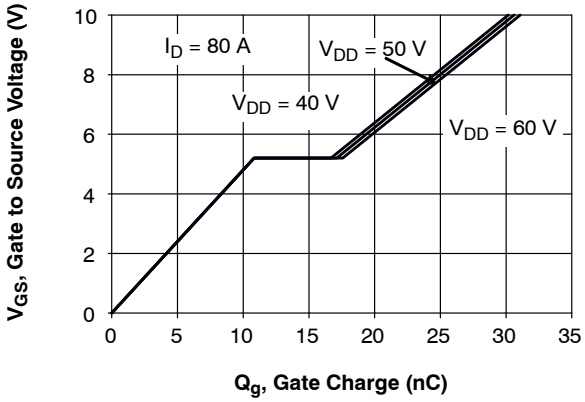
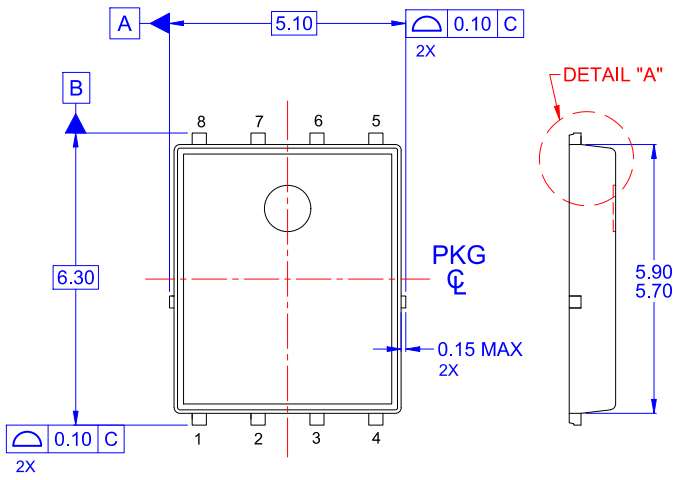


Figure 16. Gate Charge vs. Gate to Source Voltage

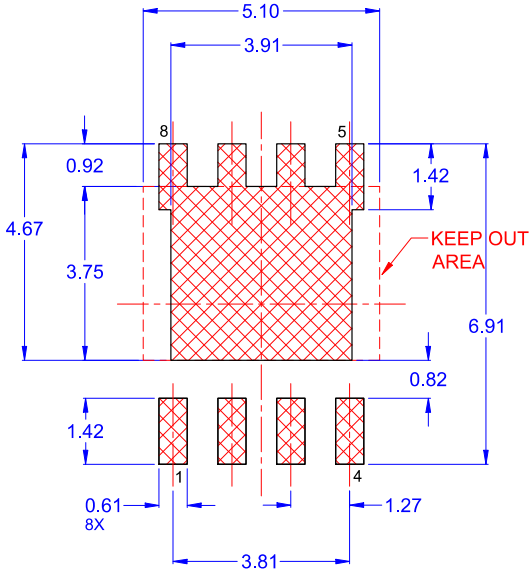
DFN8 5.1x6.3, 1.27P
CASE 506DW
ISSUE O

DATE 28 FEB 2017

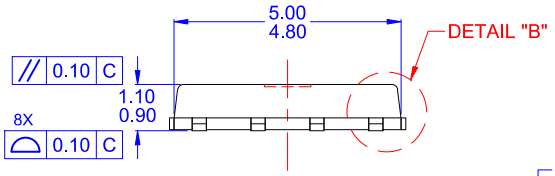


TOP VIEW

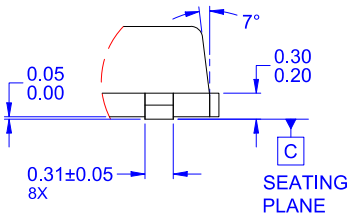
SIDE VIEW

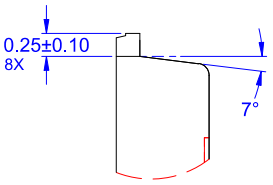


LAND PATTERN
RECOMMENDATION



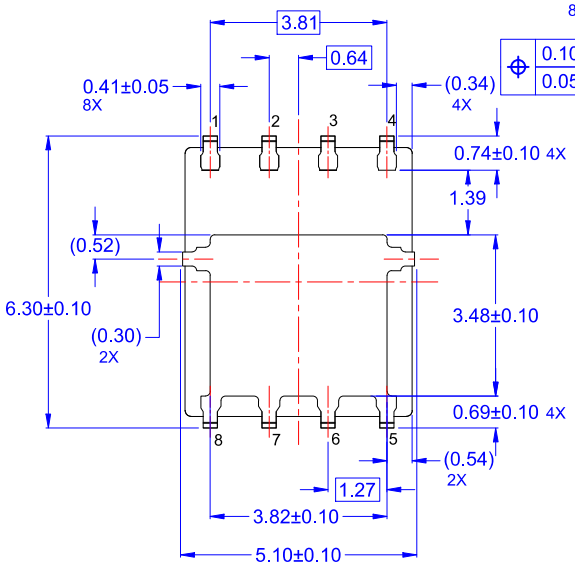
FRONT VIEW





DETAIL "B"

DETAIL "A"



BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED
A) PACKAGE STANDARD REFERENCE: JEDEC REGISTRATION, MO-240, ISSUE B, VAR AA, DATED 10/2009.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.

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NEW STANDARD:		
DESCRIPTION:	**DFN8 5.1x6.3, 1.27P**	**PAGE 1 OF 2**

ISSUE	REVISION	DATE
O	RELEASED FOR PRODUCTION FROM FAIRCHILD MKT−PQFN08P TO ON SEMICONDUCTOR. REQ. BY D. TRUHITTE.	28 FEB 2017

PUBLICATION ORDERING INFORMATION

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