FDS4465

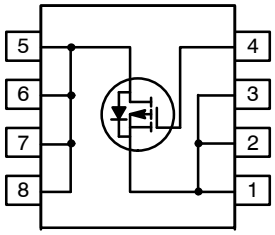
P-Channel 1.8V Specified POWERTRENCH® MOSFET

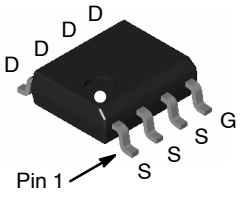
ON Semiconductor®

www.onsemi.com

V_{DSS}	$R_{DS(on)}$ MAX	$I_{D\ MAX}$
−20 V	8.5 mΩ @ −4.5 V	−13.5 A
	10.5 mΩ @ −2.5 V	
	14 mΩ @ −1.8 V	

P−Channel





SOIC8
CASE 751EB

Description

This P−Channel 1.8 V specified MOSFET is a rugged gate version of ON Semiconductor's advanced POWERTRENCH process. It has been optimized for power management applications with a wide range of gate drive voltage (1.8 V – 8 V).

Features

- −13.5 A, −20 V
  - $R_{DS(ON)}$ = 8.5 mΩ @ V_{GS} = −4.5 V
  - $R_{DS(ON)}$ = 10.5 mΩ @ V_{GS} = −2.5 V
  - $R_{DS(ON)}$ = 14 mΩ @ V_{GS} = −1.8 V
- Fast Switching Speed
- High Performance Trench Technology for Extremely Low $R_{DS(ON)}$
- High Current and Power Handling Capability

Applications

- Power Management
- Load Switch
- Battery Protection

Specifications

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

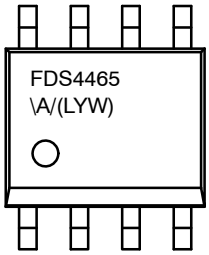
Symbol	Parameter		Value	Unit
V_{DSS}	Drain−to−Source Voltage		−20	V
V_{GSS}	Gate−to−Source Voltage		±8	V
I_D	Drain Current	Continuous (Note 1a)	−13.5	A
		Pulsed	−50	
P_D	Power Dissipation	(Note 1a)	2.5	W
		(Note 1b)	1.5	
		(Note 1c)	1.2	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		−55 to +175	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient (Note 1a)	50	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient (Note 1c)	125	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction−to−Ambient (Note 1)	25	°C/W

MARKING DIAGRAM



A	= Assembly Site
L	= Wafer Lot Number
YW	= Assembly Start Week
FDS4465	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

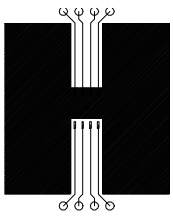
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ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

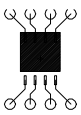
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	–20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = –250 μA, Referenced to 25°C		–12		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = –16 V, V_{GS} = 0 V			–1	μA
I_{GSSF}	Gate–Body Leakage, Forward	V_{GS} = 8 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate–Body Leakage, Reverse	V_{GS} = –8 V, V_{DS} = 0 V			–100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	–0.4	–0.6	–1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = –250 μA, Referenced to 25°C		3		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = –4.5 V, I_D = –13.5 A		6.7	8.5	mΩ
		V_{GS} = –2.5 V, I_D = –12 A		8.0	10.5	
		V_{GS} = –1.8 V, I_D = –10.5 A		9.8	14	
		V_{GS} = –4.5 V, I_D = –13.5 A, T_J = 125°C		9.0	13	
$I_{D(on)}$	On–State Drain Current	V_{GS} = –4.5 V, V_{DS} = –5 V	–50			A
g_{FS}	Forward Transconductance	V_{DS} = –5 V, I_D = –13.5 A		70		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = –10 V, V_{GS} = 0 V, f = 1.0 MHz		8237		pF
C_{oss}	Output Capacitance			1497		pF
C_{rss}	Reverse Transfer Capacitance			750		pF
R_g	Gate Resistance		0.1	3.0	6.0	Ω
SWITCHING CHARACTERISTICS (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = –10 V, I_D = –1 A, V_{GS} = –4.5 V, R_{GEN} = 6 Ω		20	36	ns
t_r	Turn–On Rise Time			24	38	ns
$t_{d(off)}$	Turn–Off Delay Time			300	480	ns
t_f	Turn–Off Fall Time			140	224	ns
Q_g	Total Gate Charge	V_{DS} = –10 V, I_D = –1 A, V_{GS} = –4.5 V		86	120	nC
Q_{gs}	Gate–Source Charge			20		nC
Q_{gd}	Gate–Drain Charge			11		nC
DRAIN–SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain–Source Diode Forward Current				–2.1	A
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = –2.1 A (Note 2)		–0.6	–1.2	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

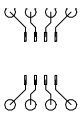
1. $R_{\theta JA}$ is the sum of the junction–to–case and case–to–ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 50°C/W when mounted on a 1 in^2 pad of 2 oz copper



b) 105°C/W when mounted on a .04 in^2 pad of 2 oz copper



c) 125°C/W when mounted on a minimum pad

Scale 1:1 on letter size paper

2. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%

TYPICAL CHARACTERISTICS

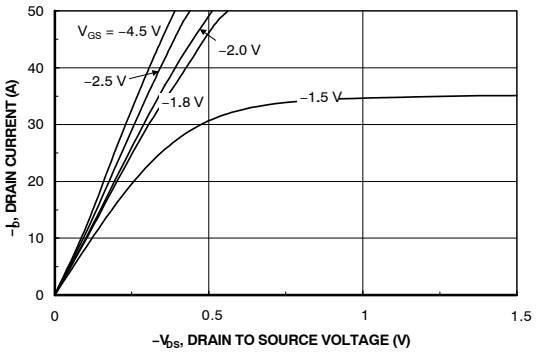


Figure 1. On−Region Characteristics

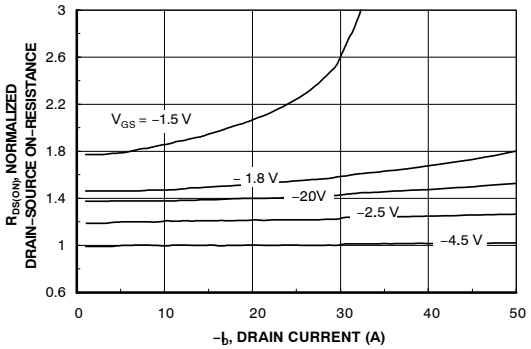


Figure 2. On−Resistance Variation with Drain Current and Gate Voltage

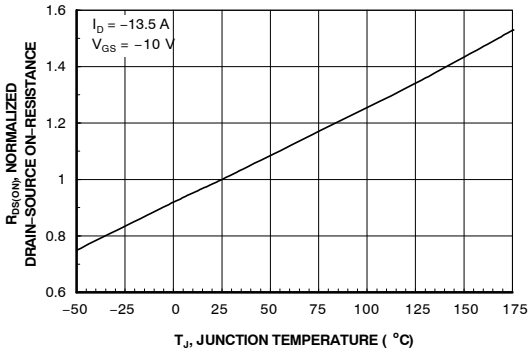


Figure 3. On−Resistance Variation with Temperature

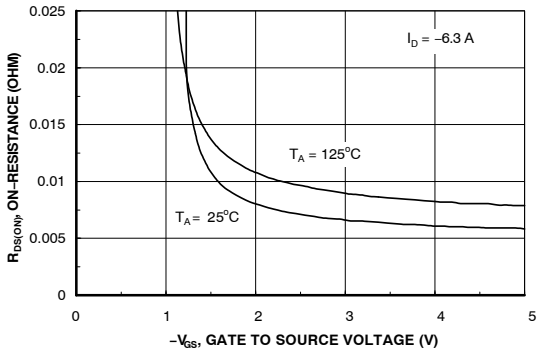


Figure 4. On−Resistance Variation with Gate−to−Source Voltage

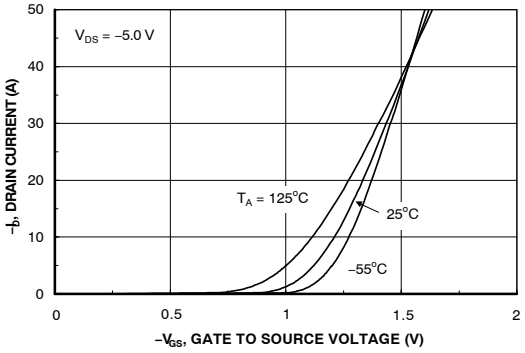


Figure 5. Transfer Characteristics

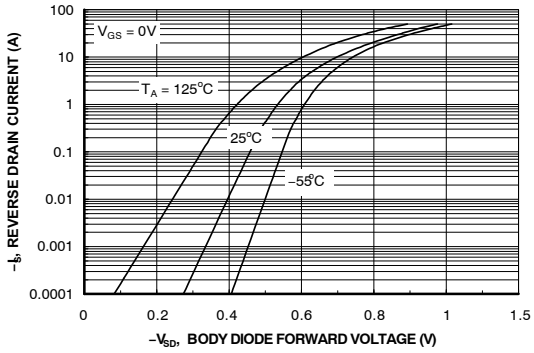


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL CHARACTERISTICS

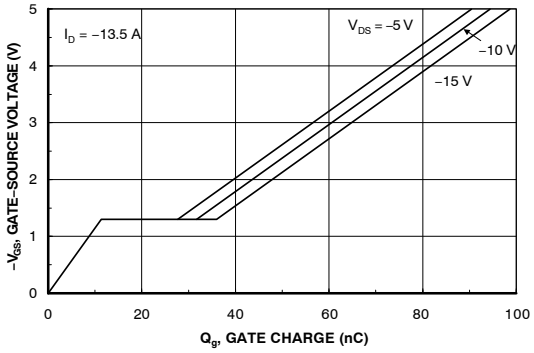


Figure 7. Gate Charge Characteristics

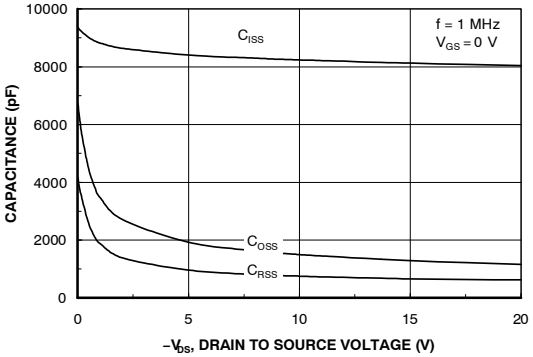


Figure 8. Capacitance Characteristics

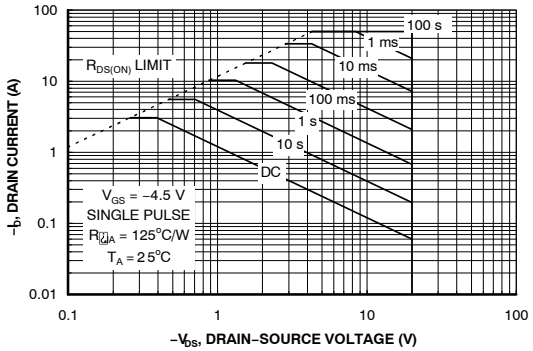


Figure 9. Maximum Safe Operating Area

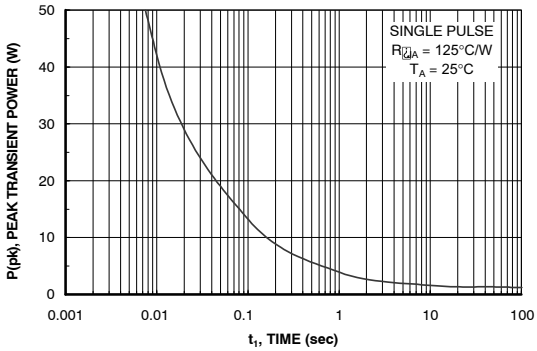


Figure 10. Single Pulse Maximum Power Dissipation

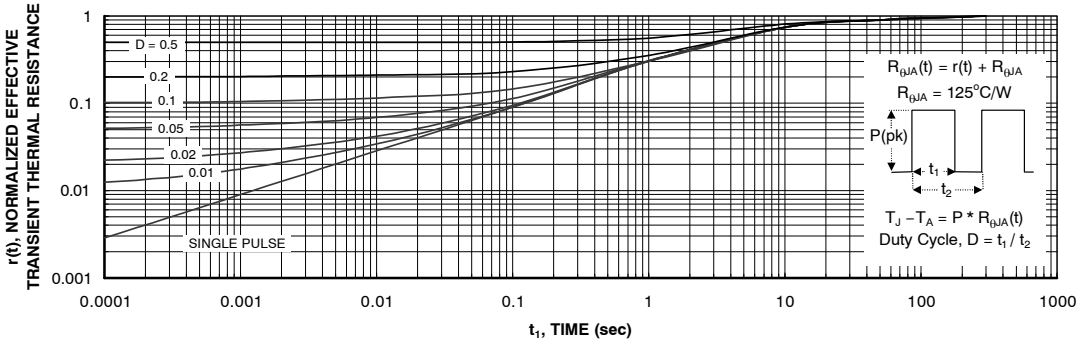


Figure 11. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on circuit board design.

PACKAGE MARKING AND ORDERING INFORMATION

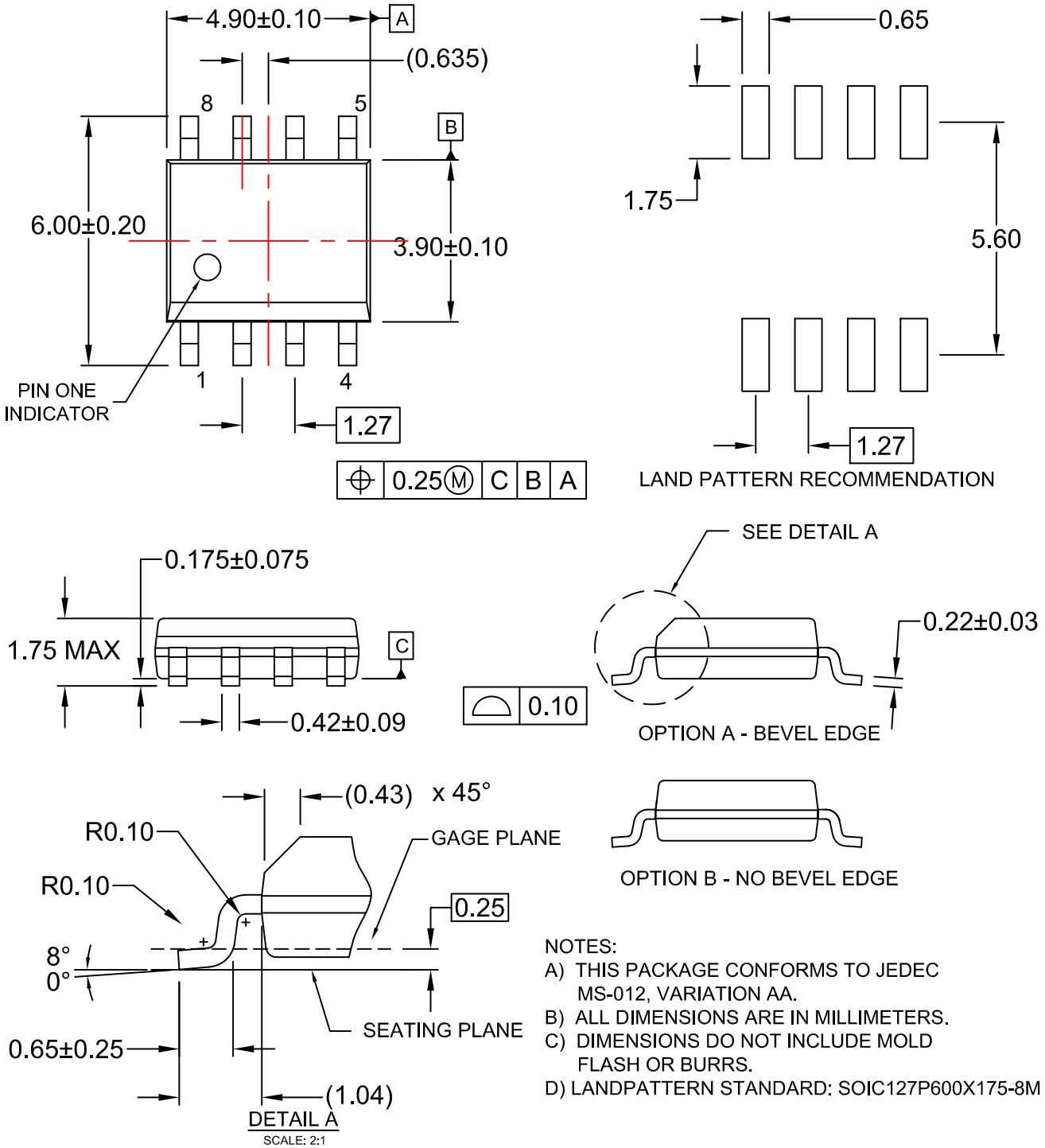
Device Marking	Device	Reel Size	Tape Width	Shipping†
FDS4465	FDS4465	13″	12 mm	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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CASE 751EB
ISSUE A

DATE 24 AUG 2017



NOTES:
A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M

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