

FDS3992

N-Channel PowerTrench® MOSFET

100V, 4.5A, 62mΩ

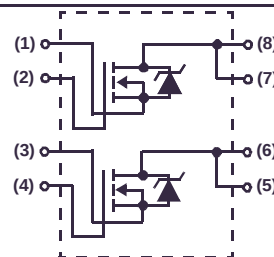
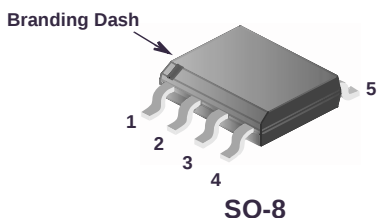
Features

- $r_{DS(ON)} = 54m\Omega$ (Typ.), $V_{GS} = 10V$, $I_D = 4.5A$
- $Q_g(tot) = 11nC$ (Typ.), $V_{GS} = 10V$
- Low Miller Charge
- Low Q_{RR} Body Diode
- Optimized efficiency at high frequencies
- UIS Capability (Single Pulse and Repetitive Pulse)

Applications

- DC/DC converters and Off-Line UPS
- Distributed Power Architectures and VRMs
- Primary Switch for 24V and 48V Systems
- High Voltage Synchronous Rectifier
- Direct Injection / Diesel Injection Systems
- 42V Automotive Load Control
- Electronic Valve Train Systems

Formerly developmental type 82745



MOSFET Maximum Ratings $T_A = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	100	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current		
	Continuous ($T_A = 25^\circ C$, $V_{GS} = 10V$, $R_{\theta JA} = 50^\circ C/W$)	4.5	A
	Continuous ($T_A = 100^\circ C$, $V_{GS} = 10V$, $R_{\theta JA} = 50^\circ C/W$)	2.8	A
	Pulsed	Figure 4	A
E_{AS}	Single Pulse Avalanche Energy (Note 1)	167	mJ
P_D	Power dissipation	2.5	W
	Derate above $25^\circ C$	20	mW/ $^\circ C$
T_J, T_{STG}	Operating and Storage Temperature	-55 to 150	$^\circ C$

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient at 10 seconds (Note 3)	50	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient at 1000 seconds (Note 3)	85	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 2)	25	$^\circ C/W$

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDS3992	FDS3992	SO-8	330mm	12mm	2500 units

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

B_{VDSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$	100	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80\text{V}$ $V_{GS} = 0\text{V}$ $T_C = 150^\circ\text{C}$	-	-	1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(TH)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$	2	-	4	V
$r_{DS(ON)}$	Drain to Source On Resistance	$I_D = 4.5\text{A}$, $V_{GS} = 10\text{V}$	-	0.054	0.062	Ω
		$I_D = 2\text{A}$, $V_{GS} = 6\text{V}$	-	0.072	0.108	
		$I_D = 4.5\text{A}$, $V_{GS} = 10\text{V}$, $T_C = 150^\circ\text{C}$	-	0.107	0.123	

Dynamic Characteristics

C_{ISS}	Input Capacitance	$V_{DS} = 25\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$	-	750	-	pF
C_{OSS}	Output Capacitance		-	118	-	pF
C_{RSS}	Reverse Transfer Capacitance		-	27	-	pF
$Q_{g(TOT)}$	Total Gate Charge at 10V	$V_{GS} = 0\text{V}$ to 10V	-	11	15	nC
$Q_{g(TH)}$	Threshold Gate Charge	$V_{GS} = 0\text{V}$ to 2V	-	1.4	1.9	nC
Q_{gs}	Gate to Source Gate Charge	$V_{DD} = 50\text{V}$ $I_D = 4.5\text{A}$ $I_g = 1.0\text{mA}$	-	3.5	-	nC
Q_{gs2}	Gate Charge Threshold to Plateau		-	2.1	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	2.8	-	nC

Switching Characteristics ($V_{GS} = 10\text{V}$)

t_{ON}	Turn-On Time	$V_{DD} = 50\text{V}$, $I_D = 4.5\text{A}$ $V_{GS} = 10\text{V}$, $R_{GS} = 27\Omega$	-	-	47	ns
$t_{d(ON)}$	Turn-On Delay Time		-	8	-	ns
t_r	Rise Time		-	23	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time		-	28	-	ns
t_f	Fall Time		-	26	-	ns
t_{OFF}	Turn-Off Time		-	-	81	ns

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Voltage	$I_{SD} = 4.5\text{A}$	-	-	1.25	V
		$I_{SD} = 2\text{A}$	-	-	1.0	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 4.5\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	48	ns
Q_{RR}	Reverse Recovery Charge	$I_{SD} = 4.5\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	65	nC

Notes:

1: Starting $T_J = 25^\circ\text{C}$, $L = 37\text{mH}$, $I_{AS} = 3\text{A}$.

2: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

3: $R_{\theta JA}$ is measured with 1.0 in² copper on FR-4 board

Typical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

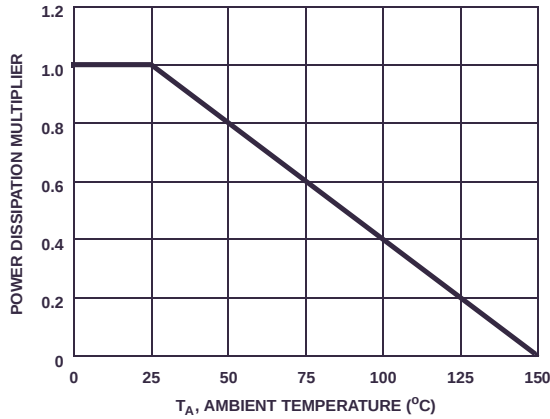


Figure 1. Normalized Power Dissipation vs Ambient Temperature

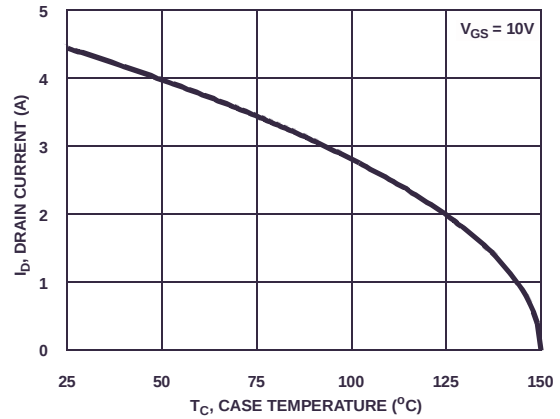


Figure 2. Maximum Continuous Drain Current vs Case Temperature

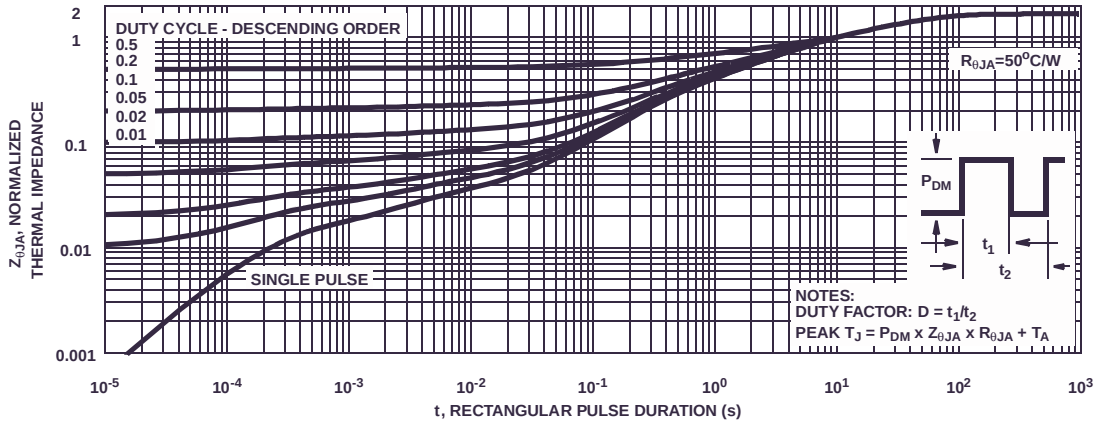


Figure 3. Normalized Maximum Transient Thermal Impedance

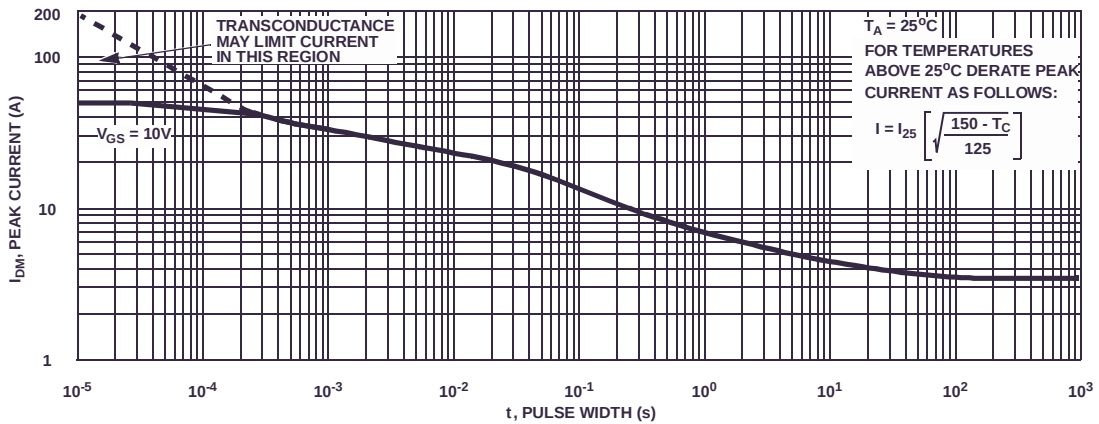


Figure 4. Peak Current Capability

Typical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

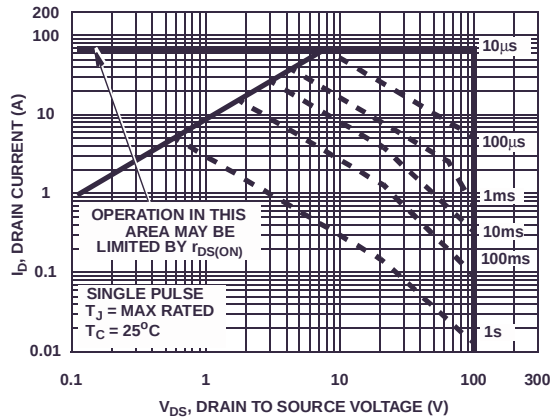
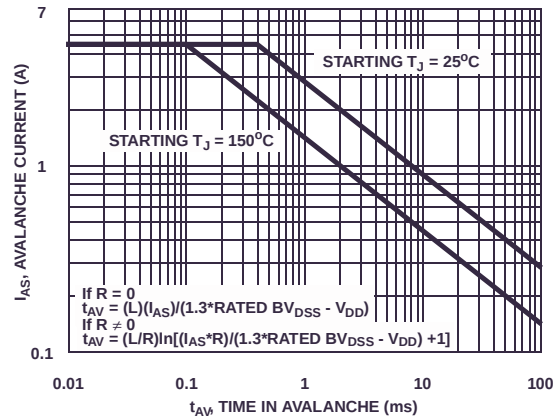


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

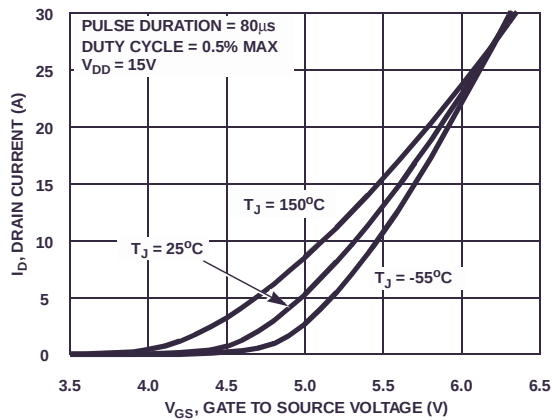


Figure 7. Transfer Characteristics

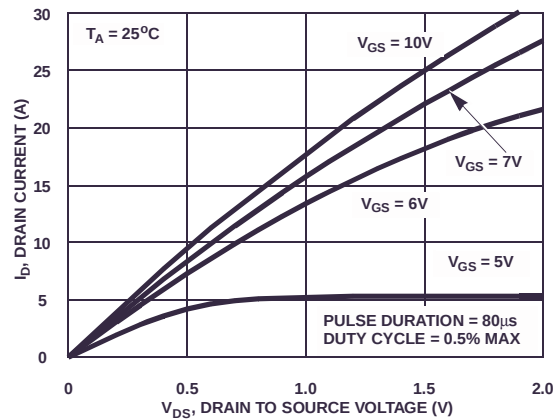


Figure 8. Saturation Characteristics

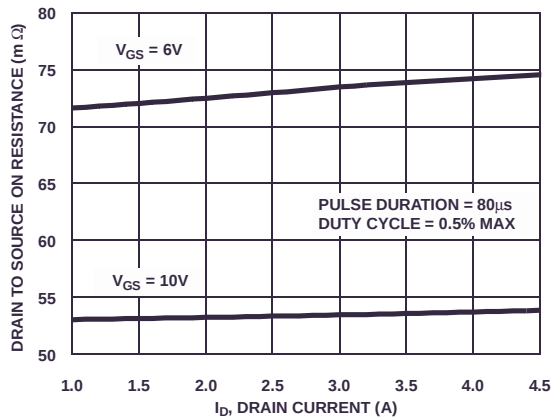


Figure 9. Drain to Source On Resistance vs Drain Current

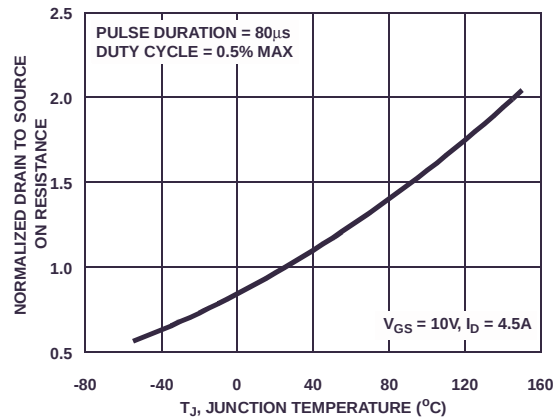


Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature

Typical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

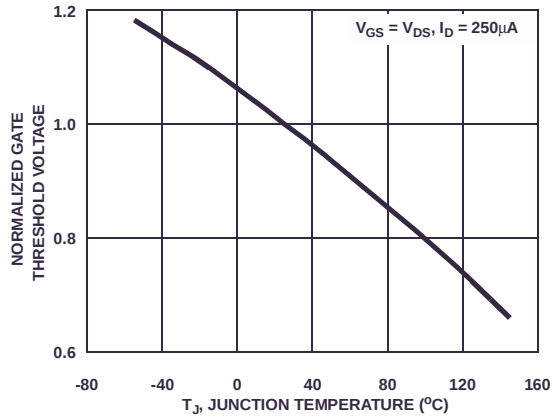


Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature

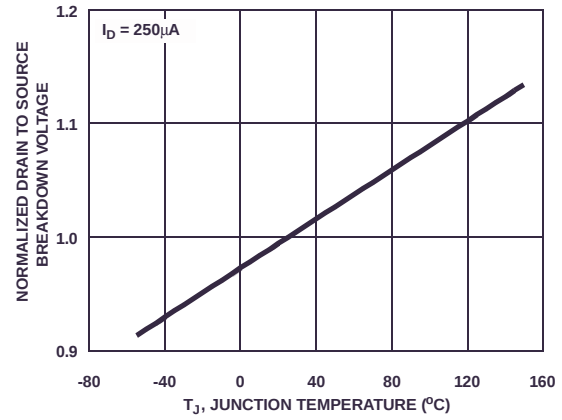


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

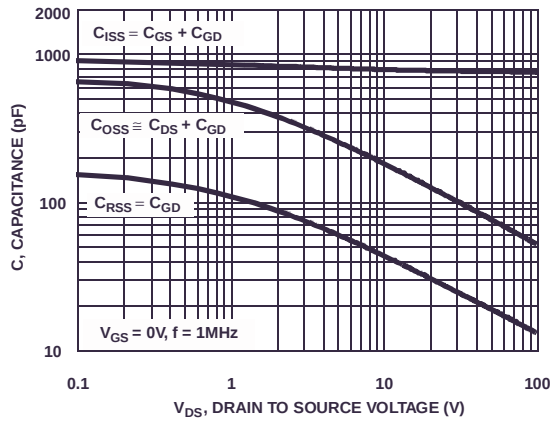


Figure 13. Capacitance vs Drain to Source Voltage

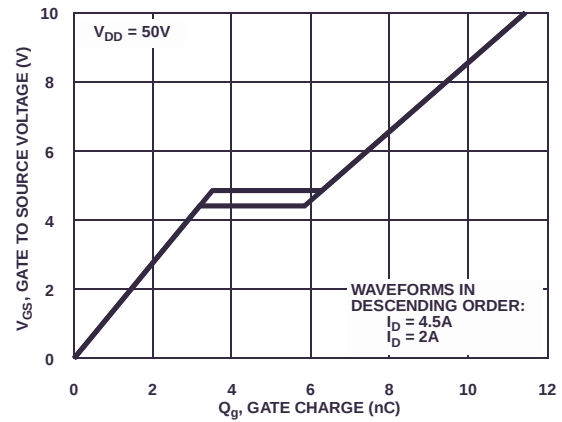


Figure 14. Gate Charge Waveforms for Constant Gate Currents

Test Circuits and Waveforms

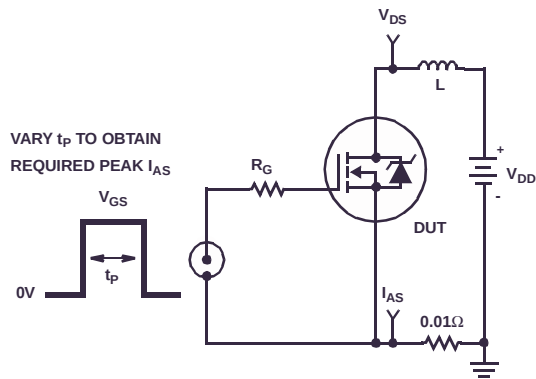


Figure 15. Unclamped Energy Test Circuit

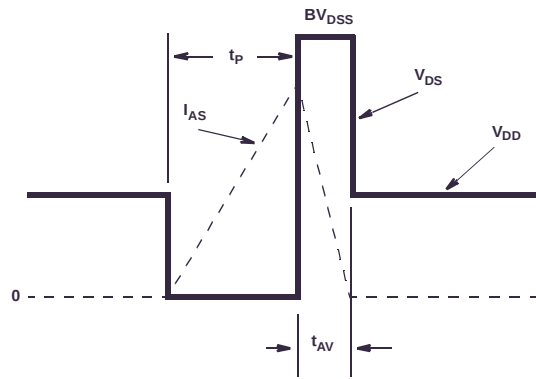


Figure 16. Unclamped Energy Waveforms

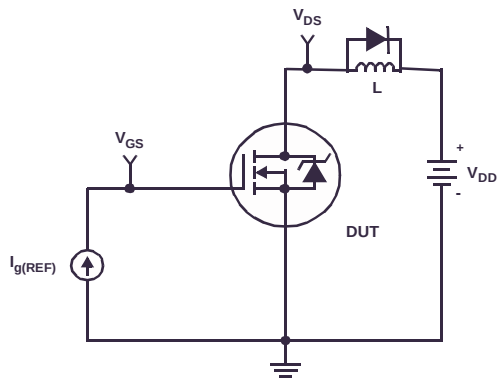


Figure 17. Gate Charge Test Circuit

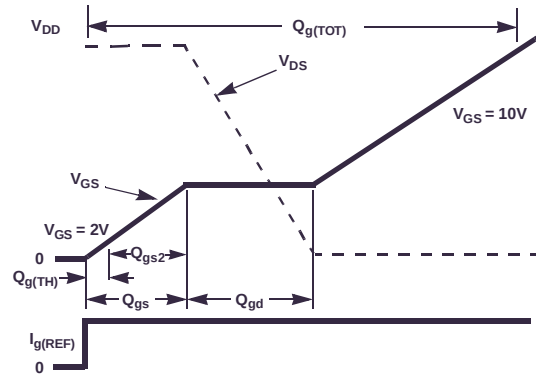


Figure 18. Gate Charge Waveforms

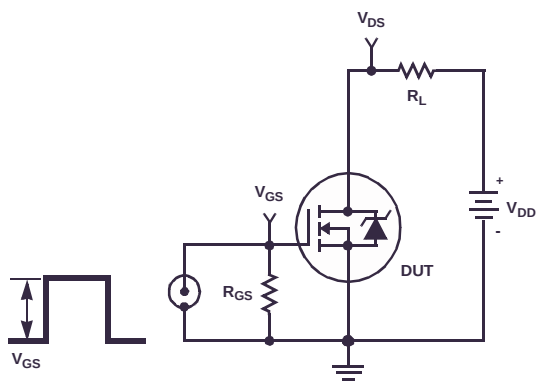


Figure 19. Switching Time Test Circuit

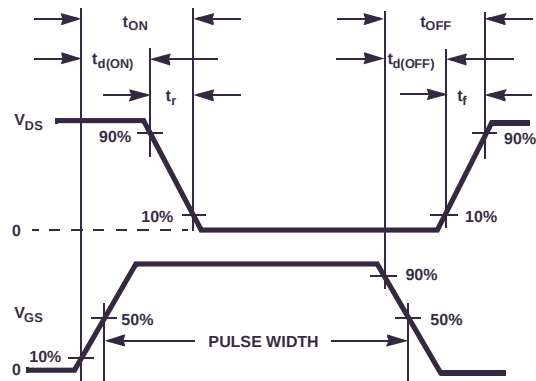


Figure 20. Switching Time Waveforms

Thermal Resistance vs. Mounting Pad Area

The maximum rated junction temperature, T_{JM} , and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation, P_{DM} , in an application. Therefore the application's ambient temperature, T_A ($^{\circ}\text{C}$), and thermal resistance $R_{\theta JA}$ ($^{\circ}\text{C/W}$) must be reviewed to ensure that T_{JM} is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{R_{\theta JA}} \quad (\text{EQ. 1})$$

In using surface mount devices such as the SO8 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of P_{DM} is complex and influenced by many factors:

1. Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
2. The number of copper layers and the thickness of the board.
3. The use of external heat sinks.
4. The use of thermal vias.
5. Air flow and board orientation.
6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

Fairchild provides thermal information to assist the designer's preliminary application evaluation. Figure 21 defines the $R_{\theta JA}$ for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 1oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the Fairchild device Spice thermal model or manually utilizing the normalized

maximum transient thermal impedance curve.

Thermal resistances corresponding to other copper areas can be obtained from Figure 21 or by calculation using Equation 2. The area, in square inches is the top copper area including the gate and source pads.

$$R_{\theta JA} = 64 + \frac{26}{0.23 + \text{Area}} \quad (\text{EQ. 2})$$

The transient thermal impedance ($Z_{\theta JA}$) is also effected by varied top copper board area. Figure 22 shows the effect of copper pad area on single pulse transient thermal impedance. Each trace represents a copper pad area in square inches corresponding to the descending list in the graph. Spice and SABER thermal models are provided for each of the listed pad areas.

Copper pad area has no perceivable effect on transient thermal impedance for pulse widths less than 100ms. For pulse widths less than 100ms the transient thermal impedance is determined by the die and package. Therefore, CHERM1 through CHERM5 and RHERM1 through RHERM5 remain constant for each of the thermal models. A listing of the model component values is available in Table 1.

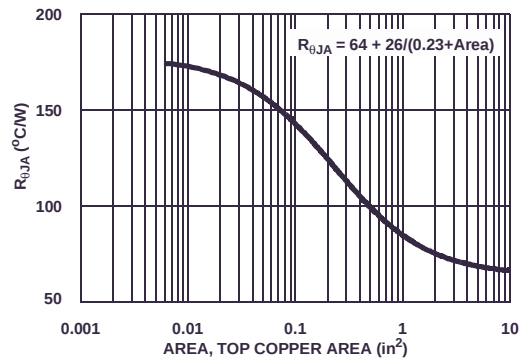


Figure 21. Thermal Resistance vs Mounting Pad Area

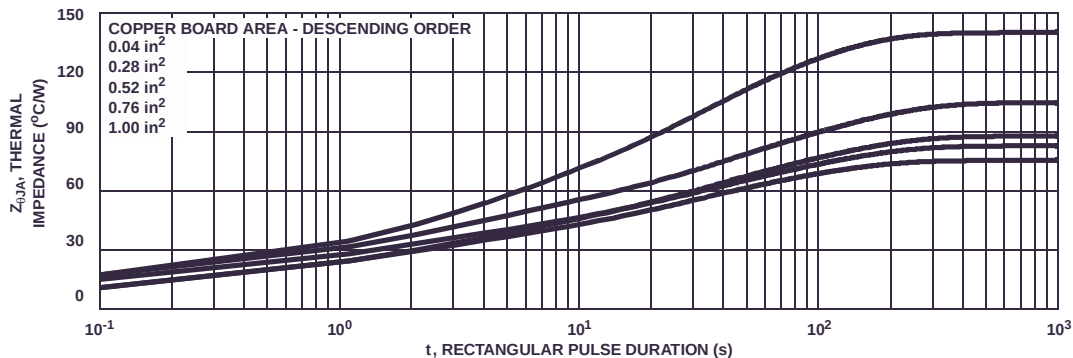


Figure 22. Thermal Impedance vs Mounting Pad Area

PSPICE Electrical Model

.SUBCKT FDS3992 2 1 3 ; rev Aug 2002
 Ca 12 8 2.3e-10
 Cb 15 14 3.5e-10
 Cin 6 8 7.47e-10

Dbody 7 5 DbodyMOD
 Dbreak 5 11 DbreakMOD
 Dplcap 10 5 DplcapMOD

Ebreak 11 7 17 18 108
 Eds 14 8 5 8 1
 Egs 13 8 6 8 1
 Esg 6 10 6 8 1
 Evthres 6 21 19 8 1
 Evttemp 20 6 18 22 1

It 8 17 1

Lgate 1 9 5.61e-9
 Ldrain 2 5 1e-9
 Lsource 3 7 1.98e-9

RLgate 1 9 56.1
 RLdrain 2 5 10
 RLsource 3 7 19.8

Mmed 16 6 8 8 MmedMOD
 Mstro 16 6 8 8 MstroMOD
 Mweak 16 21 8 8 MweakMOD

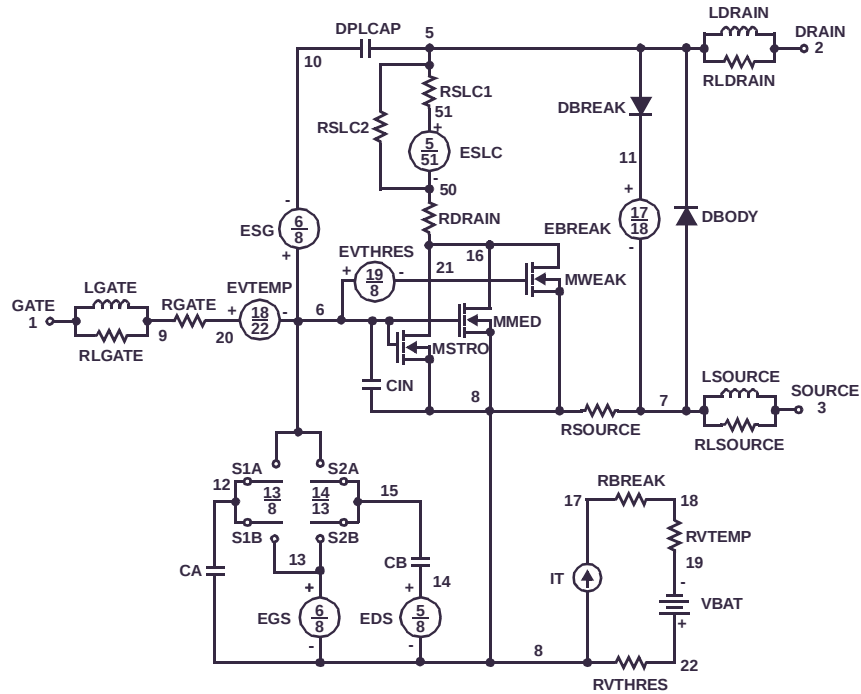
Rbreak 17 18 RbreakMOD 1
 Rdrain 50 16 RdrainMOD 25.e-3
 Rgate 9 20 3.7
 RSLC1 5 51 RSLCMOD 1e-6
 RSLC2 5 50 1e3
 Rsource 8 7 RsourceMOD 20e-3
 Rvthres 22 8 Rvthresmod 1
 Rvtemp 18 19 RvtempMOD 1
 S1a 6 12 13 8 S1AMOD
 S1b 13 12 13 8 S1BMOD
 S2a 6 15 14 13 S2AMOD
 S2b 13 15 14 13 S2BMOD

Vbat 22 19 DC 1

ESLC 51 50 VALUE={{(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*45),2.5))}}

.MODEL DbodyMOD D (IS=2.4E-12 N=1.04 RS=13e-3 TRS1=2.1e-3 TRS2=4.7e-7
 + CJO=5.5e-10 M=0.57 TT=3.25e-8 XTI=4.6)
 .MODEL DbreakMOD D (RS=1.6 TRS1=2.4e-3 TRS2=-1e-5)
 .MODEL DplcapMOD D (CJO=1.6e-10 IS=1e-30 N=10 M=0.54)
 .MODEL MmedMOD NMOS (VTO=3.8 KP=2 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=3.7)
 .MODEL MstroMOD NMOS (VTO=4.35 KP=28 IS=1e-30 N=10 TOX=1 L=1u W=1u)
 .MODEL MweakMOD NMOS (VTO=3.26 KP=0.04 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=37 RS=0.1)
 .MODEL RbreakMOD RES (TC1=1.1e-3 TC2=-1e-8)
 .MODEL RdrainMOD RES (TC1=1.15e-2 TC2=2.8e-5)
 .MODEL RSLCMOD RES (TC1=3.3e-3 TC2=1e-6)
 .MODEL RsourceMOD RES (TC1=1e-3 TC2=1e-6)
 .MODEL RvthresMOD RES (TC1=-4.8e-3 TC2=-1.1e-5)
 .MODEL RvtempMOD RES (TC1=-3e-3 TC2=1.5e-6)
 .MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-3 VOFF=-2)
 .MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-2 VOFF=-3)
 .MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-1.5 VOFF=1)
 .MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=1 VOFF=-1.5)
 .ENDS

Note: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.



SPICE Thermal Model

REV Aug 2002
 FDS3992
 Copper Area = 1.0 in²
 CTHERM1 TH 8 4e-4
 CTHERM2 8 7 5e-3
 CTHERM3 7 6 6e-2
 CTHERM4 6 5 9e-2
 CTHERM5 5 4 3e-1
 CTHERM6 4 3 4e-1
 CTHERM7 3 2 9e-1
 CTHERM8 2 TL 2

RTHERM1 TH 8 5e-1
 RTHERM2 8 7 6e-1
 RTHERM3 7 6 4
 RTHERM4 6 5 5
 RTHERM5 5 4 8
 RTHERM6 4 3 9
 RTHERM7 3 2 15
 RTHERM8 2 TL 23

SABER Thermal Model

Copper Area = 1.0 in²
 template thermal_model th tl
 thermal_c th, tl
 {
 CTHERM1 TH 8 4e-4
 CTHERM2 8 7 5e-3
 CTHERM3 7 6 6e-2
 CTHERM4 6 5 9e-2
 CTHERM5 5 4 3e-1
 CTHERM6 4 3 4e-1
 CTHERM7 3 2 9e-1
 CTHERM8 2 TL 2
 RTHERM1 TH 8 5e-1
 RTHERM2 8 7 6e-1
 RTHERM3 7 6 4
 RTHERM4 6 5 5
 RTHERM5 5 4 8
 RTHERM6 4 3 9
 RTHERM7 3 2 15
 RTHERM8 2 TL 23
 }

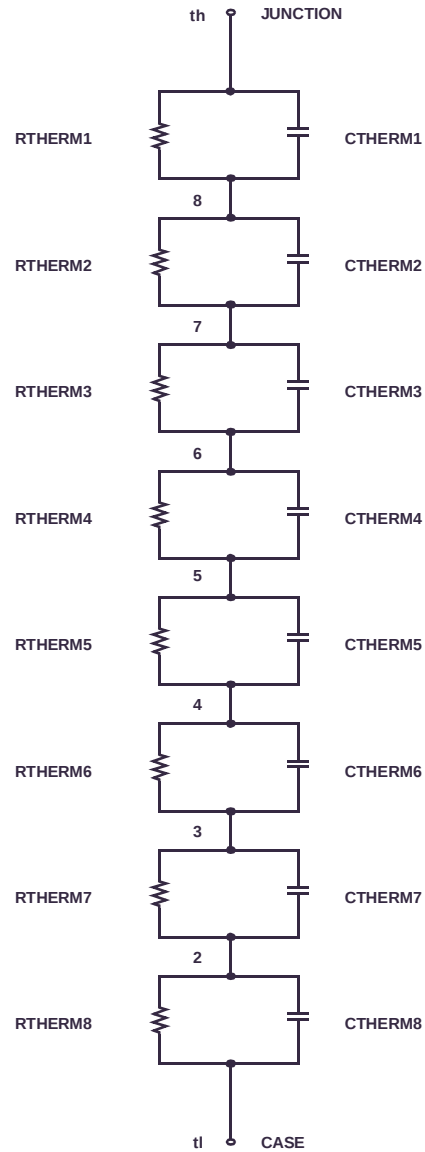


TABLE 1. THERMAL MODELS

COMPONANT	0.04 in ²	0.28 in ²	0.52 in ²	0.76 in ²	1.0 in ²
CTHERM6	3.2e-1	3.5e-1	4.0e-1	4.0e-1	4.0e-1
CTHERM7	8.5e-1	9.0e-1	9.0e-1	9.0e-1	9.0e-1
CTHERM8	0.3	1.8	2.0	2.0	2.0
RTHERM6	24	18	12	10	9
RTHERM7	36	21	18	16	15
RTHERM8	53	37	30	28	23

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Bottomless [™]	FAST [®]	LittleFET [™]	Power247 [™]	SuperSOT [™] -3
CoolFET [™]	FAST [™]	MicroFET [™]	PowerTrench [®]	SuperSOT [™] -6
CROSSVOLT [™]	FRFET [™]	MicroPak [™]	QFET [™]	SuperSOT [™] -8
DOME [™]	GlobalOptoisolator [™]	MICROWIRE [™]	QS [™]	SyncFET [™]
EcoSPARK [™]	GTO [™]	MSX [™]	QT Optoelectronics [™]	TinyLogic [™]
E ² CMOS [™]	HiSeC [™]	MSXPro [™]	Quiet Series [™]	TruTranslation [™]
EnSigna [™]	I ² C [™]	OCX [™]	RapidConfigure [™]	UHC [™]
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PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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