

Is Now Part of



ON Semiconductor®

To learn more about ON Semiconductor, please visit our website at
www.onsemi.com

Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

ON Semiconductor and the ON Semiconductor logo are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

FAIRCHILD SEMICONDUCTOR®

April 2013

FDMF6705 - Extra-Small, High-Performance, High-Frequency DrMOS Module

Benefits

- Ultra-Compact 6x6 mm PQFN, 72% Space-Saving Compared to Conventional Discrete Solutions
- Fully Optimized System Efficiency
- Clean Switching Waveforms with Minimal Ringing
- High-Current Handling

Features

- Over 93% Peak-Efficiency
- High-Current Handling of 40 A, at 12 V_{IN}
- High-Current Handling of 38 A at 19 V_{IN}
- High-Performance PQFN Copper-Clip Package
- 3-State 5 V PWM Input Driver
- Skip-Mode SMOD# (Low-Side Gate Turn Off) Input
- Thermal Warning Flag for Over-Temperature Condition
- Driver Output Disable Function (DISB# Pin)
- Internal Pull-Up and Pull-Down for SMOD# and DISB# Inputs, Respectively
- Fairchild PowerTrench® Technology MOSFETs for Clean Voltage Waveforms and Reduced Ringing
- Fairchild SyncFET™ (Integrated Schottky Diode) Technology in the Low-Side MOSFET
- Integrated Bootstrap Schottky Diode
- Adaptive Gate Drive Timing for Shoot-through Protection
- Under-Voltage Lockout (UVLO)
- Optimized for Switching Frequencies up to 1 MHz
- Low-Profile SMD Package
- Fairchild Green Packaging and RoHS Compliant
- Based on the Intel® 4.0 DrMOS Standard

Description

The XS™ DrMOS family is Fairchild's next-generation, fully optimized, ultra-compact, integrated MOSFET plus driver power stage solutions for high-current, high-frequency, synchronous buck DC-DC applications. The FDMF6705 integrates a driver IC, two power MOSFETs, and a bootstrap Schottky diode into a thermally enhanced, ultra-compact 6x6mm PQFN package.

With an integrated approach, the complete switching power stage is optimized with regards to driver and MOSFET dynamic performance, system inductance, and Power MOSFET $R_{DS(ON)}$. XS™ DrMOS uses Fairchild's high-performance PowerTrench® MOSFET technology, which dramatically reduces switch ringing, eliminating the need for a snubber circuit in most buck converter applications.

A new driver IC with reduced dead times and propagation delays further enhances the performance of this part. A thermal warning function has been included to warn of a potential over-temperature situation. The FDMF6705 also incorporates features, such as Skip Mode (SMOD), for improved light-load efficiency along with a 3-state PWM input for compatibility with a wide range of PWM controllers.

Applications

- High-Performance Gaming Motherboards
- Notebook Computer V-Core and Non-V-Core
- Compact Blade Server, V-Core and Non-V-Core DC-DC Converters
- Desktop Computer, V-Core and Non-V-Core DC-DC Converters
- Workstations
- High-Current DC-DC Point-of-Load (POL) Converters
- Small Form-Factor Voltage Regulator Modules

Ordering Information

Part Number	Current Rating	Package	Top Mark
FDMF6705	40 A	40-Lead, Clipbond PQFN DrMOS, 6.0x6.0 mm Package	FDMF6705

© 2011 Fairchild Semiconductor Corporation

Typical Application Circuit

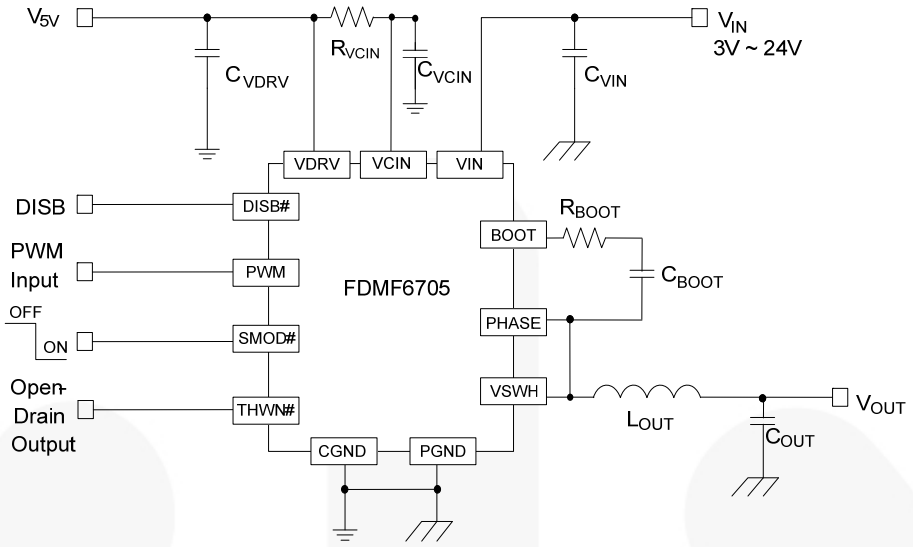


Figure 1. Typical Application Circuit

DrMOS Block Diagram

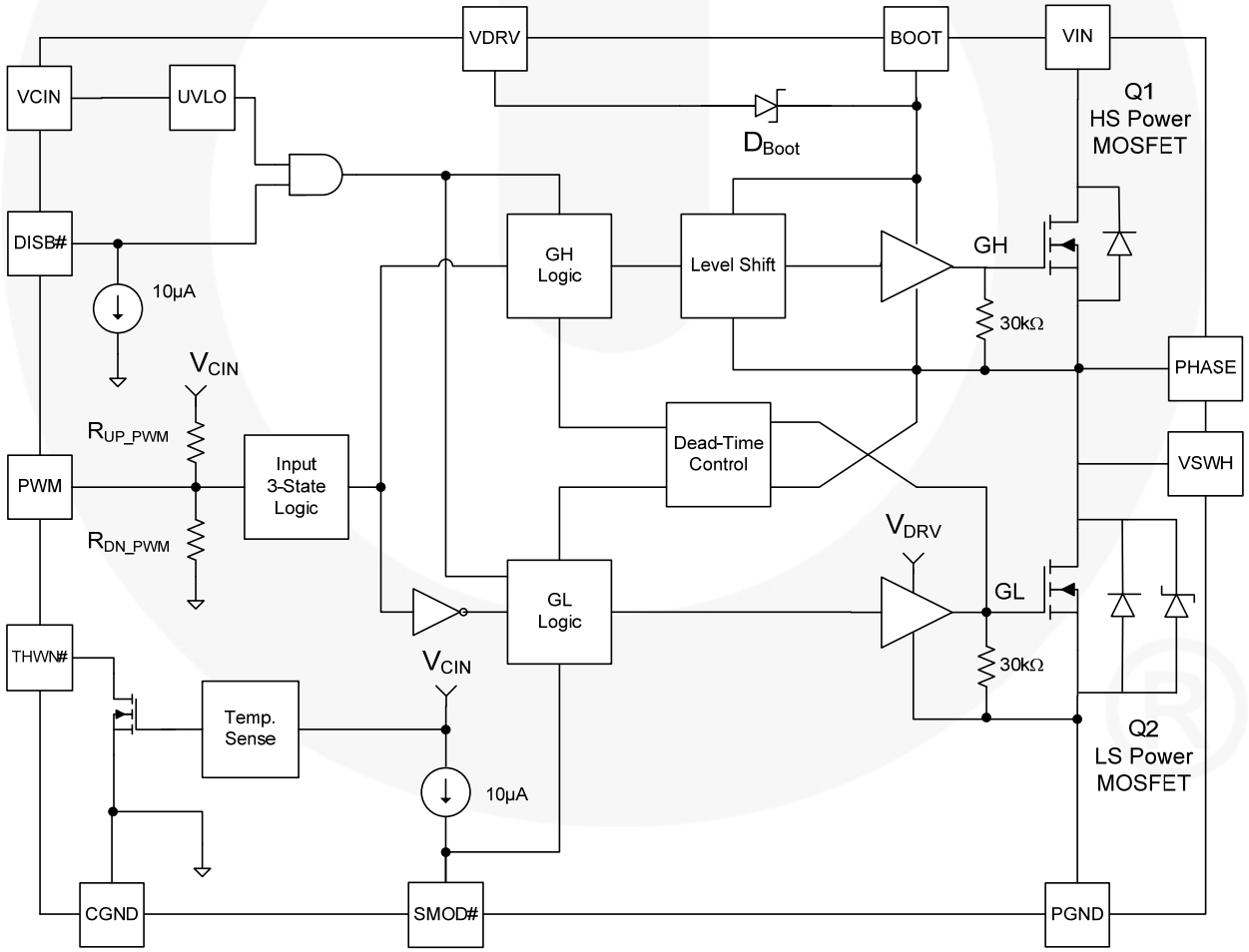
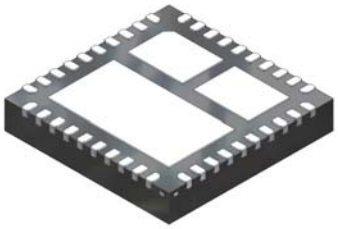


Figure 2. DrMOS Block Diagram

Pin Configuration



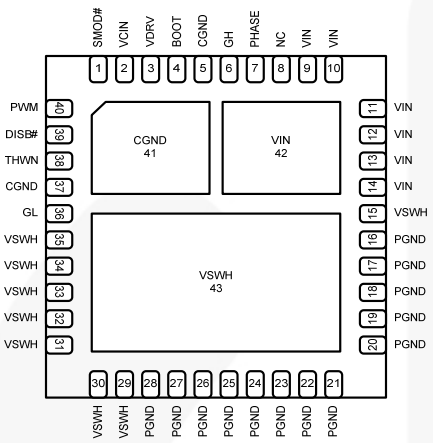
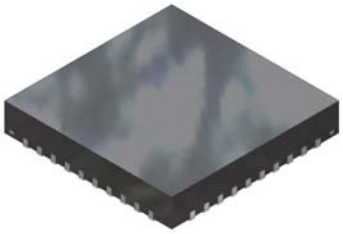


Figure 3. Bottom View



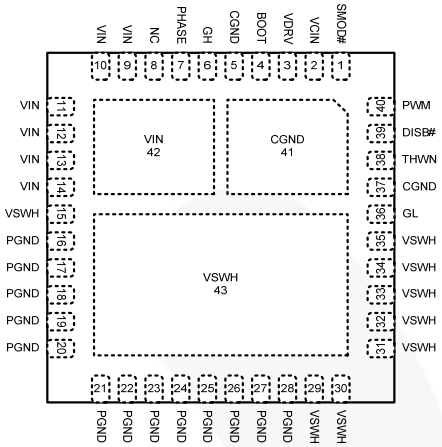


Figure 4. Top View

Pin Definitions

Pin #	Name	Description
1	SMOD#	When SMOD#=HIGH, the low-side driver is the inverse of PWM input. When SMOD#=LOW, the low-side driver is disabled. This pin has a 10 µA internal pull-up current source. Do not add a noise filter capacitor.
2	VCIN	IC bias supply. Minimum 1 µF ceramic capacitor is recommended from this pin to CGND.
3	VDRV	Power for gate driver. Minimum 1 µF ceramic capacitor is recommended to be connected as close as possible from this pin to CGND.
4	BOOT	Bootstrap supply input. Provides voltage supply to high-side MOSFET driver. Connect bootstrap capacitor from this pin to PHASE.
5, 37, 41	CGND	IC ground. Ground return for driver IC.
6	GH	For manufacturing test only. This pin must float. Must not be connected to any pin.
7	PHASE	Switch node pin for bootstrap capacitor routing. Electrically shorted to VSWH pin.
8	NC	No connect. The pin is not electrically connected internally, but can be connected to VIN for convenience.
9 - 14, 42	VIN	Power input. Output stage supply voltage.
15, 29 - 35, 43	VSWH	Switch node input. Provides return for high-side bootstrapped driver and acts as a sense point for the adaptive shoot-through protection.
16 – 28	PGND	Power ground. Output stage ground. Source pin of low-side MOSFET.
36	GL	For manufacturing test only. This pin must float. Must not be connected to any pin.
38	THWN#	Thermal warning flag, open collector output. When temperature exceeds the trip limit, the output is pulled LOW. THWN# does not disable the module.
39	DISB#	Output disable. When LOW, this pin disables Power MOSFET switching (GH and GL are held LOW). This pin has a 10 µA internal pull-down current source. Do not add a noise filter capacitor.
40	PWM	PWM signal input. This pin accepts a 3-state logic-level PWM signal from the controller.

© 2011 Fairchild Semiconductor Corporation

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
	VCIN, VDRV, DISB#, PWM, SMOD#, GL, THWN# to CGND Pins		-0.3	6.0	V
	VIN to PGND, CGND Pins		-0.3	30.0	
	BOOT, GH to VSWH, PHASE Pins		-0.3	6.0	
	BOOT, PHASE, GH to CGND Pins		-0.3	30.0	
	VSWH to CGND/PGND (DC Only)		-0.3	30.0	
	VSWH to PGND (<20 ns)		-8.0	33.0	
	BOOT to VDRV			22.0	
	BOOT to VDRV (<20 ns)			25.0	
$I_{THWN\#}$	THWN# Sink Current		-0.1	7.0	mA
$I_{O(AV)}$ [1]	V_{IN}=19 V, V_O=1.0 V	f_{SW}=300 kHz		38	A
		f_{SW}=1 MHz		35	
θ_{JPCB}	Junction-to-PCB Thermal Resistance			3.5	°C/W
T_A	Ambient Temperature Range		-40	+125	°C
T_J	Maximum Junction Temperature			+150	°C
T_{STG}	Storage Temperature Range		-55	+150	°C
ESD	Electrostatic Discharge Protection	Human Body Model, JESD22-A114	2000		V
		Charged Device Model, JESD22-C101	1000		

Note:

1. $I_{O(AV)}$ is rated using Fairchild's DrMOS evaluation board, T_A = 25°C, natural convection cooling. This rating is limited by the peak DrMOS temperature, T_J = 150°C, and varies depending on operating conditions and PCB layout. This rating can be changed with different application settings.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CIN}	Control Circuit Supply Voltage	4.5	5.0	5.5	V
V_{DRV}	Gate Drive Circuit Supply Voltage	4.5	5.0	5.5	V
V_{IN}	Output Stage Supply Voltage	3.0	12.0	24.0 [2]	V

Note:

2. Operating at high V_{IN} can create excessive AC overshoots on the VSWH-to-GND and BOOT-to-GND nodes during MOSFET switching transients. For reliable DrMOS operation, VSWH-to-GND and BOOT-to-GND must remain at or below the Absolute Maximum Ratings shown in the table above. *Refer to the "Application Information" and "PCB Layout Guidelines" sections of this datasheet for additional information.*

© 2011 Fairchild Semiconductor Corporation

Electrical Characteristics

Typical values are V_{IN} = 12 V, V_{CIN} = 5 V, V_{DRV} = 5 V, and T_A = +25°C unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Basic Operation						
I_Q	Quiescent Current	$I_Q=I_{VCIN}+I_{VDRV}$, PWM=LOW or HIGH or Float			2	mA
UVLO	UVLO Threshold	V_{CIN} Rising	2.9	3.1	3.3	V
$UVLO_{_Hyst}$	UVLO Hysteresis			0.4		V
PWM Input (V_{CIN} = V_{DRV} = 5 V ±10%)						
R_{UP_PWM}	Pull-Up Impedance			10		kΩ
R_{DN_PWM}	Pull-Down Impedance			10		kΩ
V_{IH_PWM}	PWM High Level Voltage		3.04	3.55	4.05	V
V_{TRI_HI}	3-State Upper Threshold		2.95	3.45	3.94	V
V_{TRI_LO}	3-State Lower Threshold		0.98	1.25	1.52	V
V_{IL_PWM}	PWM Low Level Voltage		0.84	1.15	1.42	V
$t_{D_HOLD-OFF}$	3-State Shutoff Time			160	200	ns
V_{HiZ_PWM}	3-State Open Voltage		2.2	2.5	2.8	V
PWM Input (V_{CIN} = V_{DRV} = 5 V ±5%)						
R_{UP_PWM}	Pull-Up Impedance			10		kΩ
R_{DN_PWM}	Pull-Down Impedance			10		kΩ
V_{IH_PWM}	PWM High Level Voltage		3.22	3.55	3.87	V
V_{TRI_HI}	3-State Upper Threshold		3.13	3.45	3.77	V
V_{TRI_LO}	3-State Lower Threshold		1.04	1.25	1.46	V
V_{IL_PWM}	PWM Low Level Voltage		0.90	1.15	1.36	V
$t_{D_HOLD-OFF}$	3-State Shutoff Time			160	200	ns
V_{HiZ_PWM}	3-State Open Voltage		2.3	2.5	2.7	V
DISB# Input						
V_{IH_DISB}	High-Level Input Voltage		2			V
V_{IL_DISB}	Low-Level Input Voltage				0.8	V
I_{PLD}	Pull-Down Current			10		µA
t_{PD_DISBL}	Propagation Delay	PWM=GND, Delay Between DISB# from HIGH to LOW to GL from HIGH to LOW		25		ns
t_{PD_DISBH}	Propagation Delay	PWM=GND, Delay Between DISB# from LOW to HIGH to GL from LOW to HIGH		25		ns
SMOD# Input						
V_{IH_SMOD}	High-Level Input Voltage		2			V
V_{IL_SMOD}	Low-Level Input Voltage				0.8	V
I_{PLU}	Pull-Up Current			10		µA
t_{PD_SLGLL}	Propagation Delay	PWM=GND, Delay Between SMOD# from HIGH to LOW to GL from HIGH to LOW		10		ns
t_{PD_SHGLH}	Propagation Delay	PWM=GND, Delay Between SMOD# from LOW to HIGH to GL from LOW to HIGH		10		ns

Continued on the following page…

© 2011 Fairchild Semiconductor Corporation

Electrical Characteristics

Typical values are V_{IN} = 12 V, V_{CIN} = 5 V, V_{DRV} = 5 V, and T_A = +25°C unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Thermal Warning Flag						
T_{ACT}	Activation Temperature			150		°C
T_{RST}	Reset Temperature			135		°C
R_{THWN}	Pull-Down Resistance	I_{PLD}=5 mA		30		Ω
250 ns Timeout Circuit						
$t_{D_TIMEOUT}$	Timeout Delay	SW=0 V, Delay Between GH from HIGH to LOW and GL from LOW to HIGH		250		ns
High-Side Driver						
R_{SOURCE_GH}	Output Impedance, Sourcing	Source Current=100 mA		1		Ω
R_{SINK_GH}	Output Impedance, Sinking	Sink Current=100 mA		0.8		Ω
t_{R_GH}	Rise Time	GH=10% to 90%, C_{LOAD}=1.1 nF		6		ns
t_{F_GH}	Fall Time	GH=90% to 10%, C_{LOAD}=1.1 nF		5		ns
t_{D_DEADON}	LS to HS Deadband Time	GL going LOW to GH going HIGH, 1 V GL to 10% GH		10		ns
t_{PD_PLGHL}	PWM LOW Propagation Delay	PWM going LOW to GH going LOW, V_{IL_PWM} to 90% GH		16	30	ns
t_{PD_PHGHH}	PWM HIGH Propagation Delay (SMOD Held LOW)	PWM going HIGH to GH going HIGH, V_{IH_PWM} to 10% GH (SMOD=LOW)		30		ns
t_{PD_TSGHH}	Exiting 3-State Propagation Delay	PWM (from 3-State) going HIGH to GH going HIGH, V_{IH_PWM} to 10% GH		30		ns
Low-Side Driver						
R_{SOURCE_GL}	Output Impedance, Sourcing	Source Current=100 mA		1		Ω
R_{SINK_GL}	Output Impedance, Sinking	Sink Current=100 mA		0.5		Ω
t_{R_GL}	Rise Time	GL=10% to 90%, C_{LOAD}=2.7 nF		10		ns
t_{F_GL}	Fall Time	GL=90% to 10%, C_{LOAD}=2.7 nF		8		ns
$t_{D_DEADOFF}$	HS to LS Deadband Time	SW going LOW to GL going HIGH, 2.2 V SW to 10% GL		12		ns
t_{PD_PHGLL}	PWM-HIGH Propagation Delay	PWM going HIGH to GL going LOW, V_{IH_PWM} to 90% GL		9	25	ns
t_{PD_TSGLH}	Exiting 3-State Propagation Delay	PWM (from 3-State) going LOW to GL going HIGH, V_{IL_PWM} to 10% GL		20		ns
Boot Diode						
V_F	Forward-Voltage Drop	I_F=10 mA		0.35		V
V_R	Breakdown Voltage	I_R=1 mA	22			V

© 2011 Fairchild Semiconductor Corporation

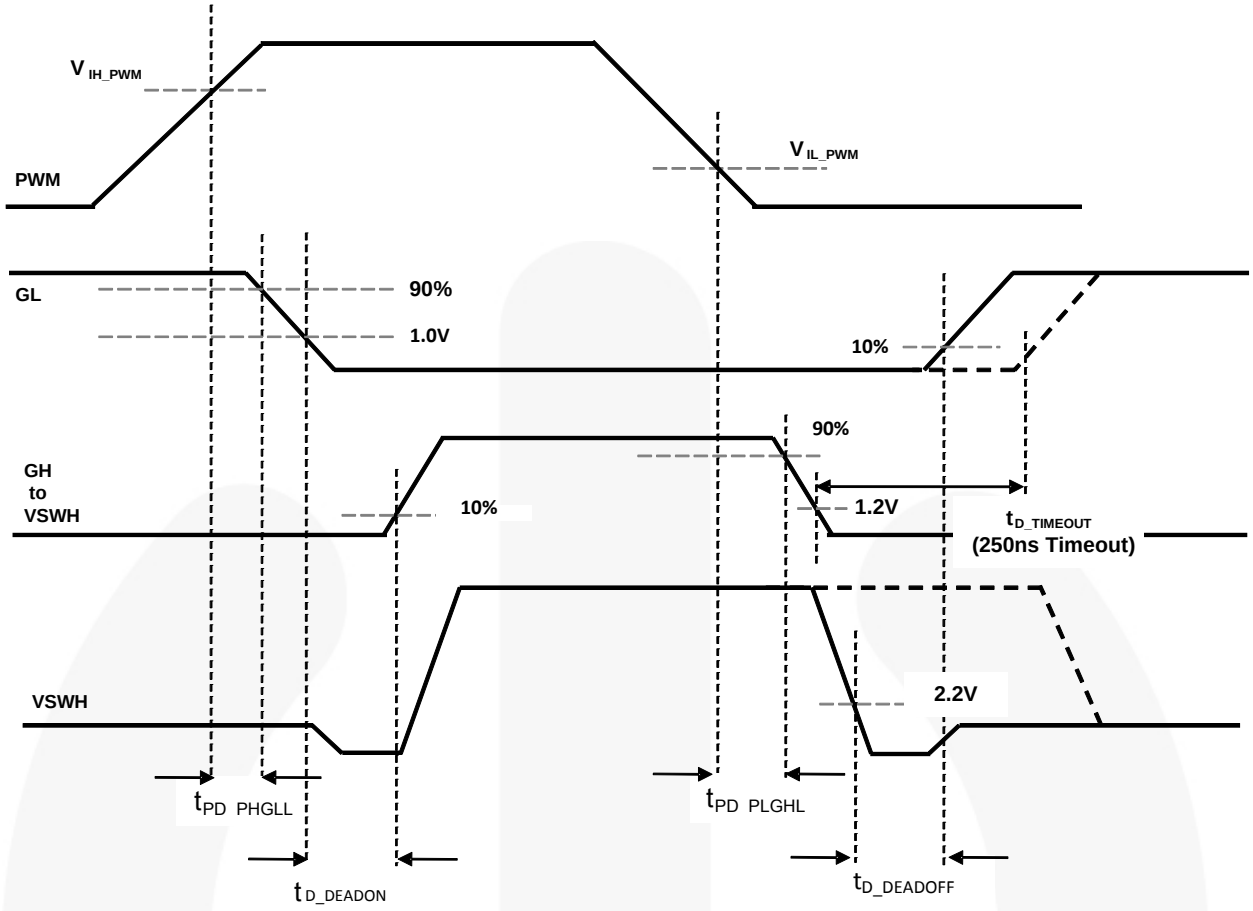


Figure 5. PWM Timing Diagram

Typical Performance Characteristics

Test Conditions: V_{IN}=12 V, V_{OUT}=1.0 V, V_{CIN}=5 V, V_{DRV}=5 V, L_{OUT}=320 nH, T_A=25°C, and natural convection cooling, unless otherwise specified.

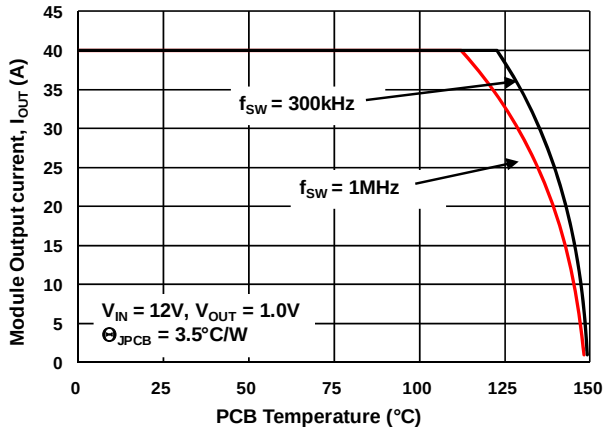


Figure 6. Safe Operating Area

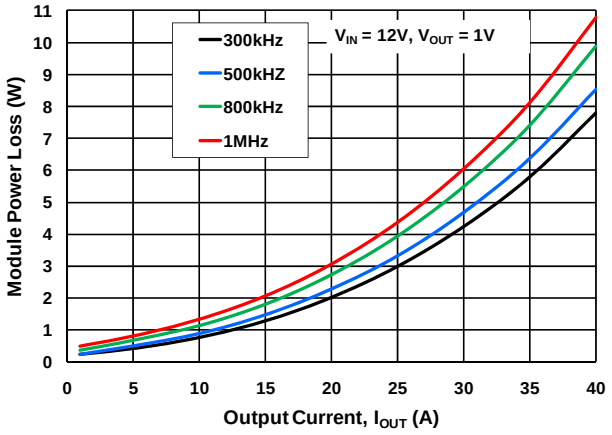


Figure 7. Module Power Loss vs. Output Current

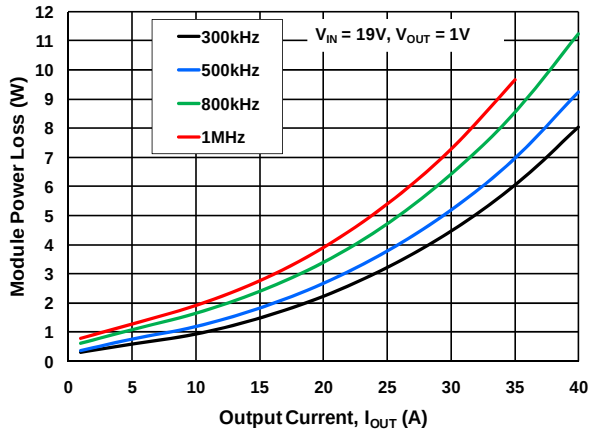


Figure 8. Module Power Loss vs. Output Current

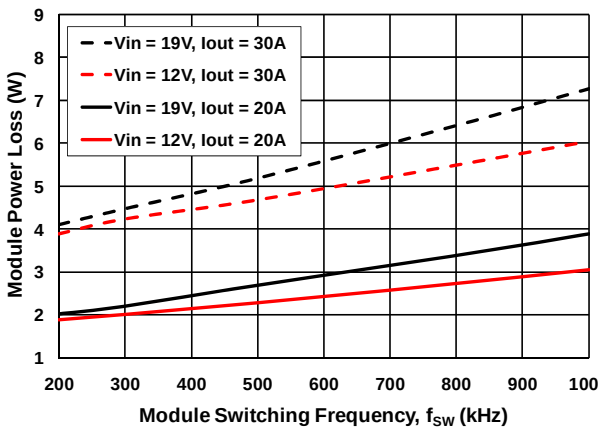


Figure 9. Module Power Loss vs. Switching Frequency

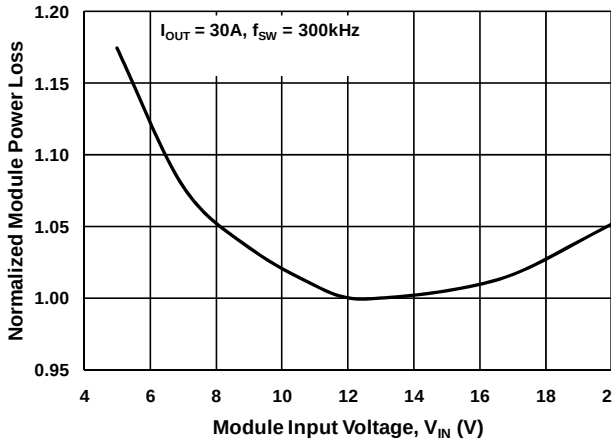


Figure 10. Normalized Power Loss vs. Input Voltage

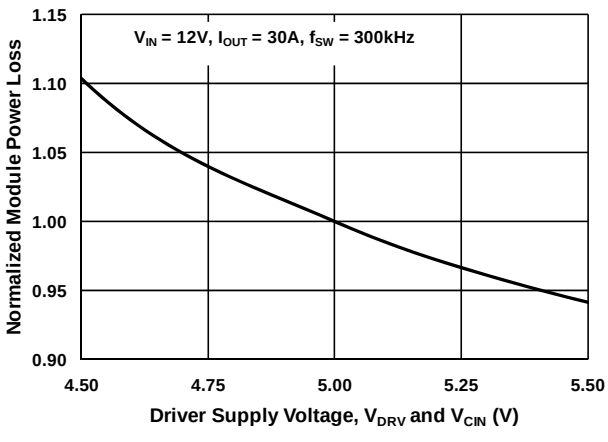


Figure 11. Normalized Power Loss vs. Driver Supply Voltage

© 2011 Fairchild Semiconductor Corporation

Typical Performance Characteristics (Continued)

Test Conditions: V_{IN}=12 V, V_{OUT}=1.0 V, V_{CIN}=5 V, V_{DRV}=5 V, L_{OUT}=320 nH, T_A=25°C, and natural convection cooling, unless otherwise specified.

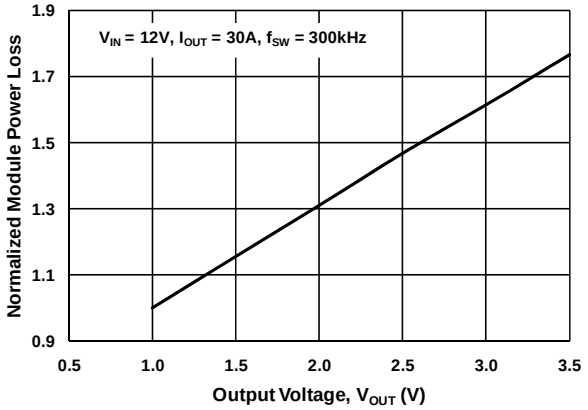


Figure 12. Normalized Power Loss vs. Output Voltage

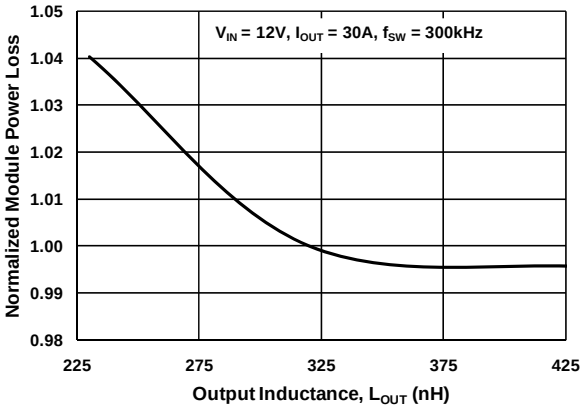


Figure 13. Module Power Loss vs. Output Inductance

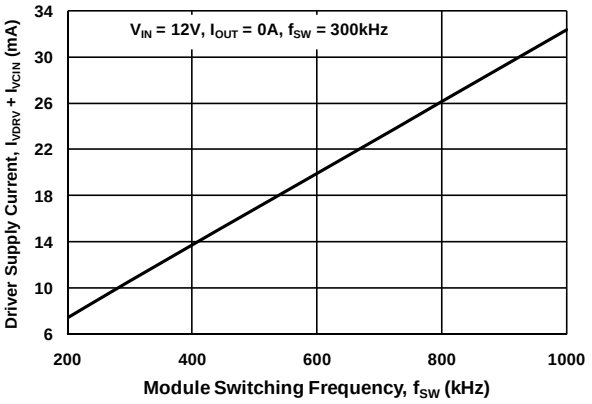


Figure 14. Driver Supply Current vs. Frequency

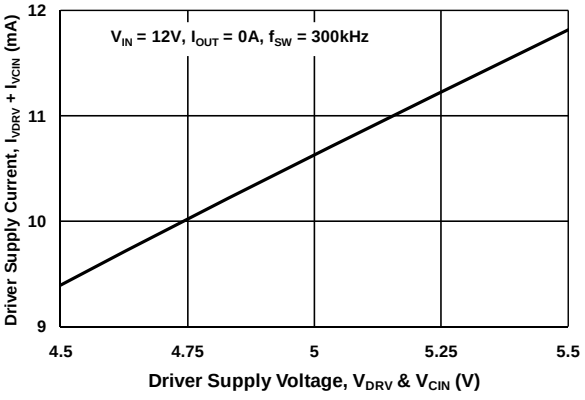


Figure 15. Driver Supply Current vs. Driver Supply Voltage

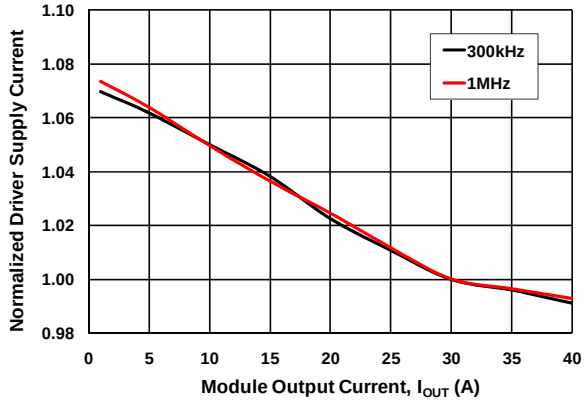


Figure 16. Normalized Driver Supply Current vs. Output Current

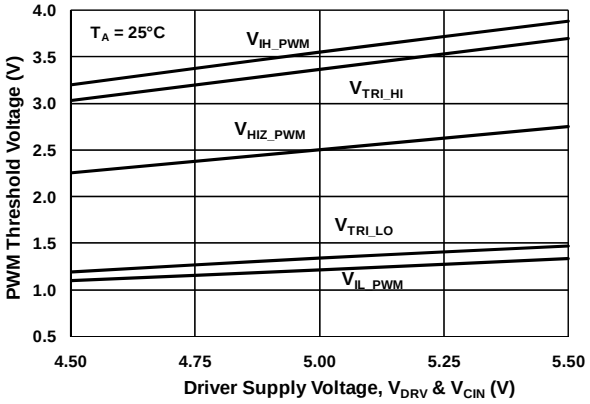


Figure 17. PWM Thresholds vs. Driver Supply Voltage

© 2011 Fairchild Semiconductor Corporation

Typical Performance Characteristics (Continued)

Test Conditions: V_{IN}=12 V, V_{OUT}=1.0 V, V_{CIN}=5 V, V_{DRV}=5 V, L_{OUT}=320 nH, T_A=25°C, and natural convection cooling, unless otherwise specified.

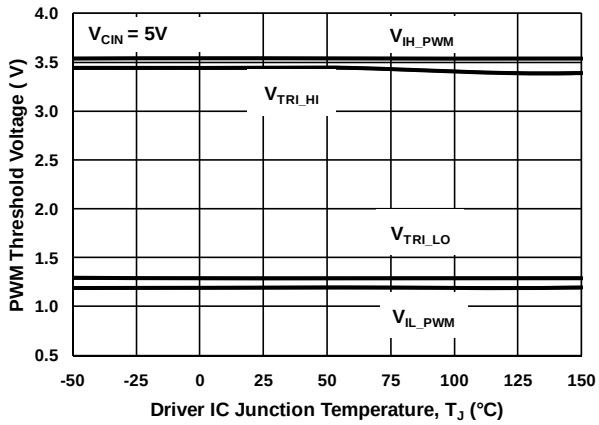


Figure 18. PWM Thresholds vs. Temperature

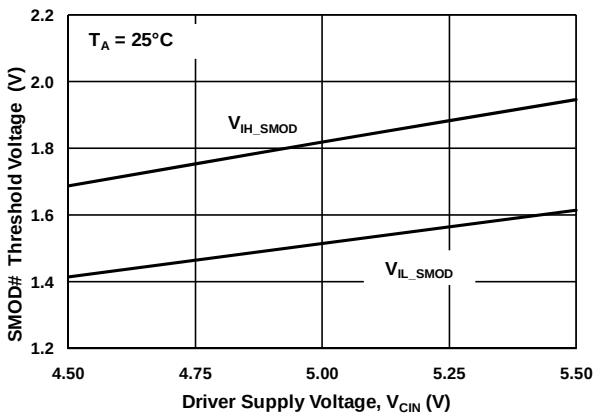


Figure 19. SMOD# Thresholds vs. Driver Supply Voltage

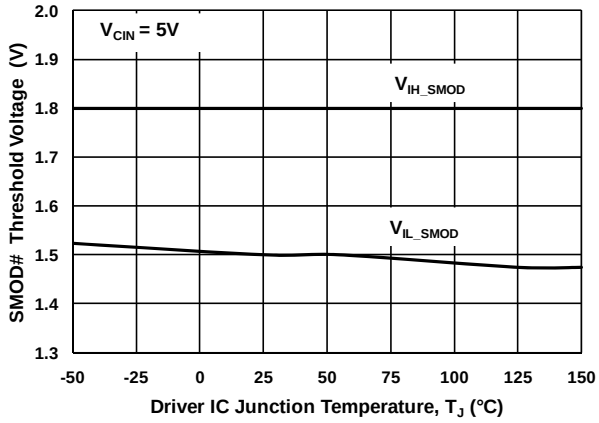


Figure 20. SMOD# Thresholds vs. Temperature

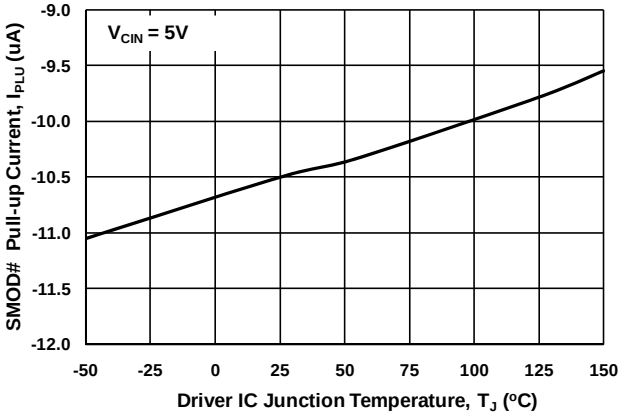


Figure 21. SMOD# Pull-Up Current vs. Temperature

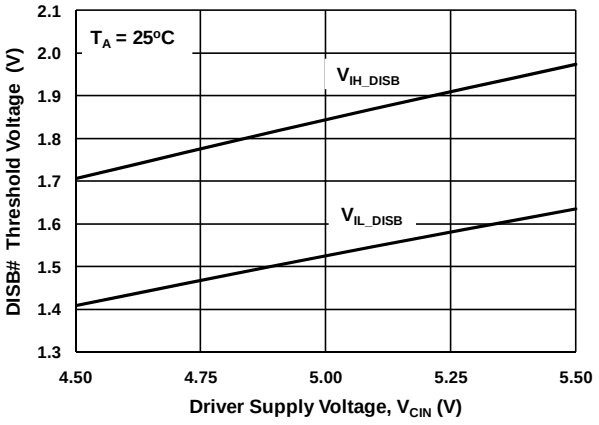


Figure 22. DISB# Thresholds vs. Driver Supply Voltage

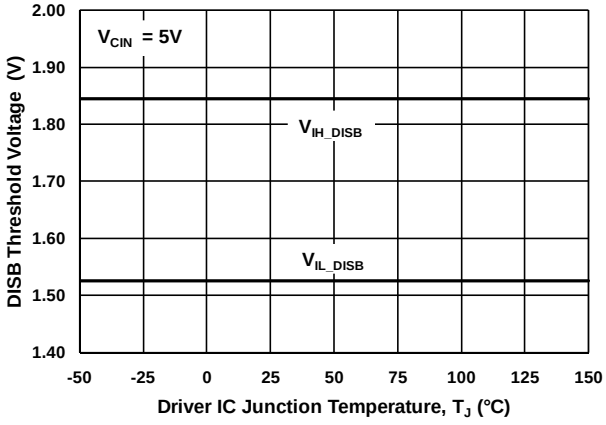


Figure 23. DISB# Thresholds vs. Temperature

© 2011 Fairchild Semiconductor Corporation

Typical Performance Characteristics (Continued)

Test Conditions: V_{IN}=12 V, V_{OUT}=1.0 V, V_{CIN}=5 V, V_{DRV}=5 V, L_{OUT}=320 nH, T_A=25°C, and natural convection cooling, unless otherwise specified.

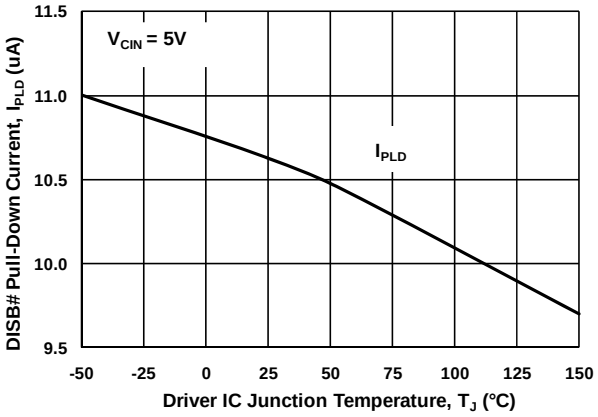


Figure 24. DISB# Pull-Down Current vs. Temperature

Functional Description

The FDMF6705 is a driver-plus-FET module optimized for the synchronous buck converter topology. A single PWM input signal is all that is required to properly drive the high-side and the low-side MOSFETs. Each part is capable of driving speeds up to 1 MHz.

VCIN and Disable

The VCIN pin is monitored by an under-voltage lockout (UVLO) circuit. When V_{CIN} rises above ~3.1 V, the driver is enabled for operation. When V_{CIN} falls below ~2.7 V, the driver is disabled (GH, GL=0). The driver can also be disabled by pulling the DISB# pin LOW (DISB# < V_{IL_DISB}), which holds both GL and GH LOW regardless of the PWM input state. The driver can be enabled by raising the DISB# pin voltage HIGH (DISB# > V_{IH_DISB}).

Table 1. UVLO and Disable Logic

UVLO	DISB#	Driver State
0	X	Disabled (GH, GL=0)
1	0	Disabled (GH, GL=0)
1	1	Enabled (*See Table 2*)
1	Open	Disabled (GH, GL=0)

Note:

3. DISB# has an internal pull-down current source of 10 µA.

Thermal Warning Flag

The FDMF6705 provides a thermal warning flag (THWN) to warn of over-temperature conditions. The thermal warning flag uses an open-drain output that pulls to CGND when the activation temperature (150°C) is reached. The THWN output returns to a high-impedance state once the temperature falls to the reset temperature (135°C). For use, the THWN output requires a pull-up resistor, which can be connected to VCIN. THWN does NOT disable the DrMOS module.

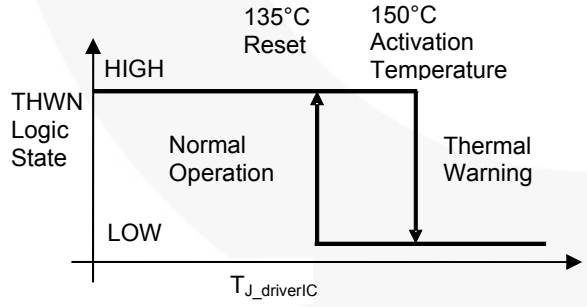


Figure 25. THWN Operation

3-State PWM Input

The FDMF6705 incorporates a 3-state PWM input gate drive design. The 3-state gate drive has both logic HIGH level and LOW level, along with a 3-state shutdown window. When the PWM input signal enters and remains within the 3-state window for a defined hold-off time ($t_{D_HOLD-OFF}$), both GL and GH are pulled LOW. This feature enables the gate drive to shut down both high- and low-side MOSFETs to support features such as phase shedding, which is a common feature on multiphase voltage regulators.

Operation when Exiting 3-State Condition

When exiting a valid 3-state condition, the FDMF6705 design follows the PWM input command. If the PWM input goes from 3-state to LOW, the low side MOSFET is turned on. If the PWM input goes from 3-state to HIGH, the high-side MOSFET is turned on. This is illustrated in Figure 26. The FDMF6705 design allows for short propagation delays when exiting the 3-state window (*see Electrical Characteristics*).

Low-Side Driver

The low-side driver (GL) is designed to drive a ground-referenced low $R_{DS(ON)}$ N-channel MOSFET. The bias for GL is internally connected between VDRV and CGND. When the driver is enabled, the driver's output is 180° out of phase with the PWM input. When the driver is disabled (DISB#=0 V), GL is held LOW.

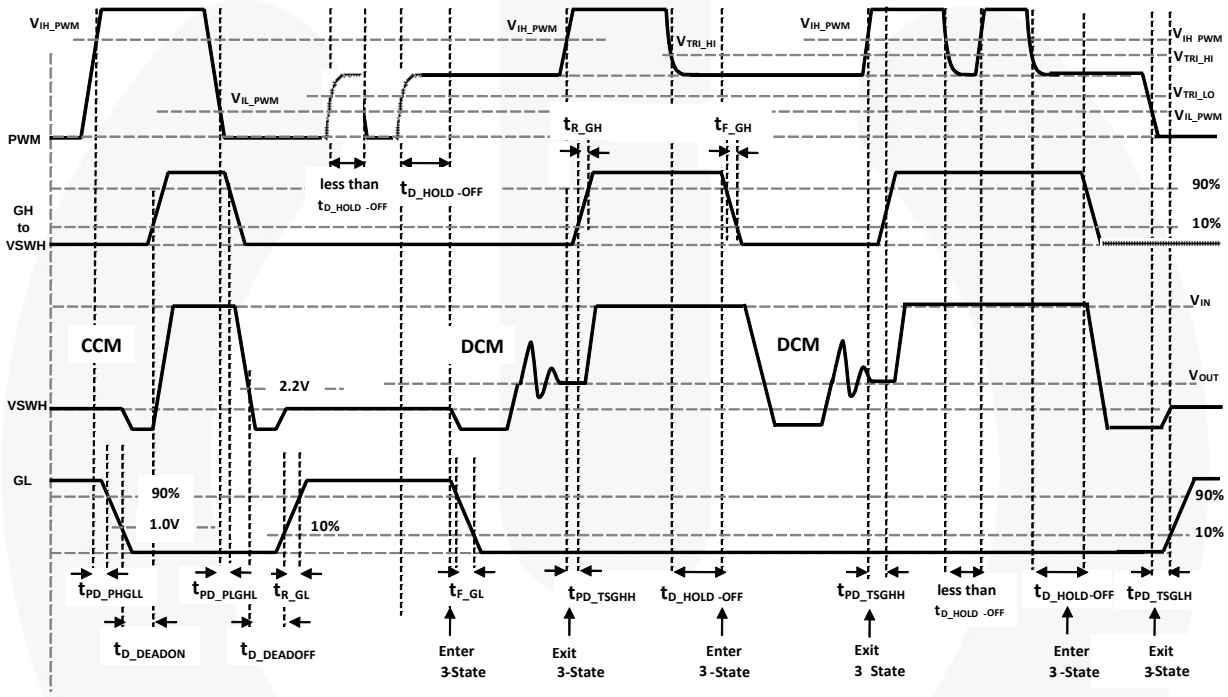
High-Side Driver

The high-side driver is designed to drive a floating N-channel MOSFET. The bias voltage for the high-side driver is developed by a bootstrap supply circuit, consisting of the internal Schottky diode and external bootstrap capacitor (C_{BOOT}). During startup, VSWH is held at PGND, allowing C_{BOOT} to charge to VDRV through the internal diode. When the PWM input goes HIGH, GH begins to charge the gate of the high-side MOSFET (Q1). During this transition, the charge is removed from C_{BOOT} and delivered to the gate of Q1. As Q1 turns on, V_{SWH} rises to V_{IN}, forcing the BOOT pin to V_{IN} + V_{BOOT}, which provides sufficient V_{GS} enhancement for Q1. To complete the switching cycle, Q1 is turned off by pulling GH to VSWH. C_{BOOT} is then recharged to VDRV when VSWH falls to PGND. GH output is in-phase with the PWM input. The high-side gate is held LOW when the driver is disabled or the PWM signal is held within the 3-state window for longer than the 3-state hold-off time, $t_{D_HOLD-OFF}$.

© 2011 Fairchild Semiconductor Corporation

Adaptive Gate Drive Circuit

The driver IC advanced design ensures minimum MOSFET dead-time while eliminating potential shoot through (cross-conduction) currents. It senses the state of the MOSFETs and adjusts the gate drive adaptively to ensure they do not conduct simultaneously. Figure 26 provides the relevant timing waveforms. To prevent overlap during the LOW-to-HIGH switching transition (Q2 off to Q1 on), the adaptive circuitry monitors the voltage at the GL pin. When the PWM signal goes HIGH, Q2 begins to turn off after some propagation delay (t_{PD_PHGLL}). Once the GL pin is discharged below ~1 V, Q1 begins to turn on after adaptive delay t_{D_DEADON}. To preclude overlap during the HIGH-to-LOW transition (Q1 off to Q2 on), the adaptive circuitry monitors the voltage at the VSWH pin. When the PWM signal goes LOW, Q1 begins to turn off after some propagation delay (t_{PD_PLGHL}). Once the VSWH pin falls below ~2.2 V, Q2 begins to turn on after adaptive delay $t_{D_DEADOFF}$. Additionally, $V_{GS(Q1)}$ is monitored. When $V_{GS(Q1)}$ is discharged below ~1.2 V, a secondary adaptive delay is initiated, which results in Q2 being driven on after $t_{D_TIMEOUT}$, regardless of SW state. This function is implemented to ensure C_{BOOT} is recharged each switching cycle in the event that the SW voltage does not fall below the 2.2 V adaptive threshold. Secondary delay $t_{D_TIMEOUT}$ is longer than $t_{D_DEADOFF}$.



Notes:

t_{PD_xxx} = propagation delay from external signal (PWM, SMOD#, etc.) to IC generated signal. Example (t_{PD_PHGLL} – PWM going HIGH to LS V_{GS} (GL) going LOW)

t_{D_xxx} = delay from IC generated signal to IC generated signal. Example (t_{D_DEADON} – LS V_{GS} (GL) LOW to HS V_{GS} (GH) HIGH)

PWM

t_{PD_PHGLL} = PWM rise to LS V_{GS} fall, V_{IH_PWM} to 90% LS V_{GS}

t_{PD_PLGHL} = PWM fall to HS V_{GS} fall, V_{IL_PWM} to 90% HS V_{GS}

t_{PD_PHGHH} = PWM rise to HS V_{GS} rise, V_{IH_PWM} to 10% HS V_{GS} (SMOD# held LOW)

SMOD#

t_{PD_SLGLL} = SMOD# fall to LS V_{GS} fall, V_{IL_SMOD} to 90% LS V_{GS}

t_{PD_SHGLH} = SMOD# rise to LS V_{GS} rise, V_{IH_SMOD} to 10% LS V_{GS}

Exiting 3-state

t_{PD_TSGHH} = PWM 3-state to HIGH to HS V_{GS} rise, V_{IH_PWM} to 10% HS V_{GS}

t_{PD_TSGLH} = PWM 3-state to LOW to LS V_{GS} rise, V_{IL_PWM} to 10% LS V_{GS}

Dead Times

t_{D_DEADON} = LS V_{GS} fall to HS V_{GS} rise, LS-comp trip value (~1.0V GL) to 10% HS V_{GS}

$t_{D_DEADOFF}$ = VSWH fall to LS V_{GS} rise, SW-comp trip value (~2.2V VSWH) to 10% LS V_{GS}

Figure 26. PWM and 3-StateTiming Diagram

Skip Mode (SMOD)

The SMOD function allows for higher converter efficiency under light-load conditions. During SMOD, the low-side FET gate signal is disabled (held LOW), preventing discharging of the output capacitors as the filter inductor current attempts reverse current flow – also known as “Diode Emulation” Mode. When the SMOD pin is pulled HIGH, the synchronous buck converter works in Synchronous Mode, gating on the low-side FET. When the SMOD pin is pulled LOW, the low-side FET is gated off. The SMOD pin is connected to the PWM controller, which enables or disables the SMOD automatically when the controller detects light-load condition from output current sensing. Normally this pin is active LOW. *See Figure 27 for timing delays*.

Table 2. SMOD Logic

DISB#	PWM	SMOD#	GH	GL
0	X	X	0	0
1	3-State	X	0	0
1	0	0	0	0
1	1	0	1	0
1	0	1	0	1
1	1	1	1	0

Note:

4. The SMOD feature is intended to have low propagation delay between the SMOD signal and the low-side FET V_{GS} response time to control diode emulation on a cycle-by-cycle basis.

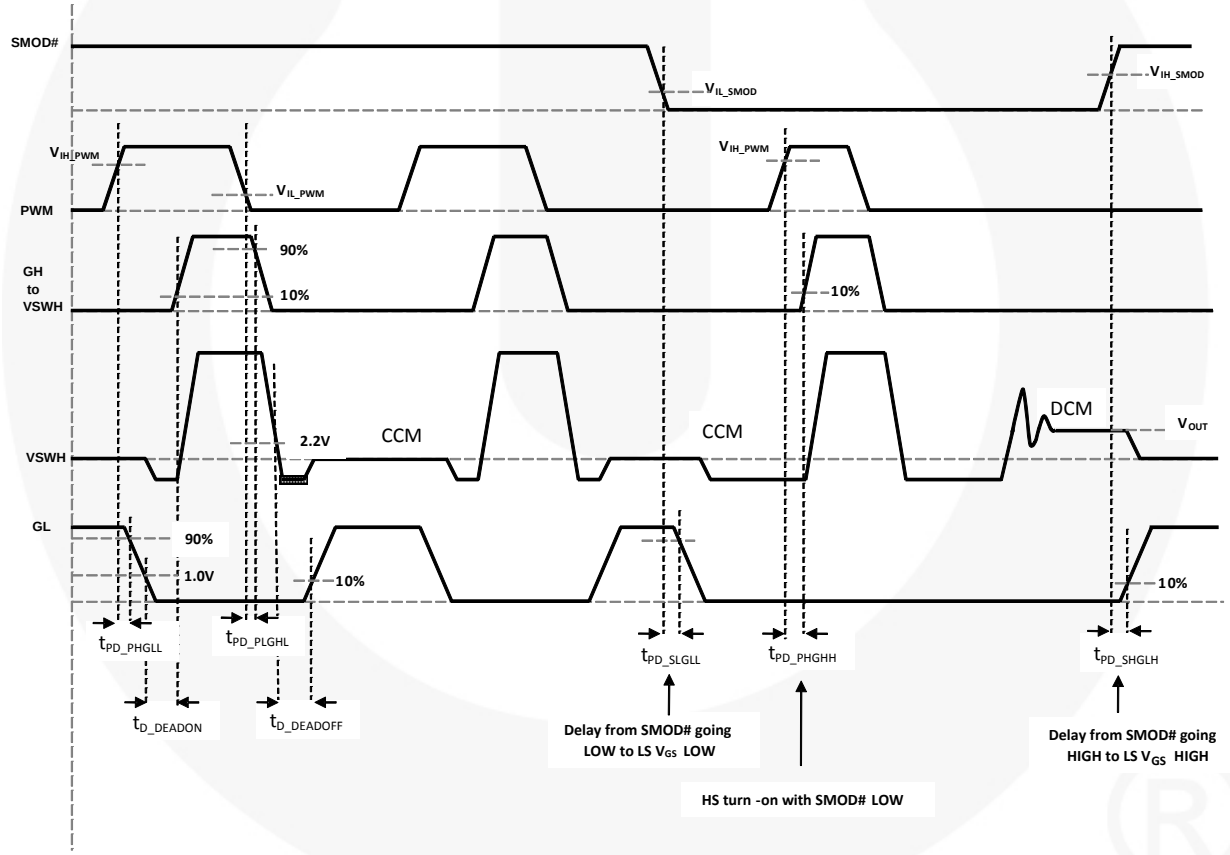


Figure 27. SMOD Timing Diagram

Application Information

Supply Capacitor Selection

For the supply inputs (VDRV & VCIN), a local ceramic bypass capacitor is required to reduce noise and to supply peak transient currents during gate drive switching action. It is recommended to use a minimum capacitor value of 1 µF X7R or X5R. Keep this capacitor close to the VCIN and VDRV pins and connect it to the GND plane with vias.

Bootstrap Circuit

The bootstrap circuit uses a charge storage capacitor (C_{BOOT}), as shown in Figure 28. A bootstrap capacitance of 100 nF X7R or X5R capacitor is typically adequate. A series bootstrap resistor would be needed for specific applications to improve switching noise immunity. The boot resistor (R_{BOOT}) may be required when operating near the maximum rated V_{IN} and is effective at controlling the high-side MOSFET turn-on slew rate and V_{SHW} overshoot. Typical R_{BOOT} values from 0.5 Ω to 3.0 Ω are effective in reducing V_{SWH} overshoot for the FDMF6705.

VCIN Filter

The VDRV pin provides power to the gate drive of the high-side and low-side power MOSFETs. In most cases, VDRV can be connected directly to VCIN, which supplies power to the logic circuitry of the gate driver. For additional noise immunity, an RC filter can be inserted between VDRV and VCIN. Recommended values of 10 Ω (R_{VCIN}) placed between VDRV and VCIN and 1 µF (C_{VCIN}) from VCIN to CGND *(see Figure 29)*.

Power Loss and Efficiency

Measurement and Calculation

Refer to Figure 28 for power loss testing method.

Power loss calculations are:

$$P_{IN}=(V_{IN} \times I_{IN}) + (V_{5V} \times I_{5V}) \text{ (W)} \quad (1)$$

$$P_{SW}=V_{SW} \times I_{OUT} \text{ (W)} \quad (2)$$

$$P_{OUT}=V_{OUT} \times I_{OUT} \text{ (W)} \quad (3)$$

$$P_{LOSS_MODULE}=P_{IN} - P_{SW} \text{ (W)} \quad (4)$$

$$P_{LOSS_BOARD}=P_{IN} - P_{OUT} \text{ (W)} \quad (5)$$

$$EFF_{MODULE}=100 \times P_{SW}/P_{IN} \text{ (\%)} \quad (6)$$

$$EFF_{BOARD}=100 \times P_{OUT}/P_{IN} \text{ (\%)} \quad (7)$$

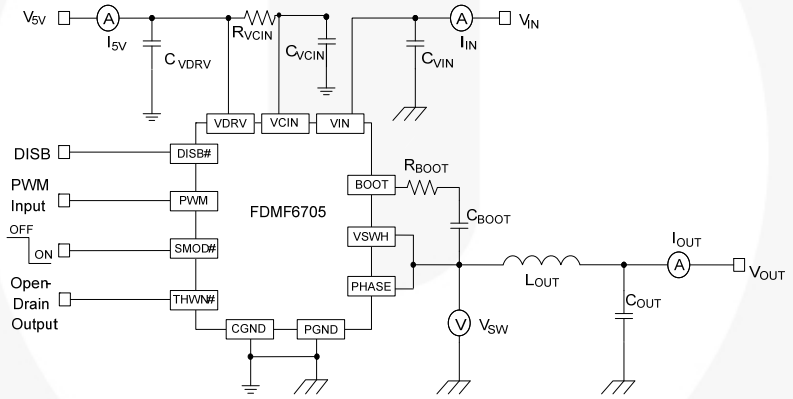


Figure 28. Power Loss Measurement Block Diagram

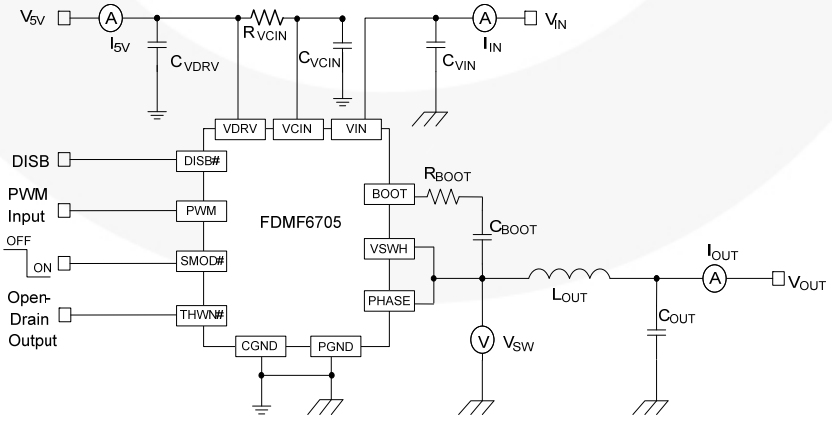


Figure 29. Block Diagram with V_{CIN} Filter

PCB Layout Guidelines

Figure 30 provides an example of a proper layout for the FDMF6705 and critical components. All of the high-current paths, such as V_{IN}, V_{SWH}, V_{OUT}, and GND copper, should be short and wide for low inductance and resistance. This technique aids in achieving a more stable and evenly distributed current flow, along with enhanced heat radiation and system performance.

The following guidelines are recommendations for the PCB designer:

1. Input ceramic bypass capacitors must be placed close to the VIN and PGND pins. This helps reduce the high-current power loop inductance and the input current ripple induced by the power MOSFET switching operation.

2. The V_{SWH} copper trace serves two purposes. In addition to being the high-frequency current path from the DrMOS package to the output inductor, it also serves as a heat sink for the low-side MOSFET in the DrMOS package. The trace should be short and wide enough to present a low-impedance path for the high-frequency, high-current flow between the DrMOS and inductor to minimize losses and temperature rise. Note that the VSWH node is a high voltage and high-frequency switching node with high noise potential. Care should be taken to minimize coupling to adjacent traces. Since this copper trace also acts as a heat sink for the lower FET, balance using the largest area possible to improve DrMOS cooling while maintaining acceptable noise emission.

3. An output inductor should be located close to the FDMF6705 to minimize the power loss due to the VSWH copper trace. Care should also be taken so the inductor dissipation does not heat the DrMOS.

4. PowerTrench® MOSFETs are used in the output stage. The Power MOSFETs are effective at minimizing ringing due to fast switching. In most cases, no VSWH snubber is required. If a snubber is used, it should be placed close to the VSWH and PGND pins. The resistor and capacitor need to be of proper size for the power dissipation.

5. VCIN, VDRV, and BOOT capacitors should be placed as close as possible to the VCIN to CGND, VDRV to CGND, and BOOT to PHASE pins to ensure clean and stable power. Routing width and length should be considered as well.

6. Include a trace from PHASE to VSWH to improve noise margin. Keep the trace as short as possible.

7. The layout should include a placeholder to insert a small-value series boot resistor (R_{BOOT}) between the boot capacitor (C_{BOOT}) and DrMOS BOOT pin. The BOOT-to-VSWH loop size, including R_{BOOT} and C_{BOOT}, should be as small as possible. The boot resistor may be required when operating near the maximum rated V_{IN}. The boot resistor is effective at controlling the high-side MOSFET turn-on slew rate and V_{SHW} overshoot. R_{BOOT} can improve noise operating margin in synchronous buck designs that may have noise issues due to ground bounce or high positive and negative VSWH ringing. However, inserting a boot resistance lowers the DrMOS efficiency. Efficiency versus noise trade-offs must be considered. R_{BOOT} values from 0.5 Ω to 3.0 Ω are typically effective in reducing VSWH overshoot for the FDMF6705.

   The VIN and PGND pins handle large current transients with frequency components greater than 100MHz. If possible, these pins should be connected directly to the VIN and board GND planes. The use of thermal relief traces in series with these pins is **discouraged** since this adds inductance to the power path. This added inductance in series with either the VIN or PGND pin degrades system noise immunity by increasing positive and negative VSWH ringing.

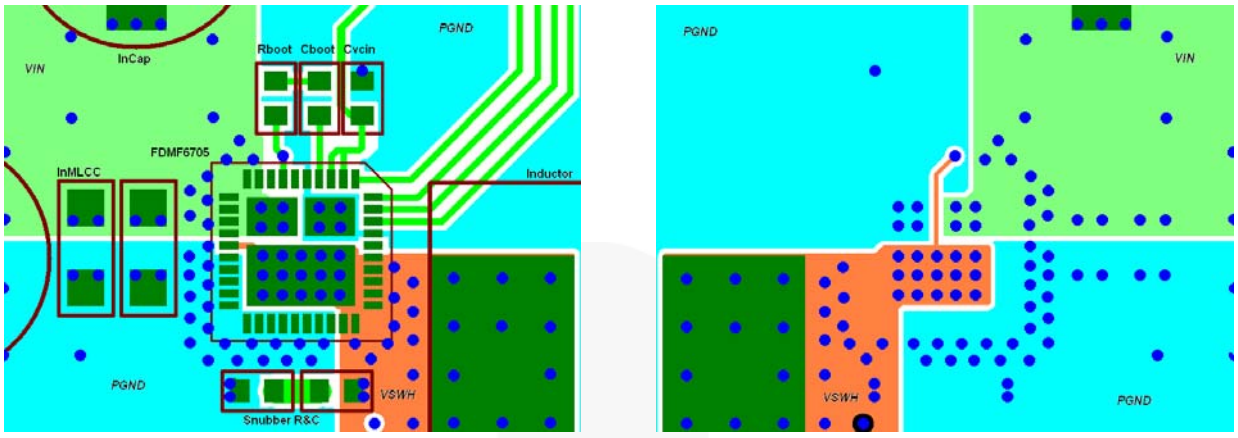
8. CGND pad and PGND pins should be connected to the GND plane copper with multiple vias for stable grounding. Poor grounding can create a noise transient offset voltage level between CGND and PGND. This could lead to faulty operation of the gate driver and MOSFETs.

9. Ringing at the BOOT pin is most effectively controlled by close placement of the boot capacitor. Do not add an additional BOOT to the PGND capacitor. This may lead to excess current flow through the BOOT diode.

10. The SMOD# and DISB# pins have weak internal pull-up and pull-down current sources, respectively. These pins should not have any noise filter capacitors. Do not to float these pins unless absolutely necessary.

11. Use multiple vias on each copper area to interconnect top, inner, and bottom layers to help distribute current flow and heat conduction. Vias should be relatively large and of reasonably low inductance. Critical high-frequency components, such as R_{BOOT}, C_{BOOT}, the RC snubber, and bypass capacitors should be located as close to the respective DrMOS module pins as possible on the top layer of the PCB. If this is not feasible, they should be connected from the backside through a network of low-inductance vias.

© 2011 Fairchild Semiconductor Corporation



Top View Bottom View

Figure 30. PCB Layout Example

Physical Dimensions

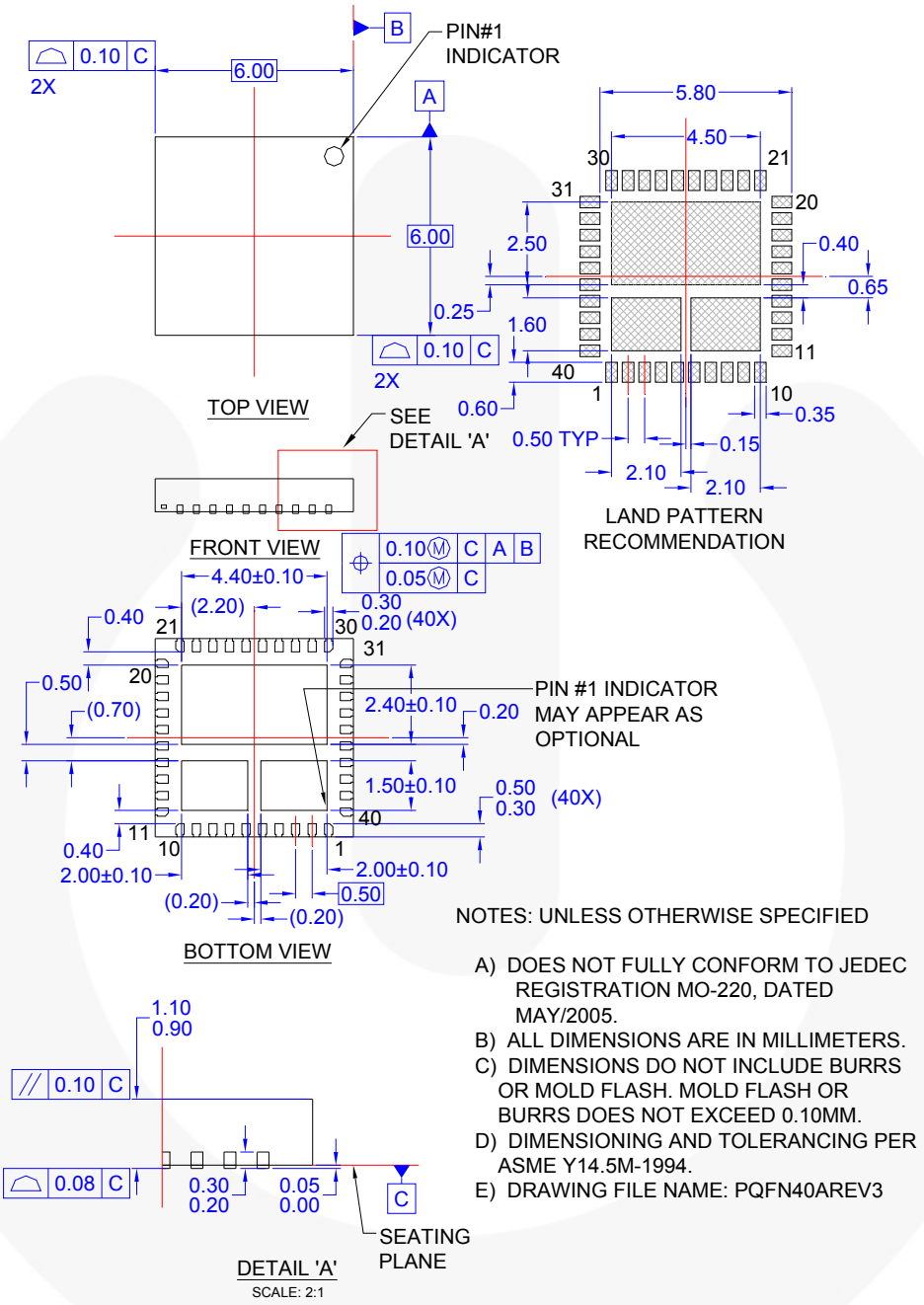


Figure 31. 40-Lead, Clipbond PQFN DrMOS, 6.0x6.0 mm Package

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:
http://www.fairchildsemi.com/packaging/.

© 2011 Fairchild Semiconductor Corporation

FAIRCHILD SEMICONDUCTOR®

TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

2Cool™
AccuPower™
AX-CAP®*
BitSiC™
Build it Now™
CorePLUS™
CorePOWER™
CROSSVOLT™
CTL™
Current Transfer Logic™
DEUXPEED®
Dual Cool™
EcoSPARK®
EfficientMax™
ESBC™
Fairchild®
Fairchild Semiconductor®
FACT Quiet Series™
FACT®
FAST®
FastvCore™
FETBench™
FPS™
F-PFS™
FRFET®
Global Power Resource℠
GreenBridge™
Green FPS™
Green FPS™ e-Series™
Gmax™
GTO™
IntelliMAX™
ISOPLANAR™
Making Small Speakers Sound Louder and Better™
MegaBuck™
MICROCOUPLER™
MicroFET™
MicroPak™
MicroPak2™
MillerDrive™
MotionMax™
mWSaver™
OptoHiT™
OPTOLOGIC®
OPTOPLANAR®
PowerTrench®
PowerXS™
Programmable Active Droop™
QFET®
QS™
Quiet Series™
RapidConfigure™
Saving our world, 1mW/W/kW at a time™
SignalWise™
SmartMax™
SMART START™
Solutions for Your Success™
SPM®
STEALTH™
SuperFET®
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SupreMOS®
SyncFET™
Sync-Lock™
SYSTEM GENERAL®*
TinyBoost™
TinyBuck™
TinyCalc™
TinyLogic®
TINYOPTO™
TinyPower™
TinyPWM™
TinyWire™
TranSiC™
TriFault Detect™
TRUECURRENT®*
µSerDes™
SerDes
UHC®
Ultra FRFET™
UniFET™
VCX™
VisualMax™
VoltagePlus™
XS™

* Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, www.fairchildsemi.com, under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I64

© 2011 Fairchild Semiconductor Corporation

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative