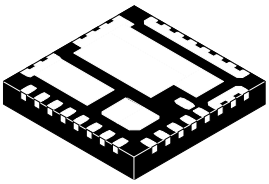
FDMF5833

Smart Power Stage (SPS) Module with Integrated Thermal Warning and Thermal Shutdown

ON Semiconductor®

www.onsemi.com



PQFN31 5x5, 0.5P
CASE 483BR

Description

The SPS family is ON Semiconductor's next−generation, fully optimized, ultra−compact, integrated MOSFET plus driver power stage solution for high−current, high−frequency, synchronous buck, DC−DC applications. The FDMF5833 integrates a driver IC with a bootstrap Schottky diode, two power MOSFETs, and a thermal monitor into a thermally enhanced, ultra−compact 5 mm x 5 mm package.

With an integrated approach, the SPS switching power stage is optimized for driver and MOSFET dynamic performance, minimized system inductance, and power

MOSFET $R_{DS(ON)}$. The SPS family uses ON Semiconductor's high−performance POWERTRENCH® MOSFET technology, which reduces switch ringing, eliminating the need for a snubber circuit in most buck converter applications.

A driver IC with reduced dead times and propagation delays further enhances the performance. A thermal warning function warns of a potential over−temperature situation. A thermal shutdown function turns off the driver if an over−temperature condition occurs. The FDMF5833 incorporates an Auto−DCM Mode (ZCD#) for improved light−load efficiency. The FDMF5833 also provides a 3−state 5 V PWM input for compatibility with a wide range of PWM controllers.

Features

- Ultra−Compact 5 mm x 5 mm PQFN Copper−Clip Package with Flip Chip Low−Side MOSFET
- High Current Handling: 50 A
- 3−State 5 V PWM Input Gate Driver
- Dynamic Resistance Mode for Low−Side Drive (LDRV) Slows Low−Side MOSFET during Negative Inductor Current Switching
- Auto DCM (Low−Side Gate Turn Off) Using ZCD# Input
- Thermal Warning (THWN#) to Warn Over− Temperature of Gate Driver IC
- Thermal Shutdown (THDN)
- HS−Short Detect Fault# / Shutdown
- Dual Mode Enable / Fault# Pin
- Internal Pull−Up and Pull−Down for ZCD# and EN Inputs, respectively
- ON Semiconductor POWERTRENCH MOSFETs for Clean Voltage Waveforms and Reduced Ringing
- ON Semiconductor SyncFET™ Technology (Integrated Schottky Diode) in Low−Side MOSFET
- Integrated Bootstrap Schottky Diode
- Optimized / Extremely Short Dead−Times

MARKING DIAGRAMS

FDMF5833



$Y	= Logo
&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
FDMF5833	= Specific Device Code

FDMF5833−F085



5833 F085	= Specific Device Code
A	= Assembly Location
ZZ	= Wafer Lot
YY	= Year
WW	= Work Week

ORDERING INFORMATION

See detailed ordering and shipping information on page 24 of this data sheet.

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Features (continued)

- Under−Voltage Lockout (UVLO) on VCC
- Optimized for Switching Frequencies up to 1.5 MHz
- PWM Minimum Controllable On−Time: 30 ns
- Low Shutdown Current: < 3 μA
- Optimized FET Pair for Highest Efficiency: 10 ~ 15% Duty Cycle
- Operating Junction Temperature Range: −40°C to +125°C
- ON Semiconductor Green Packaging
- Automotive Qualified to AEC−Q100 (F085 Version)
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Notebook, Tablet PC and Ultrabook
- Servers and Workstations, V−Core and Non−V−Core DC−DC Converters
- Desktop and All−in−One Computers, V−Core and Non−V−Core DC−DC Converters
- High−Performance Gaming Motherboards
- High−Current DC−DC Point−of−Load Converters
- Networking and Telecom Microprocessor Voltage Regulators
- Small Form−Factor Voltage Regulator Modules
- Automotive−qualified Systems (F085 Version)

PIN CONFIGURATION

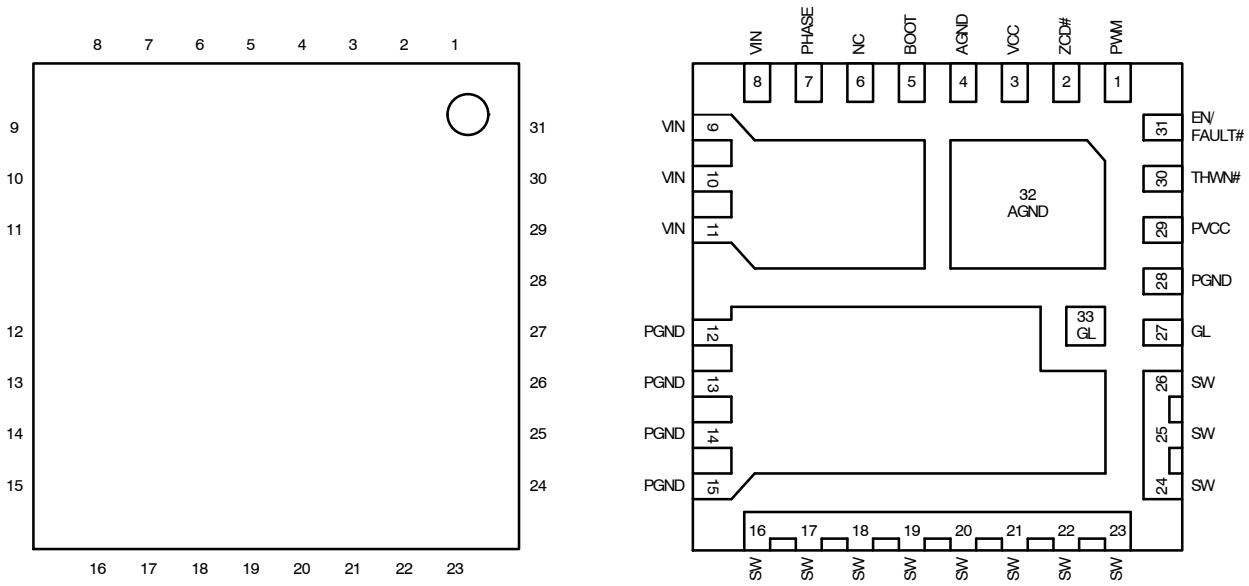


Figure 1. Pin Configuration – Top View and Transparent View

PIN DESCRIPTION

Pin No.	Symbol	Description
1	PWM	PWM input to the gate driver IC
2	ZCD#	Enable input for the ZCD (Auto DCM) comparator
3	VCC	Power supply input for all analog control functions; this is the “quiet” V_{CC}
4, 32	AGND	Analog ground for analog portions of the IC and for substrate, internally tied to PGND
5	BOOT	Supply for the high−side MOSFET gate driver. A capacitor from BOOT to PHASE supplies the charge to turn on the N−channel high−side MOSFET.
6	NC	No connect
7	PHASE	Return connection for the boot capacitor, internally tied to SW node
8~11	VIN	Power input for the power stage
12~15, 28	PGND	Power return for the power stage
16~26	SW	Switching node junction between high−side and low−side MOSFETs; also input to the gate driver SW node comparator and input into the ZCD comparator
27, 33	GL	Gate Low, Low−side MOSFET gate monitor
29	PVCC	Power supply input for LS (Note1) gate driver and boot diode
30	THWN#	125°C Thermal Warning Flag – pulls LOW upon detection of 125°C thermal warning pre− set temperature
31	EN / FAULT#	Dual−functionality, enable input to the gate driver IC. FAULT# – internal pull−down physically pulls this pin LOW upon detection of fault condition (HS (Note 2) MOSFET short or 150°C THDN).

1. LS = Low Side
2. HS = High Side

DIAGRAMS

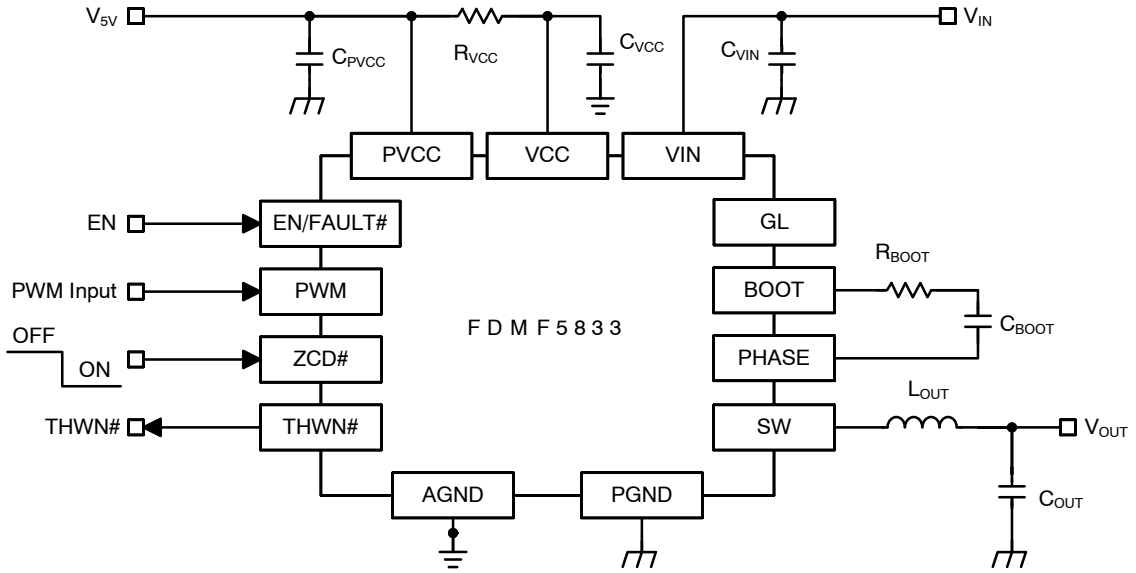


Figure 2. Typical Application Diagram

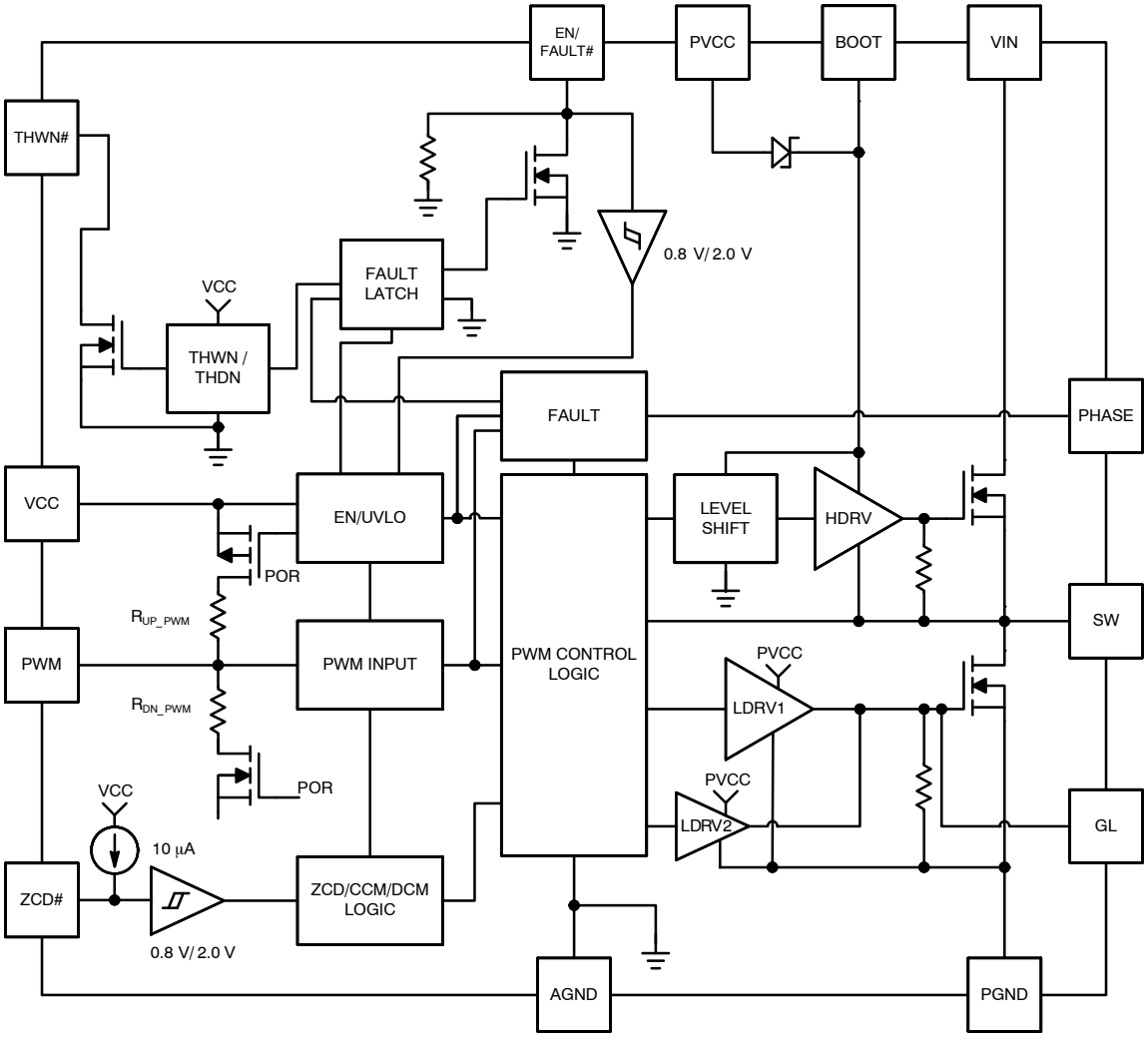


Figure 3. Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS (T_A = T_J = 25°C)

Symbol	Parameter	Value	Value	Ratings	Unit
V_{CC}	Supply Voltage	Referenced to AGND	−0.3	6.0	V
PV_{CC}	Drive Voltage	Referenced to AGND	−0.3	6.0	V
$V_{EN/FAULT\#}$	Output Enable / Disable	Referenced to AGND	−0.3	6.0	V
V_{PWM}	PWM Signal Input	Referenced to AGND	−0.3	V_{CC}+0.3	V
$V_{ZCD\#}$	ZCD Mode Input	Referenced to AGND	−0.3	6.0	V
V_{GL}	Low Gate Manufacturing Test Pin	Referenced to AGND (DC Only)	−0.3	6.0	V
		Referenced to AGND, AC < 20 ns	−3.0	6.0	
$V_{THWN\#}$	Thermal Warning	Referenced to AGND	−0.3	6.0	V
V_{IN}	Power Input	Referenced to PGND, AGND	−0.3	30.0	V
V_{PHASE}	PHASE	Referenced to PGND, AGND (DC Only)	−0.3	30.0	V
		Referenced to PGND, AC < 20 ns	−7.0	35.0	
V_{SW}	Switch Node Input	Referenced to PGND, AGND (DC Only)	−0.3	30.0	V
		Referenced to PGND, AC < 20 ns	−7.0	35.0	
V_{BOOT}	Bootstrap Supply	Referenced to AGND (DC Only)	−0.3	35.0	V
		Referenced to AGND, AC < 20 ns	−5.0	40.0	
$V_{BOOT-PHASE}$	Boot to PHASE Voltage	Referenced to PVCC	−0.3	6.0	V
$I_{O(AV)}$ (Note3)	Output Current	f_{SW} = 300 kHz, V_{IN} = 12 V, V_{OUT} = 1.8 V	–	50	A
		f_{SW} = 1 MHz, V_{IN} = 12 V, V_{OUT} = 1.8 V	–	45	
I_{FAULT}	EN / FAULT# Sink Current		−0.1	7.0	mA
D_{J-A}	Junction−to−Ambient Thermal Resistance		–	12.4	°C/W
D_{J-PCB}	Junction−to−PCB Thermal Resistance (under ON Semiconductor SPS Thermal Board)		–	1.8	°C/W
T_A	Ambient Temperature Range		−40	+125	°C
T_J	Maximum Junction Temperature			+150	°C
T_{STG}	Storage Temperature Range		−55	+150	°C
ESD	Electrostatic Discharge Protection	Human Body Model, ANSI/ESDA/JEDEC JS−001−2012	3000	–	V
		Charged Device Model, JESD22−C101	2500	–	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

3. $I_{O(AV)}$ is rated with testing ON Semiconductor's SPS evaluation board at T_A = 25°C with natural convection cooling. This rating is limited by the peak SPS temperature, T_J = 150°C, and varies depending on operating conditions and PCB layout. This rating may be changed with different application settings.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Control Circuit Supply Voltage	4.5	5.0	5.5	V
PV_{CC}	Gate Drive Circuit Supply Voltage	4.5	5.0	5.5	V
V_{IN}	Output Stage Supply Voltage	4.5 (Note 4)	19.0	24.0 (Note 5)	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. 3.0 V V_{IN} is possible according to the application condition.
5. Operating at high V_{IN} can create excessive AC voltage overshoots on the SW−to−GND and BOOT−to−GND nodes during MOSFET switching transient. For reliable SPS operation, SW to GND and BOOT to GND must remain at or below the Absolute Maximum Ratings in the table above.

ELECTRICAL CHARACTERISTICS

(Typical value is under V_{IN} = 12 V, V_{CC} = PV_{CC} = 5 V and T_A = T_J = +25°C unless otherwise noted. Minimum and maximum values are under V_{IN} = 12 V, V_{CC} = PV_{CC} = 5 V ±10% and T_J = T_A = −40°C ~ +125°C)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
BASIC OPERATION						
V_F	Forward−Voltage Drop	I_F = 10 mA	–	0.4	–	V
I_Q	Quiescent Current	I_Q = I_{VCC} + I_{PVCC}, EN = HIGH, PWM = LOW or HIGH or Float (Non−Switching)	–	–	2	mA
I_{SHDN}	Shutdown Current	I_{SHDN} = I_{VCC} + I_{PVCC}, EN = GND	–	–	3	μA
V_{UVLO}	UVLO Threshold	V_{CC} Rising	3.5	3.8	4.1	V
V_{UVLO_HYST}	UVLO Hysteresis		–	0.4	–	V
t_{D_POR}	POR Delay to Enable IC	V_{CC} UVLO Rising to Internal PWM Enable	–	–	20	μs
EN INPUT						
V_{IH_EN}	High−Level Input Voltage		2.0	–	–	V
V_{IL_EN}	Low−Level Input Voltage		–	–	0.8	V
R_{PLD_EN}	Pull−Down Resistance		–	250		kΩ
t_{PD_ENL}	EN LOW Propagation Delay	PWM = GND, EN Going LOW to GL Going LOW	–	25	–	ns
t_{PD_ENH}	EN HIGH Propagation Delay	PWM = GND, EN Going HIGH to GL Going HIGH	–	–	69	μs
ZCD# INPUT						
$V_{IH_ZCD\#}$	High−Level Input Voltage		2.0	–	–	V
$V_{IL_ZCD\#}$	Low−Level Input Voltage		–	–	0.8	V
$I_{PLU_ZCD\#}$	Pull−Up Current		–	10	–	μA
t_{PD_ZLGLL}	ZCD# LOW Propagation Delay	PWM = GND, ZCD# Going LOW to GL Going LOW (assume $I_L \le 0$)	–	10	–	ns
t_{PD_ZHGLH}	ZCD# HIGH Propagation Delay	PWM = GND, ZCD# Going HIGH to GL Going HIGH	–	10	–	ns
PWM INPUT						
R_{UP_PWM}	Pull−Up Impedance	Typical Values: T_A = T_J = 25°C, V_{CC} = PV_{CC} = 5 V; Min. / Max. Values: T_A = T_J = −40°C to 125°C, V_{CC} = PV_{CC} = 5 V ±10%	–	10	–	kΩ
R_{DN_PWM}	Pull−Down Impedance		–	10	–	kΩ
V_{IH_PWM}	PWM High Level Voltage		3.8	–	–	V
V_{TRI_Window}	3−State Window		1.2	–	3.1	V
V_{IL_PWM}	PWM Low Level Voltage		–	–	0.8	V
$t_{D_HOLD-OFF}$	3−State Shut−Off Time		–	90	130	ns
V_{HIZ_PWM}	3−State Open Voltage		2.1	2.5	2.9	V
MINIMUM CONTROLLABLE ON−TIME						
$t_{MIN_PWM_ON}$	PWM Minimum Controllable On−Time	Minimum PWM HIGH Pulse Required for SW Node to Switch from GND to VIN	30	–	–	ns
FORCED MINIMUM GL HIGH TIME						
$t_{MIN_GL_HIGH}$	Forced Minimum GL HIGH	Minimum GL HIGH Time when LOW $V_{BOOT-SW}$ detected and PWM LOW ≤ 100 ns	–	100	–	ns
PWM INPUT PROPAGATION DELAYS AND DEAD TIMES (V_{IN} = 12 V, V_{CC} = PV_{CC} = 5 V, f_{sw} = 1 MHz, I_{OUT} = 20 A, T_A = 25°C)						
t_{PD_PHGLL}	PWM HIGH Propagation Delay	PWM Going HIGH to GL Going LOW, V_{IH_PWM} to 90% GL	–	15	–	ns
t_{PD_PLGHL}	PWM LOW Propagation Delay	PWM Going LOW to GH (Note 6) Going LOW, V_{IL_PWM} to 90% GH	–	30	–	ns

ELECTRICAL CHARACTERISTICS (continued)
(Typical value is under V_{IN} = 12 V, V_{CC} = PV_{CC} = 5 V and T_A = T_J = +25°C unless otherwise noted. Minimum and maximum values are under V_{IN} = 12 V, V_{CC} = PV_{CC} = 5 V ±10% and T_J = T_A = −40°C ~ +125°C)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
PWM INPUT PROPAGATION DELAYS AND DEAD TIMES (V_{IN} = 12 V, V_{CC} = PV_{CC} = 5 V, f_{sw} = 1 MHz, I_{OUT} = 20 A, T_A = 25°C)						
t_{PD_PHGHH}	PWM LOW Propagation Delay (ZCD# Held LOW)	PWM Going HIGH to GH Going HIGH, V_{IH_PWM} to 10% GH (ZCD# = LOW, I_L = 0, assumes DCM)	–	10	–	ns
t_{D_DEADON}	LS Off to HS On Dead Time	GL Going LOW to GH Going HIGH, 10% GL to 10% GH, PWM Transition LOW to HIGH (See Figure 29)	–	10	–	ns
$t_{D_DEADOFF}$	HS Off to LS On Dead Time	GH Going LOW to GL Going HIGH, 10% GH to 10% GL, PWM Transition HIGH to LOW (See Figure 29)	–	5	–	ns
$t_{R_GH_20A}$	GH Rise Time under 20 A I_{OUT}	10% GH to 90% GH, I_{OUT} = 20 A	–	9	–	ns
$t_{F_GH_20A}$	GH Fall Time under 20 A I_{OUT}	90% GH to 10% GH, I_{OUT} = 20 A	–	9	–	ns
$t_{R_GL_20A}$	GL Rise Time under 20 A I_{OUT}	10% GL to 90% GL, I_{OUT} = 20 A	–	9	–	ns
$t_{F_GL_20A}$	GL Fall Time under 20 A I_{OUT}	90% GL to 10% GL, I_{OUT} = 20 A	–	6	–	ns
t_{PD_TSGHH}	Exiting 3−State Propagation Delay	PWM (from 3−State) Going HIGH to GH Going HIGH, V_{IH_PWM} to 10% GH	–	–	45	ns
t_{PD_TSGLH}	Exiting 3−State Propagation Delay	PWM (from 3−State) Going LOW to GL Going HIGH, V_{IL_PWM} to 10% GL	–	–	45	ns
HIGH−SIDE DRIVER (HDRV, V_{CC} = PV_{CC} = 5 V)						
R_{SOURCE_GH}	Output Impedance, Sourcing	Source Current = 100 mA	–	0.68	–	Ω
R_{SINK_GH}	Output Impedance, Sinking	Sink Current = 100 mA	–	0.9	–	Ω
t_{R_GH}	GH Rise Time	10% GH to 90% GH, C_{LOAD} = 1.3 nF	–	4	–	ns
t_{F_GH}	GH Fall Time	90% GH to 10% GH, C_{LOAD} = 1.3 nF	–	3	–	ns
WEAK LOW−SIDE DRIVER (LDRV2 Only under CCM2 Mode Operation, V_{CC} = PV_{CC} = 5 V)						
R_{SOURCE_GL}	Output Impedance, Sourcing	Source Current = 100 mA	–	0.82	–	Ω
I_{SOURCE_GL}	Output Sourcing Peak Current	GL = 2.5 V	–	2	–	A
R_{SINK_GL}	Output Impedance, Sinking	Sink Current = 100 mA	–	0.86	–	Ω
I_{SINK_GL}	Output Sinking Peak Current	GL = 2.5 V	–	2	–	A
LOW−SIDE DRIVER (Paralleled LDRV1 + LDRV2 under CCM1 Mode Operation, V_{CC} = PV_{CC} = 5 V)						
R_{SOURCE_GL}	Output Impedance, Sourcing	Source Current = 100 mA	–	0.47	–	Ω
I_{SOURCE_GL}	Output Sourcing Peak Current	GL = 2.5 V	–	4	–	A
R_{SINK_GL}	Output Impedance, Sinking	Sink Current = 100 mA	–	0.29	–	Ω
I_{SINK_GL}	Output Sinking Peak Current	GL = 2.5 V	–	7	–	A
t_{R_GL}	GL Rise Time	10% GL to 90% GL, C_{LOAD} = 7.0 nF	–	9	–	ns
t_{F_GL}	GL Fall Time	90% GL to 10% GL, C_{LOAD} = 7.0 nF	–	6	–	ns
THERMAL WARNING FLAG (125°C)						
$T_{ACT_THWN_125}$	Activation Temperature	Measured on the driver IC with T_J = T_A	–	125	–	°C
$T_{RST_THWN_125}$	Reset Temperature		–	110	–	°C
R_{PLD_THWN}	Pull−Down Resistance	I_{PLD_THWN} = 1 mA	–	100	–	Ω
THERMAL SHUTDOWN (150°C)						
T_{ACT_THDN}	Activation Temperature	Measured on the driver IC with T_J = T_A	–	150	–	°C
$R_{PLD_EN-THDN}$	Pull−Down Resistance	$I_{PLD_EN-THDN}$ = 1 mA	–	50	–	Ω

ELECTRICAL CHARACTERISTICS (continued)
(Typical value is under V_{IN} = 12 V, V_{CC} = PV_{CC} = 5 V and T_A = T_J = +25°C unless otherwise noted. Minimum and maximum values are under V_{IN} = 12 V, V_{CC} = PV_{CC} = 5 V ±10% and T_J = T_A = −40°C ~ +125°C)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
CATASTROPHIC FAULT (SW Monitor)						
V_{SW_MON}	SW Monitor Reference Voltage		–	1.3	2	V
t_{D_FAULT}	Propagation Delay to Pull EN / FAULT# Signal = LOW		–	20	–	ns
BOOT DIODE						
V_F	Forward−Voltage Drop	I_F = 10 mA	–	0.4	–	V
V_R	Breakdown Voltage	I_R = 1 mA	30	–	–	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
6. GH = Gate High, internal gate pin of the high−side MOSFET.

TYPICAL PERFORMANCE CHARACTERISTICS

Test Conditions: V_{IN} = 12 V, V_{CC} = PV_{CC} = 5 V, V_{OUT} = 1.8 V, L_{OUT} = 250 nH, T_A = 25°C and natural convection cooling, unless otherwise noted.

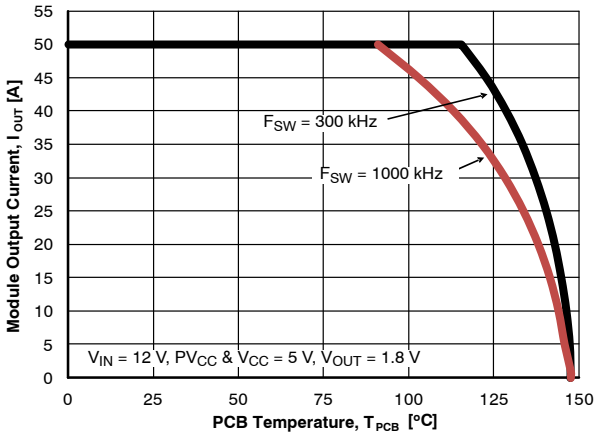


Figure 4. Safe operating Area 12 V_{IN}

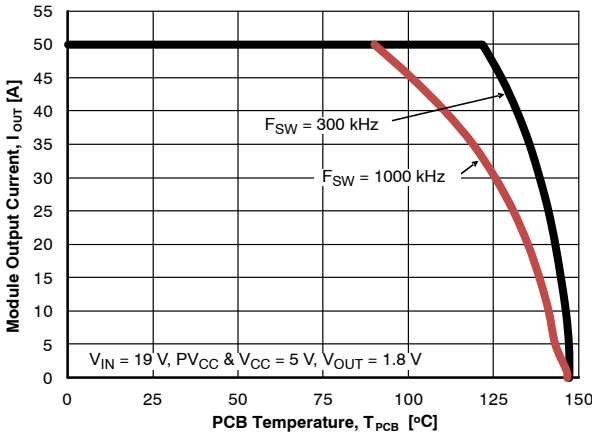


Figure 5. Safe operating Area 19 V_{IN}

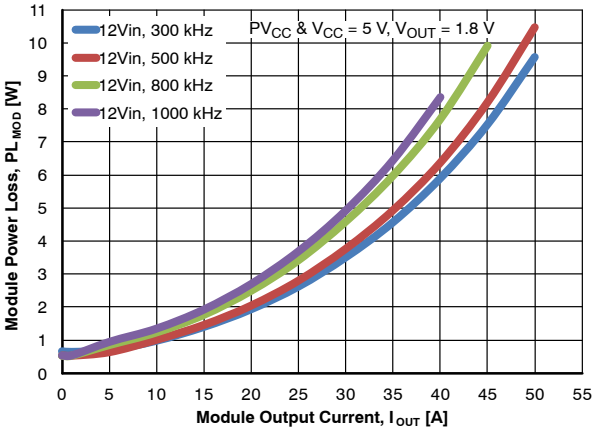


Figure 6. Power Loss vs. Output Current with 12 V_{IN}

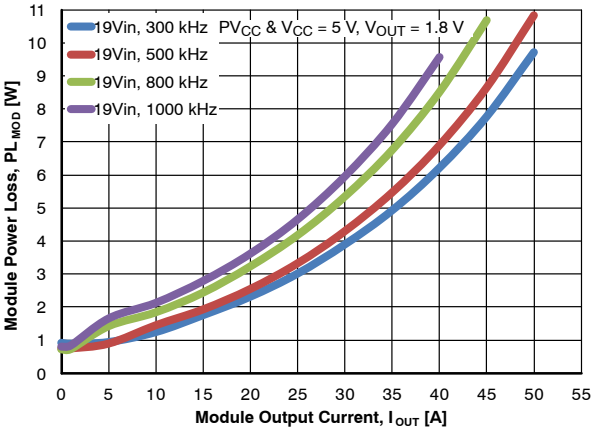


Figure 7. Power Loss vs. Output Current with 19 V_{IN}

TYPICAL PERFORMANCE CHARACTERISTICS

Test Conditions: V_{IN} = 12 V, V_{CC} = PV_{CC} = 5 V, V_{OUT} = 1.8 V, L_{OUT} = 250 nH, T_A = 25°C and natural convection cooling, unless otherwise noted.

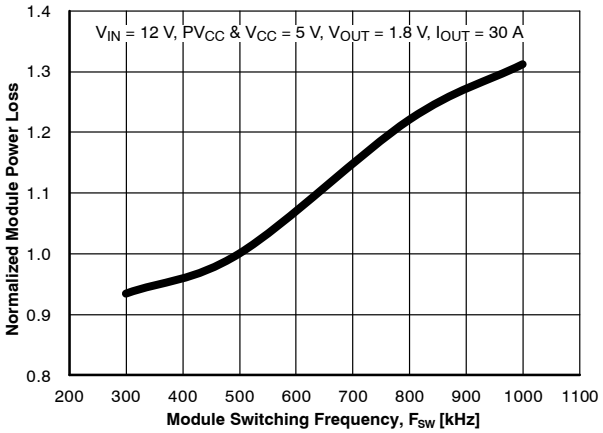


Figure 8. Power Loss vs. Switching Frequency

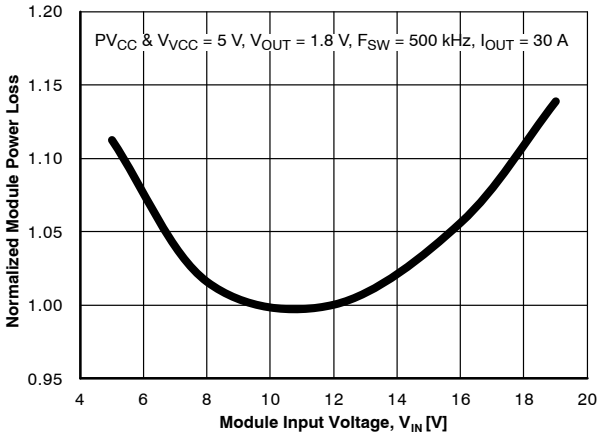


Figure 9. Power Loss vs. Input Voltage

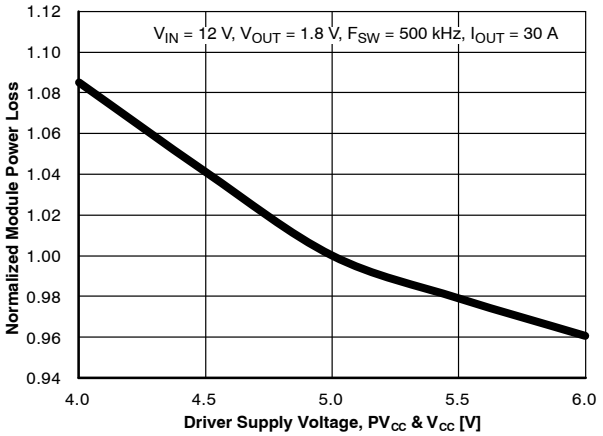


Figure 10. Power Loss vs. Driver Supply Voltage

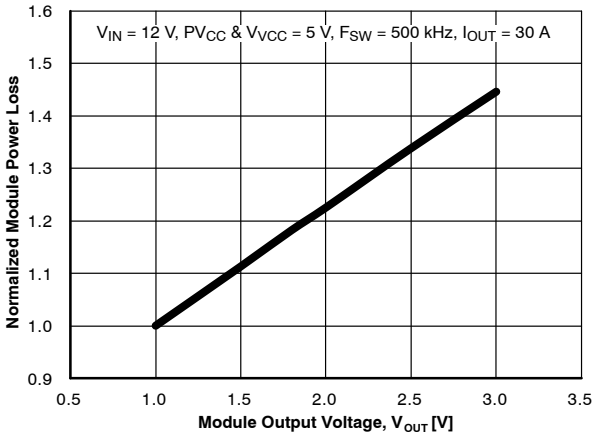


Figure 11. Power Loss vs. Output Voltage

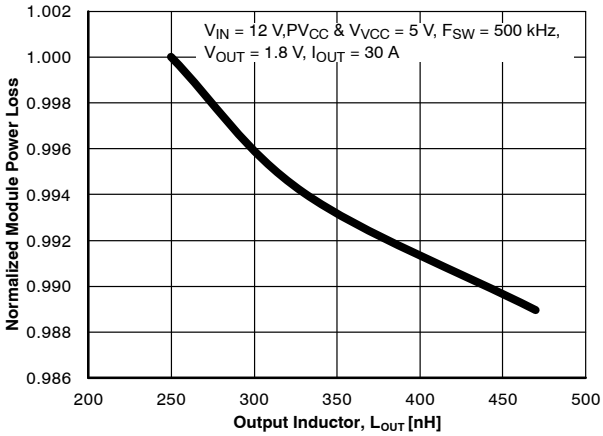


Figure 12. Power Loss vs. Output Inductor

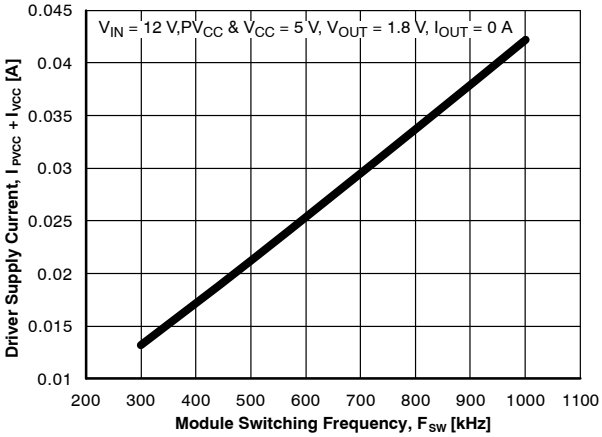


Figure 13. Driver Supply Current vs. Switching Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

Test Conditions: V_{IN} = 12 V, V_{CC} = PV_{CC} = 5 V, V_{OUT} = 1.8 V, L_{OUT} = 250 nH, T_A = 25°C and natural convection cooling, unless otherwise noted.

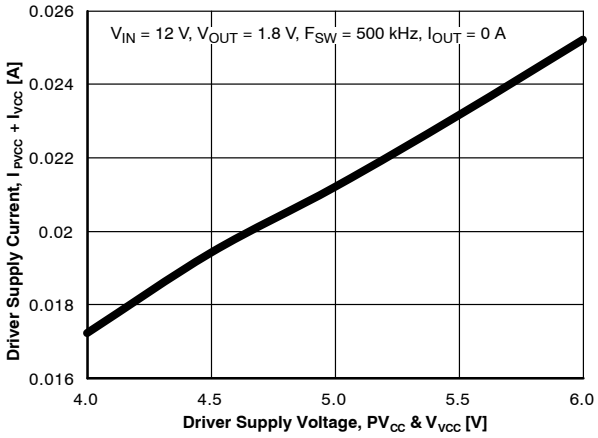


Figure 14. Driver Supply Current vs. Driver Supply Voltage

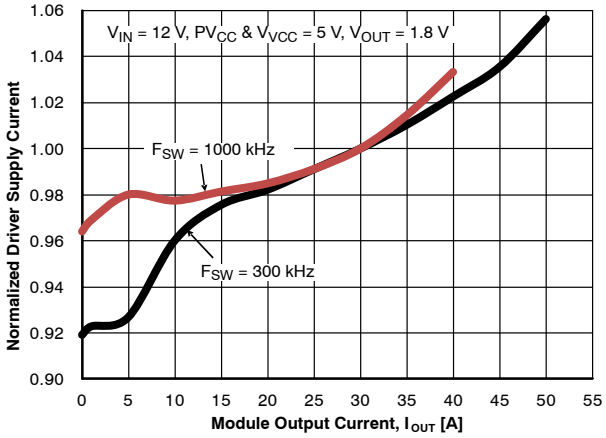


Figure 15. Driver Supply Current vs. Output Current

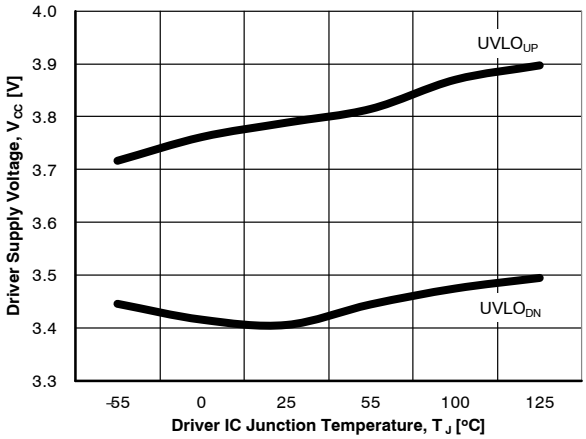


Figure 16. UVLO Threshold vs. Temperature

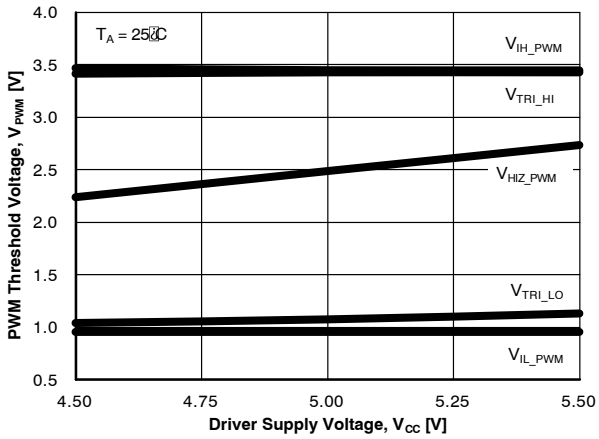


Figure 17. PWM Threshold vs. Driver Supply Voltage

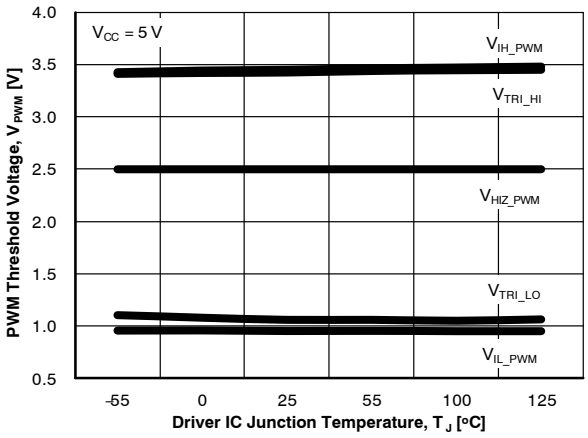


Figure 18. PWM Threshold vs. Temperature

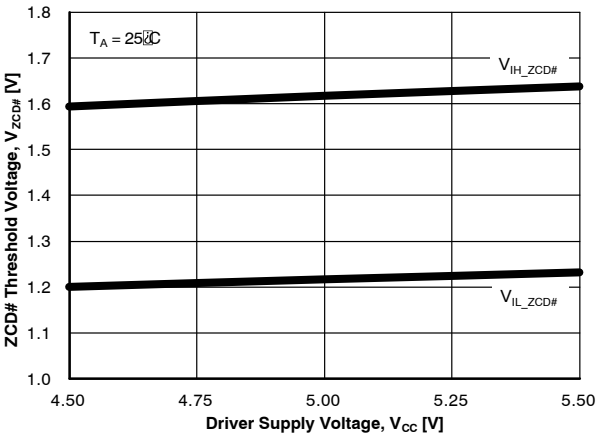


Figure 19. ZCD# Threshold vs. Driver Supply Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

Test Conditions: V_{IN} = 12 V, V_{CC} = PV_{CC} = 5 V, V_{OUT} = 1.8 V, L_{OUT} = 250 nH, T_A = 25°C and natural convection cooling, unless otherwise noted.

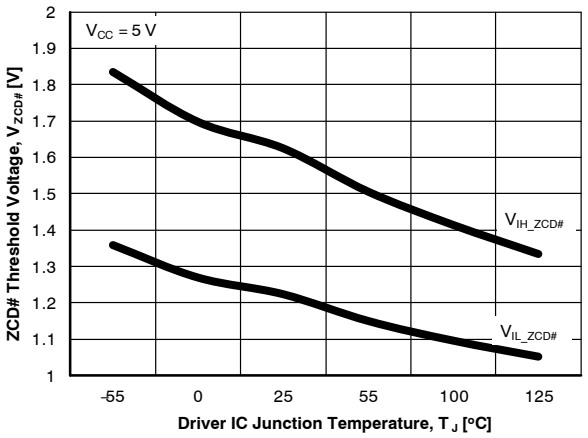


Figure 20. ZCD# Threshold vs. Temperature

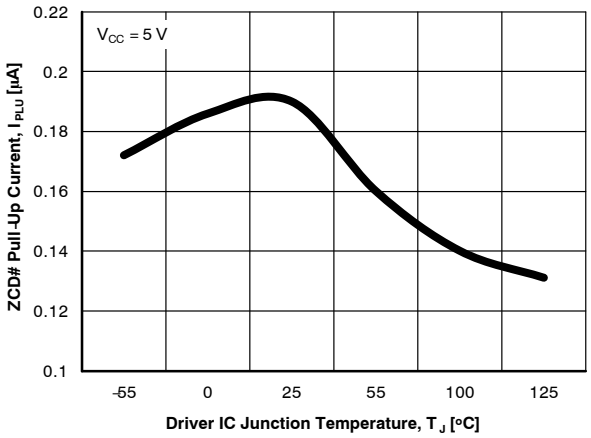


Figure 21. ZCD# Pull−Up Current vs. Temperature

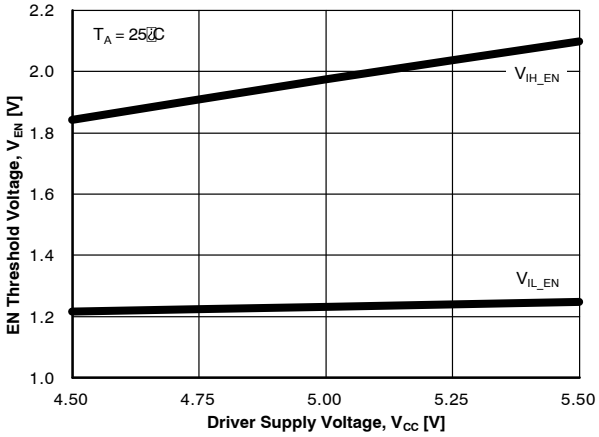


Figure 22. EN Threshold vs. Driver Supply Voltage

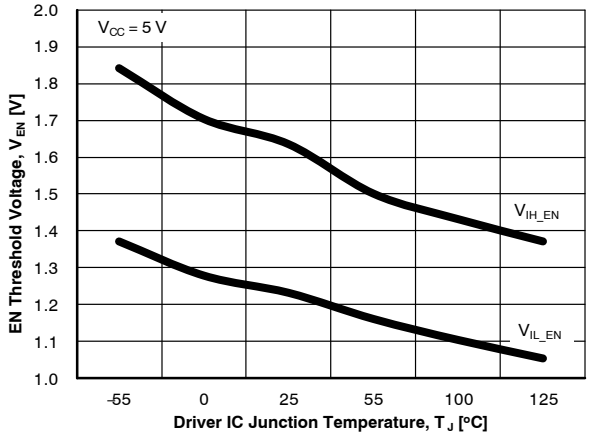


Figure 23. EN Threshold vs. Temperature

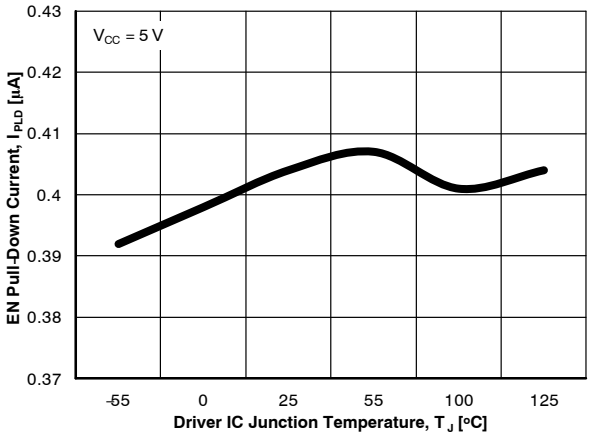


Figure 24. EN Pull−Down Current vs. Temperature

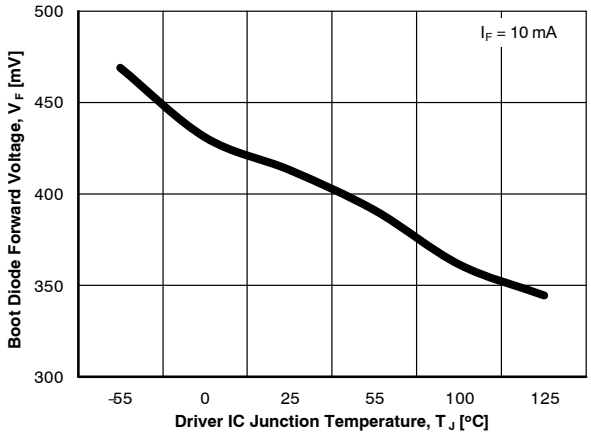


Figure 25. Boot Diode Forward Voltage vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

Test Conditions: V_{IN} = 12 V, V_{CC} = PV_{CC} = 5 V, V_{OUT} = 1.8 V, L_{OUT} = 250 nH, T_A = 25°C and natural convection cooling, unless otherwise noted.

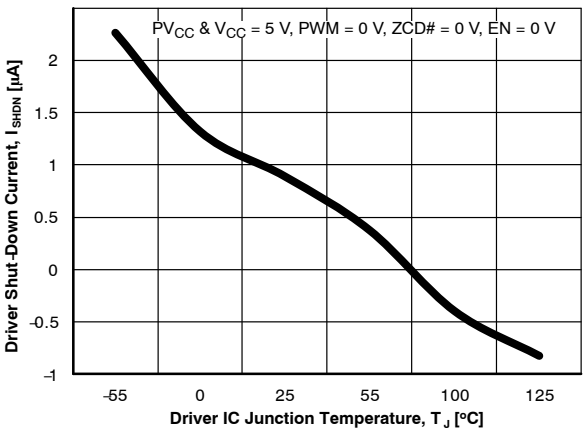


Figure 26. Driver Shutdown vs. Temperature

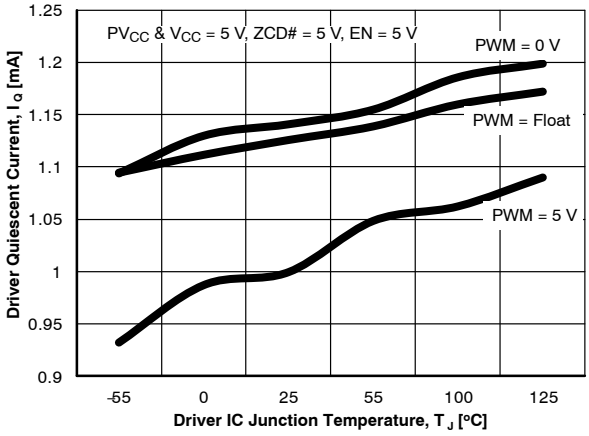


Figure 27. Driver Quiescent Current vs. Temperature

FUNCTIONAL DESCRIPTION

The SPS FDMF5833 is a driver−plus−MOSFET module optimized for the synchronous buck converter topology. A PWM input signal is required to properly drive the high−side and the low−side MOSFETs. The part is capable of driving speed up to 1.5 MHz.

Power−On Reset (POR)

The PWM input stage should incorporate a POR feature to ensure both LDRV and HDRV are forced inactive (LDRV = HDRV = 0) until UVLO > ~3.8 V (rising threshold). After all gate drive blocks are fully powered on and have finished the startup sequence, the internal driver IC EN_PWM signal is released HIGH, enabling the driver outputs. Once the driver POR has finished (< 20 μs maximum), the driver follows the state of the PWM signal (it is assumed that at startup the controller is either in a high−impedance state or forcing the PWM signal to be within the driver 3−state window).

Three conditions below must be supported for normal startup / power−up.

- V_{CC} rises to 5 V, then EN goes HIGH:
- EN pin is tied to the VCC pin:
- EN is commanded HIGH prior to 5 V V_{CC} reaching the UVLO rising threshold.

The POR method is to increase the V_{CC} over than UVLO > rising threshold and EN = HIGH.

Under−Voltage Lockout (UVLO)

UVLO is performed on V_{CC} only, not on PV_{CC} or V_{IN}. When the EN is set HIGH and V_{CC} is rising over the UVLO threshold level (3.8 V), the part starts switching operation after a maximum 20 μs POR delay. The delay is implemented to ensure the internal circuitry is biased, stable, and ready to operate. Two VCC pins are provided: PVCC and VCC. The gate driver circuitry is powered from the PVCC rail. The user connects PVCC to VCC through a low−pass R−C filter. This provides a filtered 5 V bias to the analog circuitry on the IC.

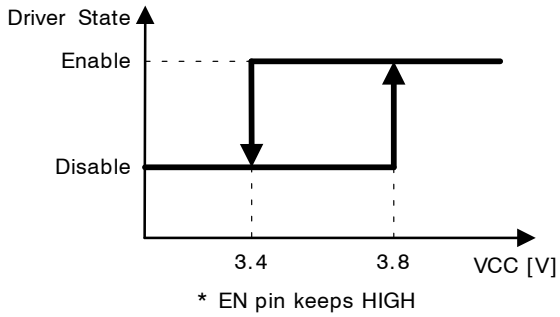


Figure 28. UVLO on VCC

EN / FAULT# (Enable / Fault Flag)

The driver can be disabled by pulling the EN / FAULT# pin LOW (EN < V_{IL_EN}), which holds both GL and GH LOW regardless of the PWM input state. The driver can be enabled by raising the EN / FAULT# pin voltage HIGH (EN > V_{IH_EN}). The driver IC has less than 3 μA shutdown current when it is disabled. Once the driver is re−enabled, it takes a maximum of 20 μs startup time.

EN / FAULT# pin is an open−drain output for fault flag with an internal 250 kΩ pull−down resistor. Logic HIGH signal from PWM controller or ~10 kΩ external pull−up resistor from EN / FAULT# pin to VCC is required to start driver operation.

Table 1. UVLO AND DRIVER STATE

UVLO	EN	Driver State
0	X	Disabled (GH & GL = 0)
1	0	Disabled (GH & GL = 0)
1	1	Enabled (see Table 2)
1	Open	Disabled (GH & GL = 0)

The EN / FAULT# pin has two functions; enabling / disabling driver and fault flag. The fault flag signal is active LOW. When the driver detects a fault condition during operation, it turns on the open−drain on the EN / FAULT# pin and the pin voltage is pulled LOW. The fault conditions are:

- High−side MOSFET false turn−on or VIN ~ SW short during low−side MOSFET turn on:
- THDN by 150°C of driver T_J.

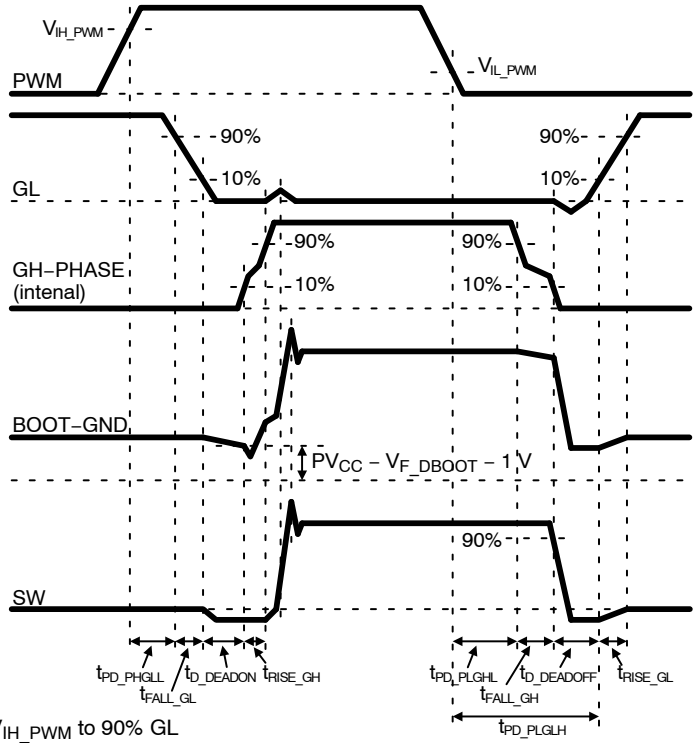
When the driver detects a fault condition and disables itself, a POR event on VCC is required to restart the driver operation.

3−State PWM Input

The FDMF5833 incorporates a 3−state 5 V PWM input gate drive design. The 3−state gate drive has both logic HIGH and LOW levels, along with a 3−state shutdown window. When the PWM input signal enters and remains within the 3−state window for a defined hold−off time ($t_{D_HOLD-OFF}$), both GL and GH are pulled LOW. This feature enables the gate drive to shut down both the high−side and the low−side MOSFETs to support features such as phase shedding, a common feature on multi−phase voltage regulators.

Table 2. EN / PWM / 3−STATE / ZCD# LOGIC STATES

EN	PWM	ZCD#	GH	GL
0	X	X	0	0
1	3−State	X	0	0
1	0	0	0	1 (IL > 0), 0 (IL < 0)
1	1	0	1	0
1	0	1	0	1
1	1	1	1	0



t_{PD_PHGLL} = PWM HI to GL LO, V_{IH_PWM} to 90% GL
t_{FALL_GL} = 90% GL to 10% GL
t_{D_DEADON} = LS Off to HS On Dead Time, 10% GL to $V_{BOOT-GND} \le PV_{CC} - V_{F_DBOOT} - 1V$ or BOOT−GND dip start point
t_{RISE_GH} = 10% GH to 90% GH, $V_{BOOT-GND} \le PV_{CC} - V_{F_DBOOT} - 1V$ or BOOT−GND dip start point to GL bounce start point

t_{PD_PLGHL} = PWM LO to GH LO, V_{IL_PWM} to 90% GH or BOOT−GND decrease start point, $t_{PD_PLGLH} - t_{D_DEADOFF} - t_{FALL_GH}$
t_{FALL_GH} = 90% GH to 10% GH, BOOT−GND decrease start point to 90% V_{SW} or GL dip start point
$t_{D_DEADOFF}$ = HS Off to LS On Dead Time, 90% V_{SW} or GL dip start point to 10% GL
t_{RISE_GL} = 10% GL to 90% GL
t_{PD_PLGLH} = PWM LO to GL HI, V_{IL_PWM} to 10% GL

Figure 29. PWM Timing Diagram

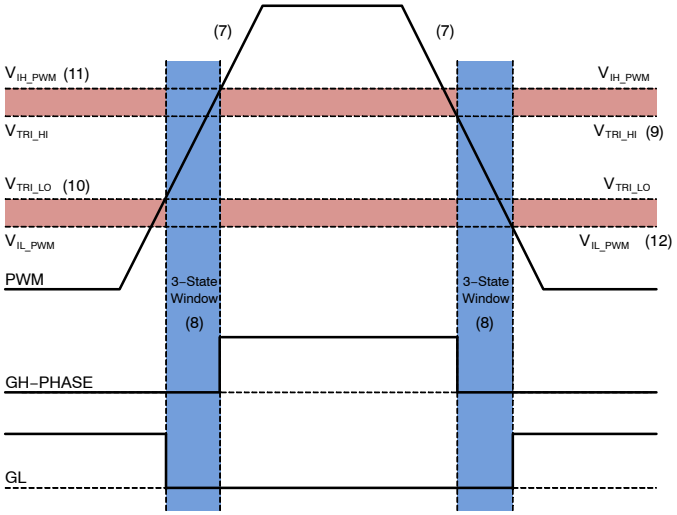


Figure 30. PWM Threshold Definition

NOTE:
7. The timing diagram in Figure 30 assumes very slow ramp on PWM.
8. Slow ramp of PWM implies the PWM signal remains within the 3−state window for a time >>> $t_{D_HOLD-OFF}$.
9. V_{TRI_HI} = PWM trip level to enter 3−state on PWM falling edge.
10. V_{TRI_LO} = PWM trip level to enter 3−state on PWM rising edge.
11. V_{IH_PWM} = PWM trip level to exit 3−state on PWM rising edge and enter the PWM HIGH logic state.
12. V_{IL_PWM} = PWM trip level to exit 3−state on PWM falling edge and enter the PWM LOW logic state.

Power Sequence

SPS FDMF5833 requires four (4) input signals to conduct normal switching operation: V_{IN}, V_{CC} / PV_{CC}, PWM, and EN. PWM should not be applied before V_{CC} and the amplitude of PWM should not be higher than V_{CC}. All other combinations of their power sequences are allowed. The below example of a power sequence is for a reference application design:

- From no input signals
  - V_{IN} On: Typical 12 V_{DC}
  - V_{CC} / PV_{CC} On: Typical 5 V_{DC}
  - EN HIGH: Typical 5 V_{DC}
  - PWM Signaling: 5 V HIGH / 0 V LOW

The VIN pins are tied to the system main DC power rail.

PVCC and VCC pins are tied together to supply gate driving and logic circuit powers from the system V_{CC} rail. Or the PVCC pin can be directly tied to the system V_{CC} rail, and the VCC pin is powered by PVCC pin through a filter resistor located between PVCC pin and VCC pin. The filter resistor reduces switching noise impact from PV_{CC} to V_{CC}.

The EN pin can be tied to the V_{CC} rail with an external pull−up resistor and it will maintain HIGH once the V_{CC} rail turns on. Or the EN pin can be directly tied to the PWM controller for other purposes.

High−Side Driver

The high−side driver (HDRV) is designed to drive a floating N−channel MOSFET (Q1). The bias voltage for the high−side driver is developed by a bootstrap supply circuit, consisting of the internal Schottky diode and external bootstrap capacitor (C_{BOOT}). During startup, the SW node is held at PGND, allowing C_{BOOT} to charge to PVCC through the internal bootstrap diode. When the PWM input goes HIGH, HDRV begins to charge the gate of the high−side MOSFET (internal GH pin). During this transition, the charge is removed from the C_{BOOT} and delivered to the gate of Q1. As Q1 turns on, SW rises to V_{IN}, forcing the BOOT pin to V_{IN} + V_{BOOT}, which provides sufficient V_{GS} enhancement for Q1. To complete the switching cycle, Q1 is turned off by pulling HDRV to SW. C_{BOOT} is then recharged to PVCC when the SW falls to PGND. HDRV output is in phase with the PWM input. The high−side gate is held LOW when the driver is disabled or the PWM signal is held within the 3−state window for longer than the 3−state hold−off time, $t_{D_HOLD-OFF}$.

Low−Side Driver

The low−side driver (LDRV) is designed to drive the gate−source of a ground−referenced, low−$R_{DS(ON)}$, N−channel MOSFET (Q2). The bias for LDRV is internally connected between the PVCC and AGND. When the driver is enabled, the driver output is 180° out of phase with the PWM input. When the driver is disabled (EN = 0 V), LDRV is held LOW.

Continuous Current Mode 2 (CCM2) Operation

A main feature of the low−side driver design in SPS FMDF5833 is the ability to control the part of the low− side gate driver upon detection of negative inductor current, called CCM2 operation. This is accomplished by using the ZCD comparator signal. The primary reason for scaling back on the drive strength is to limit the peak V_{DS} stress when the low−side MOSFET hard−switches inductor current. This peak V_{DS} stress has been an issue with

applications with large amounts of load transient and fast and wide output voltage regulation.

The MOSFET gate driver in SPS FDMF5833 operates in one of three modes, described below.

Continuous Current Mode 1 (CCM1) with Positive Inductor Current

In this mode, inductor current is always flowing towards the output capacitor, typical of a heavily loaded power stage. The high−side MOSFET turns on with the low−side body diode conducting inductor current and SW is approximately V_F below ground, meaning hard−switched turn on and off the high−side MOSFET.

Discontinuous Current Mode (DCM)

Typical of lightly loaded power stage; the high−side MOSFET turns on with zero inductor current, ramps the inductor current, then returns to zero every switching cycle. When the high−side MOSFET turns on under DCM operation, the SW node may be at any voltage from a V_F below ground to a V_F above V_{IN}. This is because after the low−side MOSFET turns off, the SW node capacitance resonates with the inductor current.

The level shifter in driver IC should be able to turn on the high−side MOSFET regardless of the SW node voltage. In this case, the high−side MOSFET turns off a positive current.

During this mode, both LDRV1 and LDRV2 operate in parallel and the low−side gate driver pull−up and pull− down resistors are operating at full strength.

Continuous Current Mode 2 (CCM2) with Negative Inductor Current

This mode is typical in a synchronous buck converter pulling energy from the output capacitors and delivering the energy to the input capacitors (Boost Mode). In this mode, the inductor current is negative (meaning towards the MOSFETs) when the low−side MOSFET is turned off (may be negative when the high−side MOSFET turns on as well). This situation causes the low−side MOSFET to hard switch while the high−side MOSFET acts as a synchronous rectifier (temporarily operated in synchronous Boost Mode).

During this mode, only the “weak” LDRV2 is used for low−side MOSFET turn−on and turn−off. The intention is to slow down the low−side MOSFET switching speed when it is hard switching to reduce peak V_{DS} stress.

Dead−Times in CCM1 / DCM / CCM2

The driver IC design ensures minimum MOSFET dead times, while eliminating potential shoot−through (cross−conduction) currents. To ensure optimal module efficiency, body diode conduction times must be reduced to the low nano−second range during CCM1 and DCM operation. CCM2 alters the gate drive impedance while operating the power MOSFETs in a different mode versus CCM1 / DCM. Altered dead−time operation must be considered.

Low−Side MOSFET Off to High−Side MOSFET On Dead Time in CCM1 / DCM

To prevent overlap during the low−side MOSFET off to high−side MOSFET on switching transition, an adaptive circuitry monitors the voltage at the GL pin. When the PWM signal goes HIGH, GL goes LOW after a propagation delay (t_{PD_PHGLL}). Once the GL pin is discharged below ~ 1 – 2 V, GH is pulled HIGH after an adaptive delay, t_{D_DEADON}.

Some situations where the ZCD# rising−edge signal leads the PWM rising edge by tens of nanoseconds, can cause GH and GL overlap. This event can occur when the PWM controller sends PWM and ZCD# signals that lead, lag, or are synchronized. To avoid this phenomenon, a secondary fixed propagation delay (t_{FD_ON1}) is added to ensure there is always a minimum delay between low−side MOSFET off to high−side MOSFET on.

Low−Side MOSFET Off to High−Side MOSFET On Dead Time in CCM2

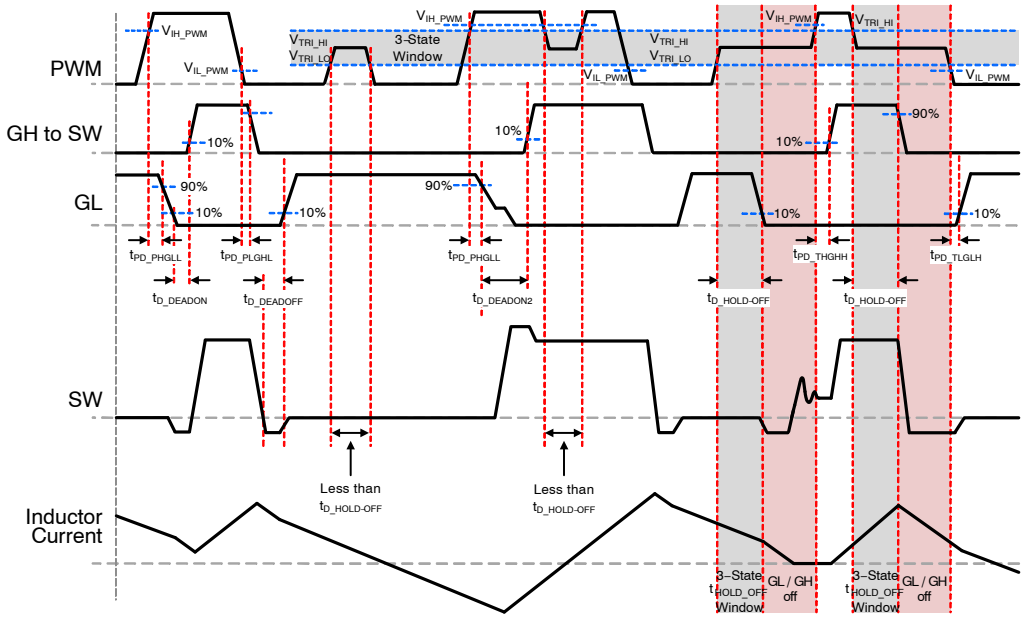
As noted in the CCM2 Operation section, the low−side driver strength is scale−able upon detection of CCM2. CCM2 feature slows the charge and discharge of the low−side MOSFET gate to minimize peak switching voltage overshoots during low−side MOSFET hardswitching (negative inductor current). To avoid cross−conduction, the slowing of the low−side gate also requires an adjustment (increase) of the dead time between low−side MOSFET off to high−side MOSFET on. A fairly long fixed dead time (t_{FD_ON2}) is implemented to ensure there is no cross conduction during this CCM2 operation.

High−Side MOSFET Off to Low−Side MOSFET On Dead Time in CCM1 / DCM

To get very short dead time during high−side MOSFET off to low−side MOSFET on transition, a fixed dead time method is implemented in the SPS gate driver. The fixed−dead−time circuitry monitors the internal HS signal and adds a fixed delay long enough to gate on GL after a desired $t_{D_DEADOFF}$ (~5 ns, $t_{D_DEADOFF} = t_{FD_OFF1}$) regardless of SW node state.

Exiting 3−State Condition

When exiting a valid 3−state condition, the gate driver of the FDMF5833 follows the PWM input command. If the PWM input goes from 3−state to LOW, the low−side MOSFET is turned on. If the PWM input goes from 3− state to HIGH, the high−side MOSFET is turned on. This is illustrated in Figure 31 below.



NOTES:

t_{PD_XXX} = propagation delay from external signal (PWM, ZCD#, etc.) to IC generated signal. Example : t_{PD_PHGLL} – PWM going HIGH to low−side MOSFET V_{GS} (GL) going LOW
t_{D_XXX} = delay from IC generated signal to IC generated signal. Example : t_{D_DEADON} – low−side MOSFET V_{GS} LOW to high−side MOSFET V_{GS} HIGH

PWM
t_{PD_PHGLL} = PWM rise to LS V_{GS} fall, V_{IH_PWM} to 90% LS V_{GS}
t_{PD_PLGHL} = PWM fall to HS V_{GS} fall, V_{IL_PWM} to 90% HS V_{GS}
t_{PD_PHGHH} = PWM rise to HS V_{GS} rise, V_{IH_PWM} to 10% HS V_{GS} (ZCD# held LOW)

ZCD#
t_{PD_ZLGLL} = ZCD# fall to LS V_{GS} fall, $V_{IL_ZCD\#}$ to 90% LS V_{GS}
t_{PD_ZHGLH} = ZCD# rise to LS V_{GS} rise, $V_{IH_ZCD\#}$ to 10% LS V_{GS}

Exiting 3−State
t_{PD_TSGHH} = PWM 3−State to HIGH to HS V_{GS} rise, V_{IH_PWM} to 10% HS V_{GS}
t_{PD_TSGLH} = PWM 3−State to LOW to LS V_{GS} rise, V_{IL_PWM} to 10% LS V_{GS}

Dead Times
t_{D_DEADON} = LS V_{GS} fall to HS V_{GS} rise, LS−Comp trip value to 10% HS V_{GS}
$t_{D_DEADOFF}$ = SW fall to LS V_{GS} rise, SW−Comp trip value to 10% LS V_{GS}

Figure 31. PWM HIGH / LOW / 3−State Timing Diagram

Exiting 3−State with Low BOOT−SW Voltage

The SPS module is used in multi−phase VR topologies requiring the module to wait in 3−state condition for an indefinite time. These long idle times can bleed the boot capacitor down until eventual clamping occurs based on PV_{CC} and V_{OUT}. Low BOOT−SW can cause increased propagation delays in the level−shift circuit as well as all HDRV floating circuitry, which is biased from the BOOT−SW rail. Another issue with a depleted BOOT−SW capacitor voltage is the voltage applied to the HS MOSFET gate during turn−on. A low BOOT−SW voltage results in a very weak HS gate drive, hence, much larger HS $R_{DS(ON)}$ and increased risk for unreliable operation since the HS MOSFET may not turn−on if BOOT−SW falls too low.

To address this issue, the SPS monitors for a low BOOT−SW voltage when the module is in 3−state condition. When the module exits 3−state condition with a low BOOT−SW voltage, a 100 ns minimum GL on time is output regardless of the PWM input. This ensures the boot capacitor is adequately charged to a safe operating level and has minimal impact on transient response of the system. Scenarios of exiting 3−state condition are listed below.

- If the part exits 3−state with a low BOOT−SW voltage condition and the controller commands PWM=HIGH, the SPS outputs a 100 ns GL pulse and follows the PWM=HIGH command (see Figure 32).
- If the part exits 3−state with a low BOOT−SW voltage condition and the controller commands PWM=LOW for 100 ns or more, the SPS follows the PWM input. If PWM=LOW for less than 100 ns, GL remains on for 100 ns then follows the PWM input (see Figure 33 and Figure 34).

- If no low BOOT−SW condition is detected, the SPS follows the PWM command when exiting 3−state (see Figure 35).

The SPS momentarily stays in an adaptive dead time mode when exiting 3−state condition or at initial power−up. This adaptive dead time mode lasts for no more than two (2) consecutive switching cycles, giving the boot capacitor ample time to recharge to a safe level. The module switches back to fixed dead time control for maximum efficiency.

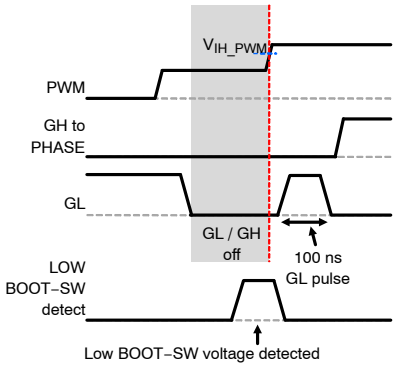


Figure 32. Low BOOT−SW Voltage Detected and PWM from 3−State to HIGH

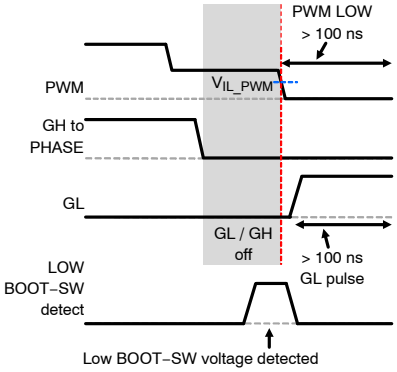


Figure 33. Low BOOT−SW Voltage Detected and PWM from 3−State to LOW for more than 100 ns

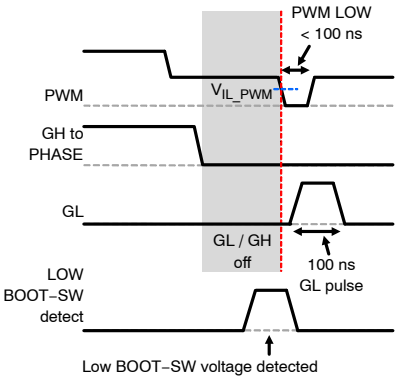


Figure 34. Low BOOT−SW voltage Detected and PWM from 3−State to LOW for Less than 100 ns

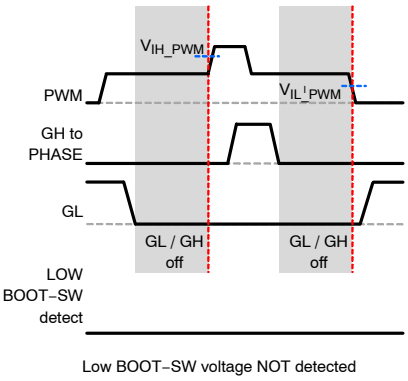


Figure 35. Low BOOT−SW Voltage NOT Detected and PWM from 3−State to HIGH or LOW

Zero Cross Detect (ZCD) Operation

The ZCD control block houses the circuitry that determines when the inductor current reverses direction and controls when to turn off the low−side MOSFET. A low offset comparator monitors the SW−to−PGND voltage of the low−side MOSFET during the LS MOSFET on−time. When the sensed voltage switches polarity from negative to positive, the comparator changes state and reverse current has been detected. This comparator offset must sense the negative V_{SW} within a 0.5 mV worst−case range. The negative offset is to ensure the inductor current never reverses; some small body−diode conduction is preferable to having negative current.

The comparator is switched on after the rising edge of the low−side gate drive and turned off by the signal at the input to the low−side gate driver. In this way, the zero−current comparator is connected with a break−before−make connection, allowing the comparator to be designed with all low−voltage transistors.

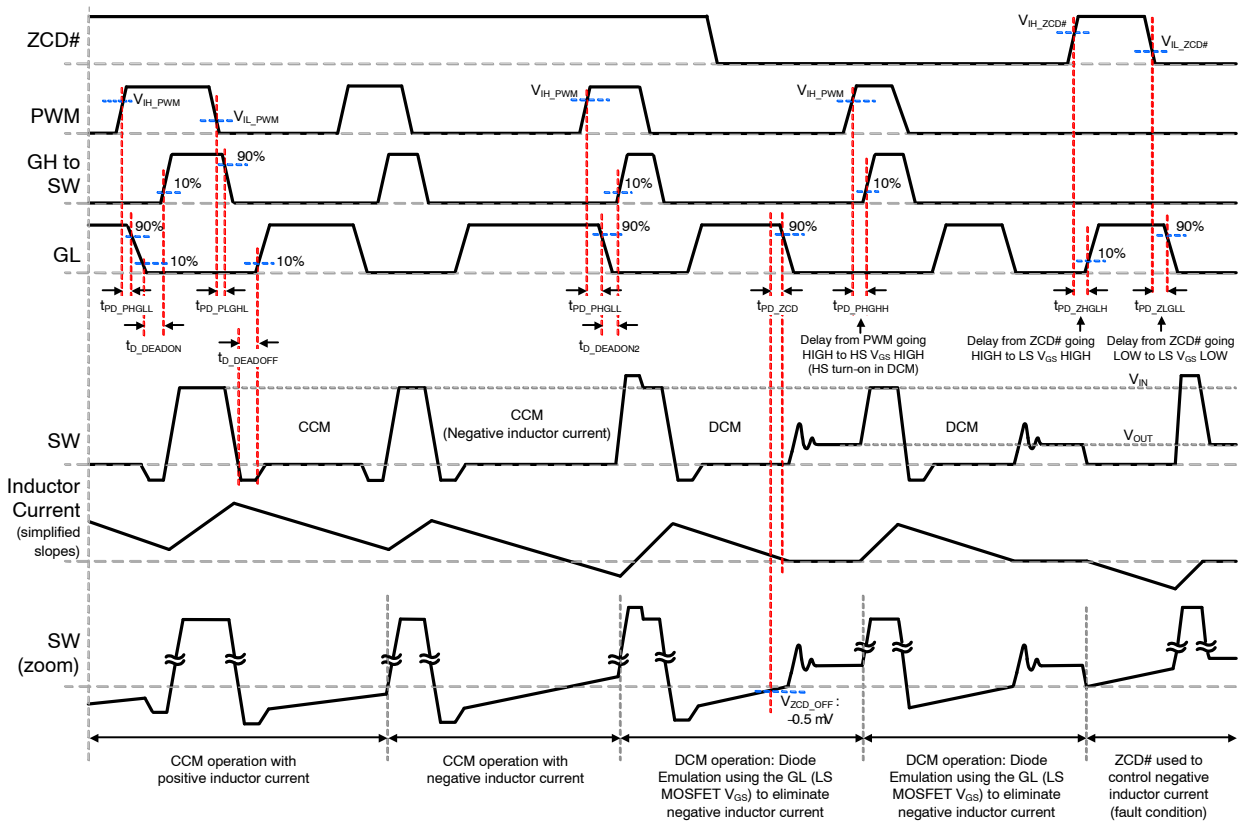


Figure 36. FZCD# & PWM Timing Diagram

Thermal Warning Flag (THWN#)

The FDMF5833 provides a thermal warning (THWN) for over−temperature conditions. The THWN flag pulls THWN# pin LOW (to AGND) if the driver IC detects the 125°C activation temperature. The THWN# pin output returns to high−impedance state once the temperature falls to the 110°C reset temperature. Figure 37 shows the THWN# operation. THWN does not disable the SPS module and works independently of other features.

The THWN mode of operation requires a pull−up resistor to V_{CC} rail. THWN# flag is active LOW.

Thermal Shutdown (THDN)

A programmed thermal shutdown engages once the driver TJ reaches 150°C. The shutdown event is a latched shut down, where the THDN signal clocks the fault latch and physically pulls down the EN pin.

Recycling 5 V V_{CC} (POR event) is required to re−enable the driver IC.

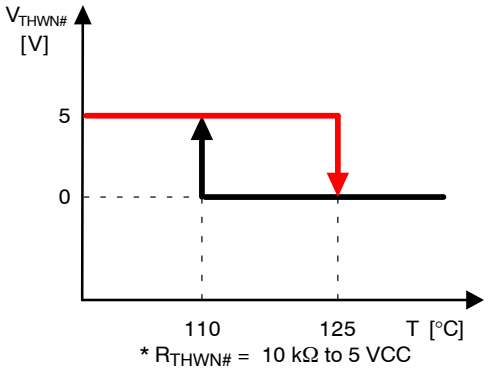


Figure 37. Gate Driver T_J vs. $V_{THWN\#}$

The 150°C THDN feature is combined with a 125°C THWN# flag. If the driver temperature reaches 125°C, the THWN# pin is pulled LOW. If the driver continues operation and its temperature increases up to 150°C, thermal shutdown is activated. The SPS module is shut down by EN LOW and the THWN# flag is de−asserted, so the $V_{THWN\#}$ returns HIGH. Figure 38 shows the relationship among THWN#, EN, and driver temperature.

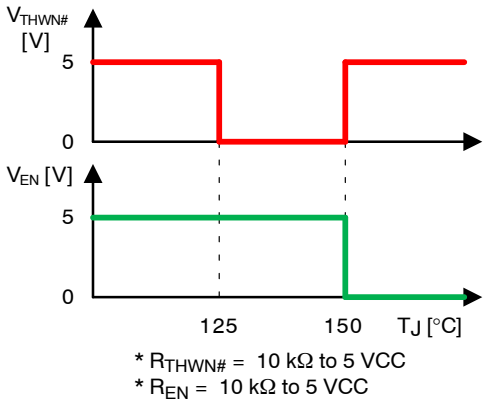


Figure 38. $V_{THWN\#}$, V_{EN} vs. Driver Temperature

Catastrophic Fault

SPS FDMF5833 includes a catastrophic fault feature. If a HS MOSFET short is detected, the driver internally pulls the EN / FAULT# pin LOW and shuts down the SPS driver. The intention is to implement a basic circuit to test the HS MOSFET short by monitoring LDRV and the state of SW node.

If a HS short fault is detected, the SPS module clocks the fault latch shutting down the module. The module requires a V_{CC} POR event to restart.

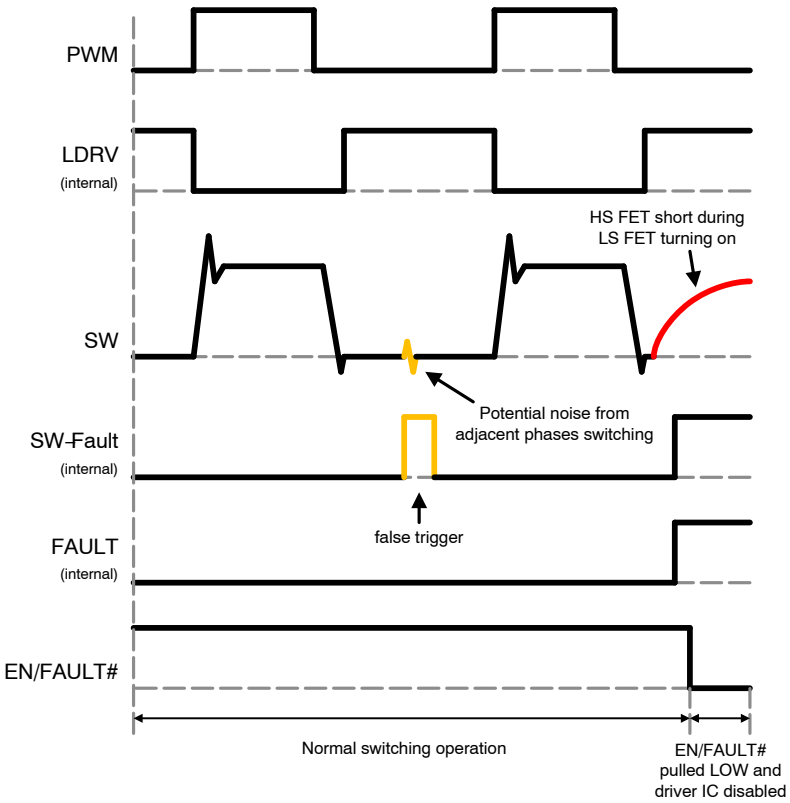


Figure 39. Catastrophic Fault Waveform

APPLICATION INFORMATION

Decoupling Capacitor for PVCC & VCC

For the supply inputs (PVCC and VCC pins), local decoupling capacitors are required to supply the peak driving current and to reduce noise during switching operation. Use at least 0.68 ~ 1 μF / 0402 ~ 0603 / X5R

~ X7R multi−layer ceramic capacitors for both power rails. Keep these capacitors close to the PVCC and VCC pins and PGND and AGND copper planes. If they need to be located on the bottom side of board, put through−hole vias on each pads of the decoupling capacitors to connect the capacitor pads on bottom with PVCC and VCC pins on top.

The supply voltage range on PVCC and VCC is 4.5 V ~ 5.5 V, and typically 5 V for normal applications.

R−C Filter on VCC

The PVCC pin provides power to the gate drive of the high−side and low−side power MOSFETs. In most cases, PVCC can be connected directly to VCC, which is the pin that provides power to the analog and logic blocks of the driver. To avoid switching noise injection from PVCC into VCC, a filter resistor can be inserted between PVCC and VCC decoupling capacitors.

Recommended filter resistor value range is 0 ~ 10 Ω, typically 0 Ω for most applications.

Bootstrap Circuit

The bootstrap circuit uses a charge storage capacitor (CBOOT). A bootstrap capacitor of 0.1 ~ 0.22 μF / 0402 ~ 0603 / X5R ~ X7R is usually appropriate for most switching applications. A series bootstrap resistor may be needed for specific applications to lower high−side MOSFET switching speed. The boot resistor is required when the SPS is switching above 15 V VIN; when it is effective at controlling VSW overshoot. R_{BOOT} value from zero to 6 Ω is typically recommended to reduce excessive voltage spike and ringing on the SW node. A higher R_{BOOT} value can cause lower efficiency due to high switching loss of high−side MOSFET.

Do not add a capacitor or resistor between the BOOT pin and GND.

EN / FAULT# (Input / Output)

The driver in SPS is enabled by pulling the EN pin HIGH. The EN pin has internal 250 kΩ pull−down resistor, so it needs to be pulled−up to V_{CC} with an external resistor or connected to the controller or system to follow up the command from them. If the EN pin is floated, it cannot turn on the driver.

The fault flag LOW signal is asserted on the EN / FAULT# pin when the driver temperature reaches THDN temperature or a high−side MOSFET fault occurs. Then the driver shuts down.

The typical pull−up resistor value on EN ~ VCC is 10 kΩ. Do not add a noise filter capacitor on the EN pin.

PWM (Input)

The PWM pin recognizes three different logic levels from PWM controller: HIGH, LOW, and 3−state. When the PWM pin receives a HIGH command, the gate driver turns on the high−side MOSFET. When the PWM pin receives a LOW command, the gate driver turns on the low−side MOSFET. When the PWM pin receives a voltage signal inside of the 3−state window (V_{TRI_Window}) and exceeds the 3−state hold−off time, the gate driver turns off both high−side and low−side MOSFETs. To recognize the high−impedance 3−state signal from the controller, the PWM pin has an internal resistor divider from VCC to PWM to AGND. The resistor divider sets a voltage level on the PWM pin inside the 3−state window when the PWM signal from the controller is high−impedance.

ZCD# (Input)

When the ZCD# pin sets HIGH, the ZCD function is disabled and high−side and low−side MOSFETs switch in CCM (or FCCM, Forced CCM) by PWM signal. When the ZCD# pin is LOW, the low−side MOSFET turns off when the SPS driver detects negative inductor current during the low−side MOSFET turn−on period. This ZCD feature allows higher converter efficiency under light− load condition and PFM / DCM operation.

The ZCD# pin has an internal current source from VCC, so it may not need an external pull−up resistor. Once V_{CC} is supplied and the driver is enabled, the ZCD# pin holds logic HIGH without external components and the driver operates switching in CCM or FCCM. The ZCD# pin can be grounded for automatic diode emulation in DCM by the SPS itself, or it can be connected to the controller or system to follow the command from them.

The typical pull−up resistor value on ZCD# ~ VCC is 10 kΩ for stable ZCD# HIGH level. If not using the ZCD feature, tie the ZCD# pin to VCC with a pull−up resistor. Do not add any noise filter capacitor on the ZCD# pin.

THWN# (Output) / THDN

The THWN# pin is an open−drain, so needs an external pull−up resistor to VCC. If the driver temperature reaches 125°C, the $V_{THWN\#}$ is pulled LOW. When the driver T_J cools to less than 110°C, the $V_{THWN\#}$ returns HIGH. This THWN# flag operates when the driver T_J is below 150°C.

If the driver T_J continuously increases over 150°C after asserting the 125°C THWN flag, the thermal shutdown feature activates and the SPS module is turned off. This shutdown is a latch function, so the driver remains shut down even if its temperature cools down to 25°C. The SPS module needs to be re−enabled by V_{CC} POR once the THDN is activated.

A typical pull−up resistor on THWN# ~ VCC is 10 kΩ. If not using THWN#/THDN features, tie THWN# to GND. Do not add a noise filter capacitor on the THWN# pin.

Power Loss and Efficiency

Figure 40 shows an example diagram for power loss and efficiency measurement.

Power loss calculation and equation examples:

$P_{IN} = (V_{IN} * I_{IN}) + (V_{CC} * I_{CC})$ [W]

$P_{SW} = V_{SW} * I_{OUT}$ [W]

$P_{OUT} = V_{OUT} * I_{OUT}$ [W]

$P_{LOSS_MODULE} = P_{IN} - P_{SW}$ [W]

$P_{LOSS_TOTAL} = P_{IN} - P_{OUT}$ [W]

$EFFI_{MODULE} = (P_{SW} / P_{IN}) * 100$ [%]

$EFFI_{TOTAL} = (P_{OUT} / P_{IN}) * 100$ [%]

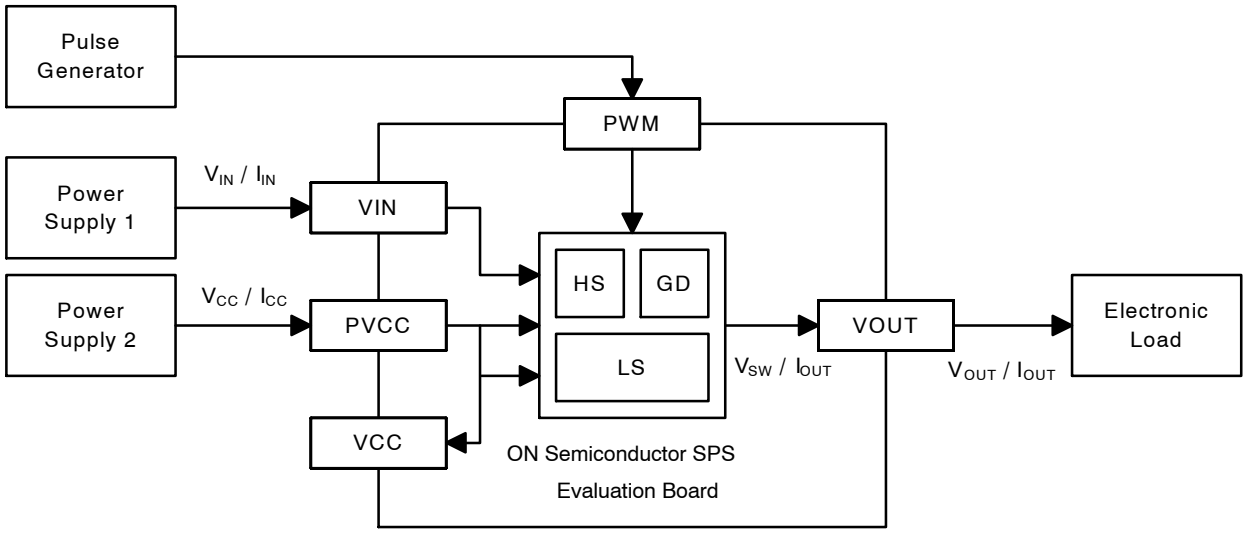


Figure 40. Power Loss and Efficiency Measurement Diagram

PCB LAYOUT GUIDELINE

Figure 41 through Figure 44 provide examples of single−phase and multi−phase layouts for the FDMF5833 and critical components. All of the high−current paths; such as VIN, SW, VOUT, and GND coppers; should be short and wide for low parasitic inductance and resistance. This helps achieve a more stable and evenly distributed current flow, along with enhanced heat radiation and system performance.

Input ceramic bypass capacitors must be close to the VIN and PGND pins. This reduces the high−current power loop inductance and the input current ripple induced by the power MOSFET switching operation.

The SW copper trace serves two purposes. In addition to being the high−frequency current path from the SPS package to the output inductor, it serves as a heat sink for the low−side MOSFET. The trace should be short and wide enough to present a low−impedance path for the high−frequency, high−current flow between the SPS and the inductor. The short and wide trace minimizes electrical losses and SPS temperature rise. The SW node is a high−voltage and high−frequency switching node with high noise potential. Care should be taken to minimize coupling to adjacent traces. Since this copper trace acts as a heat sink for the low−side MOSFET, balance using the largest area possible to improve SPS cooling while maintaining acceptable noise emission.

An output inductor should be located close to the FDMF5833 to minimize the power loss due to the SW copper trace. Care should also be taken so the inductor dissipation does not heat the SPS.

POWERTRENCH MOSFETs are used in the output stage and are effective at minimizing ringing due to fast switching. In most cases, no RC snubber on SW node is required. If a snubber is used, it should be placed close to the SW and PGND pins. The resistor and capacitor of the snubber must be sized properly to not generate excessive heating due to high power dissipation.

Decoupling capacitors on PVCC, VCC, and BOOT capacitors should be placed as close as possible to the PVCC ~ PGND, VCC ~ AGND, and BOOT ~ PHASE pin

pairs to ensure clean and stable power supply. Their routing traces should be wide and short to minimize parasitic PCB resistance and inductance.

The board layout should include a placeholder for small−value series boot resistor on BOOT ~ PHASE. The boot−loop size, including series R_{BOOT} and C_{BOOT}, should be as small as possible.

A boot resistor may be required when the SPS is operating above 15 V V_{IN} and it is effective to control the high−side MOSFET turn−on slew rate and SW voltage overshoot. R_{BOOT} can improve noise operating margin in synchronous buck designs that may have noise issues due to ground

bounce or high positive and negative V_{SW} ringing. Inserting a boot resistance lowers the SPS module efficiency. Efficiency versus switching noise must be considered. R_{BOOT} values from 0.5 Ω to 0.6 Ω are typically effective in reducing V_{SW} overshoot.

The VIN and PGND pins handle large current transients with frequency components greater than 100 MHz. If possible, these pins should be connected directly to the VIN and board GND planes. The use of thermal relief traces in series with these pins is not recommended since this adds extra parasitic inductance to the power path. This added inductance in series with either the VIN or PGND pin degrades system noise immunity by increasing positive and negative V_{SW} ringing.

PGND pad and pins should be connected to the GND copper plane with multiple vias for stable grounding. Poor grounding can create a noisy and transient offset voltage level between PGND and AGND. This could lead to faulty operation of gate driver and MOSFETs.

Ringing at the BOOT pin is most effectively controlled by close placement of the boot capacitor. Do not add any additional capacitors between BOOT to PGND. This may lead to excess current flow through the BOOT diode, causing high power dissipation.

The ZCD# and EN pins have weak internal pull−up and pull−down current sources, respectively. These pins should not have any noise filter capacitors. Do not float these pins unless absolutely necessary.

Put multiple vias on the VIN and VOUT copper areas to interconnect top, inner, and bottom layers to evenly distribute current flow and heat conduction. Do not put too many vias on the SW copper to avoid extra parasitic inductance and noise on the switching waveform. As long as efficiency and thermal performance are acceptable, place only one SW node copper on the top layer and put no vias on the SW copper to minimize switch node parasitic noise. Vias should be relatively large and of reasonably low inductance. Critical high−frequency components; such as R_{BOOT}, C_{BOOT}, RC snubber, and bypass capacitors; should be located as close to the respective SPS module pins as possible on the top layer of the PCB. If this is not feasible, they can be placed on the board bottom side and their pins connected from bottom to top through a network of low−inductance vias.

PCB LAYOUT GUIDELINE

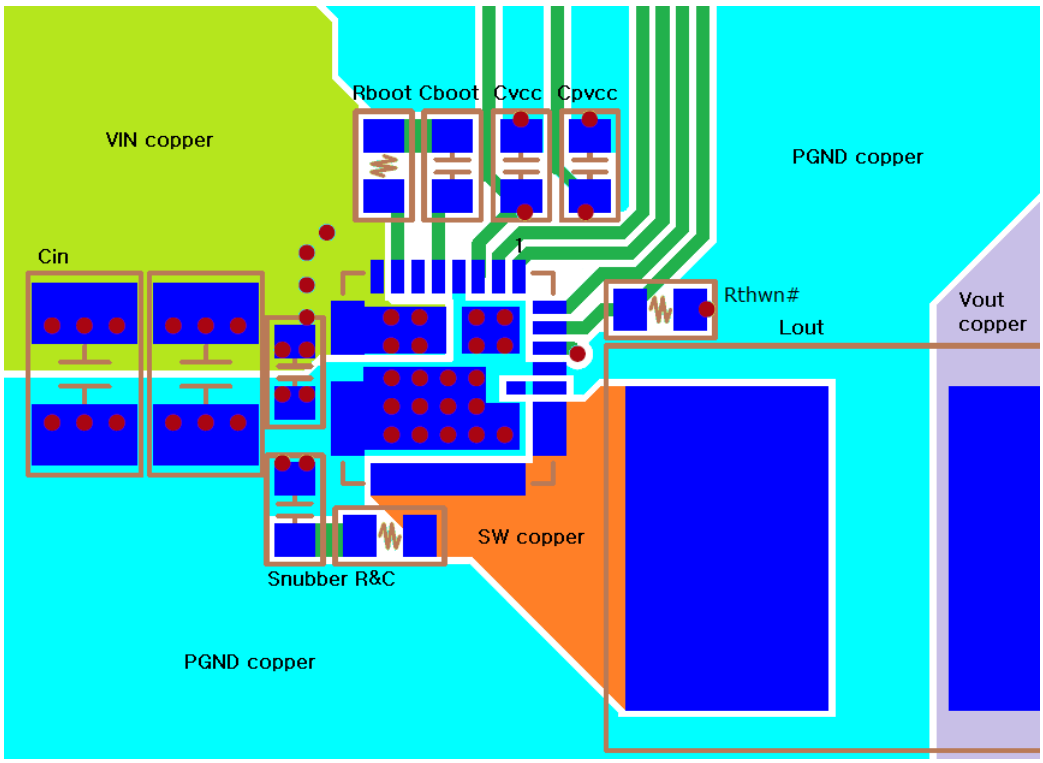


Figure 41. Single−Phase Board Layout Example – Top View

PCB LAYOUT GUIDELINE (continued)

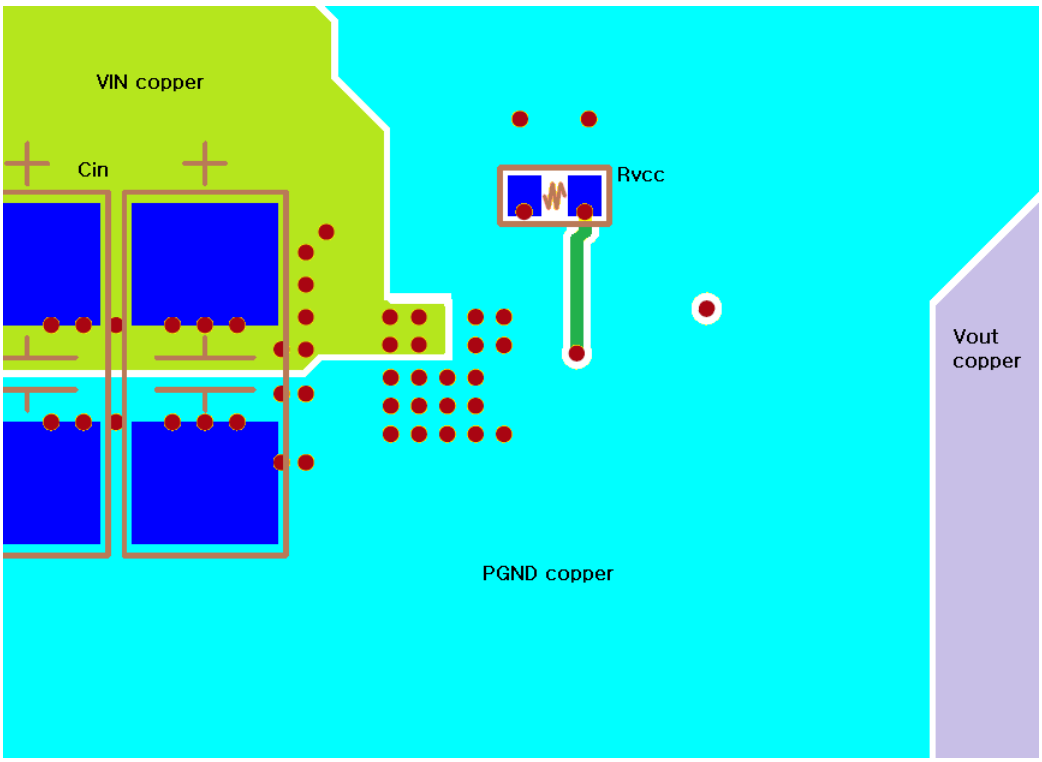


Figure 42. Single−Phase Board Layout Example – Bottom View (Mirrored)

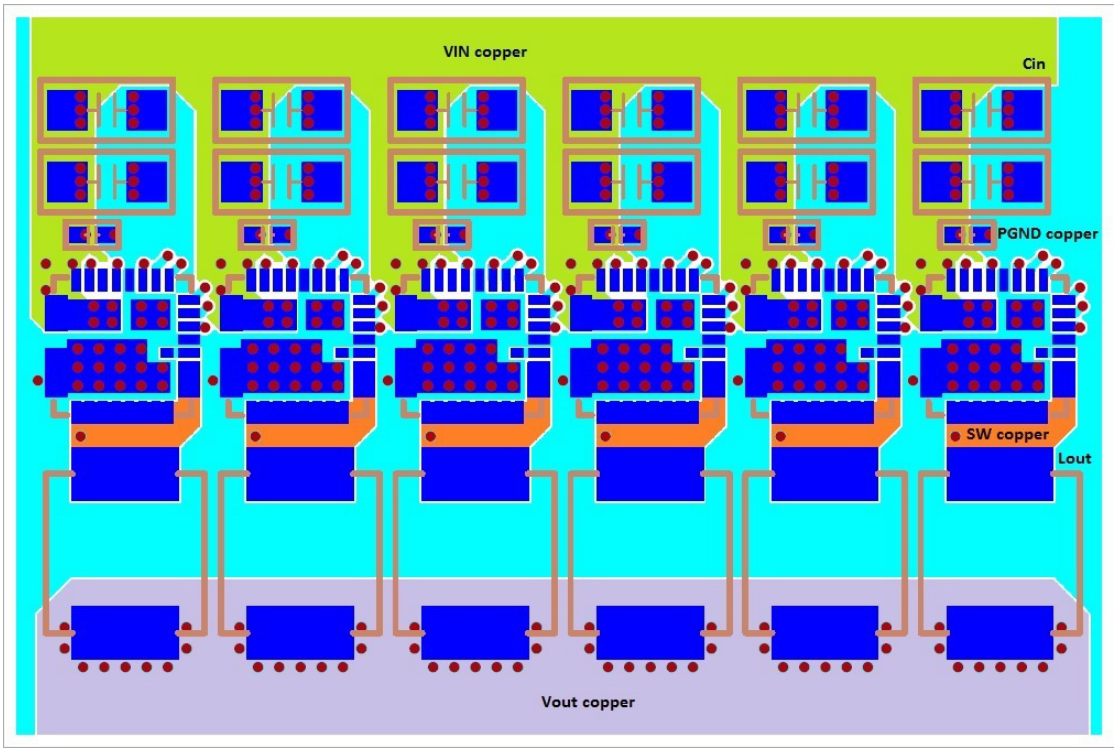


Figure 43. 6−Phase Board Layout Example with 6 mm x 6 mm Inductor – Top View

PCB LAYOUT GUIDELINE (continued)

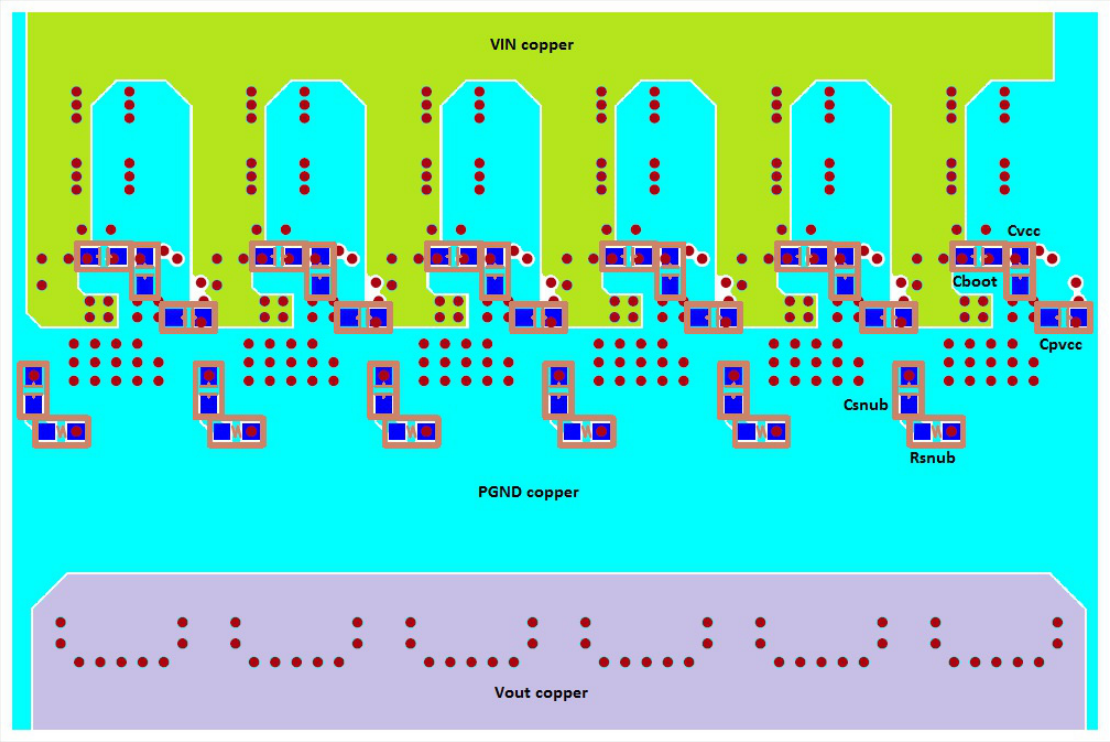


Figure 44. 6−Phase Board Layout Example with 6 mm x 6 mm Inductor – Bottom View (Mirrored)

PACKAGE MARKING AND ORDERING INFORMATION

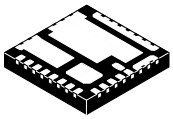
Part Number	Top Marking	Current Rating	Package	Shipping (Qty / Packing)†
FDMF5833	5833	50 A	31−Lead, Clip Bond PQFN31 5x5, 0.5P (Pb−Free/Halogen Free)	3000 / Tape & Reel
FDMF5833−F085	5833 F085	50 A	31−Lead, Clip Bond PQFN31 5x5, 0.5P (Pb−Free/Halogen Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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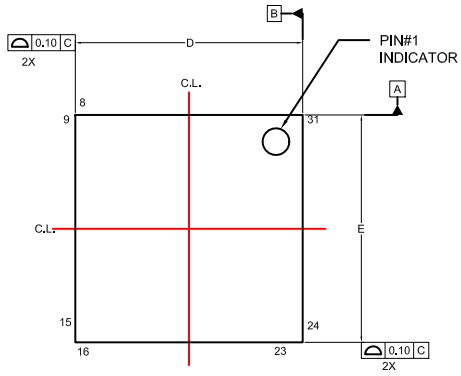
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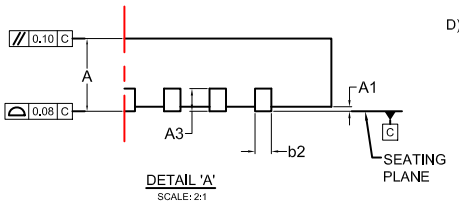
PQFN31 5X5, 0.5P
CASE 483BR
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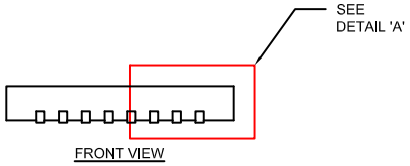
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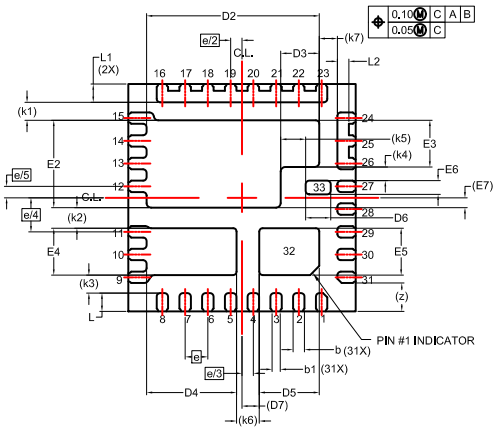
TOP VIEW



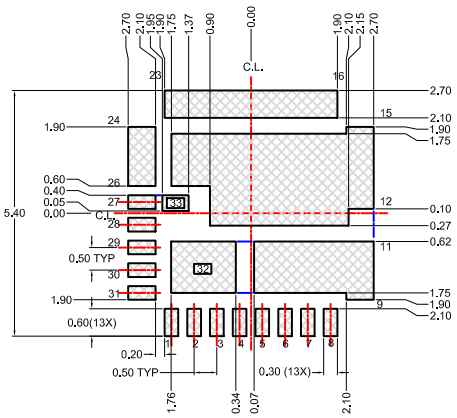
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FRONT VIEW



BOTTOM VIEW



LAND PATTERN
RECOMMENDATION

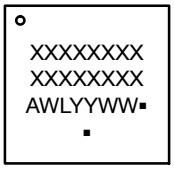
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B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE BURRS AND SMEAR OR MOLD FLASH. MOLD FLASH OR BURRS AND SMEAR DOES NOT EXCEED 0.10MM.
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3	0.20	0.25	0.30
b	0.20	0.25	0.30
b1	0.13	0.18	0.30
b2	0.13	0.18	0.30
D	4.90	5.00	5.10
D2	3.70	3.80	3.90
D3	0.75	0.85	0.95
D4	1.88	1.98	2.08
D5	1.22	1.32	1.42
D6	0.45	0.55	0.65
D7	0.38 REF		
E	4.90	5.00	5.10
E2	1.82	1.92	2.02
E3	0.93	1.03	1.13
E4	0.93	1.03	1.13
E5	0.93	1.03	1.13
E6	0.20	0.30	0.40
E7	0.22 REF		
e	0.50 BSC		
e/2	0.25 BSC		
e/3	0.25 BSC		
e/4	0.75 BSC		
e/5	0.25 BSC		
k1	0.40 REF		
k2	0.45 REF		
k3	0.40 REF		
k4	0.30 REF		
k5	0.55 REF		
k6	0.50 REF		
k7	0.40 REF		
L	0.30	0.40	0.50
L1	0.30	0.40	0.50
L2	0.15	0.25	0.35
z	0.625 REF		

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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