ON Semiconductor®

FDMA1023PZ

Dual P-Channel PowerTrench® MOSFET

–20V, –3.7A, 72mΩ

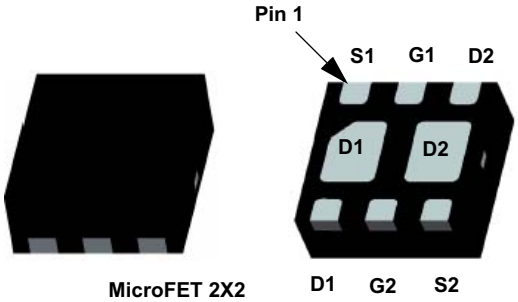
Features

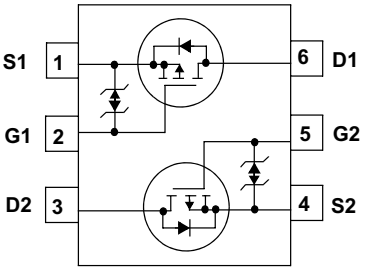
- Max $r_{DS(on)}$ = 72mΩ at V_{GS} = –4.5V, I_D = –3.7A
- Max $r_{DS(on)}$ = 95mΩ at V_{GS} = –2.5V, I_D = –3.2A
- Max $r_{DS(on)}$ = 130mΩ at V_{GS} = –1.8V, I_D = –2.0A
- Max $r_{DS(on)}$ = 195mΩ at V_{GS} = –1.5V, I_D = –1.0A
- Low profile - 0.8 mm maximum - in the new package MicroFET 2x2 mm
- HBM ESD protection level > 2kV typical (Note 3)
- RoHS Compliant
- Free from halogenated compounds and antimony oxides

General Description

This device is designed specifically as a single package solution for the battery charge switch in cellular handset and other ultra-portable applications. It features two independent P-Channel MOSFETs with low on-state resistance for minimum conduction losses. When connected in the typical common source configuration, bi-directional current flow is possible.

The MicroFET 2X2 package offers exceptional thermal performance for its physical size and is well suited to linear mode applications.





MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DS}	Drain to Source Voltage		–20	V
V_{GS}	Gate to Source Voltage		±8	V
I_D	Drain Current -Continuous	(Note 1a)	–3.7	A
	-Pulsed		–6	
P_D	Power Dissipation	(Note 1a)	1.5	W
		(Note 1b)	0.7	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance for Single Operation, Junction to Ambient	(Note 1a)	86	°C/W
$R_{\theta JA}$	Thermal Resistance for Single Operation, Junction to Ambient	(Note 1b)	173	
$R_{\theta JA}$	Thermal Resistance for Dual Operation, Junction to Ambient	(Note 1c)	69	
$R_{\theta JA}$	Thermal Resistance for Dual Operation, Junction to Ambient	(Note 1d)	151	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
023	FDMA1023PZ	MicroFET 2X2	7”	8mm	3000 units

©2009 Semiconductor Components Industries, LLC.

Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = –250μA, V_{GS} = 0V	–20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = –250μA, referenced to 25°C		–11		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = –16V, V_{GS} = 0V			–1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±8V, V_{DS} = 0V			±10	μA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = –250μA	–0.4	–0.7	–1.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = –250μA, referenced to 25°C		2.5		mV/°C
$r_{DS(on)}$	Static Drain to Source On-Resistance	V_{GS} = –4.5V, I_D = –3.7A		60	72	mΩ
		V_{GS} = –2.5V, I_D = –3.2A		75	95	
		V_{GS} = –1.8V, I_D = –2.0A		100	130	
		V_{GS} = –1.5V, I_D = –1.0A		130	195	
		V_{GS} = –4.5V, I_D = –3.7A, T_J =125°C		81	91	
g_{FS}	Forward Transconductance	V_{DS} = –5V, I_D = –3.7A		12		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = –10V, V_{GS} = 0V, f = 1MHz		490	655	pF
C_{oss}	Output Capacitance			100	135	pF
C_{rss}	Reverse Transfer Capacitance			90	135	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = –10V, I_D = –1A, V_{GS} = –4.5V, R_{GEN} = 6Ω		9	18	ns
t_r	Rise Time			12	22	ns
$t_{d(off)}$	Turn-Off Delay Time			64	103	ns
t_f	Fall Time			37	60	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{DD} = –10V, I_D = –3.7A, V_{GS} = –4.5V		8.6	12	nC
Q_{gs}	Gate to Source Gate Charge			0.7		nC
Q_{gd}	Gate to Drain “Miller” Charge			2.0		nC
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Source-Drain Diode Forward Current				–1.1	A
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0V, I_S = –1.1A (Note 2)		–0.8	–1.2	V
t_{rr}	Reverse Recovery Time	I_F = –3.7A, di/dt = 100A/μs		32	48	ns
Q_{rr}	Reverse Recovery Charge			15	23	nC

Notes:

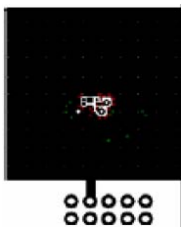
1: $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 oz. copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.

(a) $R_{\theta JA}$ = 86°C/W when mounted on a 1in^2 pad of 2 oz copper, 1.5" x 1.5" x 0.062" thick PCB. For single operation.

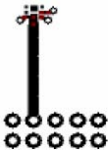
(b) $R_{\theta JA}$ = 173°C/W when mounted on a minimum pad of 2 oz copper. For single operation.

(c) $R_{\theta JA}$ = 69°C/W when mounted on a 1in^2 pad of 2 oz copper, 1.5" x 1.5" x 0.062" thick PCB, For dual operation.

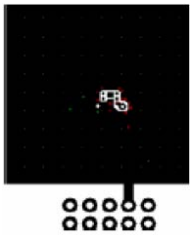
(d) $R_{\theta JA}$ = 151°C/W when mounted on a minimum pad of 2 oz copper. For dual operation.



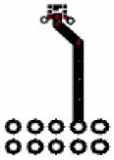
a) 86°C/W when mounted on a 1 in^2 pad of 2 oz copper.



b) 173°C/W when mounted on a minimum pad of 2 oz copper.



c) 69°C/W when mounted on a 1 in^2 pad of 2 oz copper.



d) 151°C/W when mounted on a minimum pad of 2 oz copper.

2: Pulse Test : Pulse Width < 300us, Duty Cycle < 2.0%

3: The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

Typical Characteristics T_J = 25°C unless otherwise noted

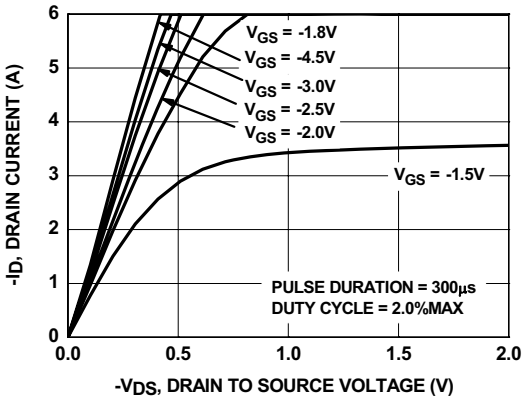


Figure 1. On Region Characteristics

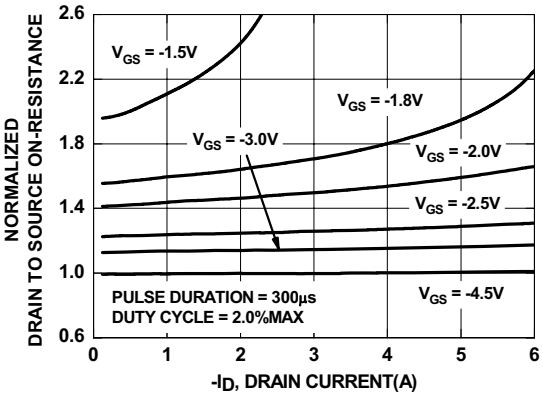


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

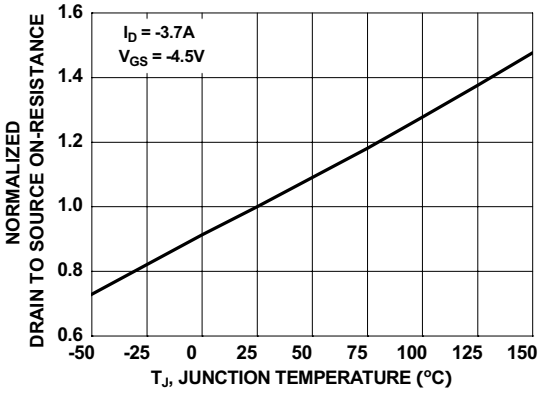


Figure 3. Normalized On-Resistance vs Junction Temperature

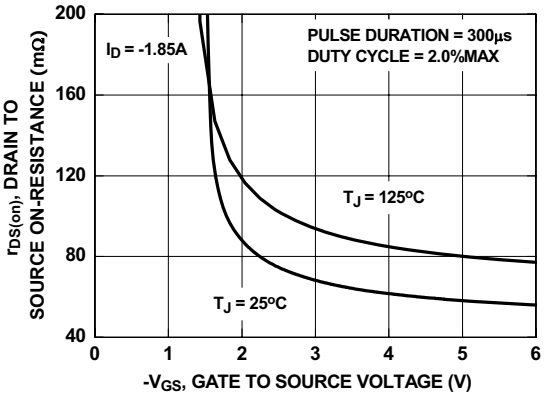


Figure 4. On-Resistance vs Gate to Source Voltage

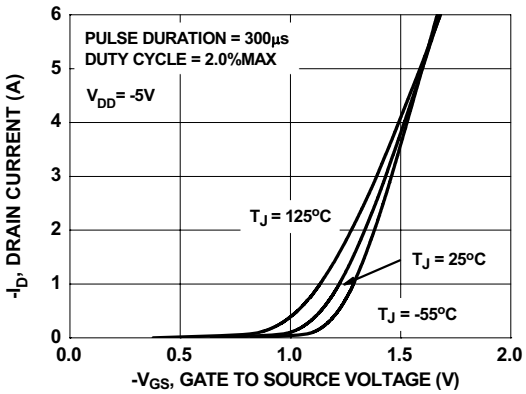


Figure 5. Transfer Characteristics

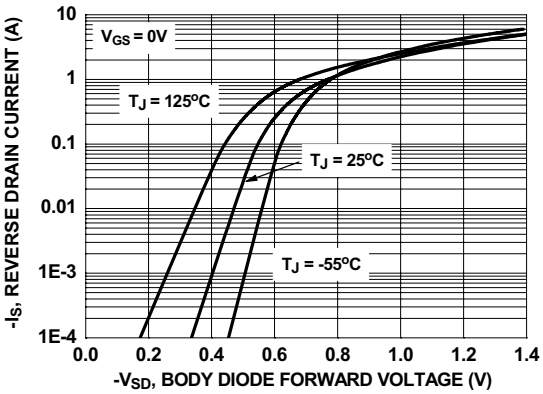


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25°C unless otherwise noted

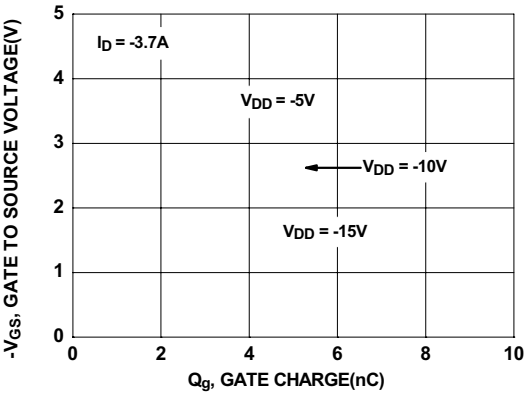


Figure 7. Gate Charge Characteristics

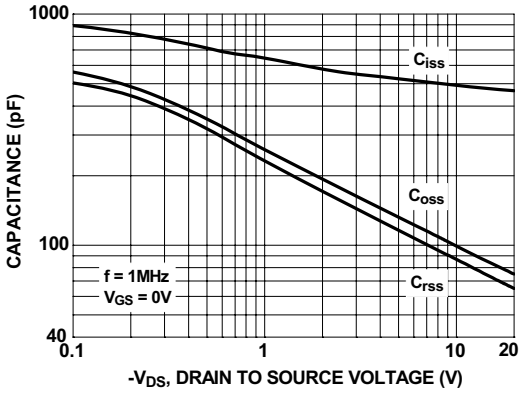


Figure 8. Capacitance Characteristics

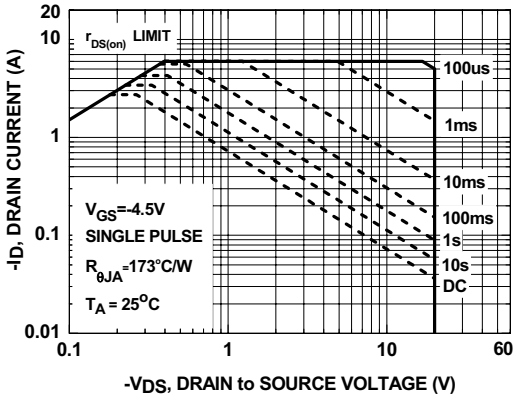


Figure 9. Forward Bias Safe Operating Area

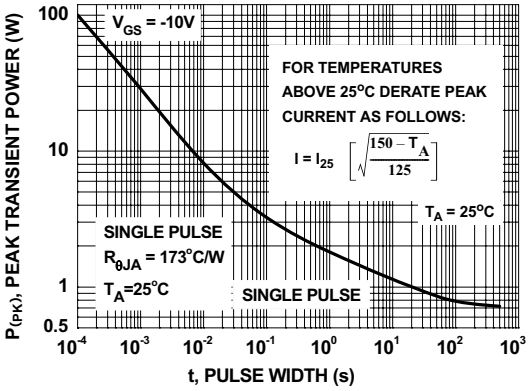


Figure 10. Single Pulse Maximum Power Dissipation

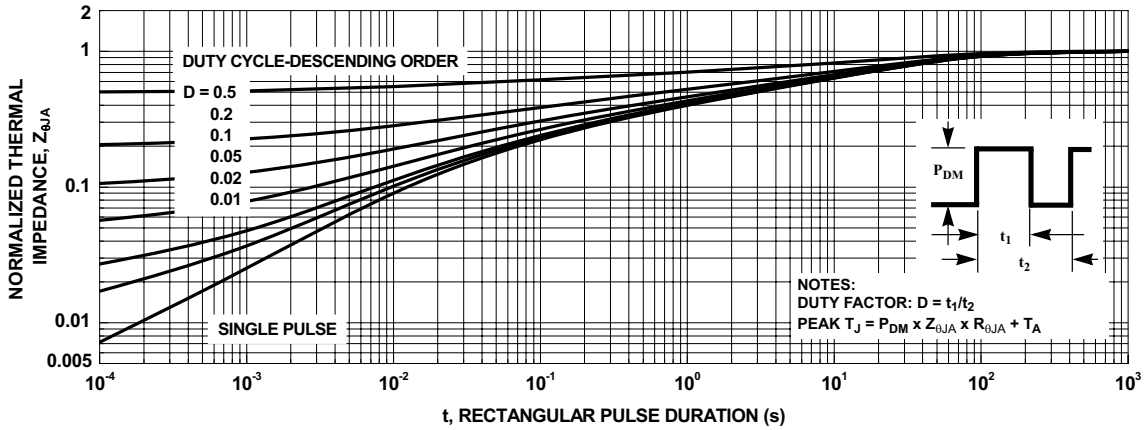
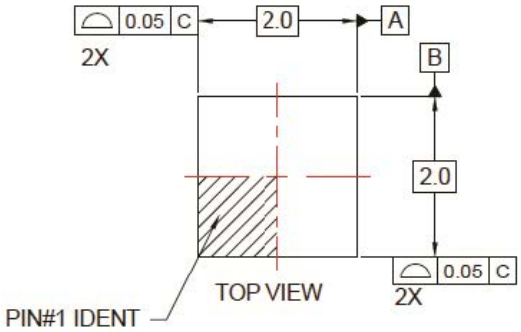
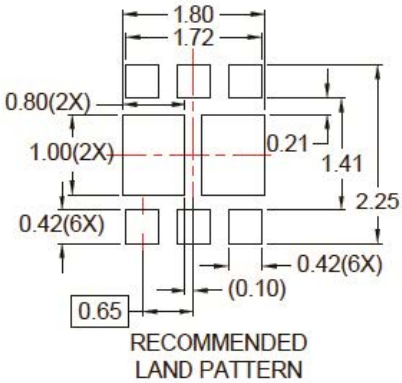
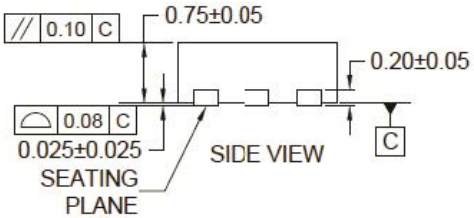


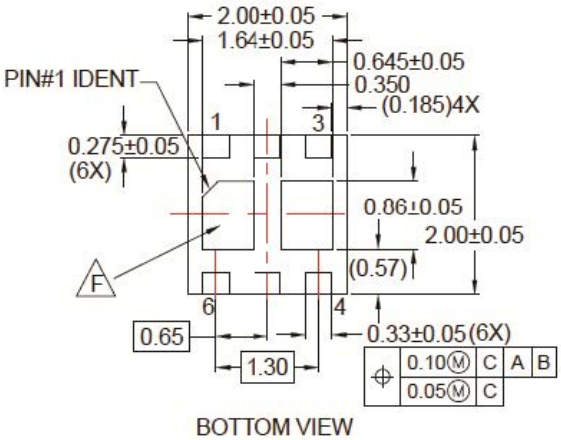
Figure 11. Transient Thermal Response Curve

Dimensional Outline and Pad Layout









NOTES:

A. CONFORM TO JADEC REGISTRATIONS MO-229, VARIATION VCCC, EXCEPT WHERE NOTED.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

E. DRAWING FILENAME: MKT-UMLP16Erev4

F. NON-JEDEC DUAL DAP

Package drawings are provided as a service to customers considering ON Semiconductor components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a ON Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of ON Semiconductor's worldwide terms and conditions, specifically the warranty therein, which covers ON Semiconductor products.

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative