FAIRCHILD SEMICONDUCTOR®

September 2008

FAN3121 / FAN3122
Single 9A High-Speed, Low-Side Gate Driver

Features

- Industry-Standard Pin-out with Enable Input
- 4.5 to 18V Operating Range
- 11.4A Peak Sink at V_{DD} = 12V
- 9.7A Sink / 7.1A Source at V_{OUT} = 6V
- Inverting Configuration (FAN3121) and Non-Inverting Configuration (FAN3122)
- Internal Resistors Turn Driver Off If No Inputs
- 23ns/19ns Typical Rise/Fall Times with 10nF Load
- 20ns Typical Propagation Delay Time
- Choice of TTL or CMOS Input Thresholds
- MillerDrive™ Technology
- Available in Thermally Enhanced 3x3mm 8-Lead MLP or 8-Lead SOIC Package (Pb-Free Finish)
- Rated from –40°C to +125°C

Applications

- Synchronous Rectifier Circuits
- High-Efficiency MOSFET Switching
- Switch-Mode Power Supplies
- DC-to-DC Converters
- Motor Control

Description

The FAN3121 and FAN3122 MOSFET drivers are designed to drive N-channel enhancement MOSFETs in low-side switching applications by providing high peak current pulses. The drivers are available with either TTL (FAN312xT) or CMOS (FAN312xC) input thresholds. Internal circuitry provides an under-voltage lockout function by holding the output low until the supply voltage is within the operating range.

FAN312x drivers incorporate the MillerDrive™ architecture for the final output stage. This bipolar / MOSFET combination provides the highest peak current during the Miller plateau stage of the MOSFET turn-on / turn-off process.

The FAN3121 and FAN3122 drivers implement an enable function on pin 3 (EN), previously unused in the industry-standard pin-out. The pin is internally pulled up to V_{DD} for active HIGH logic and can be left open for standard operation.

The FAN3121/22 is available in a 3x3mm 8-lead thermally-enhanced MLP package or an 8-lead SOIC package.

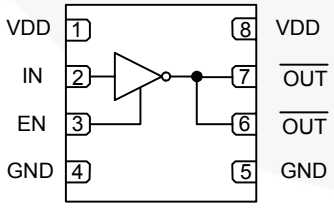


Figure 1. FAN3121 Pin Configuration

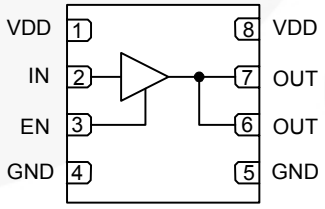


Figure 2. FAN3122 Pin Configuration

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Ordering Information

Part Number	Logic	Input Threshold	Package	Eco Status	Packing Method	Quantity per Reel
FAN3121CMPX	Inverting Channels + Enable	CMOS	3x3mm MLP-8	RoHS	Tape & Reel	3,000
FAN3121CMX			SOIC-8	RoHS	Tape & Reel	2,500
FAN3121TMPX		TTL	3x3mm MLP-8	RoHS	Tape & Reel	3,000
FAN3121TMX			SOIC-8	RoHS	Tape & Reel	2,500
FAN3122CMPX	Non-Inverting Channels + Enable	CMOS	3x3mm MLP-8	RoHS	Tape & Reel	3,000
FAN3122CMX			SOIC-8	RoHS	Tape & Reel	2,500
FAN3122TMPX		TTL	3x3mm MLP-8	RoHS	Tape & Reel	3,000
FAN3122TMX			SOIC-8	RoHS	Tape & Reel	2,500

For Fairchild's definition of "green" Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Package Outlines

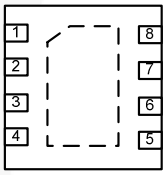


Figure 3. 3x3mm MLP-8 (Top View)

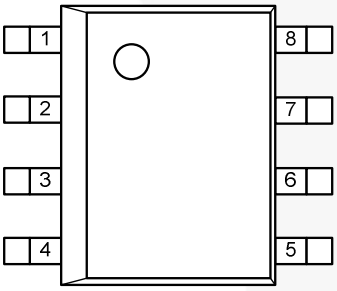


Figure 4. SOIC-8 (Top View)

Thermal Characteristics[1]

Package	Θ_{JL}[2]	Θ_{JT}[3]	Θ_{JA}[4]	Ψ_{JB}[5]	Ψ_{JT}[6]	Units
8-Lead 3x3mm Molded Leadless Package (MLP)	1.2	64	42	2.8	0.7	°C/W
8-Pin Small Outline Integrated Circuit (SOIC)	38	29	87	41	2.3	°C/W

Notes:

1. Estimates derived from thermal simulation; actual values depend on the application.
2. Theta_JL (Θ_{JL}): Thermal resistance between the semiconductor junction and the bottom surface of all the leads (including any thermal pad) that are typically soldered to a PCB.
3. Theta_JT (Θ_{JT}): Thermal resistance between the semiconductor junction and the top surface of the package, assuming it is held at a uniform temperature by a top-side heatsink.
4. Theta_JA (Θ_{JA}): Thermal resistance between junction and ambient, dependent on the PCB design, heat sinking, and airflow. The value given is for natural convection with no heatsink, as specified in JEDEC standards JESD51-2, JESD51-5, and JESD51-7, as appropriate.
5. Psi_JB (Ψ_{JB}): Thermal characterization parameter providing correlation between semiconductor junction temperature and an application circuit board reference point for the thermal environment defined in Note 4. For the MLP-8 package, the board reference is defined as the PCB copper connected to the thermal pad and protruding from either end of the package. For the SOIC-8 package, the board reference is defined as the PCB copper adjacent to pin 6.
6. Psi_JT (Ψ_{JT}): Thermal characterization parameter providing correlation between the semiconductor junction temperature and the center of the top of the package for the thermal environment defined in Note 4.

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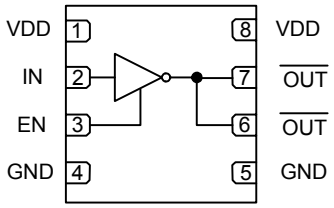


Figure 5. FAN3121 Pin Assignments (Repeated)

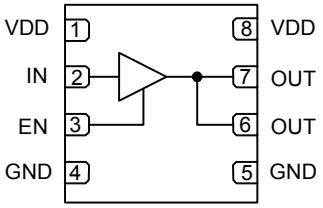


Figure 6. FAN3122 Pin Assignments (Repeated)

Pin Definitions

FAN3121	FAN3122	Name	Description
3	3	EN	**Enable Input**. Pull pin LOW to inhibit driver. EN has logic thresholds for both TTL and CMOS IN thresholds.
4, 5	4, 5	GND	**Ground**. Common ground reference for input and output circuits.
2	2	IN	**Input**.
	6, 7	OUT	**Gate Drive Output**. Held LOW unless required input is present and V_{DD} is above the UVLO threshold.
6, 7		$\overline{OUT}$	**Gate Drive Output** (inverted from the input). Held LOW unless required input is present and V_{DD} is above the UVLO threshold.
1, 8	1, 8	V_{DD}	**Supply Voltage**. Provides power to the IC.
		P1	**Thermal Pad (MLP only)**. Exposed metal on the bottom of the package; may be left floating or connected to GND; NOT suitable for carrying current.

Output Logic

FAN3121		
EN	**IN**	**$\overline{OUT}$**
0	0	0
0	1(7)	0
1(7)	0	1
1(7)	1(7)	0

FAN3122		
EN	**IN**	**OUT**
0	0(7)	0
0	1	0
1(7)	0(7)	0
1(7)	1	1

Note:

7. Default input signal if no external connection is made.

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Block Diagram

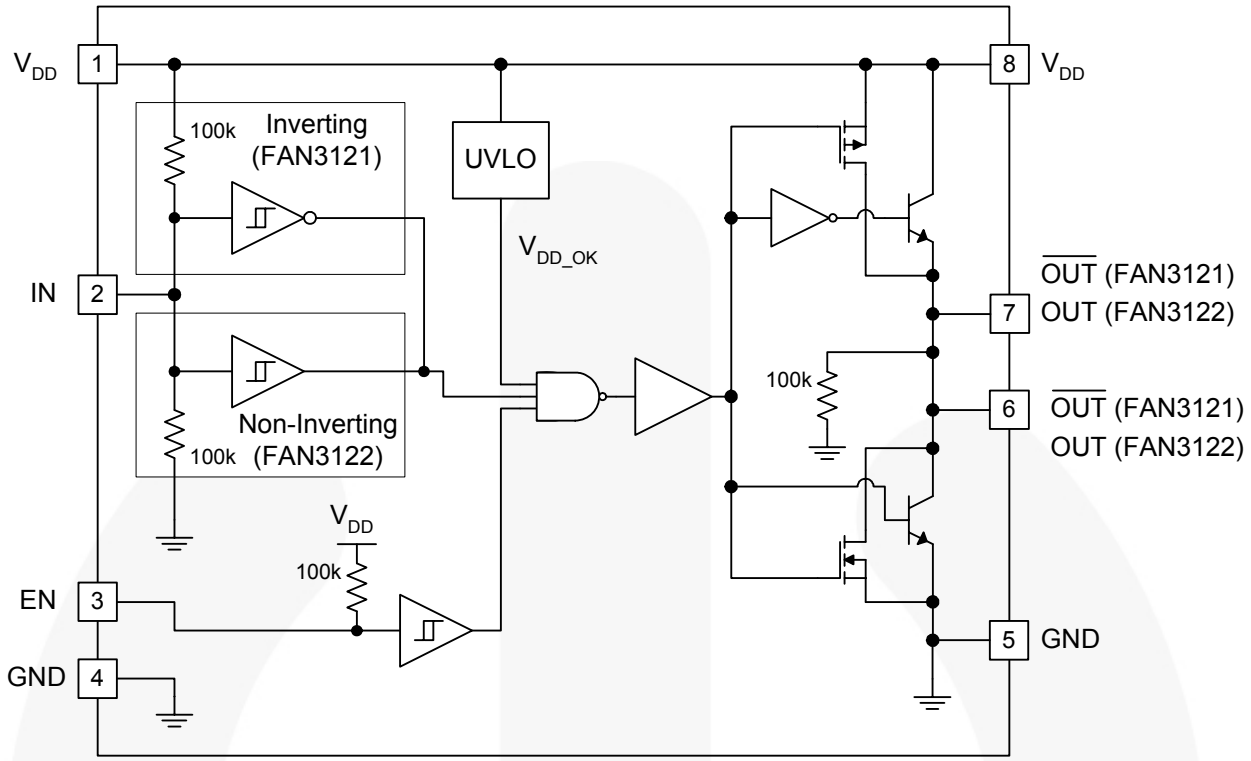


Figure 7. Block Diagram

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{DD}	V_{DD} to GND		-0.3	20.0	V
V_{EN}	EN to GND		GND - 0.3	V_{DD} + 0.3	V
V_{IN}	IN to GND		GND - 0.3	V_{DD} + 0.3	V
V_{OUT}	OUT to GND		GND - 0.3	V_{DD} + 0.3	V
T_L	Lead Soldering Temperature (10 Seconds)			+260	ºC
T_J	Junction Temperature		-55	+150	ºC
T_{STG}	Storage Temperature		-65	+150	ºC
ESD	Electrostatic Discharge Protection Level	Human Body Model, JEDEC JESD22-A114	2		kV
		Charged Device Model, JEDEC JESD22-C101	1		

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Supply Voltage Range	4.5	18.0	V
V_{EN}	Enable Voltage EN	0	V_{DD}	V
V_{IN}	Input Voltage IN	0	V_{DD}	V
T_A	Operating Ambient Temperature	-40	+125	ºC

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Electrical Characteristics

Unless otherwise noted, V_{DD}=12V and T_J=-40°C to +125°C. Currents are defined as positive into the device and negative out of the device.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Supply						
V_{DD}	Operating Range		4.5		18.0	V
I_{DD}	Supply Current, Inputs / EN Not Connected	TTL		0.65	0.90	mA
		CMOS[8]		0.58	0.85	
V_{ON}	Turn-On Voltage		3.5	4.0	4.3	V
V_{OFF}	Turn-Off Voltage		3.30	3.75	4.10	V
Inputs (FAN312xT)[9]						
V_{IL_T}	INx Logic Low Threshold		0.8	1.0		V
V_{IH_T}	INx Logic High Threshold			1.7	2.0	V
I_{IN+}	Non-Inverting Input Current	IN from 0 to V_{DD}	-1		175	µA
I_{IN-}	Inverting Input Current	IN from 0 to V_{DD}	-175		1	µA
V_{HYS_T}	TTL Logic Hysteresis Voltage		0.40	0.70	0.85	V
Inputs (FAN312xC)[9]						
V_{IL_C}	INx Logic Low Threshold		30	38		%V_{DD}
V_{IH_C}	INx Logic High Threshold			55	70	%V_{DD}
I_{IN+}	Non-Inverting Input Current	IN from 0 to V_{DD}	-1		175	µA
I_{IN-}	Inverting Input Current	IN from 0 to V_{DD}	-175		1	µA
V_{HYS_C}	CMOS Logic Hysteresis Voltage		12	17	24	%V_{DD}
ENABLE (FAN3121, FAN3122)						
V_{ENL}	Enable Logic Low Threshold	EN from 5V to 0V	1.2	1.6	2.0	V
V_{ENH}	Enable Logic High Threshold	EN from 0V to 5V	1.8	2.2	2.6	V
V_{HYS_T}	TTL Logic Hysteresis Voltage		0.2	0.6	0.8	V
R_{PU}	Enable Pull-up Resistance		68	100	134	kΩ
t_{D1}, t_{D2}	Propagation Delay, EN Rising[10]		8	17	27	ns
t_{D1}, t_{D2}	Propagation Delay, EN Falling[10]		14	21	33	ns
Output						
I_{SINK}	OUT Current, Mid-Voltage, Sinking[11]	OUT at V_{DD}/2, C_{LOAD}=1.0µF, f=1kHz		9.7		A
I_{SOURCE}	OUT Current, Mid-Voltage, Sourcing[11]	OUT at V_{DD}/2, C_{LOAD}=1.0µF, f=1kHz		7.1		A
I_{PK_SINK}	OUT Current, Peak, Sinking[11]	C_{LOAD}=1.0µF, f=1kHz		11.4		A
I_{PK_SOURCE}	OUT Current, Peak, Sourcing[11]	C_{LOAD}=1.0µF, f=1kHz		10.6		A
t_{RISE}	Output Rise Time[10]	C_{LOAD}=10nF	18	23	29	ns
t_{FALL}	Output Fall Time[10]	C_{LOAD}=10nF	11	19	27	ns
t_{D1}, t_{D2}	Output Propagation Delay, CMOS Inputs[10]	0 – 12V_{IN}, 1V/ns Slew Rate	9	18	28	ns
t_{D1}, t_{D2}	Output Propagation Delay, TTL Inputs[10]	0 – 5V_{IN}, 1V/ns Slew Rate	9	23	35	ns
I_{RVS}	Output Reverse Current Withstand[11]		1500			mA

Notes:

8. Lower supply current due to inactive TTL circuitry.
9. EN inputs have modified TTL thresholds; refer to the ENABLE section.
10. *See Timing Diagrams of Figure 8 and Figure 9.*
11. Not tested in production.

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Timing Diagrams

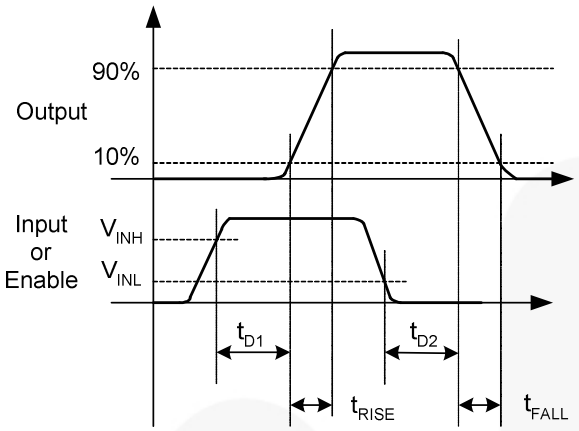


Figure 8. Non-Inverting

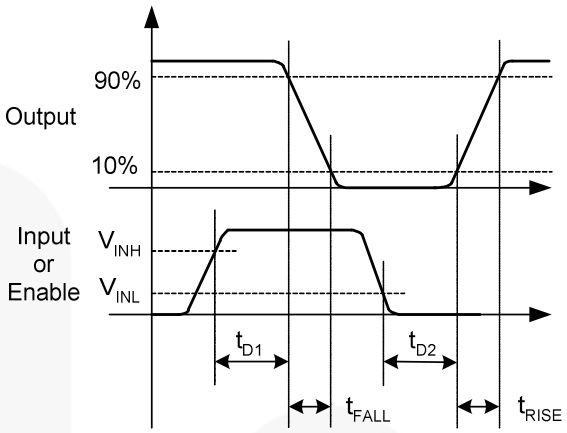


Figure 9. Inverting

Typical Performance Characteristics

Typical characteristics are provided at 25°C and V_{DD}=12V unless otherwise noted.

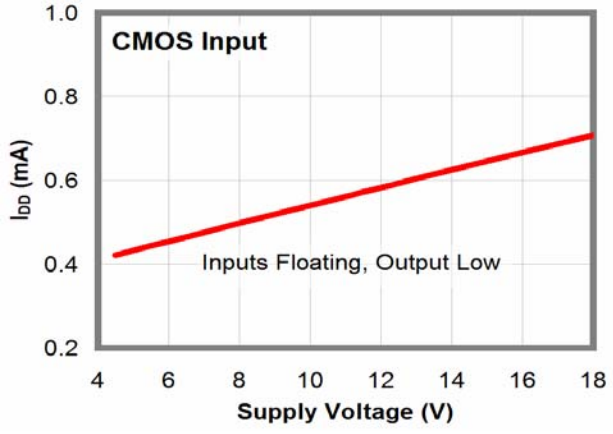


Figure 10. I_{DD} (Static) vs. Supply Voltage(12)

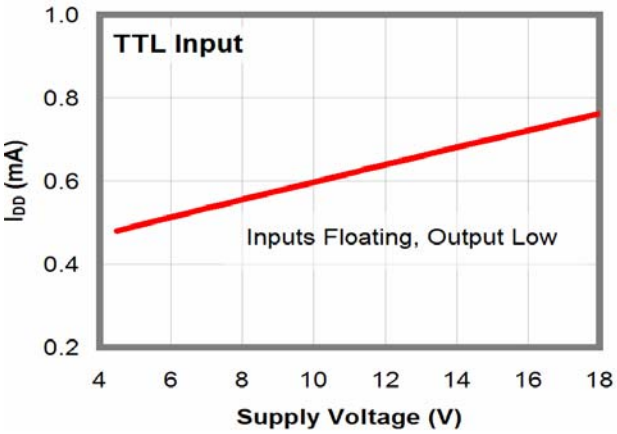


Figure 11. I_{DD} (Static) vs. Supply Voltage(12)

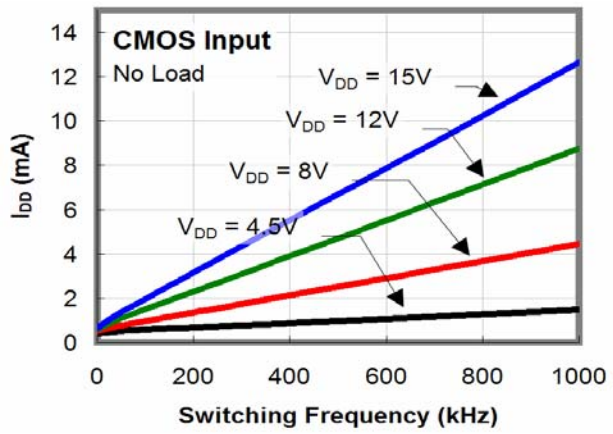


Figure 12. I_{DD} (No-Load) vs. Frequency

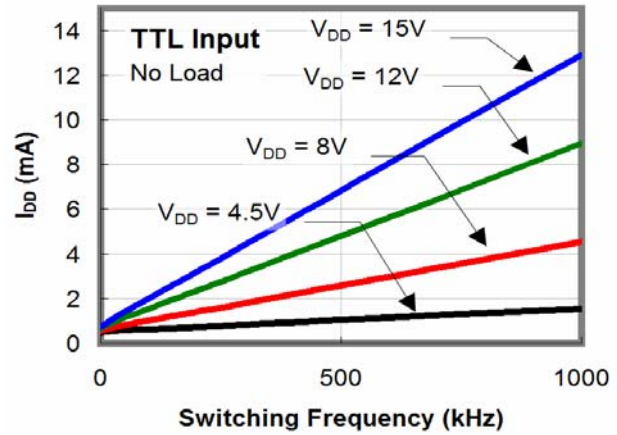


Figure 13. I_{DD} (No-Load) vs. Frequency

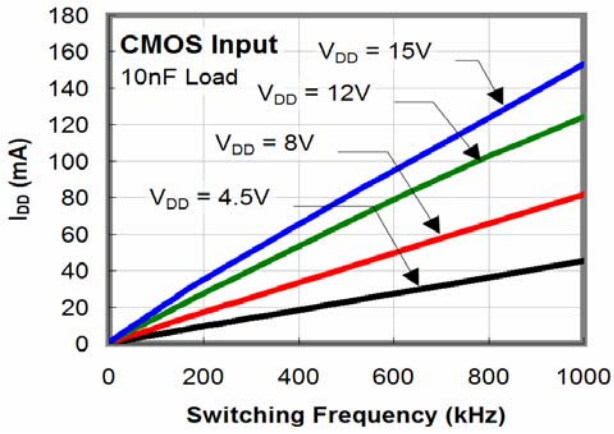


Figure 14. I_{DD} (10nF Load) vs. Frequency

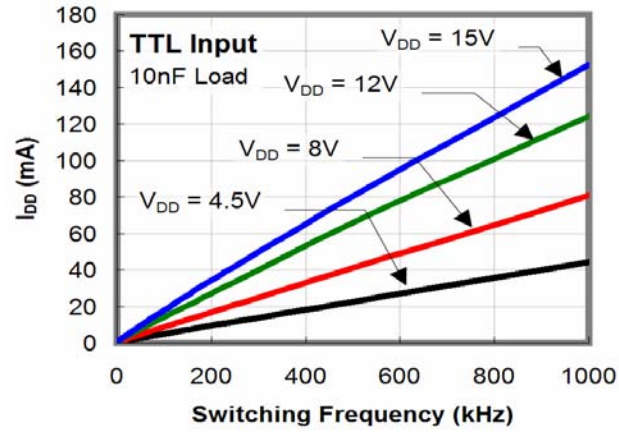


Figure 15. I_{DD} (10nF Load) vs. Frequency

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Typical Performance Characteristics

Typical characteristics are provided at 25°C and V_{DD}=12V unless otherwise noted.

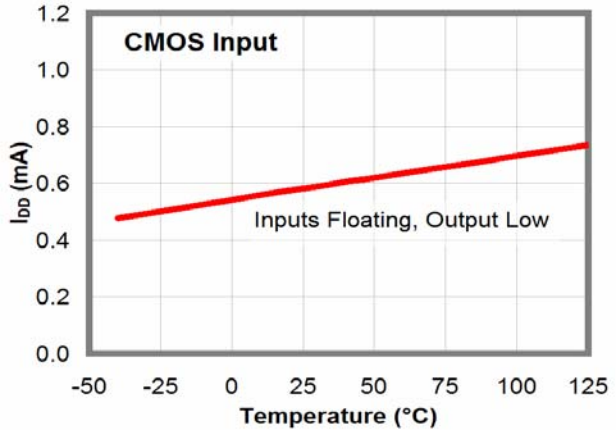


Figure 16. I_{DD} (Static) vs. Temperature[12]

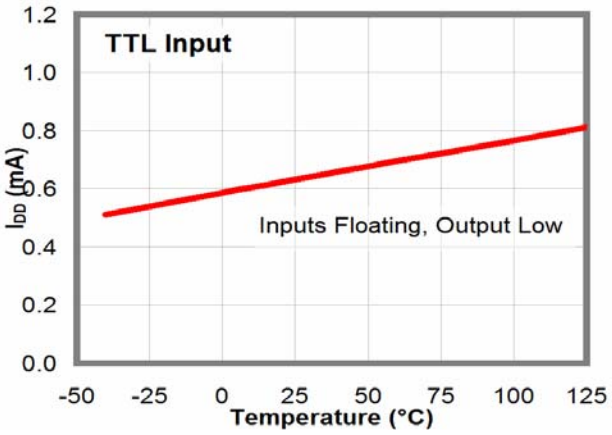


Figure 17. I_{DD} (Static) vs. Temperature[12]

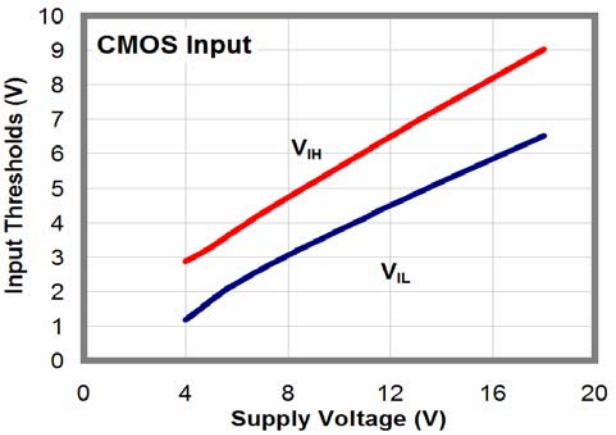


Figure 18. Input Thresholds vs. Supply Voltage

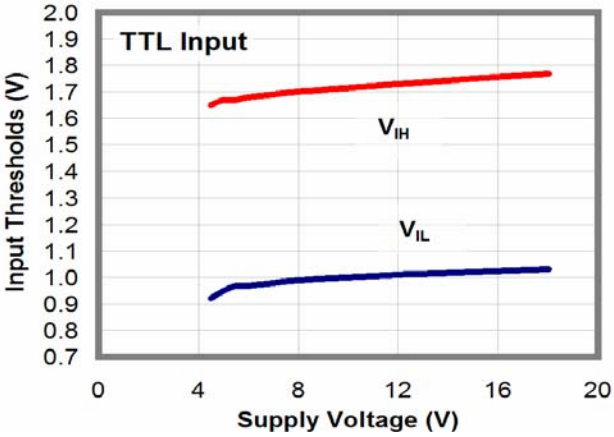


Figure 19. Input Thresholds vs. Supply Voltage

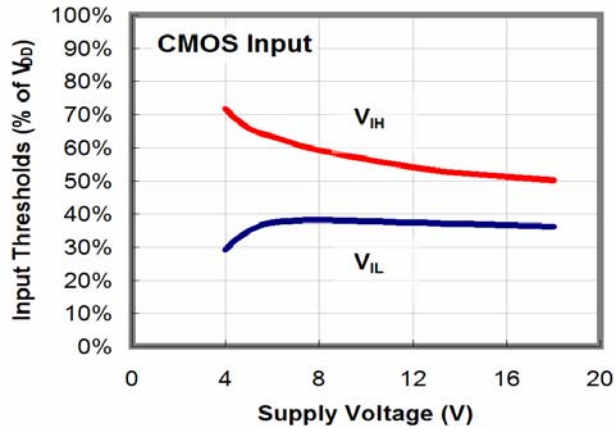


Figure 20. Input Thresholds % vs. Supply Voltage

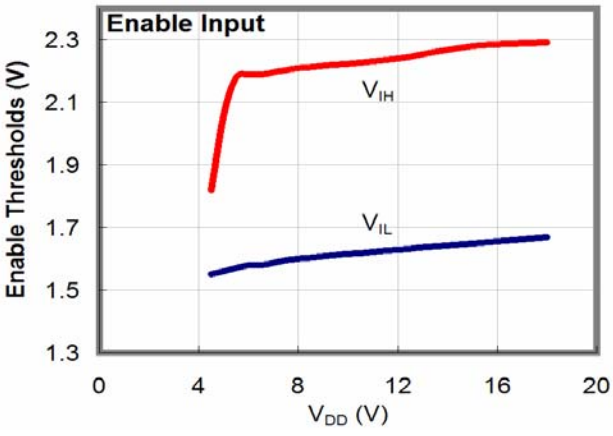


Figure 21. Enable Thresholds vs. Supply Voltage

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Typical Performance Characteristics

Typical characteristics are provided at 25°C and V_{DD}=12V unless otherwise noted.

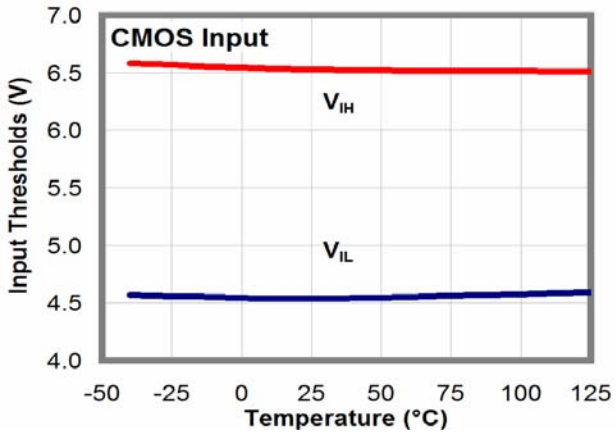


Figure 22. CMOS Input Thresholds vs. Temperature

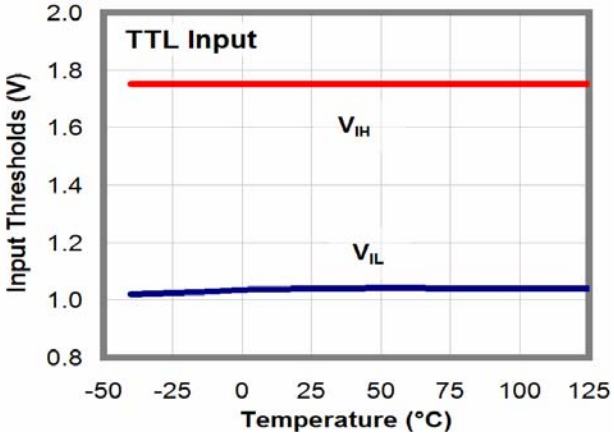


Figure 23. TTL Input Thresholds vs. Temperature

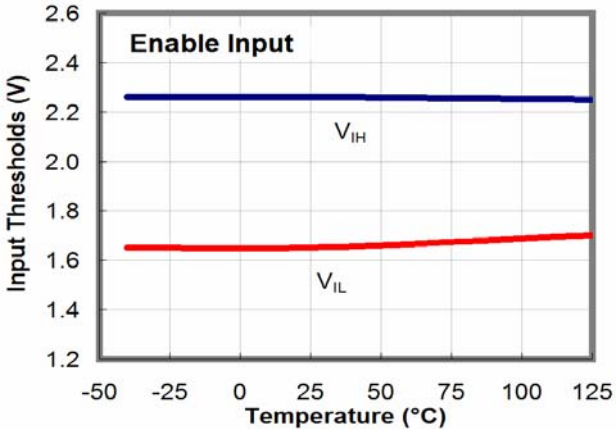


Figure 24. Enable Thresholds vs. Temperature

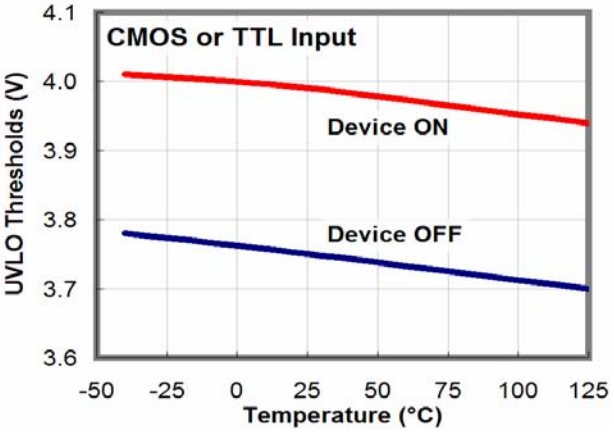


Figure 25. UVLO Thresholds vs. Temperature

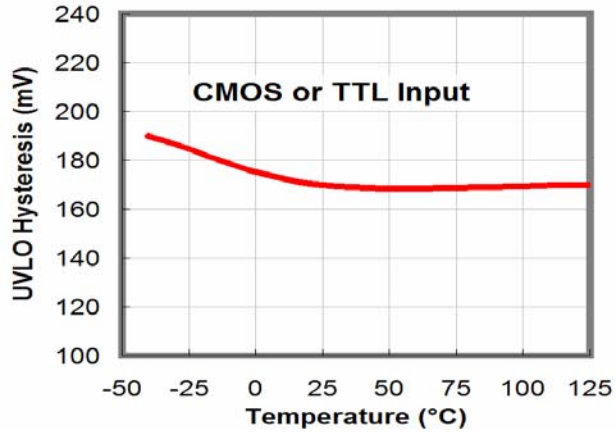


Figure 26. UVLO Hysteresis vs. Temperature

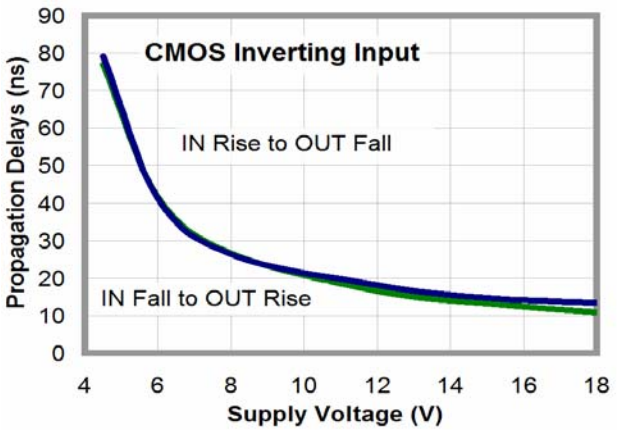


Figure 27. Propagation Delay vs. Supply Voltage

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Typical Performance Characteristics

Typical characteristics are provided at 25°C and V_{DD}=12V unless otherwise noted.

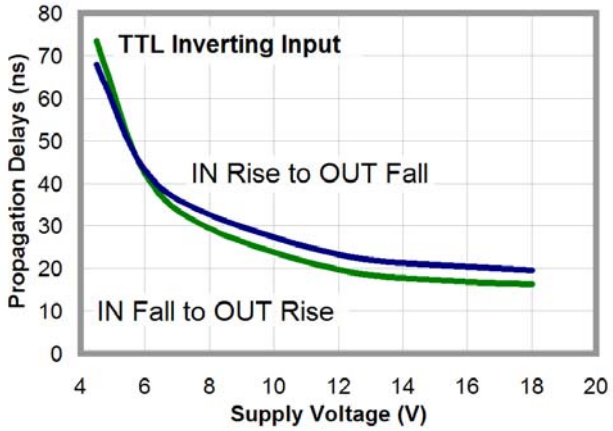


Figure 28. Propagation Delay vs. Supply Voltage

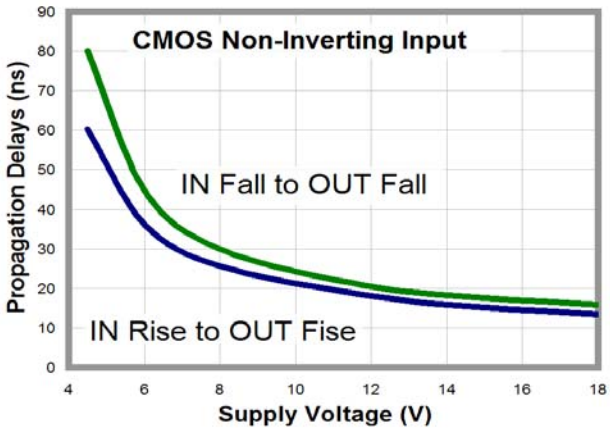


Figure 29. Propagation Delay vs. Supply Voltage

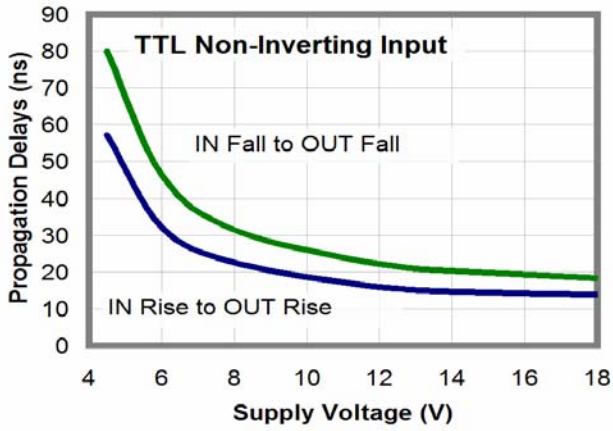


Figure 30. Propagation Delay vs. Supply Voltage

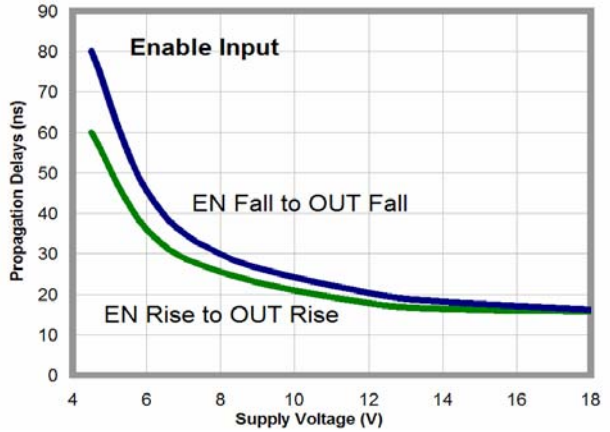


Figure 31. Propagation Delay vs. Supply Voltage

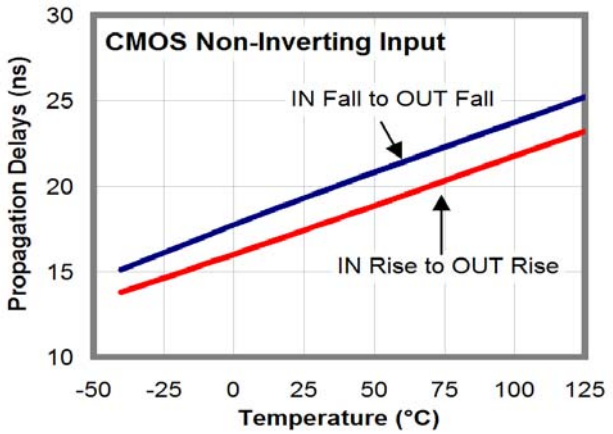


Figure 32. Propagation Delays vs. Temperature

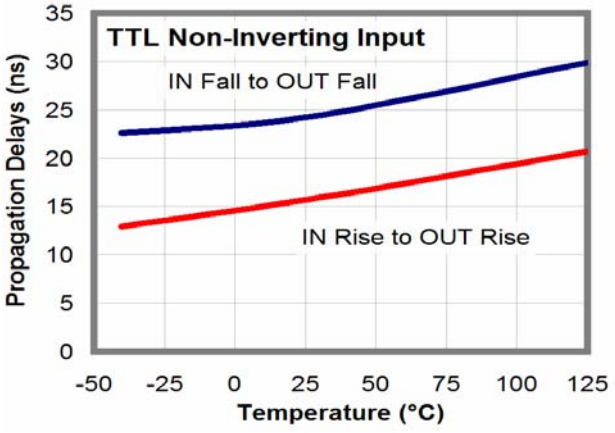


Figure 33. Propagation Delays vs. Temperature

Typical Performance Characteristics

Typical characteristics are provided at 25°C and V_{DD}=12V unless otherwise noted.

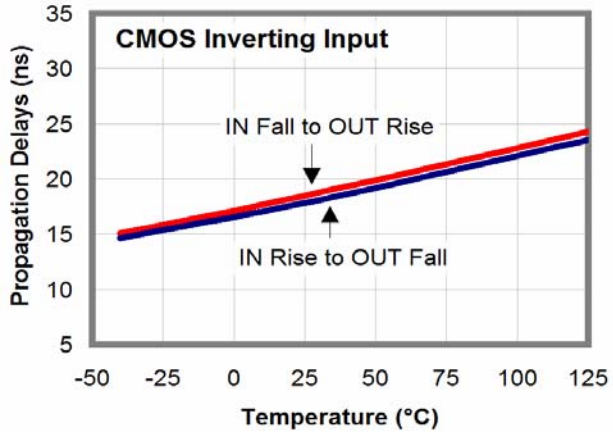


Figure 34. Propagation Delays vs. Temperature

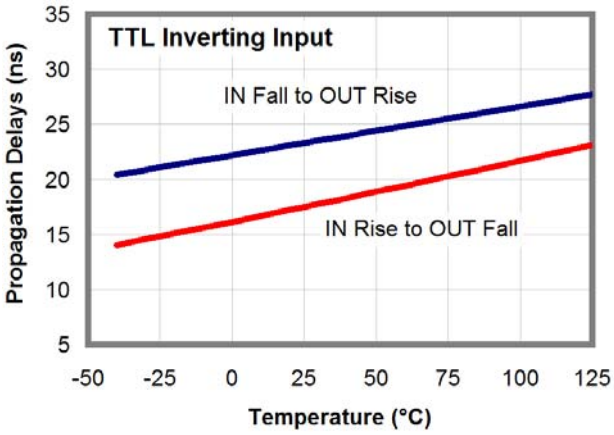


Figure 35. Propagation Delays vs. Temperature

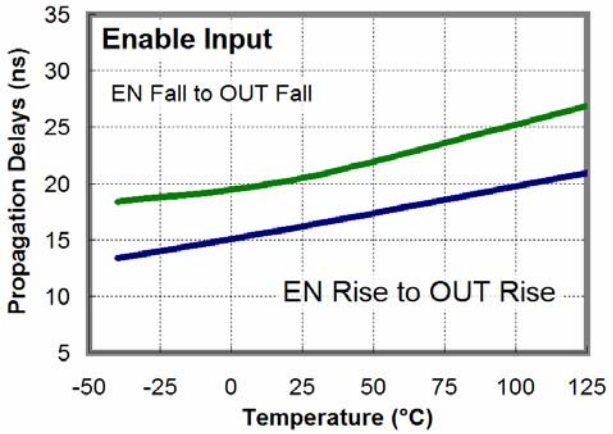


Figure 36. Propagation Delays vs. Temperature

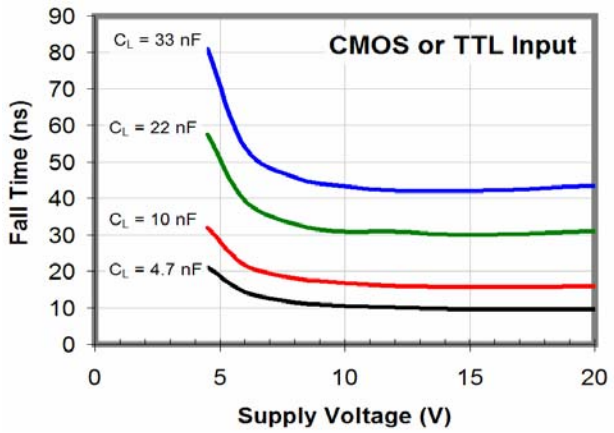


Figure 37. Fall Time vs. Supply Voltage

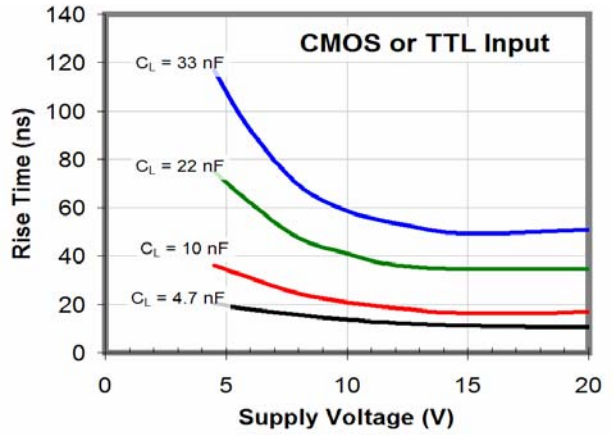


Figure 38. Rise Time vs. Supply Voltage

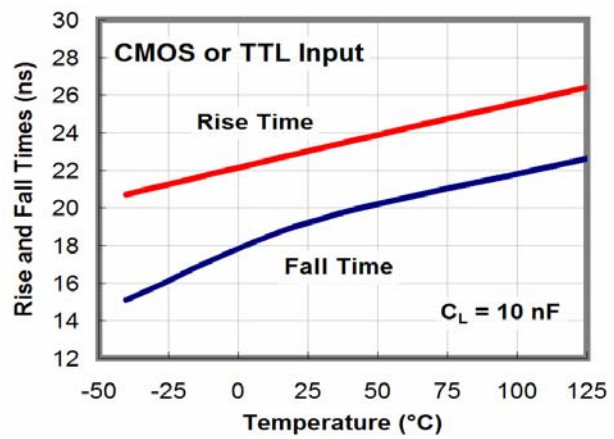


Figure 39. Rise and Fall Time vs. Temperature

Typical Performance Characteristics

Typical characteristics are provided at 25°C and V_{DD}=12V unless otherwise noted.

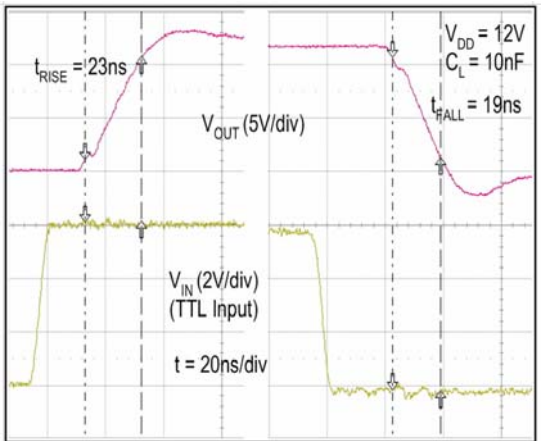


Figure 40. Rise / Fall Waveforms with 10nF Load

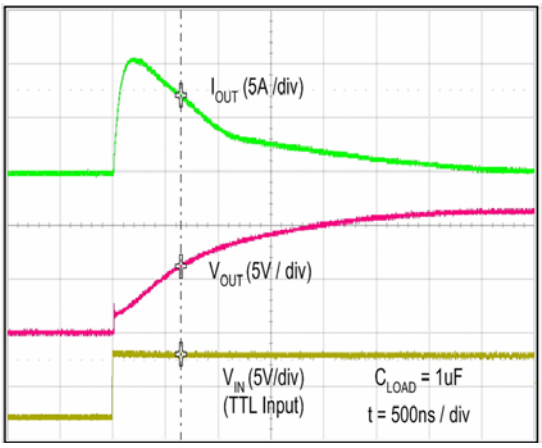


Figure 41. Quasi-Static Source Current with V_{DD}=12V[13]

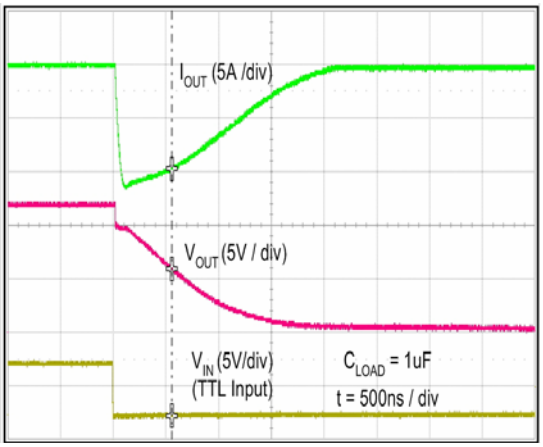


Figure 42. Quasi-Static Sink Current with V_{DD}=12V[13]

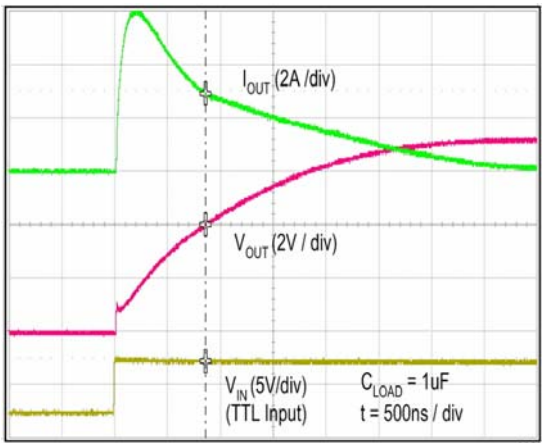


Figure 43. Quasi-Static Source Current with V_{DD}=8V[13]

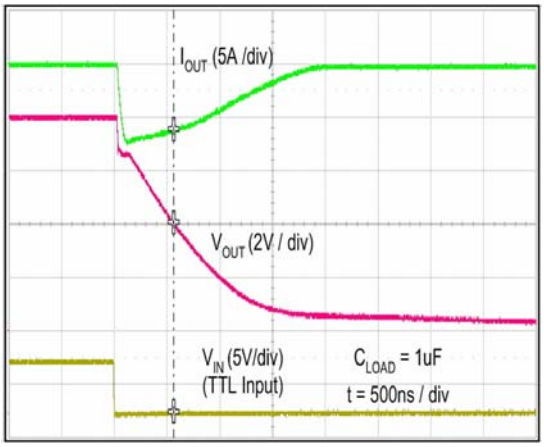


Figure 44. Quasi-Static Sink Current with V_{DD}=8V[13]

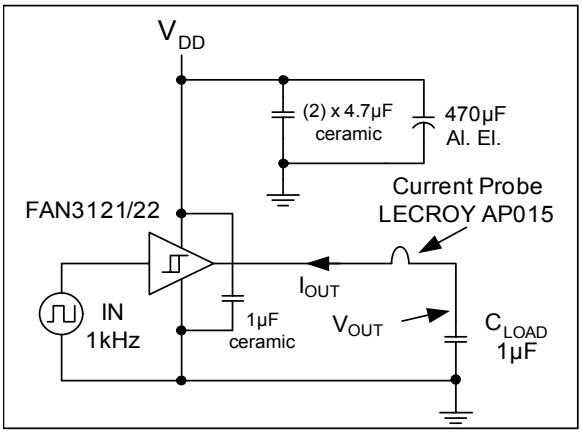


Figure 45. Quasi-Static I_{OUT} / V_{OUT} Test Circuit

Notes:

12. For any inverting inputs pulled LOW, non-inverting inputs pulled HIGH, or outputs driven HIGH; static I_{DD} increases by the current flowing through the corresponding pull-up/down resistor, shown in Figure 7.
13. The initial spike in each current waveform is a measurement artifact caused by the stray inductance of the current-measurement loop.

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Applications Information

The FAN3121 and FAN3122 family offers versions in either TTL or CMOS input configuration. In the FAN3121T and FAN3122T, the input thresholds meet industry-standard TTL-logic thresholds independent of the V_{DD} voltage, and there is a hysteresis voltage of approximately 0.7V. These levels permit the inputs to be driven from a range of input logic signal levels for which a voltage over 2V is considered logic HIGH. The driving signal for the TTL inputs should have fast rising and falling edges with a slew rate of 6V/µs or faster, so the rise time from 0 to 3.3V should be 550ns or less.

The FAN3121 and FAN3122 output can be enabled or disabled using the EN pin with a very rapid response time. If EN is not externally connected, an internal pull-up resistor enables the driver by default. The EN pin has logic thresholds for parts with either TTL or CMOS IN thresholds.

In the FAN3121C and FAN3122C, the logic input thresholds are dependent on the V_{DD} level and, with V_{DD} of 12V, the logic rising edge threshold is approximately 55% of V_{DD} and the input falling edge threshold is approximately 38% of V_{DD}. The CMOS input configuration offers a hysteresis voltage of approximately 17% of V_{DD}. The CMOS inputs can be used with relatively slow edges (approaching DC) if good decoupling and bypass techniques are incorporated in the system design to prevent noise from violating the input voltage hysteresis window. This allows setting precise timing intervals by fitting an R-C circuit between the controlling signal and the IN pin of the driver. The slow rising edge at the IN pin of the driver introduces a delay between the controlling signal and the OUT pin of the driver.

Static Supply Current

In the I_{DD} (static) Typical Performance Characteristics, the curves are produced with all inputs / enables floating (OUT is LOW) and indicates the lowest static I_{DD} current for the tested configuration. For other states, additional current flows through the 100kΩ resistors on the inputs and outputs, as shown in the block diagram *(see Figure 7)*. In these cases, the actual static I_{DD} current is the value obtained from the curves, plus this additional current.

MillerDrive™ Gate-Drive Technology

FAN312x gate drivers incorporate the MillerDrive™ architecture shown in Figure 46. For the output stage, a combination of bipolar and MOS devices provide large currents over a wide range of supply voltage and temperature variations. The bipolar devices carry the bulk of the current as OUT swings between 1/3 to 2/3 V_{DD} and the MOS devices pull the output to the HIGH or LOW rail.

The purpose of the Miller Drive™ architecture is to speed up switching by providing high current during the Miller plateau region when the gate-drain capacitance of the MOSFET is being charged or discharged as part of the turn-on / turn-off process.

For applications with zero voltage switching during the MOSFET turn-on or turn-off interval, the driver supplies high peak current for fast switching, even though the Miller plateau is not present. This situation often occurs in synchronous rectifier applications because the body diode is generally conducting before the MOSFET is switched on.

The output pin slew rate is determined by V_{DD} voltage and the load on the output. It is not user adjustable, but a series resistor can be added if a slower rise or fall time at the MOSFET gate is needed.

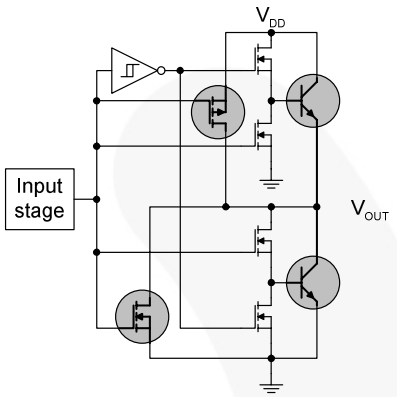


Figure 46. Miller Drive™ Output Architecture

Under-Voltage Lockout (UVLO)

The FAN312x startup logic is optimized to drive ground-referenced N-channel MOSFETs with an under-voltage lockout (UVLO) function to ensure that the IC starts in an orderly fashion. When V_{DD} is rising, yet below the 4.0V operational level, this circuit holds the output low, regardless of the status of the input pins. After the part is active, the supply voltage must drop 0.25V before the part shuts down. This hysteresis helps prevent chatter when low V_{DD} supply voltages have noise from the power switching. This configuration is not suitable for driving high-side P-channel MOSFETs because the low output voltage of the driver would turn the P-channel MOSFET on with V_{DD} below 4.0V.

V_{DD} Bypassing and Layout Considerations

The FAN3121 and FAN3122 are available in either 8-lead SOIC or MLP packages. In either package, the V_{DD} pins 1 and 8 and the GND pins 4 and 5 should be connected together on the PCB.

In typical FAN312x gate-driver applications, high-current pulses are needed to charge and discharge the gate of a power MOSFET in time intervals of 50ns or less. A bypass capacitor with low ESR and ESL should be connected directly between the V_{DD} and GND pins to provide these large current pulses without causing unacceptable ripple on the V_{DD} supply. To meet these requirements in a small size, a ceramic capacitor of 1µF or larger is typically used, with a dielectric material such as X7R, to limit the change in capacitance over the temperature and / or voltage application ranges.

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Figure 47 shows the pulsed gate drive current path when the gate driver is supplying gate charge to turn the MOSFET on. The current is supplied from the local bypass capacitor C_{BYP} and flows through the driver to the MOSFET gate and to ground. To reach the high peak currents possible with the FAN312x family, the resistance and inductance in the path should be minimized. The localized C_{BYP} acts to contain the high peak current pulses within this driver-MOSFET circuit, preventing them from disturbing the sensitive analog circuitry in the PWM controller.

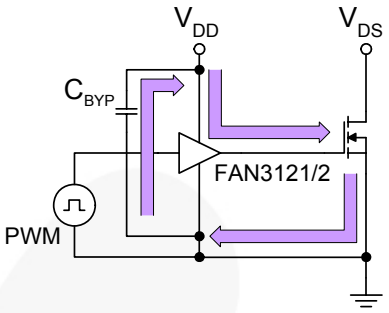


Figure 47. Current Path for MOSFET Turn-On

Figure 48 shows the path the current takes when the gate driver turns the MOSFET off. Ideally, the driver shunts the current directly to the source of the MOSFET in a small circuit loop. For fast turn-off times, the resistance and inductance in this path should be minimized.

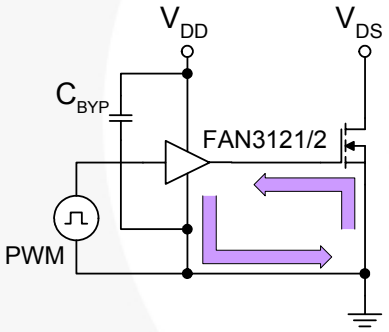


Figure 48. Current Path for MOSFET Turn-Off

Operational Waveforms

At power up, the FAN3121 inverting driver shown in Figure 49 holds the output LOW until the V_{DD} voltage reaches the UVLO turn-on threshold, as indicated in Figure 50. This facilitates proper startup control of low-side N-channel MOSFETs.

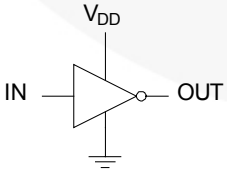


Figure 49. Inverting Configuration

The OUT pulses' magnitude follows V_{DD} magnitude with the output polarity inverted from the input until steady-state V_{DD} is reached.

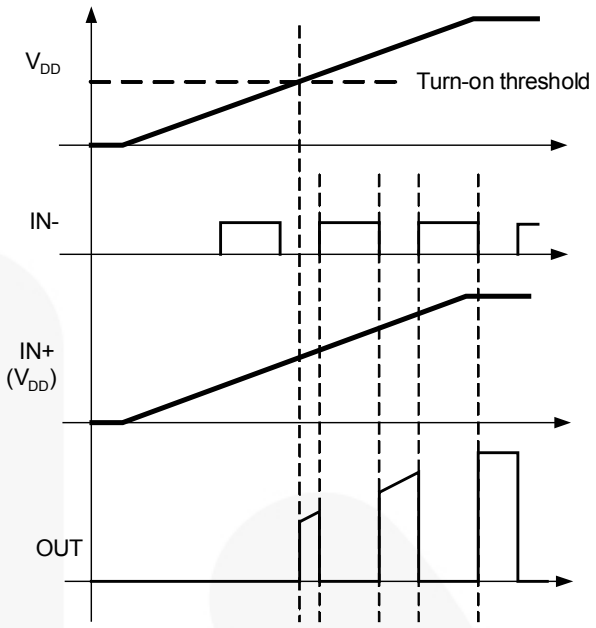


Figure 50. Inverting Startup Waveforms

At power up, the FAN3122 non-inverting driver, shown in Figure 51, holds the output LOW until the V_{DD} voltage reaches the UVLO turn-on threshold, as indicated in Figure 52. The OUT pulses magnitude follow V_{DD} magnitude until steady-state V_{DD} is reached.

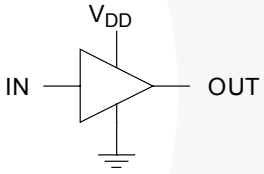


Figure 51. Non-Inverting Driver

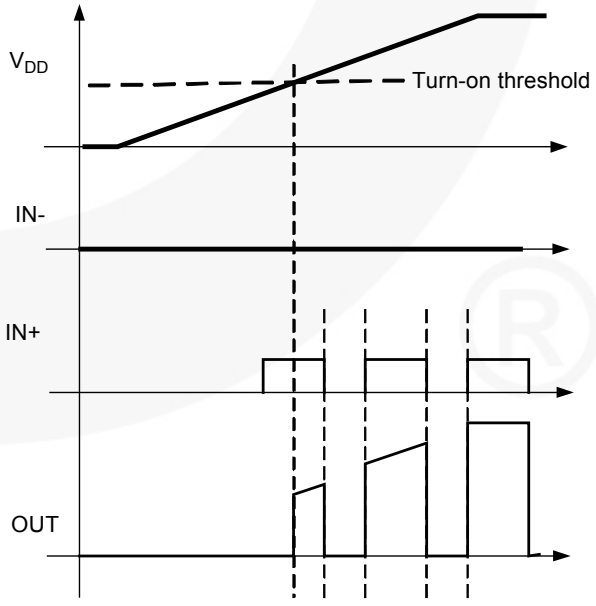


Figure 52. Non-Inverting Startup Waveforms

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Thermal Guidelines

Gate drivers used to switch MOSFETs and IGBTs at high frequencies can dissipate significant amounts of power. It is important to determine the driver power dissipation and the resulting junction temperature in the application to ensure that the part is operating within acceptable temperature limits.

The total power dissipation in a gate driver is the sum of two components, P_{GATE} and $P_{DYNAMIC}$:

$$P_{TOTAL} = P_{GATE} + P_{DYNAMIC} \quad (1)$$

Gate Driving Loss: The most significant power loss results from supplying gate current (charge per unit time) to switch the load MOSFET on and off at the switching frequency. The power dissipation that results from driving a MOSFET at a specified gate-source voltage, V_{GS}, with gate charge, Q_G, at switching frequency, f_{SW}, is determined by:

$$P_{GATE} = Q_G \bullet V_{GS} \bullet f_{SW} \quad (2)$$

Dynamic Pre-drive / Shoot-through Current: A power loss resulting from internal current consumption under dynamic operating conditions, including pin pull-up / pull-down resistors, can be obtained using the “IDD (No-Load) vs. Frequency” graphs in Typical Performance Characteristics to determine the current $I_{DYNAMIC}$ drawn from V_{DD} under actual operating conditions:

$$P_{DYNAMIC} = I_{DYNAMIC} \bullet V_{DD} \quad (3)$$

Once the power dissipated in the driver is determined, the driver junction rise with respect to circuit board can be evaluated using the following thermal equation, assuming ψ_{JB} was determined for a similar thermal design (heat sinking and air flow):

$$T_J = P_{TOTAL} \bullet \psi_{JB} + T_B \quad (4)$$

where:

T_J = driver junction temperature;

ψ_{JB} = (psi) thermal characterization parameter relating temperature rise to total power dissipation; and

T_B = board temperature in location as defined in the Thermal Characteristics table.

In a full-bridge synchronous rectifier application, shown in Figure 53, each FAN3122 drives a parallel combination of two high-current MOSFETs, (such as FDMS8660S). The typical gate charge for each SR MOSFET is 70nC with $V_{GS} = V_{DD} = 9V$. At a switching frequency of 300kHz, the total power dissipation is:

$$P_{GATE} = 2 \bullet 70nC \bullet 9V \bullet 300kHz = 0.378W \quad (5)$$

$$P_{DYNAMIC} = 2mA \bullet 9V = 18mW \quad (6)$$

$$P_{TOTAL} = 0.396W \quad (7)$$

The SOIC-8 has a junction-to-board thermal characterization parameter of $\psi_{JB} = 42°C/W$. In a system application, the localized temperature around the device is a function of the layout and construction of the PCB along with airflow across the surfaces. To ensure reliable operation, the maximum junction temperature of the device must be prevented from exceeding the maximum rating of 150°C; with 80% derating, T_J would be limited to 120°C. Rearranging Equation 4 determines the board temperature required to maintain the junction temperature below 120°C:

$$T_{B,MAX} = T_J - P_{TOTAL} \bullet \psi_{JB} \quad (8)$$

$$T_{B,MAX} = 120°C – 0.396W \bullet 42°C/W = 104°C \quad (9)$$

For comparison, replace the SOIC-8 used in the previous example with the 3x3mm MLP package with $\psi_{JB} = 2.8°C/W$. The 3x3mm MLP package can operate at a PCB temperature of 118°C, while maintaining the junction temperature below 120°C. This illustrates that the physically smaller MLP package with thermal pad offers a more conductive path to remove the heat from the driver. Consider tradeoffs between reducing overall circuit size with junction temperature reduction for increased reliability.

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Typical Application Diagrams

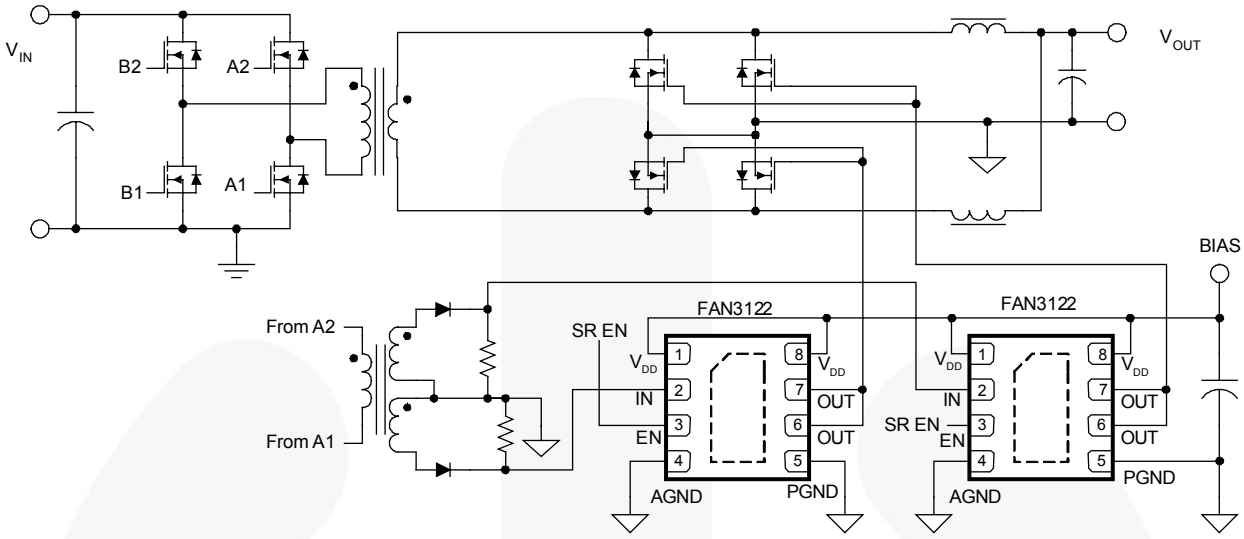


Figure 53. Full-Bridge Synchronous Rectification

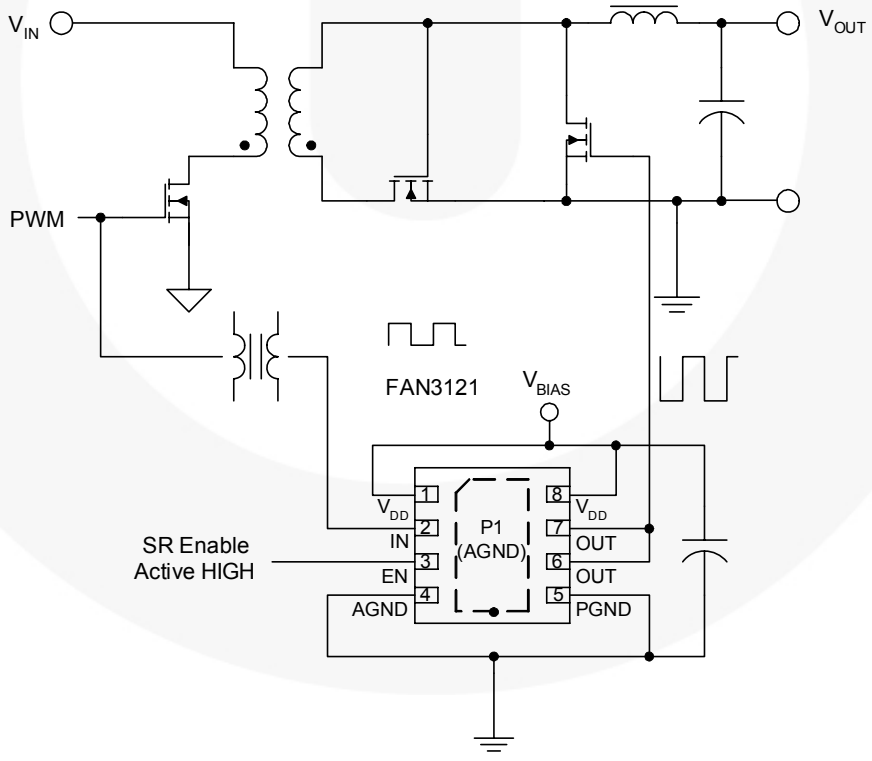


Figure 54. Hybrid Synchronous Rectification in a Forward Converter

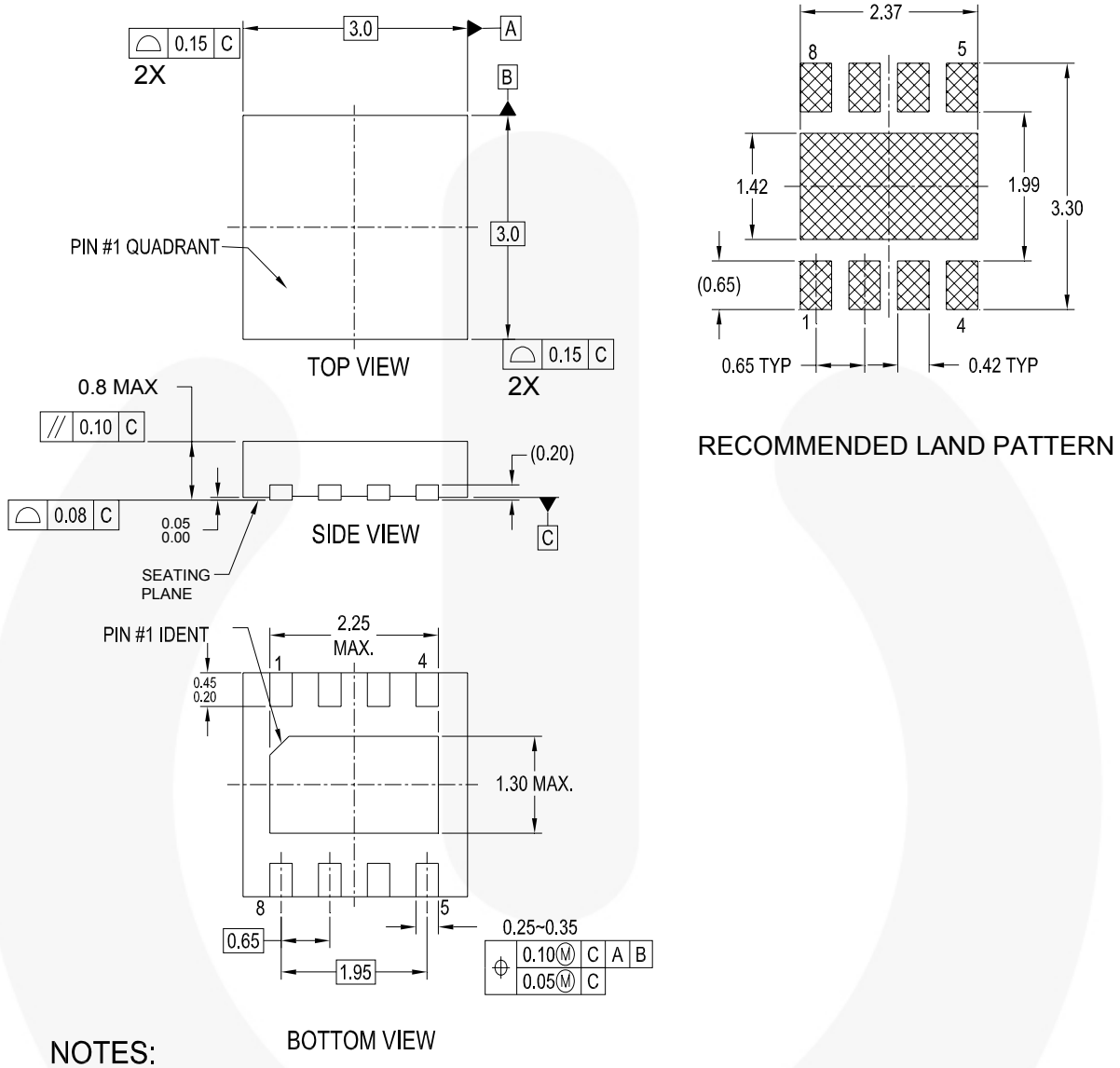
Table 1. Related Products

Part Number	Type	Gate Drive[14] (Sink/Src)	Input Threshold	Logic	Package
FAN3100C	Single 2A	+2.5A / -1.8A	CMOS	Single Channel of Two-Input/One-Output	SOT23-5, MLP6
FAN3100T	Single 2A	+2.5A / -1.8A	TTL	Single Channel of Two-Input/One-Output	SOT23-5, MLP6
FAN3226C	Dual 2A	+2.4A / -1.6A	CMOS	Dual Inverting Channels + Dual Enable	SOIC8, MLP8
FAN3226T	Dual 2A	+2.4A / -1.6A	TTL	Dual Inverting Channels + Dual Enable	SOIC8, MLP8
FAN3227C	Dual 2A	+2.4A / -1.6A	CMOS	Dual Non-Inverting Channels + Dual Enable	SOIC8, MLP8
FAN3227T	Dual 2A	+2.4A / -1.6A	TTL	Dual Non-Inverting Channels + Dual Enable	SOIC8, MLP8
FAN3228C	Dual 2A	+2.4A / -1.6A	CMOS	Dual Channels of Two-Input/One-Output, Pin Config.1	SOIC8, MLP8
FAN3228T	Dual 2A	+2.4A / -1.6A	TTL	Dual Channels of Two-Input/One-Output, Pin Config.1	SOIC8, MLP8
FAN3229C	Dual 2A	+2.4A / -1.6A	CMOS	Dual Channels of Two-Input/One-Output, Pin Config.2	SOIC8, MLP8
FAN3229T	Dual 2A	+2.4A / -1.6A	TTL	Dual Channels of Two-Input/One-Output, Pin Config.2	SOIC8, MLP8
FAN3223C	Dual 4A	+4.3A / -2.8A	CMOS	Dual Inverting Channels + Dual Enable	SOIC8, MLP8
FAN3223T	Dual 4A	+4.3A / -2.8A	TTL	Dual Inverting Channels + Dual Enable	SOIC8, MLP8
FAN3224C	Dual 4A	+4.3A / -2.8A	CMOS	Dual Non-Inverting Channels + Dual Enable	SOIC8, MLP8
FAN3224T	Dual 4A	+4.3A / -2.8A	TTL	Dual Non-Inverting Channels + Dual Enable	SOIC8, MLP8
FAN3225C	Dual 4A	+4.3A / -2.8A	CMOS	Dual Channels of Two-Input/One-Output	SOIC8, MLP8
FAN3225T	Dual 4A	+4.3A / -2.8A	TTL	Dual Channels of Two-Input/One-Output	SOIC8, MLP8
FAN3121C	Single 9A	+9.7A / -7.1A	CMOS	Single Inverting Channels + Enable	SOIC8, MLP8
FAN3121T	Single 9A	+9.7A / -7.1A	TTL	Single Inverting Channels + Enable	SOIC8, MLP8
FAN3122C	Single 9A	+9.7A / -7.1A	CMOS	Single Non-Inverting Channels + Enable	SOIC8, MLP8
FAN3122T	Single 9A	+9.7A / -7.1A	TTL	Single Non-Inverting Channels + Enable	SOIC8, MLP8

Note:
14. Typical currents with OUT at 6V and V_{DD} = 12V.

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Physical Dimensions



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-229, VARIATION VEEC, DATED 11/2001

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

D. FILENAME: MKT-MLP08Drev2

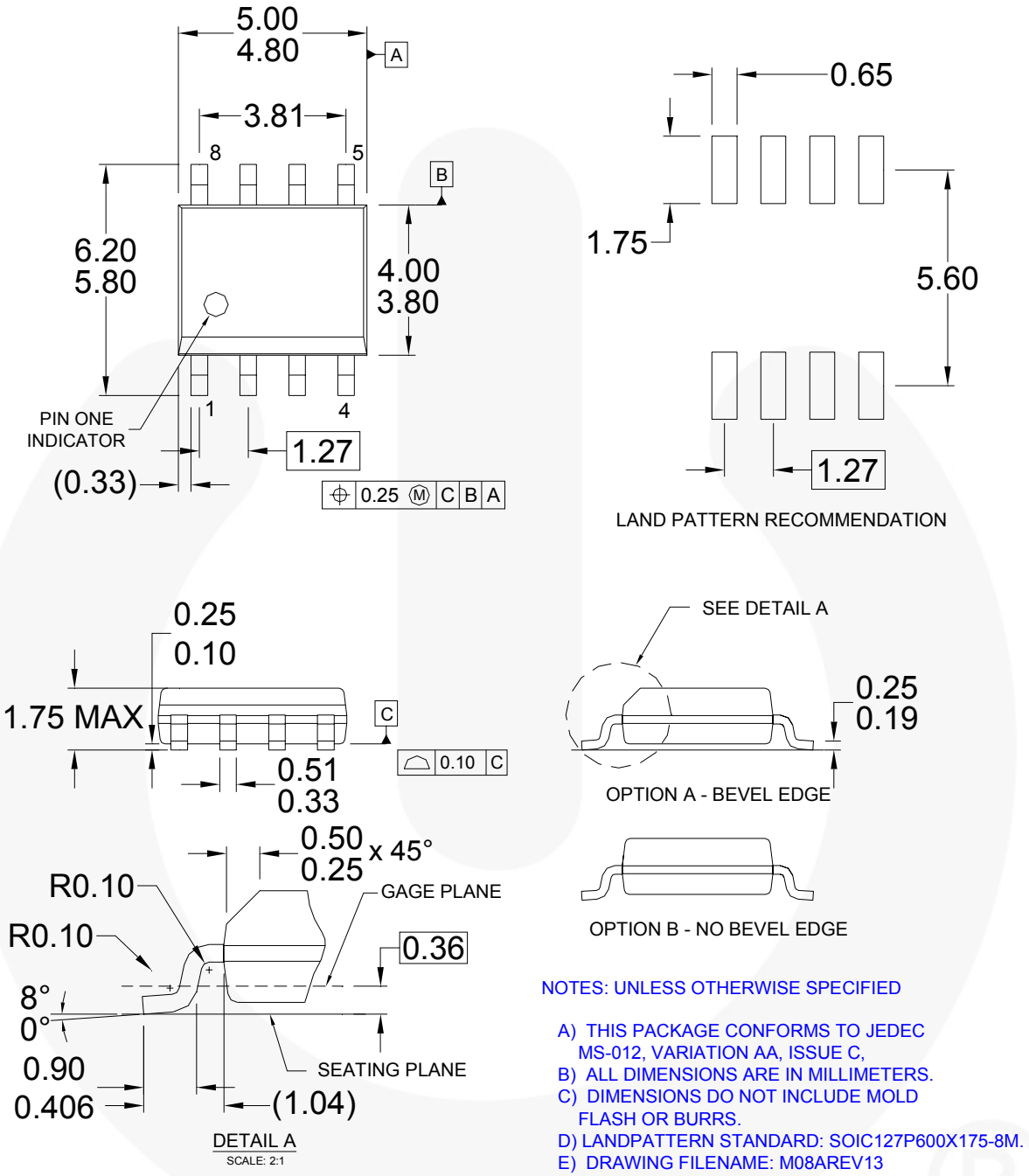
Figure 55. 3x3mm, 8-Lead Molded Leadless Package (MLP)

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Physical Dimensions (Continued)



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C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M.
E) DRAWING FILENAME: M08AREV13

Figure 56. 8-Lead SOIC

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Green FPS™
Green FPS™ e-Series™
GTO™
IntelliMAX™
ISOPLANAR™
MegaBuck™
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