

Evaluation Board for Quad, High Speed Op Amps Offered in 14-Lead SOIC Packages

FEATURES

Enables quick breadboarding/prototyping
User-defined circuit configuration
Edge-mounted SMA connector provisions
Easy connection to test equipment and other circuits
RoHS compliant

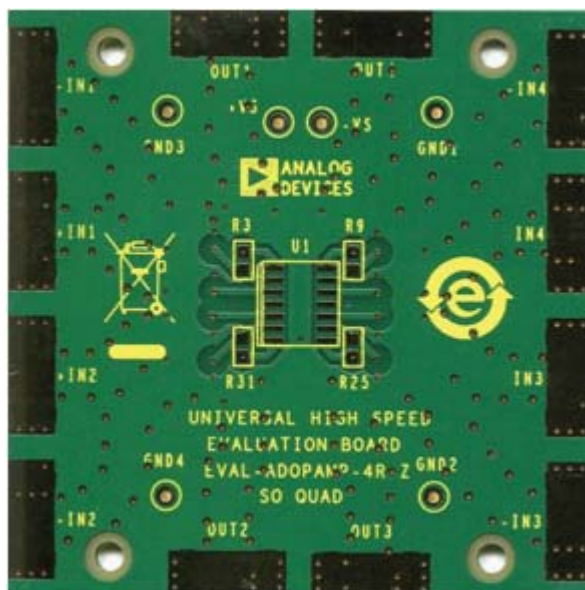
GENERAL DESCRIPTION

The Analog Devices, Inc., 14-lead SOIC evaluation board is designed to help users evaluate quad, high speed op amps offered in 14-lead SOIC packages. The evaluation board is a bare board (that is, there are no components or amplifier soldered to the board; these must be ordered separately) that enables users to quickly prototype a variety of quad op amp circuits. The evaluation board minimizes risk and reduces time to market. Figure 1 shows the component side of the bare evaluation board, and Figure 2 shows the circuit side.

The 2-layer evaluation board accepts SMA edge-mounted connectors on the inputs and outputs for efficient connection to test equipment or other circuitry. The ground plane, component placement, and supply bypassing are designed to minimize parasitic inductance and capacitance. The evaluation board components are primarily SMT 0805 case size, with the exception of the electrolytic bypass capacitors (C1 and C2), which are 3528 case size.

Figure 3 shows the evaluation board schematic. The PCB assembly drawings are shown in Figure 4 and Figure 5. The layout patterns for the PCB are shown in Figure 6 and Figure 7.

EVALUATION BOARD COMPONENT AND CIRCUIT SIDES

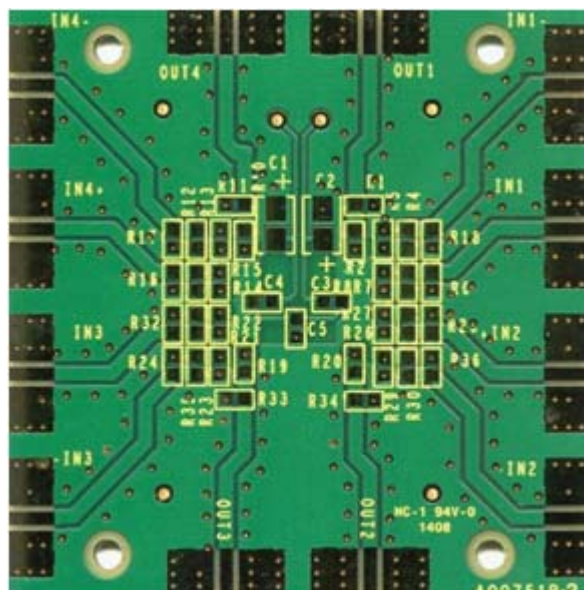


NOTES

1. THE EVALUATION BOARD SILKSCREEN PART NUMBER LABELLING ON YOUR BOARD MAY BE DIFFERENT FROM WHAT IS SHOWN HERE.

Figure 1. Component Side of Evaluation Board

08913-001



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Figure 2. Circuit Side of Evaluation Board

08913-007

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REVISION HISTORY

4/11—Rev. 0 to Rev. A	
Changes to General Description Section	1
Deleted EB-O14R-4Z Throughout.....	1

3/10—Revision 0: Initial Version

EVALUATION BOARD SCHEMATIC, ASSEMBLY DRAWINGS, AND LAYOUT PATTERNS

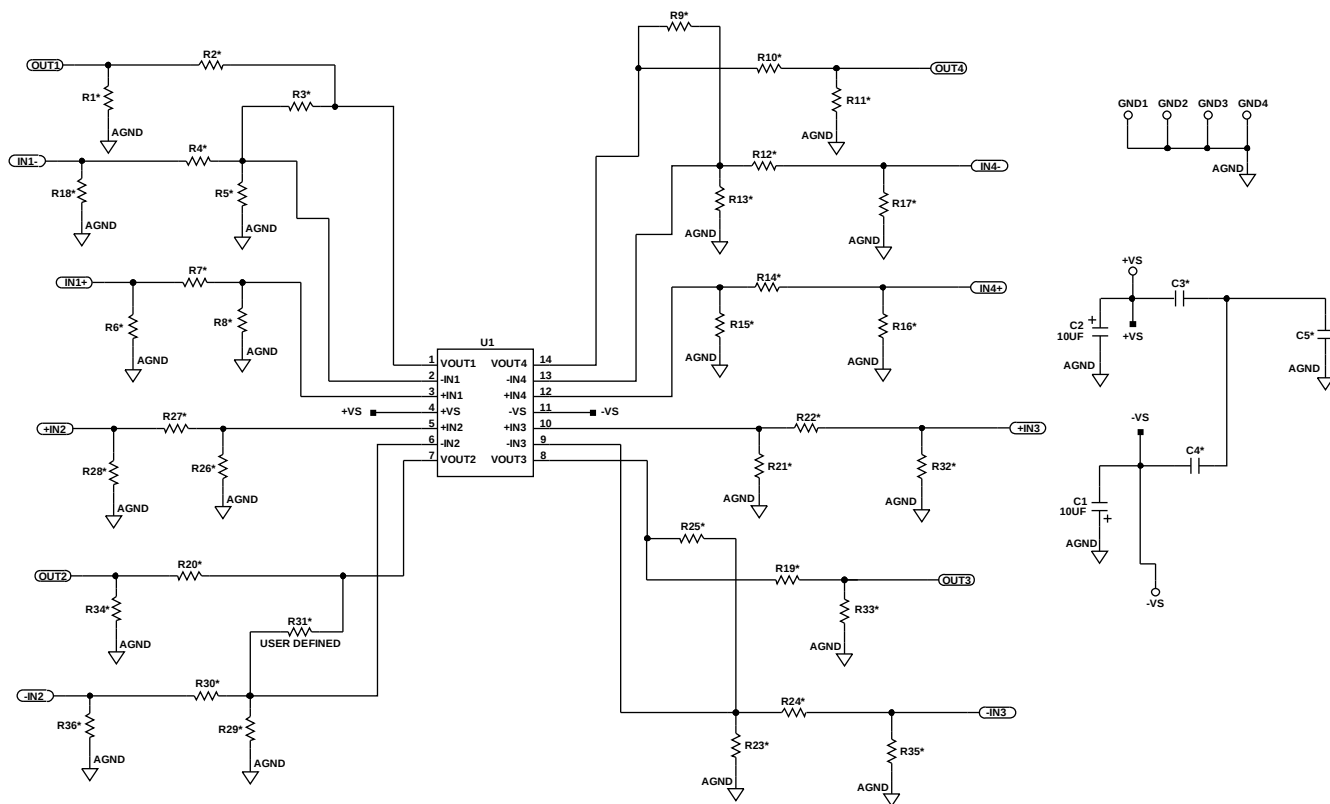


Figure 3. Evaluation Board Schematic

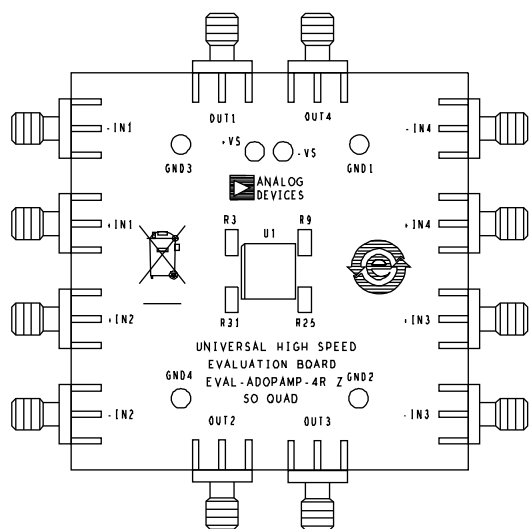


Figure 4. Component Side Assembly Drawing

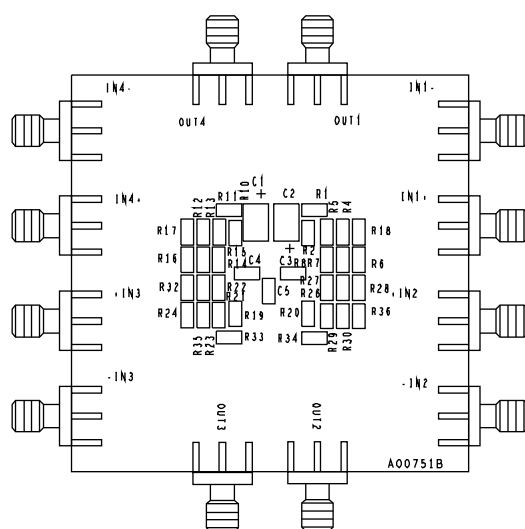


Figure 5. Circuit Side Assembly Drawing

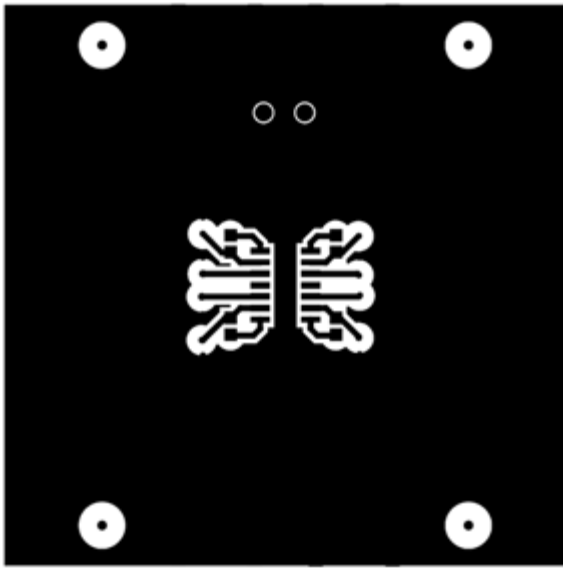


Figure 6. Component Side Layout Pattern

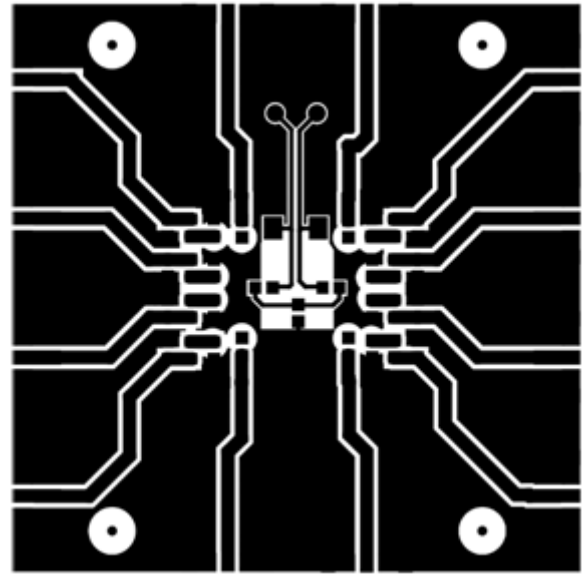


Figure 7. Circuit Side Layout Pattern

ORDERING INFORMATION

BILL OF MATERIALS

Table 1.

Quantity	Reference Designator	Description	Package
12	+IN2, +IN3, –IN2, –IN3, IN1+, IN1–, IN4+, IN4–, OUT1, OUT2, OUT3, OUT4	SMA/SMT	SMA/SMT
6	+VS, –VS, GND1, GND2, GND3, GND4	Test point	TP
2	C1, C2	10 μ F capacitor	3528
3	C3, C4, C5	Capacitor, user defined	C0805
36	R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, R21, R22, R23, R24, R25, R26, R27, R28, R29, R30, R31, R32, R33, R34, R35, R36	Resistor, user-defined	R0805
1	U1	Amplifier	14-lead SOIC

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**ESD Caution**

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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