eZ80F915005MODG

eZ80F91
Mini Enet Module

Product Specification

PS023603-0907

PRELIMINARY

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Revision History

Each instance in Revision History reflects a change to this document from its previous revision. For more details, refer to the corresponding pages and appropriate links in the table below.

Date	Revision Level	Description	Page No
August 2007	3	Changed eZ80F915005MOD to eZ80F915005MODG	i
August 2004	2	Added new dimensions figure for the module	All
May 2004	1	Original issue	All

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eZ80F91 Mini Enet Module

Zilog's eZ80F91 Mini Enet Module is a compact, high-performance Ethernet module specially designed for the rapid development and deployment of embedded systems requiring control and Internet/Intranet connectivity.

This expandable module is powered by Zilog's latest power-efficient, high-speed, optimized pipeline architecture eZ80F91 microcontroller, a member of Zilog's family of eZ80Acclaim!® Flash Microcontrollers.

The eZ80F91 is a high-speed single-cycle instruction-fetch microcontroller, which can operate with a clock speed of 50 MHz. It can operate in Z80®-compatible addressing mode (64 KB) or full 24-bit addressing mode (16 MB).

The rich peripheral set of eZ80F91 Mini Enet Module makes it suitable for a variety of applications, including industrial control, IrDA connectivity, communication, security, automation, point-of-sale terminals, and embedded networking applications.

Module Features

Features of eZ80F91 Mini Enet Module include:

- Factory-default 5 MHz crystal oscillator input, 50 MHz maximum operating speed via PLL
- 10/100 Base-T Ethernet PHY with RJ45 connector
- 128 KB fast external SRAM
- 256 KB on-chip Flash memory
- 8 KB on-chip SRAM
- Real-time clock support
- I/O connector provides 32 general-purpose 5 V-tolerant I/O pinouts
- Onboard connector provides I/O bus for external peripheral connections (IRQ, $\overline{CS}$, 24 address, 8 data)
- Connection to eZ80Acclaim! development platform via two 56-pin mini-headers
- Small footprint 50 mm x 47.5 mm
- 3.3 V power supply
- Standard operating temperature range: 0 ºC to +70 ºC

eZ80F91 Controller Features

Features of eZ80F91 Controller includes:

- The eZ80F91 device contains 256 KB of Flash memory and 8 KB of SRAM
- Single-cycle instruction fetch, high-performance, pipelined eZ80® CPU core
- 10/100 Mbps Ethernet MAC with 8 KB frame buffer
- Low power features including SLEEP mode, HALT mode, and selective peripheral power-down control
- Two UARTs with independent baud rate generators and support for 9-bit operation
- SPI with independent clock generator
- I^2C with independent clock generator
- Infrared Data Association (IrDA)-compliant infrared encoder/decoder
- DMA-like eZ80 instructions for efficient block data transfer
- External interface with 4 chip selects, individual wait state generators, and an external WAIT input pin — supports Intel- and Motorola-style buses
- Flexible-priority vectored interrupts (both internal and external) and interrupt controller
- Real-time clock with on-chip 32 kHz oscillator, selectable 50/60 Hz input, and separate V_{DD} pin for battery backup
- Four 16-bit Counter/Timers with prescalers and direct input/output drive
- Watchdog Timer
- 32 bits of general-purpose I/O
- JTAG and ZDI debug interfaces
- 144-pin BGA package
- 3.0–3.6 V supply voltage with 5 V tolerant inputs
- Standard operating temperature range: 0 ºC to +70 ºC

Block Diagram

Figure 1 displays a block diagram of the eZ80F91 Mini Enet Module.

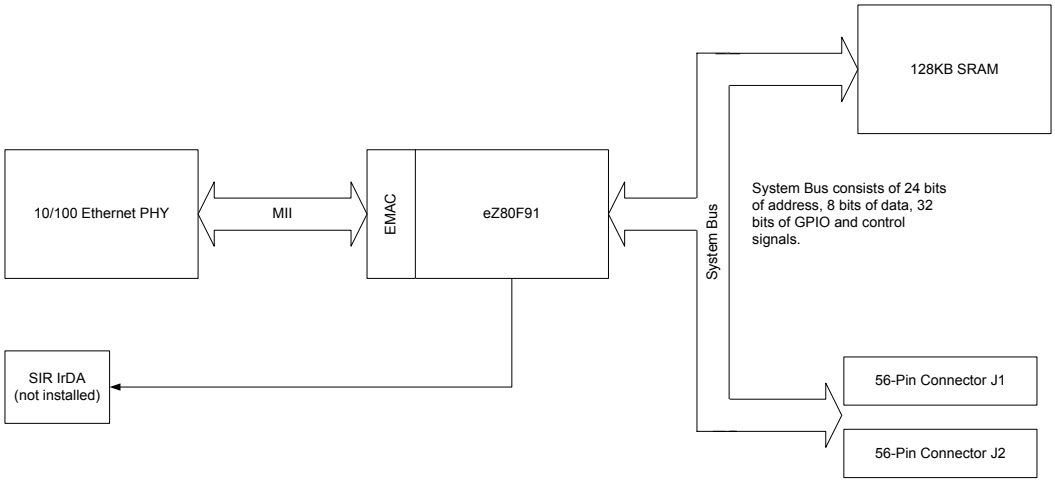


Figure 1. eZ80F91 Mini Enet Module Functional Block Diagram

Pin Description

Mini Module Connector J1 – Peripheral Bus

Figure 2 illustrates the pin layout of the 56-pin Peripheral Bus Connector (J1) of the eZ80F91 Mini Enet Module. The eZ80F91 Mini Enet Module is designed to connect to your applications via connectors J1 and J2, where the entire system bus and I/O port signals are available. The module is also compatible with Zilog's eZ80F91 Modular Development System (eZ80F910100KIT). Table 1 on page 5 lists the pins and their functions.

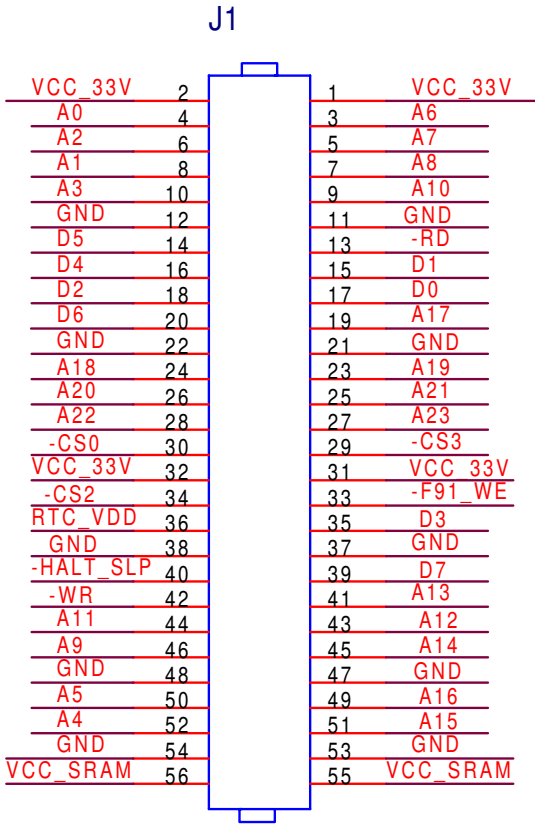


Figure 2. eZ80F91 Mini Enet Module Peripheral Bus Mini Connector Pin Configuration—J1

Note: *All signals with an overline are active Low. For example, B/$\overline{W}$, for which WORD is active Low, and $\overline{B}$/W, for which BYTE is active Low.*

Table 1. eZ80Acclaim! Development Platform Peripheral Bus Connector J1 Identification[1,2]

Pin No	Symbol	Signal Direction	Active Level	eZ80F91 Signal	Comments
3	A6	Bidirectional	n/a	Yes	
4	A0	Bidirectional	n/a	Yes	
5	A7	Bidirectional	n/a	Yes	
6	A2	Bidirectional	n/a	Yes	
7	A8	Bidirectional	n/a	Yes	
8	A1	Bidirectional	n/a	Yes	
9	A102	Bidirectional	n/a	Yes	
10	A3	Bidirectional	n/a	Yes	
13	$\overline{RD}$	Output	Low	Yes	
14	D5	Bidirectional	n/a	Yes	
15	D1	Bidirectional	n/a	Yes	
16	D4	Bidirectional	n/a	Yes	
17	D0	Bidirectional	n/a	Yes	
18	D2	Bidirectional	n/a	Yes	
19	A17	Bidirectional	n/a	Yes	
20	D6	Bidirectional	n/a	Yes	
23	A19	Bidirectional	n/a	Yes	
24	A18	Bidirectional	n/a	Yes	
25	A21	Bidirectional	n/a	Yes	
26	A20	Bidirectional	n/a	Yes	

Notes
1. For the sake of simplicity in describing the interface, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80F91 Mini Enet Module schematics on pages 16 through 17.
2. Additional note: external capacitive loads on $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$, $\overline{MREQ}$, D0–D7 and A0–A23 should be below 10 pF to satisfy the timing requirements for the eZ80 CPU. All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels to reduce power consumption and to reduce noise sensitivity. To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80F91's Peripheral Power-Down Register.

Table 1. eZ80Acclaim! Development Platform Peripheral Bus Connector J1 Identification[1,2] (Continued)

Pin No	Symbol	Signal Direction	Active Level	eZ80F91 Signal	Comments
27	A23	Bidirectional	n/a	Yes	
28	$\overline{CS0}$	Output	Low	Yes	
29	$\overline{CS3}$	Output	Low	Yes	
33	$\overline{F91_WE}$	Input	Low	No	Jumper on board
34	$\overline{CS0}$	Output	Low	Yes	
35	D3	Bidirectional	n/a	Yes	
36	RTC_V_{DD}	Input	n/a	Yes	
39	D7	Bidirectional	n/a	Yes	
40	$\overline{HALT_SLP}$	Output	Low	Yes	
41	A13	Bidirectional	n/a	Yes	
42	$\overline{WR}$	Ouput	Low	Yes	
43	A12	Bidirectional	n/a	Yes	
44	A11	Bidirectional	n/a	Yes	
45	A14	Bidirectional	n/a	Yes	
46	A9	Bidirectional	n/a	Yes	
49	A16	Bidirectional	n/a	Yes	
50	A5	Bidirectional	n/a	Yes	
51	A15	Bidirectional	n/a	Yes	
52	A4	Bidirectional	n/a	Yes	

Notes
1. For the sake of simplicity in describing the interface, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80F91 Mini Enet Module schematics on pages 16 through 17.
2. Additional note: external capacitive loads on $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$, $\overline{MREQ}$, D0–D7 and A0–A23 should be below 10 pF to satisfy the timing requirements for the eZ80 CPU. All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels to reduce power consumption and to reduce noise sensitivity. To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80F91's Peripheral Power-Down Register.

Mini Module Connector J2 – I/O Ports

Figure 3 illustrates the pin layout of the 56-pin I/O Connector (J2) of the eZ80F91 Mini Enet Module. The eZ80F91 Mini Enet Module is designed to connect to your applications via connectors J1 and J2, where the entire system bus and I/O port signals are available. The module is also compatible with Zilog's eZ80F91 Modular Development System (eZ80F910100KIT). Table 2 on page 8 lists the pins and their functions.

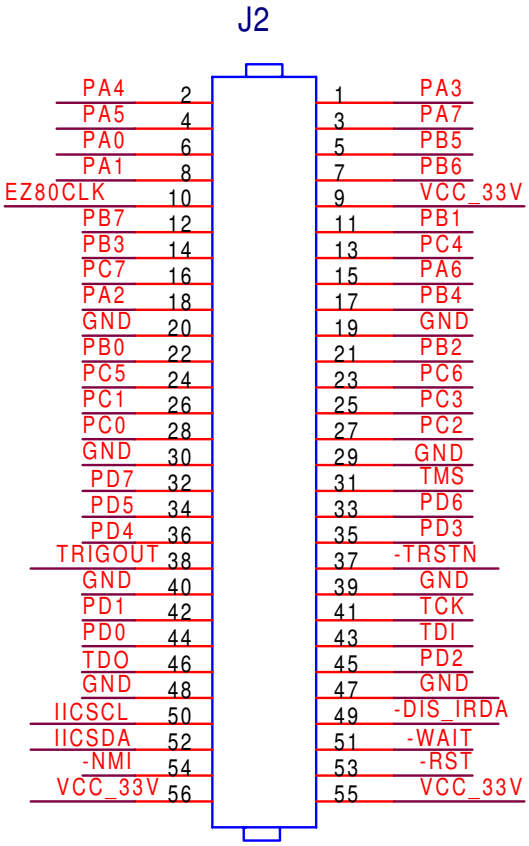


Figure 3. eZ80F91 Mini Enet Module I/O Mini Module Connector Pin Configuration—J2

Table 2. eZ80Acclaim! Development Platform/O Mini-Module Connector J2 Identification[1]

Pin No	Symbol	Signal Direction	Active Level	eZ80F91 Signal[2]
1	PA3	Bidirectional	n/a	Yes
2	PA4	Bidirectional	n/a	Yes
3	PA7	Bidirectional	n/a	Yes
4	PA5	Bidirectional	n/a	Yes
5	PB5	Bidirectional	n/a	Yes
6	PA0	Bidirectional	n/a	Yes
7	PB6	Bidirectional	n/a	Yes
8	PA1	Bidirectional	n/a	Yes
10	EZ80CLK	Output	n/a	Yes
11	PB1	Bidirectional	n/a	Yes
12	PB7	Bidirectional	n/a	Yes
13	PC4	Bidirectional	n/a	Yes
14	PB3	Bidirectional	n/a	Yes
15	PA6	Bidirectional	n/a	Yes
16	PC7	Bidirectional	n/a	Yes
17	PB4	Bidirectional	n/a	Yes
18	PA2	Bidirectional	n/a	Yes
21	PB3	Bidirectional	n/a	Yes
22	PB0	Bidirectional	n/a	Yes
23	PC6	Bidirectional	n/a	Yes
24	PC5	Bidirectional	n/a	Yes
25	PC3	Bidirectional	n/a	Yes
26	PC1	Bidirectional	n/a	Yes
27	PC2	Bidirectional	n/a	Yes
28	PC0	Bidirectional	n/a	Yes

Notes
1. For the sake of simplicity in describing the interface, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80F91 Mini Enet Module schematics on pages 16 through 17.
2. The Power and Ground nets are connected directly to the eZ80F91 device.

Table 2. eZ80Acclaim! Development Platform/O Mini-Module Connector J2 Identification[1] (Continued)

Pin No	Symbol	Signal Direction	Active Level	eZ80F91 Signal[2]
31	TMS	Input	n/a	Yes
32	PD7	Bidirectional	n/a	Yes
33	PD6	Bidirectional	n/a	Yes
34	PD5	Bidirectional	n/a	Yes
35	PD3	Bidirectional	n/a	Yes
36	PD4	Bidirectional	n/a	Yes
37	$\overline{\text{TRSTN}}$	Input	Low	Yes
38	TRIGOUT	Output	n/a	Yes
41	TCK	Input	n/a	Yes
42	PD1	Bidirectional	n/a	Yes
43	TDI	Bidirectional	n/a	Yes
44	PD0	Bidirectional	n/a	Yes
45	PD2	Bidirectional	n/a	Yes
46	TDO	Output	n/a	Yes
49	$\overline{\text{DIS_IRDA}}$	Input	Low	No
50	IICSCL	I/O	n/a	Yes
51	$\overline{\text{WAIT}}$	Input	Low	Yes
52	IICSDA	I/O	n/a	Yes
53	$\overline{\text{RST}}$	I/O	Low	Yes
54	$\overline{\text{NMI}}$	Input	Low	Yes

Notes
1. For the sake of simplicity in describing the interface, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80F91 Mini Enet Module schematics on pages 16 through 17.
2. The Power and Ground nets are connected directly to the eZ80F91 device.

Onboard Component Description

I/O Connector

The I/O connector features 32 general-purpose 3.3 V CMOS I/O pins that can be used as outputs or inputs interfacing to external logic. All I/Os are 5 V tolerant. Some of the general-purpose I/O pins support dual mode functions (SPI, Timer I/O, UARTs and bit I/O with edge- or level-triggered interrupt functions on each pin). For more information on eZ80F91 dual modes, refer to *eZ80F91 Product Specification (PS0192)*.

Peripheral Bus Connector

The peripheral bus connector features 24-pins that provide access to the eZ80F91 Mini Enet Module address bus and 8-pins that provide access to the module data bus. For more information on eZ80F91 address and data buses, refer to *eZ80F91 Product Specification (PS0192)*.

Ethernet PHY and RJ45 Connector

The eZ80F92 Ethernet Module contains a Micrel KS8721BL 10/100 Ethernet PHY with Media Independent Interface (MII) and a HALO RJ45 with integrated magnetics and two LEDs (transformer and common-mode chokes).

The eZ80F92 Ethernet Module defaults to 10 Mbps, which works in either a 100 Mbps or a 10 Mbps network. Software can also configure the PHY for 100 Mbps or autosense.

Ethernet LEDs

The Ethernet connection is provided by the HALO RJ45 connector. It contains two green LEDs that are located next to each other on the eZ80F91 Mini Enet Module. When PHY is receiving data, the left LED is on. When the PHY is transmitting data, the right LED is on.

5 MHz Clock

The eZ80F91 Mini Enet Module contains a 5 MHz crystal oscillator (Y2) which is multiplied by the phase-locked loop in the eZ80F91 MCU to create a 50 MHz system clock

Memory

The eZ80F91 MCU contains 256 KB of internal Flash memory. Additional memory can be accommodated via the system bus on connectors J1 and J2. To program the on-chip Flash memory, install jumper JP1 on the mini module. Table 3 lists the status of the jumper.

Table 3. Shunt JP1, eZ80F91 Mini Enet Module

Symbol	Jumper Name	Shunt Status	Function	Affected Device
JP1	$\overline{\text{F91_WE}}$	In (Default)	On-chip Flash is enabled for writing to boot block.	On-chip Flash
		Out	On-chip Flash memory boot block is write-protected.	On-chip Flash

There is 128 KB of fast SRAM on the eZ80F91 Mini Enet Module. Access time is 12 ns, which requires one wait-state access. The eZ80F91 on-chip SRAM can be used with zero wait states.

IrDA Transceiver

The eZ80F91 Mini Enet Module is shipped without an IrDA transceiver installed.

If you install an on-board transceiver, such as the Zilog ZHX1810, it is connected to PD0 (TX), PD1 (RX), and PD2 (Shutdown, IR_SD). The IrDA transceiver is of the LED type 870 nm Class 1.

The IrDA transceiver is accessible via the IrDA controller attached to UART0 on the eZ80F91 device.

To use the UART0 for console or to save power, the transceiver is disabled by the software or by an off-board signal when using the proper jumper selection. The transceiver is disabled by setting PD2 (IR_SD) High or by pulling the $\overline{\text{DIS_IRDA}}$ pin on the I/O connector Low. The shutdown is used for power savings. To enable the IrDA transceiver, $\overline{\text{DIS_IRDA}}$ is left floating and PD2 is set to Low.

Serial Interface Ports

The eZ80F91 MCU contains two UARTs with programmable baud rate generators. UART0 is connected to GPIO PD[0:7] on the I/O connector. UART1 is connected to GPIO PC[0:7] on the I/O connector.

Note: *Do not connect an RS232 interface without level shifters. There are no RS232-level shifters on the eZ80F91 Mini Enet Module.*

Physical Dimensions

The footprint of the eZ80F91 Mini Enet Module PCB is 2.00 " x 1.90 ". See Figure 4 for dimensions and top-layer silkscreen.

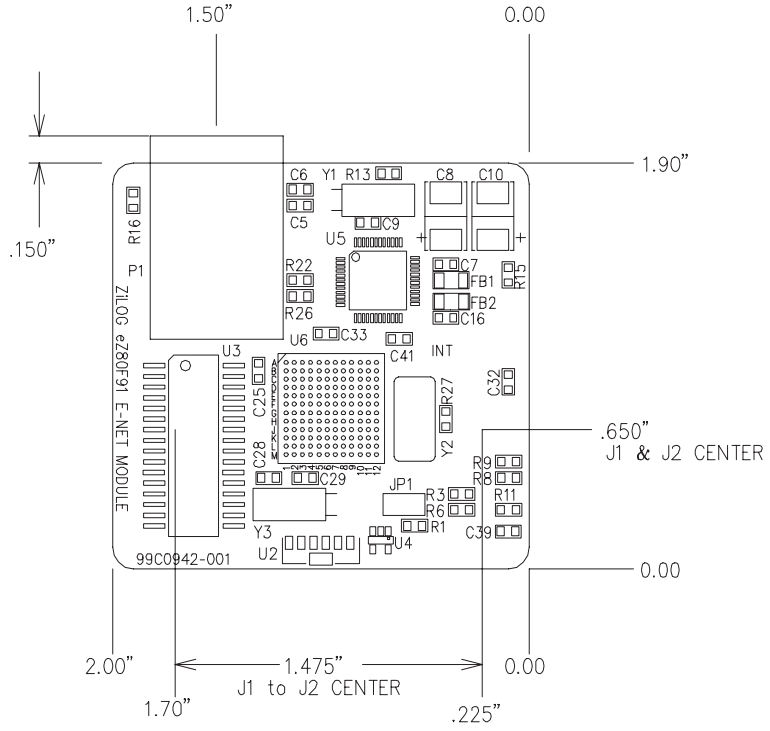


Figure 4. Physical Dimensions of the eZ80F91 Mini Enet Module

Absolute Maximum Ratings

The stress greater than those listed in Table 4 can cause permanent damage to the device. These ratings are stress ratings only. Operation of the device at any condition outside those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. For improved reliability, unused inputs should be tied to one of the supply voltages (V_{DD} or V_{SS}).

Table 4. Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units
Standard operating temperature	0	+70	ºC
Storage temperature	–45	+85	ºC
Operating Humidity (RH @ 50ºC)	25%	90%	
Operating Voltage	—	3.6	V

Module Bill of Materials

Table 5 lists the installed components of the eZ80F91 Mini Enet Module.

Table 5. Bill of Materials for the eZ80F91 Mini Enet Module,

ITEM	PART NUMBER	DESCRIPTION	QTY	LOCATION
1	98C0942-001	FAB,eZ80F91 ETHERNET MODULE, REV B Coastal Circuits	1	
2	35-0016-06	IC,74LVC3G04,3.3V,GATE,8-SSOP TEXAS INSTR SN74LVC3G04DCTR	1	U1
3	35-0179-12	IC,SRAM,128Kx8,12ns,3V,32-SOJ IDT IDT71V124SA12Y	1	U3
4	35-0062-03	IC,74AHC1G32,SNGL QUAD OR,SOR23-5 TEXAS INSTR SN74AHC1G32DBVR	1	U4
5	35-0022-02	IC,KS8721BL,PHY XCVR,48-LQFP MICREL SEMI KS8721BL	1	U5
6	EZ80F91	IC,eZ80F91,50MHZ,144BGA ZiLOG EZ80F91NA050SC	1	U6
7	17-2005-83	CAP,0.33UF,16V,CER CHIP,0603 PANASONIC ECJ-1VF1C334Z	1	C1
8	17-2005-70	CAP,1,000PF,50V,CER CHIP,0603 PANASONIC ECJ-1VC1H561J	11	C2,C18,C25-33
9	17-2005-66	CAP,0.1UF,16V,CER CHIP,0603 KEMET C0603C104K5RAC	14	C3,C7,C9,C13-17, C21,C24,C38-41
10	17-2001-05	CAP,22PF,50V,CER CHIP,0603 PANASONIC ECJ-1VC1H220J	4	C5,C6,C51,C52
11	17-0018-20	CAP,10UF,25V,TANT CHIP,SMT PANASONIC ECSH1ED106R	2	C8,C10
12	17-2005-63	CAP,0.056UF,50V,CER CHIP,0603 PANASONIC ECJ-1VB1C563K	1	C11
13	17-2001-20	CAP,270PF,50V,CER CHIP,0603 PANASONIC ECJ-1VC1H271J	1	C12
14	17-0018-47	CAP,47UF,16,TANT CHIP,SMT PANASONIC ECS-T1CD476R	2	C19,C20
15	17-2001-04	CAP,18PF,50V,CER CHIP,0603 PANASONIC ECJ-1VC1H180J	2	C22,C23
16	17-9009-10	FERRITE BEAD,3AMP,100 OHM,1206 SMT STEWARD HI1206N101R-00	2	FB1,FB2
17	46-3001-03	RES,10K OHM,1%,1/16W,0603 SMT	6	R1,R7-9,R11,R12
18	46-3000-79	RES,4.75K OHM,1%,1/16W,0603 SMT	3	R2,R3,R26
19	46-3000-35	RES,68 OHM,1%,1/16W,0603 SMT	1	R4
20	46-3000-02	RES,2.2 OHM,1%,1/16W,0603 SMT	1	R5
21	46-3000-71	RES,2.21K OHM,1%,1/16W,0603 SMT	1	R6
22	46-3000-83	RES,6.81K OHM,1%,1/16W,0603 SMT	1	R13
23	46-3000-63	RES,1K OHM,1%,1/16W,0603 SMT	2	R15,R16
24	46-3000-56	RES,499 OHM,1%,1/16W,0603 SMT	1	R18
25	46-3000-27	RES,33.2 OHM,1%,1/16W,0603 SMT	1	R19
26	46-3000-32	RES,49.9 OHM,1%,1/16W,0603 SMT	4	R20,R21,R22,R25
27	46-3000-47	RES,221 OHM,1%,1/16W,0603 SMT	2	R23,R24
28	46-3001-27	RES,100K OHM,1%,1/16W,0603 SMT	1	R27
29	23-0006-25	XTAL,25.0000MHZ,18PF,CYL EPSON CA-301 25.0000M-C	1	Y1

Table 5. Bill of Materials for the eZ80F91 Mini Enet Module (Continued)

ITEM	PART NUMBER	DESCRIPTION	QTY	LOCATION
30	23-0000-05	**XTAL,5.0000MHZ,SER/RESN,HC49US** CITIZEN HC49US5.000MABJ	1	Y2
31	23-0006-00	**XTAL,32.768KHZ,SER/RESN,TF CASE** FOX NC38-32.768KHZ OR ECS ECS-3X8	1	Y3
32	21-8010-56	**CONN,56-CKT,.8mm,HDR/PIN** SAMTEC FTE-128-01-G-DV-A	2	J1,J2
33	21-0055-01	**CONN,HDR/PIN,.025SQ,SNGL ROW** HARWIN M-20-977-3622	0.1	JP1
34	21-0907-01	**CONN,RJ45,FASTJACK,10/100BASE-T** HALO ELECTRONICS HFJ11-2450E-L11	1	P1
35	21-0192-00	**SHUNT,2-POS,.1 CNTR,LOW PRFL** AMP 382811-5	1	JP1

Schematics

Figures 5 and 6 describe the layout of the eZ80F91 Mini Enet Module. Ethernet circuiting devices are not loaded on the eZ80F91 Mini Enet Module. However, these devices appear in the following schematics for reference purposes.

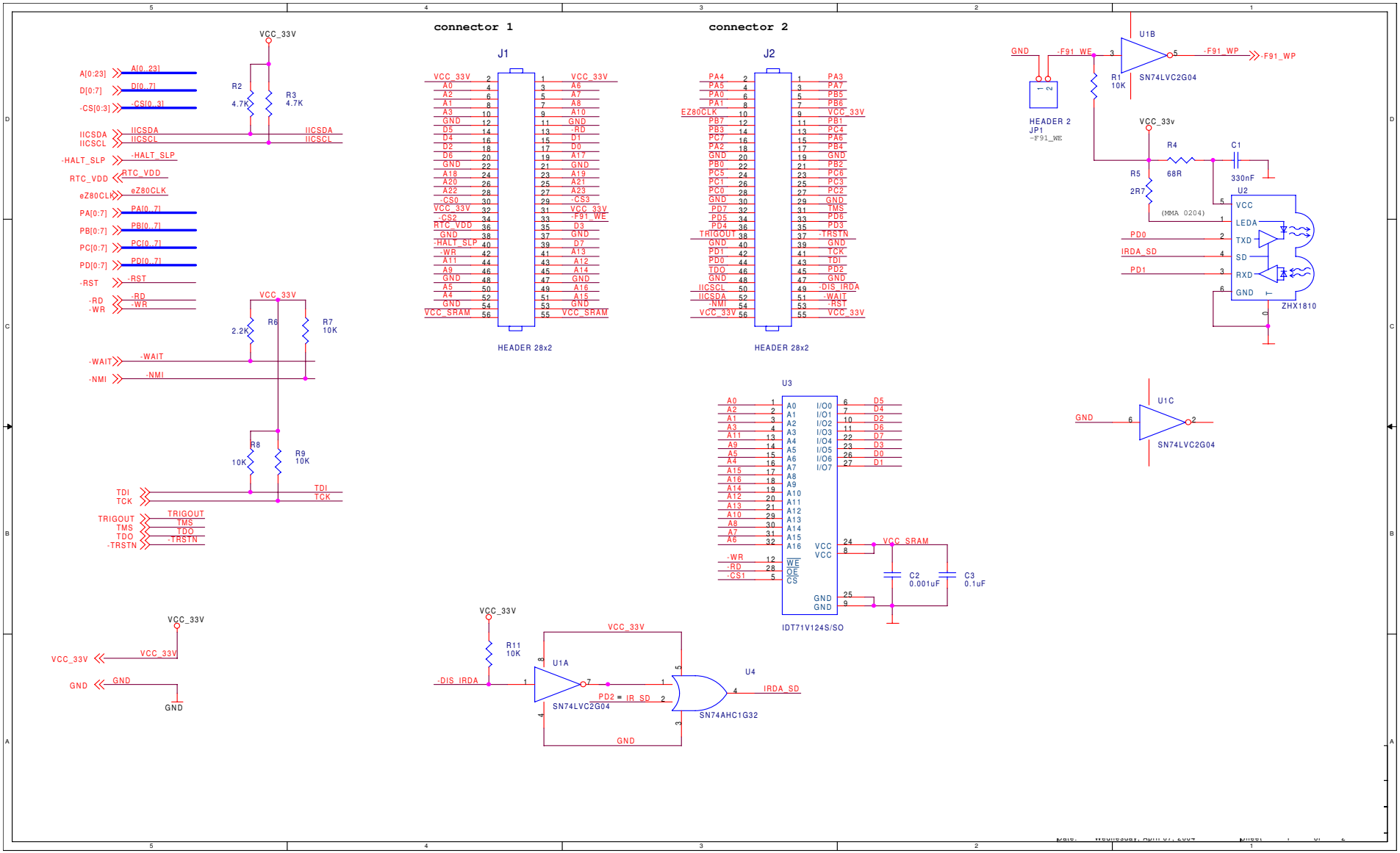


Figure 5. eZ80F91 Mini Enet Module Schematic Diagram, #1 of 2—Connectors and Miscellaneous

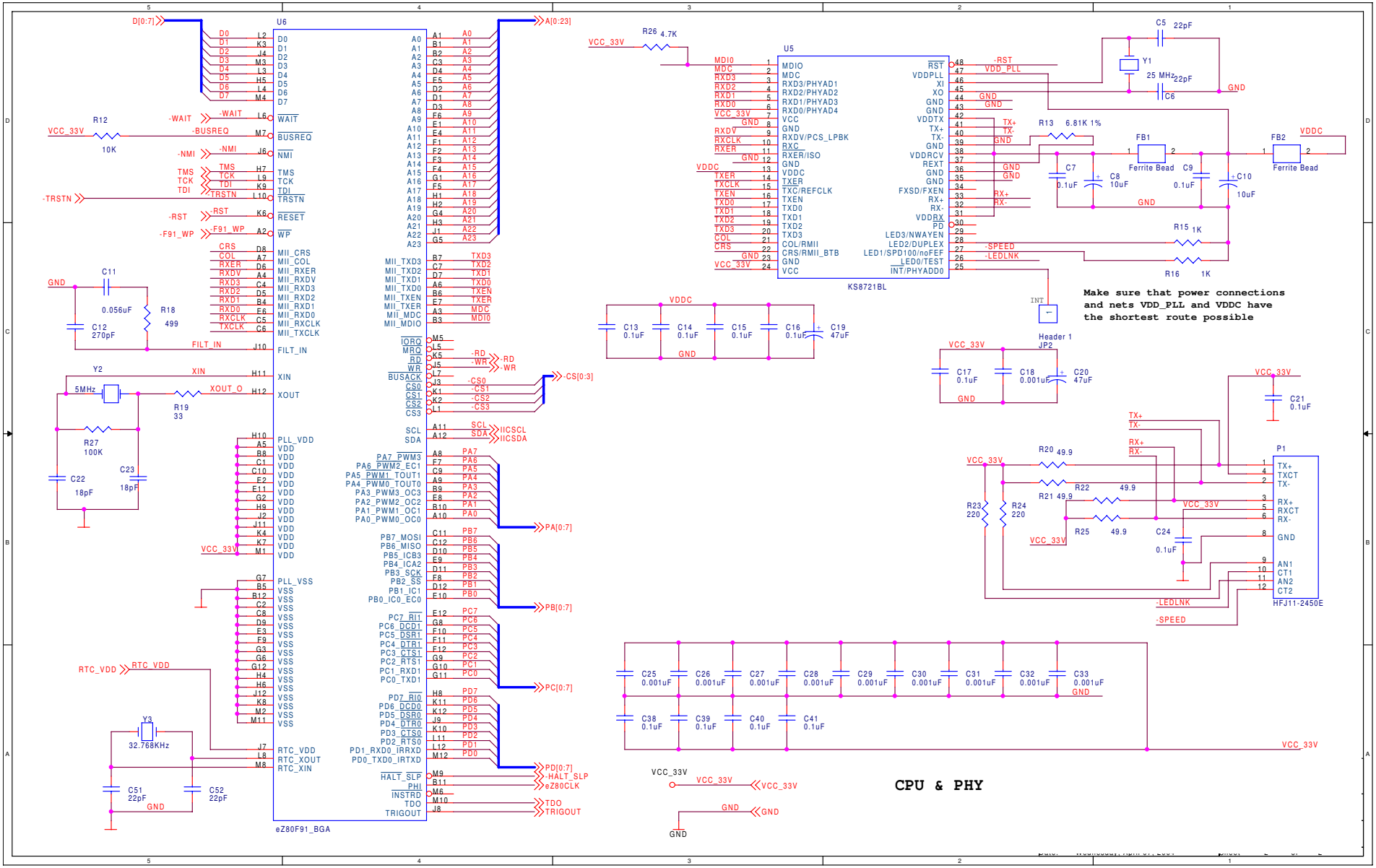


Figure 6.eZ80F91 Mini Enet Module Schematic Diagram, #2 of 2—CPU and PHY

Customer Support

For answers to technical questions about the product, documentation, or any other issues with Zilog's offerings, please visit Zilog's Knowledge Base at http://www.zilog.com/kb.

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