General Description

The IXDP610 Digital Pulse Width Modulator (DPWM) is a programmable CMOS LSI device, which accepts digital pulse width data from a microprocessor and generates two complementary non-overlapping pulse width modulated signals for direct digital control of a switching Power Bridge or other electronics. See the IXDP610 data sheet for full specifications.

The EVDP610 Evaluation Board, shown in Figure 1 below, encompasses the serial communications hardware, microprocessor, and IXDP610 chip all onto one board that is easily programmable from any PC. A Graphical User Interface (GUI) designed to run on a Windows 9X, Windows 2000 or Windows NT operating system is included with the EVDP610, providing the designer with the software and hardware tools to immediately test and evaluate the IXDP610 IC. A functional block diagram of the EVDP610 is shown in Figure 2.

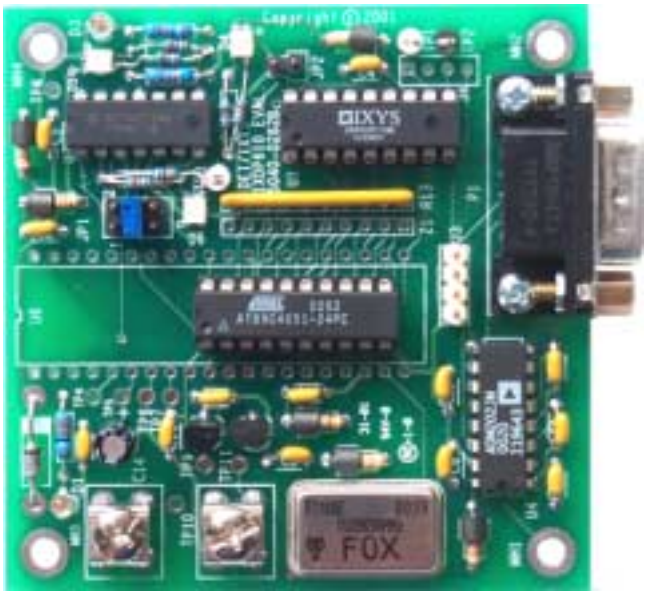

Figure 1 - EVDP610 Evaluation Board

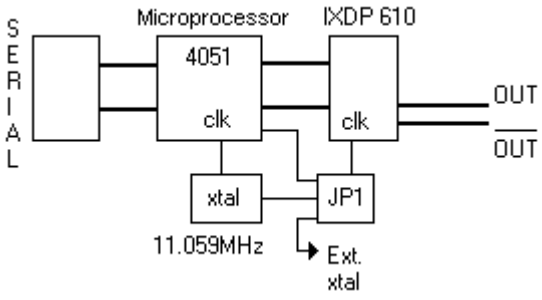

Figure 2 - EVDP610 Functional Block Diagram

1.0 EVDP610 QUICK-START INSTRUCTIONS

These quick-start instructions provide a step-by-step guide to set up and begin using the EVDP610 evaluation board and software. Please refer to the appropriate sections of the specification for additional instructions and guidelines.

1.1 Installing the IXDP610 Evalution Software

To install the Evaluation Software on the comuter, place the Evaluation Software diskette into the computer's disk drive. Run setup.exe (or double-click on the setup icon). Follow the instructions that appear on the screen.

1.2 Powering On the IXDP610 Evaluation Board

1. Connect +5 volts DC (+/- 5%) power to the two screw terminals labeled TRM1 and TRM 2. TRM 1 is the power terminal and TRM 2 is the ground terminal. When power is applied the two green LEDs labeled D1 and D3 will turn on.
2. By default, the evaluation board firmware loads the pulse width registers of the IXDP610 with a 0% duty cycle on Output1 and a 100% duty cycle on Output2 (Output1 is labeled TP1 – with a white terminal attached and Output2 is labeled TP2 – with a black terminal attached). The LED's labeled D4 and D5, corresponding to Output1 and Output2 respectively, should glow red when the output is disabled. When the outputs are enabled, the LEDs will glow green.

1.3 Connecting the Serial Communications

1. Connect one end of the null modem cable (provided with the EVDP610) to the male DB9 connector on the circuit board (labeled P1) and connect the other end to the serial port. The pin-out of the null modem cable is shown in the figure 3 below.

1.4 Checking Jumper Connections

1. There should be a jumper in the middle position on JP1 (allowing the 11.059MHz clock – the same one clocking the micro, to clock the IXDP610 chip). See section 2.3 for more information and a detailed drawing of the jumper positions.

2. There should be NO jumper in JP2 – installing this jumper disables all outputs on the IXDP610 by asserting the ODIS pin. The factory default is no jumper in JP2.

1.5 Operating the User Interface Software

1. The IXDP610 hardware must be powered on before running the GUI. In the GUI's initialization sequence the GUI will try to communicate with the EVDP610 hardware. Be aware that the GUI will reset the EVDP610 hardware as soon as it comes up and is

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running after establishing communication. This assures that both the board and the software are initialized into the same states to avoid confusion.

2. Make sure that the board is in 8 bit resolution mode by checking the resolution button (8 bit resolution is the board's default state). Flip the switch in the Pulse Settings area so that the pulse width test box is now no longer dimmed. Enter a number into this text box between 0 – 255. The duty cycle textbox will change accordingly although it will remain dimmed until the switch is toggled, ie: if you enter a 128, the duty cycle will read 50%.

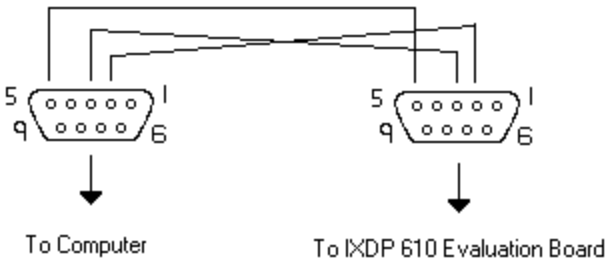
2.0 GENERAL DESCRIPTION AND THEORY OF OPERATION

For circuit design information, refer to the EVDP610 schematic and PCB layout drawing in Figures 7 and 8.

2.1 Serial Communications

The RS-232 communications interface allow the EVDP610 to communicate and respond to commands through a serial port. The serial bus operates at 9600 baud and is buffered by an RS232 driver before reaching the microprocessor. For more specific information on the serial protocol please see Section 4.

To communicate with and control the EVDP610 Board, a null modem cable (included) must be connected from a PC's serial port to the male DB9 connector on the board. For user reference a pin out of the cable is shown in Figure 3. Once the correct communications port is selected, the user can run all of the features of the IXDP610 chip from the GUI.



Female DB9 (computer)	Female DB9 (EVDP610 board)	Description
Pin 2	Pin 3	TX
Pin 3	Pin 2	RX
Pin 5	Pin 5	GND

Figure 3 - Null Modem Cable Pin-Out

The GUI software allows the user to set all functions provided on the IXDP610 with the simple click of a button or writing into a text box.

In this manner the user can easily set pulse width, dead time, resolution, among other functions such as dividing the clock signal.

2.2 IXDP610 IC

The IXDP610 chip, labeled U1 on the evaluation board, generates two complementary non-overlapping, pulse width modulated signals for direct digital control of a switching power bridge.

2.2.1 Dead Time

The PWM waveform generated by the IXDP610 results from comparing the output of the Pulse Width counter to the number stored in the Pulse Width Latch. A programmable "dead-time" (defined as t_{DT} in Fig.4) is incorporated into the PWM waveform. The Dead-Time Logic disables both outputs on each transition of the comparator output for the required dead-time interval. This feature is difficult to duplicate in equivalent analog system.

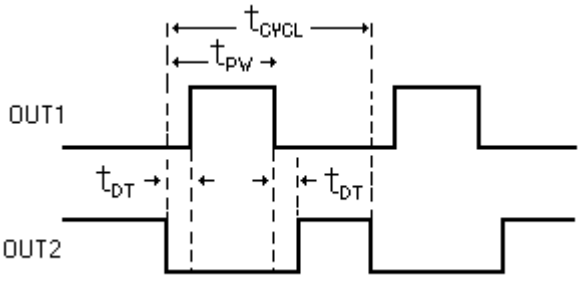


Figure 4: Output Waveform Displaying Dead-Time

For example, in a half bridge system the dead time can prevent two transistors being on at the same time. If both transistors are on for a short period of time, they could effectively short the voltage supple to ground, which is an undesirable situation.

2.2.2 Lock Bit

Setting the lock bit of the IXDP610 prevents all writes to the control latch except for the Stop bit. This locking feature prevents modification of the control latch due to software error, preventing damage to the system being controlled by the IXDP610. This prevents changing of the dead-time, clock divide, and resolution settings.

2.2.3 Clock Divide Bit

This feature allows the IXDP610 to divide the input clock by one or divided by two.

2.2.4 Resolution

The IXDP610 can run in two resolution modes, 8-bit and 7-bit. Choosing 7-bit resolution doubles the achievable PWM base frequency at the expense of decreased duty cycle resolution. With the combination of the Divide bit (labeled Clock Divide on the GUI) and the resolution bit,

the user can choose between three different PWM base periods for any given external CLOCK frequency.

When the IXDP610 is programmed in 8-bit mode, the PWM base period is equal to 256 PWM clock cycles. In 7-bit mode the PWM base period is equal to 128 PWM clock cycles. A PWM clock cycle is equal to one external CLOCK period when the clock is divided by one. The following formulas can be used to determine the PWM base period:

If 7-bit resolution and clock divide by 1 -> PWM base period = CLOCK period x 128

If 8-bit resolution and clock divide by 1 -> PWM base period = CLOCK period x 256

If 7-bit resolution and clock divide by 2 -> PWM base period = CLOCK period x 256

If 8-bit resolution and clock divide by 2 -> PWM base period = CLOCK period x 512

2.2.5 Stop
This bit in the control latch of the IXDP610 enables and disables the outputs. When enabled, the outputs will not be re-enabled until the start of the PWM period.

2.2.6 ODIS : Output Disable
Referred to as the OUPUT DISABLE pin, this pin on the IXDP610 is connected to a jumper on the board (labeled JP2), which is tied to a pull-up resistor before the jumper is installed. Installing a jumper onto these pins asserts the ODIS pin (ties the pull-up to ground putting a low signal onto ODIS). Asserting ODIS, or the OUTPUT DISABLE pin, on the IXDP610 forces the complementary outputs to be immediately disabled (forced low). These outputs will remain low as long as this input is asserted, and for the duration of the PWM cycle in which OUTPUT DISABLE goes from low to high; i.e., the complementary outputs are not re-enabled until the beginning of the next PWM cycle, and then only if the both ODIS and Stop are not enabled.

*For more information on technical specifications of the IXDP610 IC, please see the IXDP610 documentation which can be downloaded from the IXYS website (www.ixys.com).

2.2 Outputs
The IXDP610 chip, labeled U1 on the evaluation board, and its complementing outputs (labeled TP1 and TP2) can be accessed either with the black and white terminals provided or by J4, which accommodates a four pin header. Pin one and three on the header are the output signals and pins 2 and 4 are connected to ground. Pin 1 on the board is indicated by the square via. This provides easy access for outside wires or a wiring harness to connect to another board.

2.3 Input Clock Selection and Jumper Settings
The evaluation board has 3 jumper settings (labeled JP1 on the board) that allow the user to switch between three input clock selections:

1) Using the microprocessor to clock the IXDP610.

2) Using the on-board 11.059 MHz to clock the IXDP610.

3) Hooking up an external clock signal. For this either wire the clock signal to the jumper itself or the user can use the TP3 via.

Figure 5 shows the placement of the jumper for each setting. Factory default is the middle setting, clocking the IXDP610 with the on-board 11.059MHz oscillator.

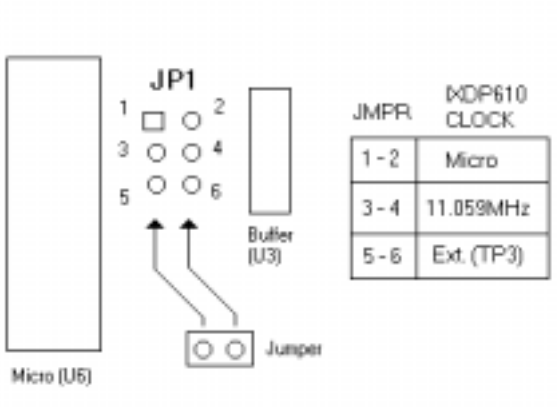


Figure 5: Placement of Jumper for IXDP610 Clock Selection

2.3.1 Using the Microprocessor as the Input Clock
The microprocessor on the evaluation board can be used as the clock signal into the IXDP610. This clock can provide output frequencies of 1 – 50 Hz on the IXDP610 chip. Due to interrupt latency this is as fast as the microprocessor can clock the IXDP610 and there is a +/- 3% frequency error associated with this arrangement.

2.3.2 Using the 11.059 MHz as the Input Clock
This is set as the factory default; it allows the same on-board oscillator that clocks the microprocessor to clock the IXDP610.

2.3.3 Using an External Clock Signal
Allowing the user to hook up an external clock signal allows any input clock (up to 50 MHz) to be used as input to the IXDP610. This results in output frequencies

up to 390KHz (in 7-bit resolution). The external clock can be installed into the via on the board labeled TP3.

3.0 GUI GENERAL DESCRIPTION AND USE

3.1 The GUI

After installing and starting up the GUI, figure 7 is the first screen that should appear. The Message box should read: "Welcome to the IXDP610 Test Environment" as seen in Figure 6. Be aware that when the GUI has established communication with the evaluation board, the GUI will reset the EVDP610 hardware to ensure that both the software and the hardware are in the same state.



Figure 6: The EVDP610 GUI GUI

3.1.1 Reset IXDP610

This toggle button will reset the EVDP610 board and the GUI back into their initial states. If the EVDP610 board's power has been cycled this button can be used to reset the GUI software. If for any reason the hardware and software disagree this button can be used to reinitialize the hardware and the software into the same state (the user will lose the current settings of the board).

3.1.2 Read IXDP610 Status

This toggle button will read the status of the EVDP610 board. It will update the GUI to the current Pulse Settings, Dead Time Settings, Lock Settings, and Output Settings. If for any reason the hardware and software disagree this button can be used to read what the hardware is doing and update the software.

3.1.3 Lock

This button will "lock" the control register of the IXDP610, which will not allow the dead-time period, clock divide, resolution or the stop bit to be changed. Hitting this button again, or hitting the RESET IXDP610 button will unlock the IXDP610.

3.1.4 Serial Settings

These buttons control the baud rate and the COM port selection (1 – 4). *Note: Baud rate is not variable and will remain dimmed.

3.1.5 Clock Settings

The CLOCK DIVIDE button will cause the input clock of the IXDP610 chip to be internally divided by 1 or by 2. The clock select button allows the microprocessor to control the input clock to the IXDP610, which can then be variably changed by the GUI. The output frequency ring allows the user to select the frequency of the output of the IXDP610 from 1 – 50 Hz. When the clock is selected the GUI will prompt the user to make sure of the correct jumper settings.

3.1.6 Pulse Settings

The Resolution toggle button allows the user to switch between seven-bit and eight-bit resolution on the EVDP610 board. The pulse width can be written to the IXDP610 by either the Duty Cycle or Pulse Width. One of these must be selected by the toggle switch. When Duty Cycle is selected and the user has entered a number into the Duty Cycle textbox the pulse width textbox will be updated with the actual number written into the pulse width latch of the IXDP610. Duty Cycle and Pulse Width are always calculated with respect to resolution, meaning if the value entered into Duty Cycle was 50%, in 7-bit mode the pulse width number will be 64 where as in 8-bit resolution the pulse width number will be 128. The pulse width text box will display the actual number written to the pulse width latch, whereas the duty cycle is calculated based on the entered values. Be aware that if you were to enter 128 in the pulse width textbox, in 8-bit resolution, the output duty cycle will be 50%. If the IXDP610 is switched into 7-bit resolution the pulse width number will remain the same, yet the duty cycle now becomes 100% and the GUI and the hardware will be updated with these values.

When the Read Pulse Settings button is pressed the evaluation board updates all pulse settings in the area.

3.1.7 Dead Time

Dead Time can either be entered manually or with the arrow buttons to the side of the test box. The Read Dead Time button updates the GUI from the evaluation board. For a detailed discussion on dead time please see section 2.2.1 or the IXDP610 specification.

3.1.8 Outputs Enable

The Outputs Enable button allows the user to turn on/off the outputs of the IXDP610. This button asserts the stop bit in the control latch of the IXDP610. When the outputs are enabled the status LED located directly above the button will light. The LED will turn off when the

outputs are not enabled or turned off.

3.1.9 Error Messages

If for some reason, the communication or instruction did not take place an error message will appear in the text box on the top of the GUI, or an error message panel will tell the user the proper actions to take. It is always a good idea to update the GUI after an error has occurred to prevent the board from differing from the GUI in any way. This maybe accomplished by hitting either the READ IXDP610 STATUS button or by hitting the RESET button (the current settings will be lost if RESET is used). Hit the close button on any error panels to close the panel.

4.0 SERIAL OPERATION

4.1 RS-232 Serial Operation

This remote control port allows a user to connect a personal computer as the remote host to the IXDP610. Utilizing a standard three wire interface and DEI's defined communication protocol the user can write a custom control program for their particular testing needs.

4.1.1 Serial Data Packets

The data packets sent to the IXDP610 over the serial bus should be of the following format:

To Address	From Address	Op Code	Data	Stop Byte

Where the data is as follows:

Data Byte	Function	Value
To Address	IXDP610 Address	0x02h
From Address	Remote Host Address	Variable [0 to255] Recommend 0x00h
Operation Code	The command hardware code	See Instruction Set
Data1	Any data to send to IXDP610	See Instruction Set
Stop Byte	Serial termination byte	0x0Ah

The data packets returned by the DEI IXDP610 will be of the following format:

To Address	From Address	Op Code	Data	Error Code	Stop Byte

Where the data is as follows:

Data Byte	Function	Value
To Address	Remote Host Address	Variable [0 to255] Recommend 0x00h
From Address	IXDP610 Address	0x02
Operation Code	The command hardware code	See Instruction Set
Data	Any data sent from the IXDP610	One unsigned byte
Error Code	Error is any non-zero byte, No Error = 0	See Error Code table
Stop Byte	Serial termination byte	0x0Ah

4.1.2 Common Instruction Set & Serial Data Packet Format:

Instruction	Opcode (hex)	Format (number of bytes=> all unsigned chars)
Get Version1	0x05	Send-5, Receive-6
Get Version2	0x06	Send-5, Receive-6
Set Dead Time	0x10	Send-5, Receive-6
Set Pulse Width	0x20	Send-5, Receive-6
Set Resolution	0x30	Send-5, Receive-6
Enable Outputs	0x40	Send-5, Receive-6
Reset	0x50	Send-5, Receive-6
Set Clock Divide	0x60	Send-5, Receive-6
Set Lockout	0x70	Send-5, Receive-6
Set Clock Select	0x80	Send-5, Receive-6
Read Pulse Width	0x90	Send-5, Receive-6
Read Resolution	0x93	Send-5, Receive-6
Read Lock Status	0x94	Send-5, Receive-6
Read Clock Divide	0x95	Send-5, Receive-6
Read Output Enable Status	0x96	Send-5, Receive-6

4.1.3 Common Error Codes

Error Code	Description	Problem	Action
0x00	No Error	N/A	Command was successful, no errors.
0xE0	General Internal Error	Timing Error on evaluation board	None Recommended – reset board. If error is repeatable contact factory.
0xE1	Invalid Opcode	Command Packet Incorrect or Corrupted	Verify packet data integrity with emphasis on op-code byte.
0xE2	Control Latch locked	Can't write to control latch	Unlock control latch or reset board.

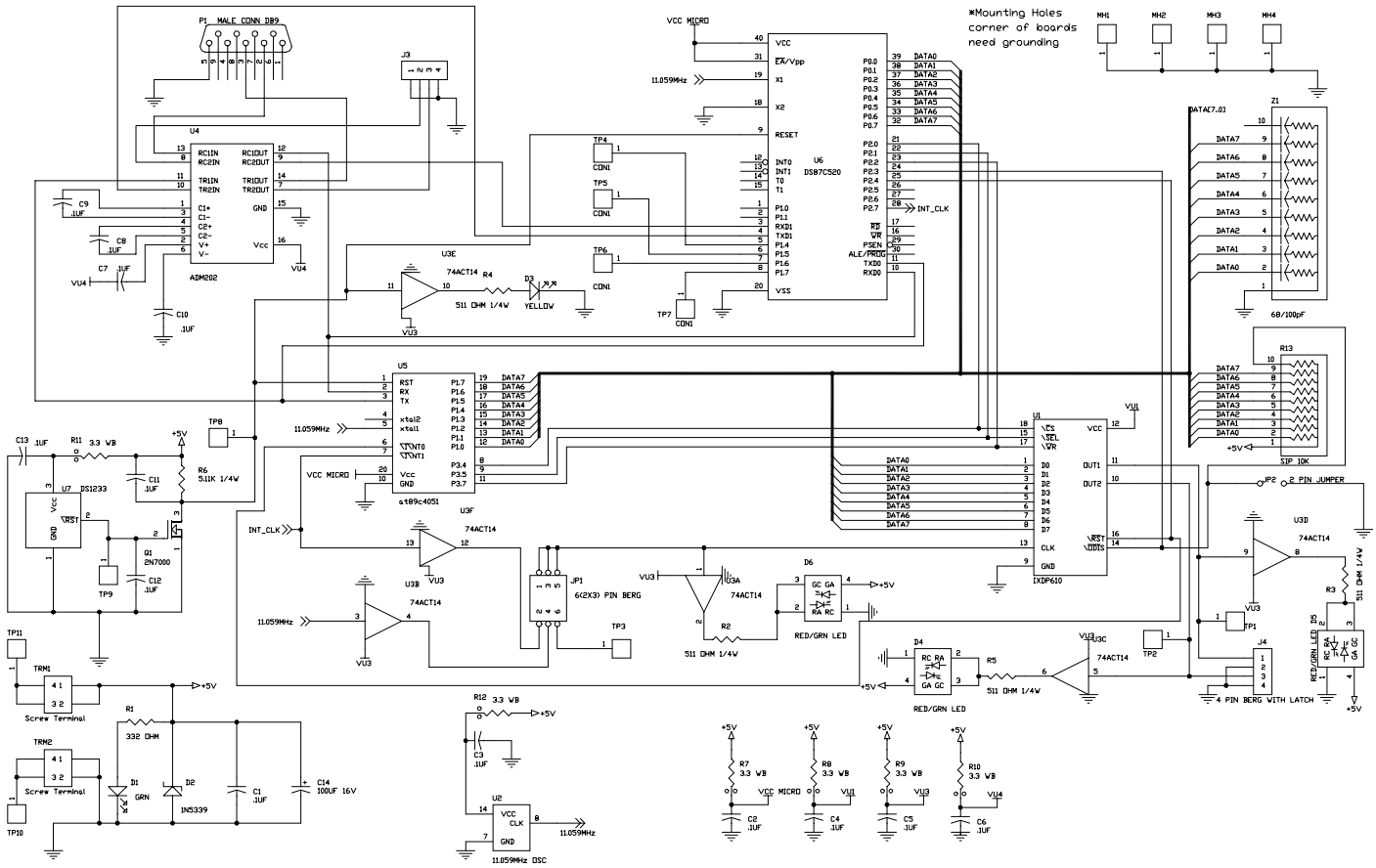


Figure 7 - EVDP610 Schematic

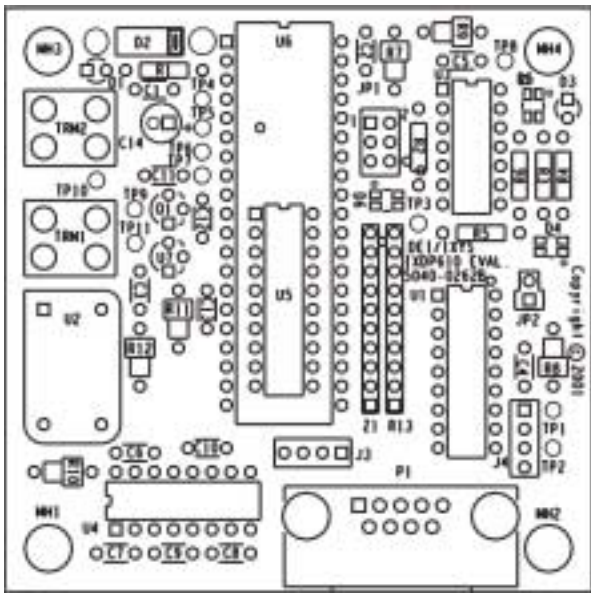


Figure 8 - EVDP610 Circuit Board Layout Drawing

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