EVAL6472H

Fully integrated stepper motor driver based on the L6472

Data brief

Features

- Voltage range from 8 V to 45 V
- Phase current up to 3 $A_{r.m.s.}$
- SPI with daisy chain feature
- SW input
- FLAG and BUSY LED indicators
- Adjustable supply voltage compensation
- Suitable for use in combination with STEVAL-PCC009V2



EVAL6472H

Description

The EVAL6472H demonstration board is a fully integrated microstepping motor driver. In combination with the STEVAL-PCC009V2 communication board and the dSPIN evaluation software, the board allows the user to investigate all the features of the L6472 device. In particular, the board can be used to regulate the L6472 parameters in order to fit application requirements.

The EVAL6472H supports the daisy chain configuration making it suitable for the evaluation of the L6472 in the multi-motor applications.

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1 Board description

Table 1. EVAL6472H specifications

Parameter	Value
Supply voltage (VS)	8 to 45 V
Maximum output current (each phase)	3 $A_{r.m.s.}$
Logic supply voltage (VREG)	Externally supplied: 3.3 V Internally supplied: 3 V typical
Logic interface voltage (VDD)	Externally supplied: 3.3 V or 5 V Internally supplied: VREG
Low level logic input voltage	0 V
High level logic input voltage	VDD(1)
Operating temperature	-25 to +125 °C
L6472H thermal resistance junction-to-ambient	21 °C/W typical

1. All logic inputs are 5 V tolerant.

Figure 1. Jumpers and connectors location

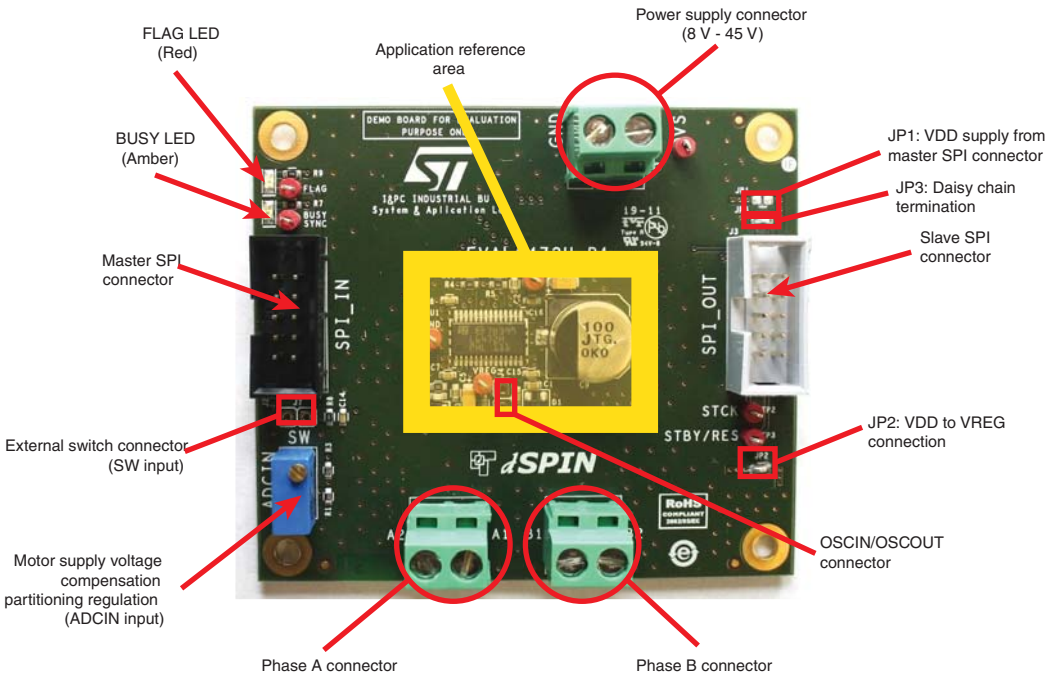


Table 2. Jumpers and connectors description

Name	Type	Function
M1	Power supply	Motor supply voltage
M2	Power output	Bridge A outputs
M3	Power output	Bridge B outputs
CN1	SPI connector	Master SPI
CN2	SPI connector	Slave SPI
CN3	NM connector	OSCIN and OSCOUT pins
CN4	NM connector	External switch input
TP1 (VS)	Test point	Motor supply voltage test point
TP2 (VDD)	Test point	Logic interface supply voltage test point
TP3 (VREG)	Test point	Logic supply voltage/L6470 internal regulator test point
TP5 (GND)	Test point	Ground test point
TP6 (GND)	Test point	Ground test point
TP8 (STCK)	Test point	Step clock input test point
TP9 (STBY/RES)	Test point	Standby/reset input test point
TP10 (FLAG)	Test point	FLAG output test point
TP11 (BUSY/SYNC)	Test point	BUSY/SYNC output test point

Table 3. Master SPI connector pinout (J10)

Pin number	Type	Description
1	Open drain output	L6472 BUSY output
2	Open drain output	L6472 FLAG output
3	Ground	Ground
4	Supply	EXT_VDD (can be used as external logic power supply)
5	Digital output	SPI master IN slave OUT signal (connected to L6472 SDO output through daisy chain termination jumper JP2)
6	Digital input	SPI serial clock signal (connected to L6472 CK input)
7	Digital input	SPI master OUT slave IN signal (connected to L6472 SDI input)
8	Digital input	SPI slave select signal (connected to L6472 CS input)
9	Digital input	L6472 step-clock input
10	Digital input	L6472 standby/reset input

Table 4. Slave SPI connector pinout (J11)

Pin number	Type	Description
1	Open drain output	L6472 BUSY output
2	Open drain output	L6472 FLAG output
3	Ground	Ground
4	Supply	EXT_VDD (can be used as external logic power supply)
5	Digital output	SPI master IN slave OUT signal (connected to pin 5 of J10)
6	Digital input	SPI serial clock signal (connected to L6472 CK input)
7	Digital input	SPI master OUT slave IN signal (connected to L6472 SDO output)
8	Digital input	SPI slave select signal (connected to L6472 CS input)
9	Digital input	L6472 step-clock input
10	Digital input	L6472 standby/reset input

Figure 2. EVAL6472H schematic

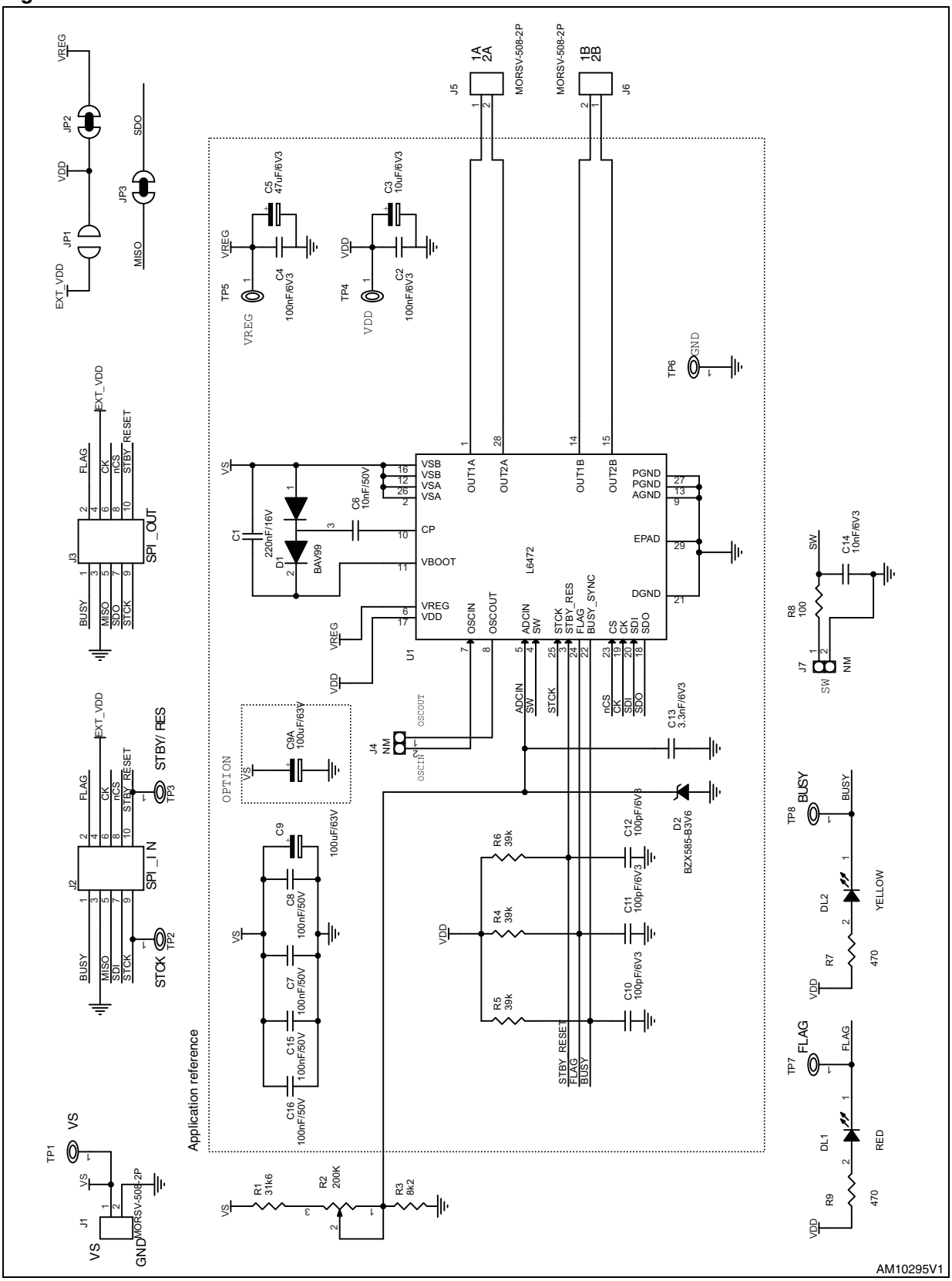


Table 5. Bill of material

Index	Quantity	Reference	Value	Package
1	1	C1	220 nF/16 V	CAPC-0603
2	2	C2,C4	100 nF/6V3	CAPC-0603
3	1	C3	10 µF/6V3	CAPC-3216
4	1	C5	47 µF/6V3	CAPC-3216
5	1	C6	10 nF/50 V	CAPC-0603
6	4	C7, C8, C15, C16	100 nF/50 V	CAPC-0603
7	1	C9A	100 µF/6V3 (option)	CAPE-R10HXX-P5
8	1	C9	100 µF/6V3	CAPES-R10HXX
9	3	C10, C11, C12	100 pF/6V3	CAPC-0603
10	1	C13	3.3 nF/6V3	CAPC-0603
11	1	C14	10 nF/6V3	CAPC-0603
12	1	DL1	LED diode (red)	LEDC-0805
13	1	DL2	LED diode (amber)	LEDC-0805
14	1	D1	BAV99	SOT23
15	1	D2	BZX585-B3V6	SOD323
16	1	JP1	Jumper - open	JP2SO
17	2	JP2, JP3	Jumper - closed	JP2SO
18	3	J1, J5, J6	Screw connector 2 poles	MORSV-508-2P
19	2	J2,J3	Pol. IDC male header vertical 10 poles	CON-FLAT-5X2-180M
20	2	J4, J7	NM	STRIP254P-M-2
21	1	R1	31.6 kΩ	RESC-0603
22	1	R2	200 kΩ	TRIMM-100X50X110-64W
23	1	R3	8.2 kΩ	RESC-0603
24	3	R4, R5, R6	39 kΩ	RESC-0603
25	2	R7, R9	470 Ω	RESC-0603
26	1	R8	100 Ω	RESC-0603
27	7	TP1, TP2, TP3, TP4, TP5, TP7, TP8	TPTH-ring-1 mm red	TH
28	1	TP6	TPTH-ring-1 mm black	TH
29	1	U1	L6472	HTSSOP28

Figure 3. EVAL6472H - silkscreen

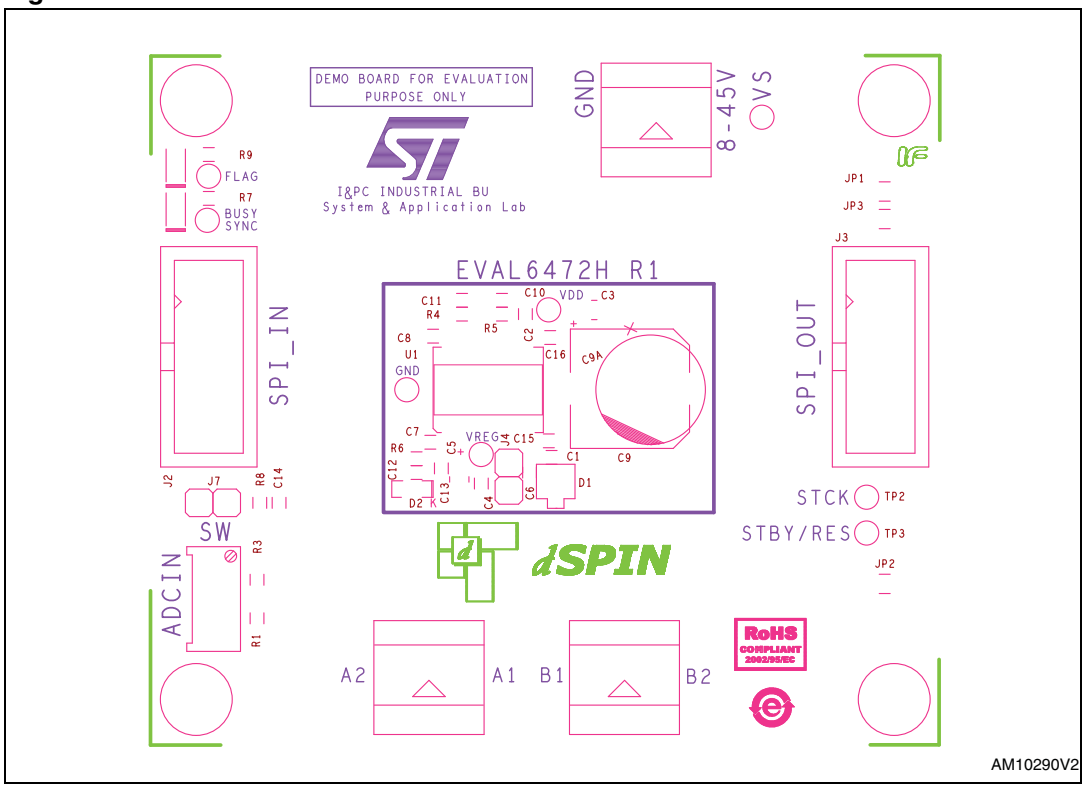


Figure 4. EVAL6472H - layout (top layer)

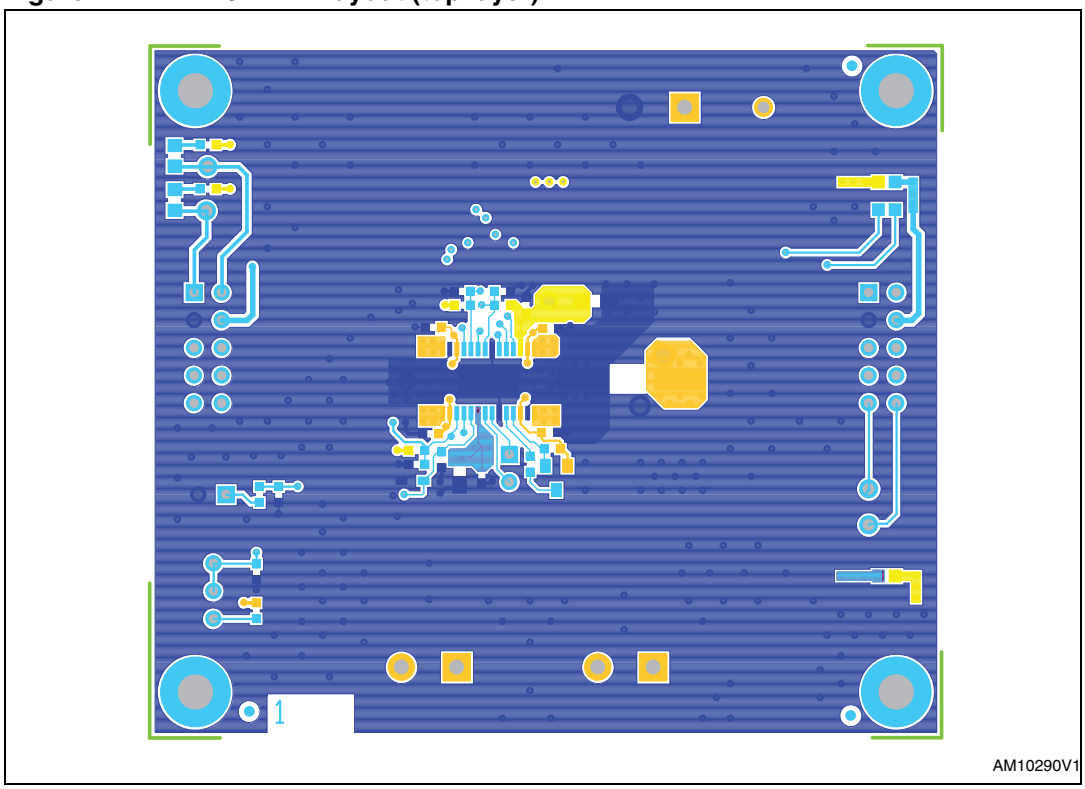


Figure 5. EVAL6472H - layout (inner layer2)

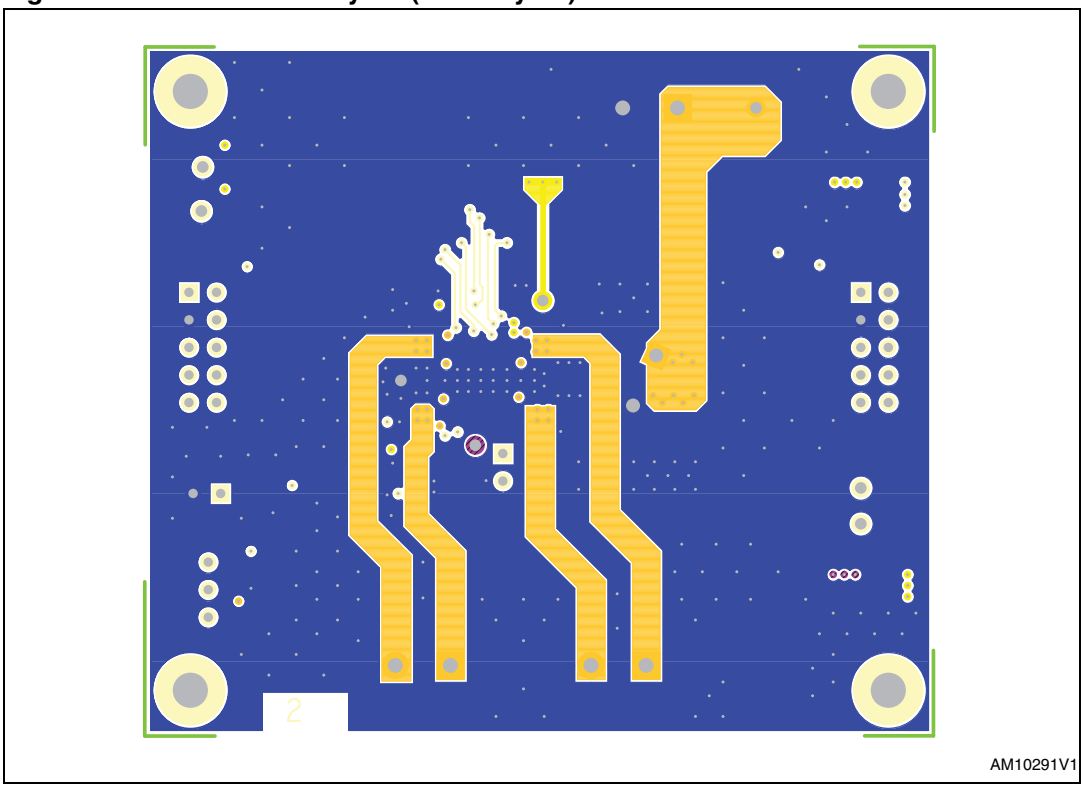


Figure 6. EVAL6472H - layout (inner layer3)

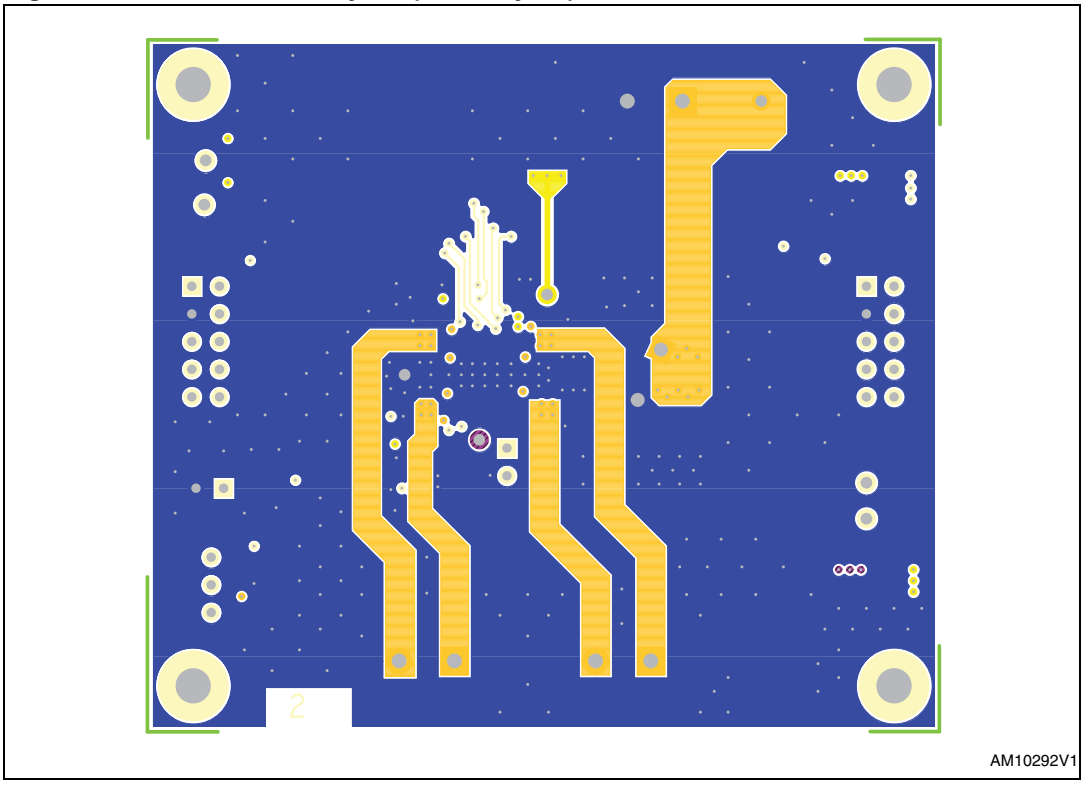
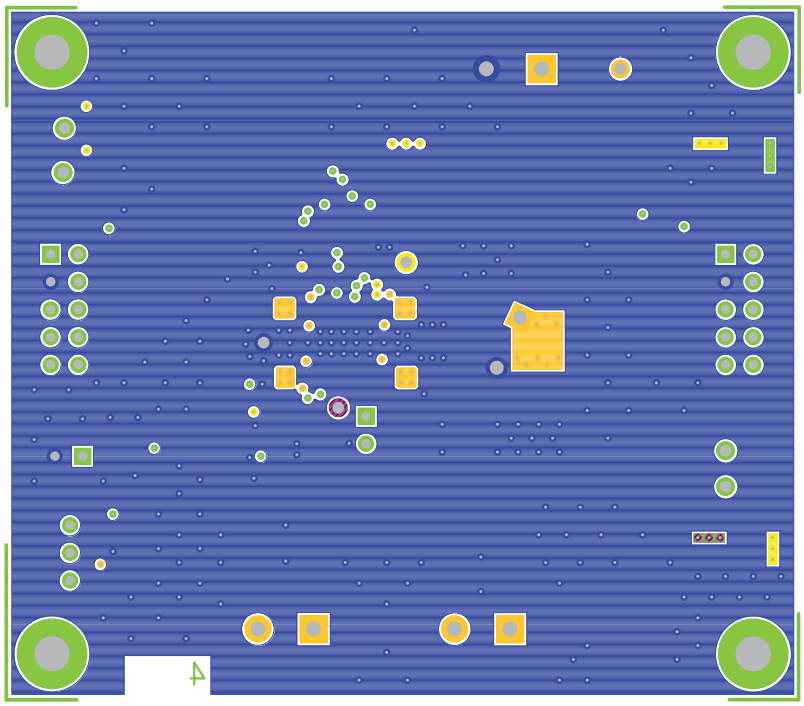
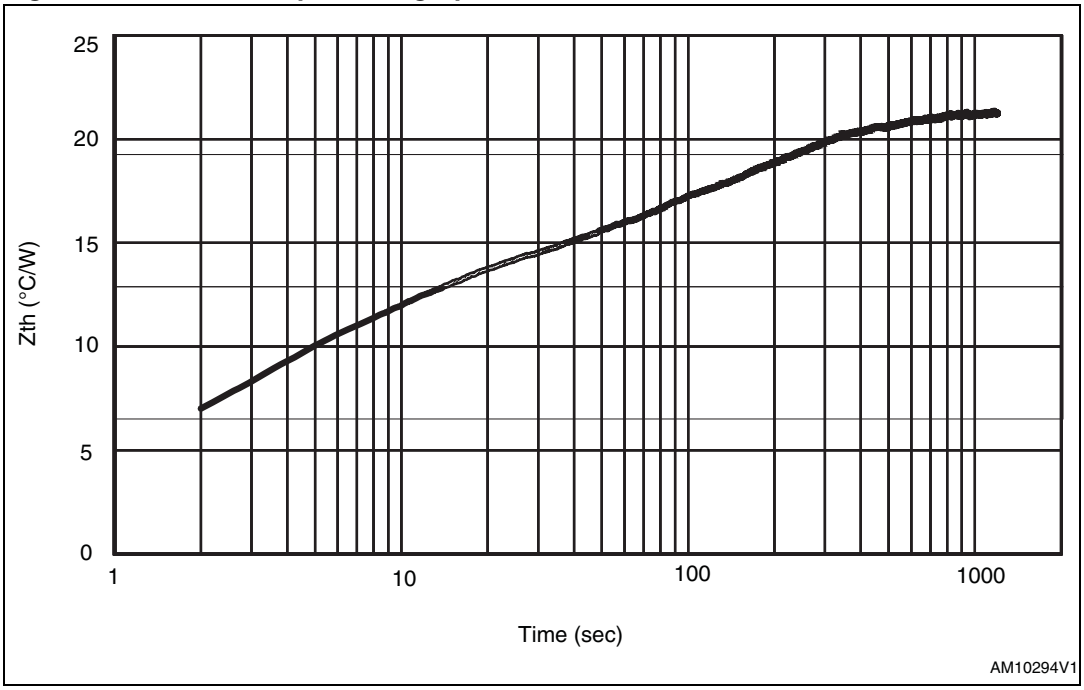


Figure 7. EVAL6472H - layout (bottom layer3)



1.1 Thermal data

Figure 8. Thermal impedance graph



2 Revision history

Table 6. Document revision history

Date	Revision	Changes
21-Mar-2012	1	Initial release.

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