Data Sheet

ADPD6000

Multimodal Sensor Front End

FEATURES

- Optical channel
  - 4 input channels with multiple operation modes for various sensor measurements
  - Dual channel processing with simultaneous sampling
  - 12 programmable time slots for synchronized sensor measurements
  - Flexible input multiplexing to support single-ended sensor measurements
  - 4 LED drivers, 2 of which can be driven simultaneously
  - Flexible sampling rate from 0.004 Hz to 9 kHz using internal oscillators
  - SNR of transmit and receive signal chain: 117 dB (with off-chip filtering)
  - AC ambient light rejection: 78 dB up to 100 Hz
  - 400 mA total LED peak drive current
  - Individual ambient light rejection DAC at TIA input with 9-bit control up to 300 µA
  - Individual LED dc cancellation DAC at TIA input with 7-bit control up to 190 µA
- ECG channel
  - 0.75 µV rms RTI noise at diagnostic filter bandwidth (150 Hz)
  - High input impedance: 3 GΩ
  - Accepts up to 1.2 V of dc differential input range
  - Common-mode rejection ratio: 116 dB
  - Two-electrode and three-electrode configurations
  - AC lead off detection and dc lead off detection
- BIA channel
  - Low power, high accuracy excitation path
  - Configurable output frequency up to 250 kHz
  - Sine wave excitation with a 12-bit DAC
  - High accuracy with large imbalance contact impedance
  - Configurable receive filters with low noise design
  - Complex impedance measurement engine
  - Supports both external calibration and internal calibration
- SPI communications supported
- 640-byte FIFO

APPLICATIONS

- Wearable health and fitness monitors: heart rate, heart rate variability, SpO2, body impedance analysis, hydration, cuffless noninvasive blood pressure
- Home patient monitoring
- Industrial monitoring: particle and aerosol, gas, and conductivity detection

GENERAL DESCRIPTION

The ADPD6000 is a highly integrated analog front end (AFE) designed for measuring various vital signals.

The optical channel is designed as an optical transceiver, stimulating up to four light emitting diodes (LEDs) and measuring the return signal on up to four separate current inputs. The signal chain rejects signal offsets and corruption from asynchronous modulated interference, typically from ambient light, eliminating the need for optical filters or externally controlled dc cancellation circuitry.

The electrocardiography (ECG) signal acquisition is designed to support low noise, diagnostic level measurement in the presence of a variety of interferers. The ECG signal chain has a number of complementary features supporting ECG measurement, such as driven reference for common-mode rejection and lead off detection to identify a fallen electrode.

The body impedance analysis (BIA) signal chain is designed for body impedance measurement with a configurable excitation path and measurement path. A 12-bit digital-to-analog (DAC) is used in the excitation path to generate the sinusoid wave and high precision measurement, with configurable filters used to measure the body response of the stimulus.

The data output and functional configuration use a serial port interface (SPI) on the ADPD6000. The control circuitry includes flexible LED signaling and synchronous detection, digital filters, digital wave generators, and configurable filters.

The ADPD6000 is available in a 2.6 mm × 2.6 mm, 0.4 mm pitch, 36-ball wafer level chip scale package (WLCSP).

Analog Devices is in the process of updating documentation to provide terminology and language that is culturally appropriate. This is a process with a wide scope and will be phased in as quickly as possible. Thank you for your patience.

Rev. 0

DOCUMENT FEEDBACK
TECHNICAL SUPPORT

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REVISION HISTORY

4/2022—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

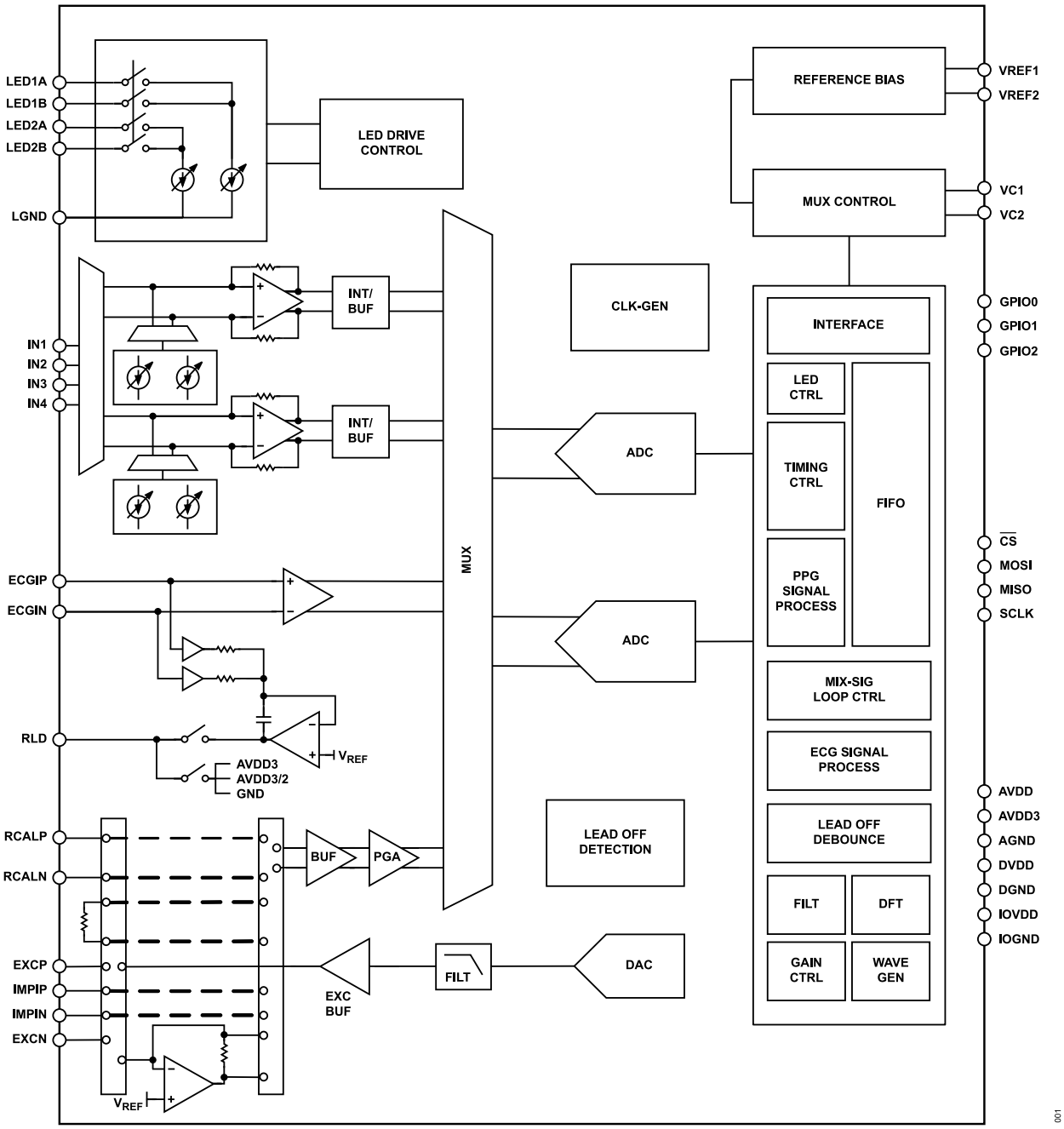


Figure 1. Functional Block Diagram

SPECIFICATIONS

TEMPERATURE AND POWER SPECIFICATIONS

Table 1. Temperature and Power Specifications

Parameter	Min	Typ	Max	Unit
TEMPERATURE RANGE				
Operating Range	−40		+85	°C
Storage Range	−65		+150	°C
POWER SUPPLY VOLTAGES				
AVDD	1.7	1.8	1.9	V
AVDD3	2.7	3.3	3.6	V
DVDD	1.7	1.8	1.9	V
IOVDD	1.7	1.8	3.6	V

PERFORMANCE SPECIFICATIONS

AVDD = DVDD = IOVDD = 1.8 V, AVDD3 = 3.3V, and T_A = 25°C, unless otherwise noted.

Table 2. Performance Specifications

Parameter	Test Condition/Comments	Min	Typ	Max	Unit
DATA ACQUISTION					
Datapath Width				32	Bits
FIRST IN, FIRST OUT (FIFO) SIZE				640	Bytes
PHOTOPLETHYSMOGRAPHY (PPG) CHANNEL					
Transimpedance Amplifier (TIA) Gain		12.5		400	kΩ
DIGITAL INTEGRATION MODE					
Analog-to-Digital Converter (ADC) Resolution	TIA feedback resistor (R_F)		5.84		nA/LSB
	25 kΩ		2.92		nA/LSB
	50 kΩ		1.46		nA/LSB
	100 kΩ		0.73		nA/LSB
	200 kΩ		0.365		nA/LSB
	400 kΩ		0.183		nA/LSB
ADC Saturation Level	TIA feedback resistor				
	12.5 kΩ		48		µA
	25 kΩ		24		µA
	50 kΩ		12		µA
	100 kΩ		6		µA
	200 kΩ		3		µA
	400 kΩ		1.5		µA
DC Ambient Light Rejection (ALR)					
ALR Range		0		300	µA
ALR Resolution			0.59		µA
LED DC Cancellation					
Range		0		190	µA
Resolution			1.48		µA
Dark Noise	Pulse = 1, ADC sample = 20				
	TIA gain = 12.5 kΩ		1490		pA rms
	TIA gain = 25 kΩ		775		pA rms
	TIA gain = 50 kΩ		401.5		pA rms
	TIA gain = 100 kΩ		204.5		pA rms

SPECIFICATIONS

Table 2. Performance Specifications

Parameter	Test Condition/Comments	Min	Typ	Max	Unit
	TIA gain = 200 kΩ		120		pA rms
	TIA gain = 400 kΩ		100		pA rms
Signal-to-Noise Ratio (SNR)	White card reflection, pulse = 1, ADC sample = 20				
	TIA gain = 12.5 kΩ		90		dB
	TIA gain = 25 kΩ		90		dB
	TIA gain = 50 kΩ		88		dB
	TIA gain = 100 kΩ		87		dB
	TIA gain = 200 kΩ		85		dB
	TIA gain = 400 kΩ		82		dB
AC ALR	Up to 100 Hz		78		dB
DC Power Supply Rejection Ratio (PSRR)	At 75% full scale (FS) input, optimal settings, all gains[1]		60		dB
LED DRIVER					
Peak Current per Driver	LED pulse enabled		200		mA
Peak Current, Total	Using multiple LED drivers simultaneously		400		mA
Current Step	High SNR mode		1.57		mA
	Low compliance mode		0.52		mA
Compliance Voltage	High SNR mode		400		mV
	Low compliance mode		200		mV
Power	AFE current only, 70% FS output data rate (ODR) = 25 Hz				
Standby	DVDD + AVDD		0.2		µA
Typical Heart Rate Monitor (HRM) Application	DVDD + AVDD		28.5		µA
SAMPLING RATE		0.004		9000	Hz
ECG CHANNEL	Resolution is 286 nV, unless otherwise noted				
Input Bias Current	ECG input pins, room temperature, lead off detection is off, measured at dc		300		pA
Input Impedance	ECG input pins, measured at dc		3		GΩ
Differential Input Range		−1.2		+1.2	V
Electrode Single-Ended Input Voltage Range		0.2		AVDD3 − 0.2	V
Input Common Mode Range		0.4		AVDD3 − 0.4	V
−3 dB Monitor Bandwidth	Data rate = 250 SPS	40			Hz
−3 dB Diagnostic Bandwidth	Data rate = 500 SPS	150			Hz
Gain Flatness	DC to 5.3 Hz (data rate = 250 SPS)		±1		%
	DC to 19 Hz (data rate = 500 SPS)		±1.5		%
Gain Error		−2		+2	%
Resolution			286		nV/LSB
			572		nV/LSB
Input Referred Noise					
10 Sec Measurement Using Internal Shorted Mode, Measured at Room Temperature	Data rate = 250 SPS, monitoring filter bandwidth (40 Hz)		0.37		µV rms
	Data rate = 500 SPS, diagnostic filter bandwidth (150 Hz)		0.75		µV rms
10 Sec System Level Measurement with Proper Electrode Model and All Functions Enabled (DCLO, ACLO)	Data rate = 250 SPS, monitoring filter bandwidth (40 Hz)		0.65		µV rms
	Data rate = 500 SPS, diagnostic filter bandwidth (150 Hz)		0.95		µV rms
Common-Mode Rejection Ratio (CMRR)	Measured at 60 Hz		116		dB

SPECIFICATIONS

Table 2. Performance Specifications

Parameter	Test Condition/Comments	Min	Typ	Max	Unit
Output Date Rate	Aligned with filter design	250		4000	Hz
Enable Time	Data rate of 500 SPS		15		ms
Overload Recovery Time			10		ms
Power			1.7		mW
DC LEAD OFF (DCLO) DETECTION					
Drive Circuit					
Lead Off Current Range	Lead fail current is programmable over the specified range, programmed current magnitude setting applies across all electrode pins, current polarity is programmable on individual electrode basis		±16		nA
Lead Off Current Step Size			2		nA
Measure Circuit					
RLD Lead Off Thresholds					
High		AVDD3 − 0.4		AVDD3 − 0.1	V
Low		0.1		0.4	V
AC LEAD OFF (ACLO) THRESHOLD					
Drive Circuit					
Excitation Frequency			4		kHz
Current		10		70	nA
Measure Circuit					
Threshold		0.04		2.33	nF
RIGHT LEG DRIVER (RLD)					
Output Voltage		GND	AVDD3/2	AVDD3	V
Stable Load Capacitance				2.2	nF
BIA CHANNEL	For Z = 1 kΩ (0.1% tolerant resistor), excitation frequency = 50 kHz, sine amplitude = 0.6 V p-p, TIA resistor (R_{TIA}) = 2 kΩ, TIA capacitor (C_{TIA}) = 7 pF, isolation capacitor = 470 nF, current-limiting resistor (R_{LIMIT}) = 1 kΩ				
SYSTEM PERFORMANCE					
Total System Accuracy					
Magnitude			0.26		%
Phase			1		Degrees
Body Impedance Magnitude Error	Contact resistor <1 kΩ		0.26		%
	Contact resistor <10 kΩ		5		%
Body Impedance Magnitude Repeatability	Room temperature, test 10 times, contact resistor <1 kΩ		0.1		%
Body Phase Angle Error			1		Degrees
TRANSMIT STAGE					
Output Frequency Range			50	250	kHz
Output Frequency Resolution			0.48		Hz
Output Voltage Range				800	mV
Output Voltage Resolution			0.39		mV
RECEIVE STAGE					
Input Leakage Current					
Input Capacitance	Toward ground for current sensing		10		pF
	Toward ground for voltage sensing		10		pF
ADC Saturation Level	Voltage		±0.8		V
	Current (TIA = 2 kΩ)		±400		µA

SPECIFICATIONS

Table 2. Performance Specifications

Parameter	Test Condition/Comments	Min	Typ	Max	Unit
CALIBRATION RESISTOR					
External			2		kΩ
Internal			2		kΩ
Power Consumption			1.24		mW

[1] DC PSRR = 20 × log((Signal(LSB)/NUM_INT_x/NUM_REPEAT_x × 0.146 mV/LSB)/V_{IN} (mV))

DIGITAL SPECIFICATIONS

IOVDD = 1.7 V to 3.6 V, unless otherwise noted.

Table 3. Digital Specifications

Parameter	Test Condition/Comments	Min	Typ	Max	Unit
LOGIC INPUTS					
Input Voltage Level					
GPIOx, MISO, MOSI, SCLK, $\overline{CS}$					
High		0.7 × IOVDD		IOVDD + 0.3	V
Low		−0.3		+0.3 × IOVDD	V
Input Current Level	All logic inputs				
High				10	μA
Low		−10			μA
Input Capacitance			2		pF
LOGIC OUTPUTS					
Output Voltage Level					
GPIOx, MISO					
High	2 mA high level output current	IOVDD – 0.5			V
Low	2 mA low level output current			0.5	V

TIMING SPECIFICATIONS

Table 4. Timing Specifications

Parameter	Symbol	Test Condition/Comments	Min	Typ	Max	Unit
SPI PORT						
SCLK						
Frequency	f_{SCLK}				10	MHz
Minimum Pulse Width						
High	$t_{SCLKPWH}$		15			ns
Low	$t_{SCLKPWL}$		15			ns
$\overline{CS}$						
Setup Time	t_{CSS}	$\overline{CS}$ setup to SCLK rising edge	11			ns
Hold Time	t_{CSH}	$\overline{CS}$ hold from SCLK rising edge	5			ns
Pulse Width High	t_{CSPWH}	$\overline{CS}$ pulse width high	15			ns
MOSI						
Setup Time	t_{MOSIS}	MOSI setup to SCLK rising edge	5			ns
Hold Time	t_{MOSIH}	MOSI hold from SCLK rising edge	5			ns
SWITCHING CHARACTERISTICS						
MISO Output Delay	t_{MISOD}	MISO valid output delay from SCLK falling edge				
		Register 0x0057 = 0x0050 (default)			21.5	ns
		Register 0x0057 = 0x005F (maximum slew rate, maximum drive strength for SPI)			14	ns

SPECIFICATIONS

Timing Diagram

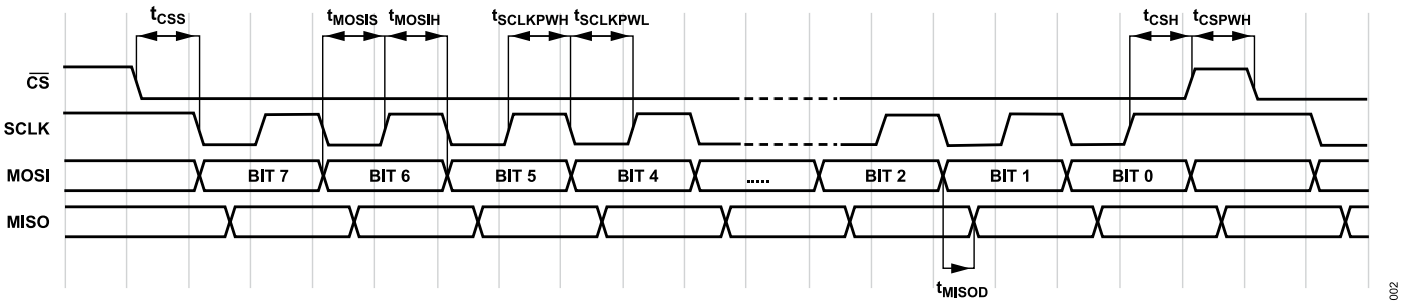


Figure 2. SPI Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 5. Absolute Maximum Ratings

Parameter	Rating
AVDD to AGND	−0.3 V to +2.2 V
AVDD3 to AGND	−0.3 V to +3.9 V
DVDD to DGND	−0.3 V to +2.2 V
IOVDD to IOGND	−0.3 V to +3.9 V
GPIOx, MOSI, MISO, SCLK, $\overline{CS}$ to DGND	−0.3 V to +3.9 V
LEDxx to LGND	−0.3 V to +3.9 V
Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CB-36-10[1]	42.15	0.98	°C/W

[1] The thermal resistance values are defined as per the JESD51-12 standard.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

Machine model (MM) per ANSI/ESD STM5.2. MM voltage values are for characterization only.

ESD Ratings for ADPD6000

Table 7. ADPD6000, 36-Ball WLCSP

ESD Model	Withstand Threshold (V)	Class
HBM	2000	2
CDM	750	C2B
MM	100	Not applicable

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

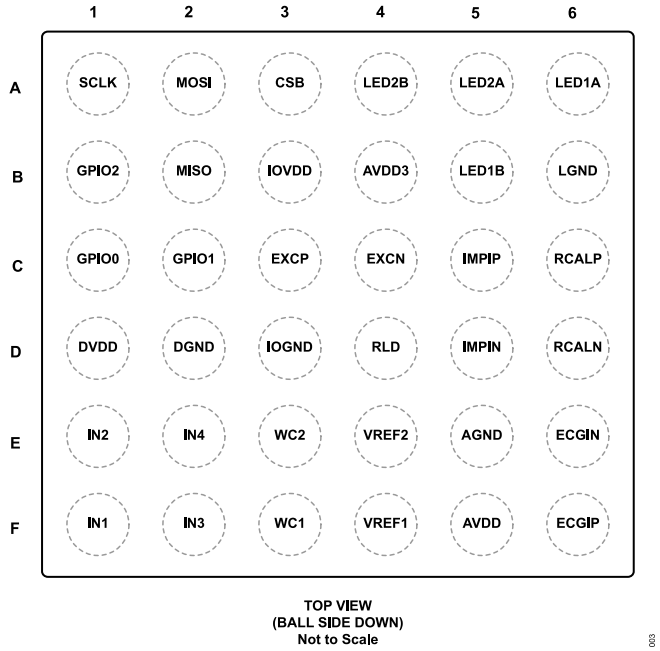


Figure 3. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
F5	AVDD	Power	1.8 V Analog Power Supply.
B4	AVDD3	Power	3.3 V Analog Power Supply.
E5	AGND	Power	Analog Ground.
D1	DVDD	Power	1.8 V Digital Power Supply.
D2	DGND	Power	Digital Ground.
B3	IOVDD	Power	I/O Power Supply.
D3	IOGND	Power	I/O Ground.
B6	LGND	Power	LED Ground.
F4	VREF1	Analog	ADC 1 Reference.
E4	VREF2	Analog	ADC 2 Reference.
F3	VC1	Analog	Output Voltage Source 1 for Photodiode Common Cathode Bias or Other Sensor Stimulus.
E3	VC2	Analog	Output Voltage Source 2 for Photodiode Common Cathode Bias or Other Sensor Stimulus.
F1	IN1	Analog	Current Input 1.
E1	IN2	Analog	Current Input 2.
F2	IN3	Analog	Current Input 3.
E2	IN4	Analog	Current Input 4.
A6	LED1A	Analog	LED Driver 1A.
B5	LED1B	Analog	LED Driver 1B.
A5	LED2A	Analog	LED Driver 2A.
A4	LED2B	Analog	LED Driver 2B.
F6	ECGIP	Analog	ECG Positive Input.
E6	ECGIN	Analog	ECG Negative Input.
D4	RLD	Analog	Right LED Driver.
C5	IMPIP	Analog	BIA Positive Input.
D5	IMPIN	Analog	BIA Negative Input.
C3	EXCP	Analog	BIA Excitation Positive Output.
C4	EXCN	Analog	BIA Excitation Negative Output.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
C6	RCALP	Analog	Calibration Resistor Positive Side.
D6	RCALN	Analog	Calibration Resistor Negative Side.
A3	$\overline{CS}$	Digital	SPI Chip Select Input.
A1	SCLK	Digital	SPI Clock Input.
B2	MISO	Digital	SPI Master Input/Slave Output.
A2	MOSI	Digital	SPI Master Output/Slave Input.
C1	GPIO0	Digital	General-Purpose Input/Output 0.
C2	GPIO1	Digital	General-Purpose Input/Output 1.
B1	GPIO2	Digital	General-Purpose Input/Output 2.

TYPICAL PERFORMANCE CHARACTERISTICS

DVDD = AVDD = 1.8 V, AVDD3 = 3.3 V, LGND = DGND = AGND = IOGND = 0 V, and T_A = 25°C, unless otherwise noted.

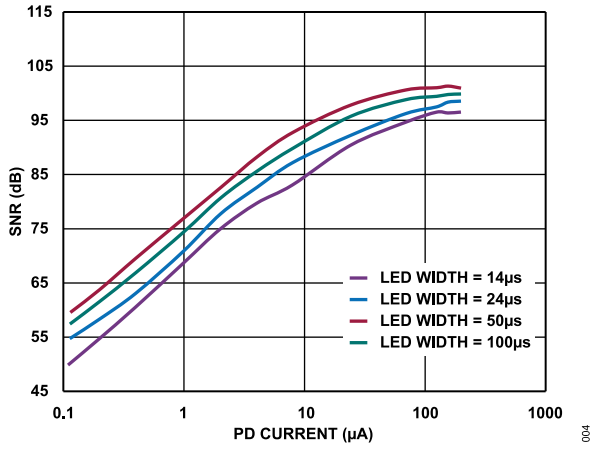


Figure 4. SNR vs. Photodiode (PD) Current, Number of Sequence Repeats = 1, TIA Gain = 100 kΩ

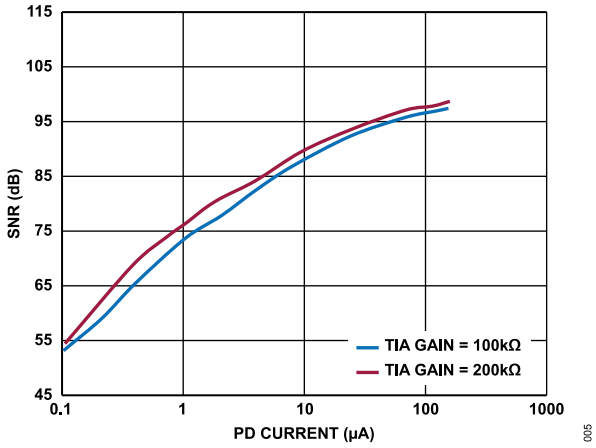


Figure 5. SNR vs. PD Current, LED Width = 24 µs, Number of Sequence Repeats = 1

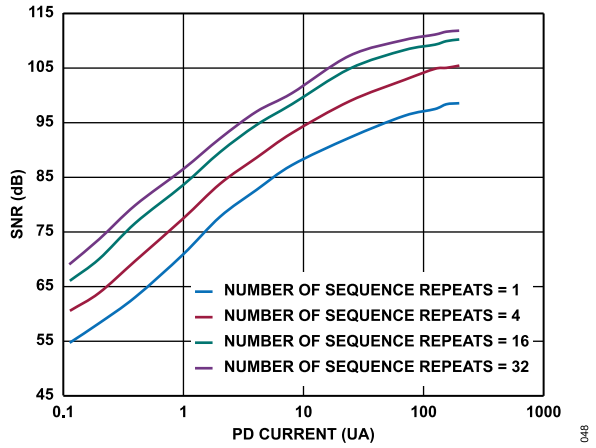


Figure 6. SNR vs. PD Current, LED Width = 24 µs, TIA Gain = 100 kΩ

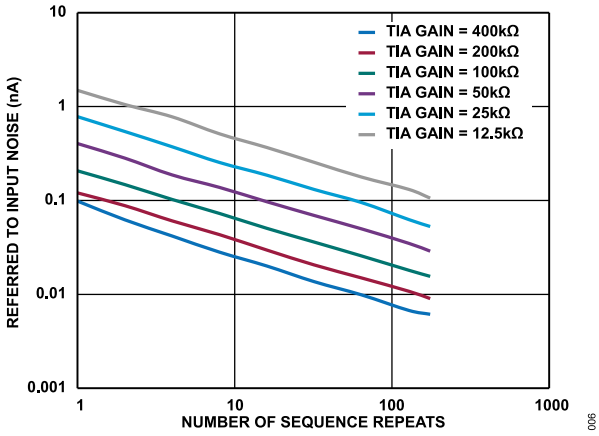


Figure 7. Referred to Input Noise vs. Number of Sequence Repeats

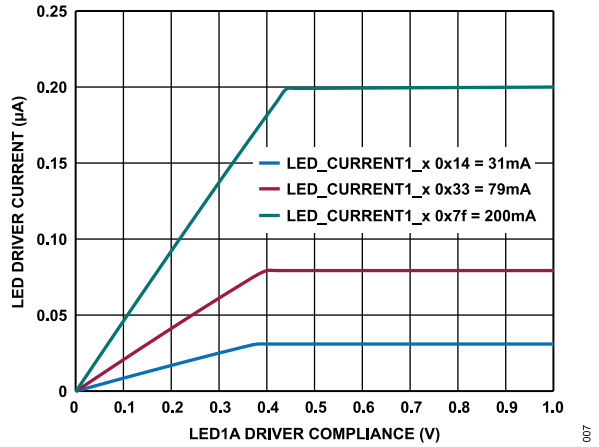


Figure 8. LED Driver Current vs. LED1A Driver Compliance, High SNR Mode

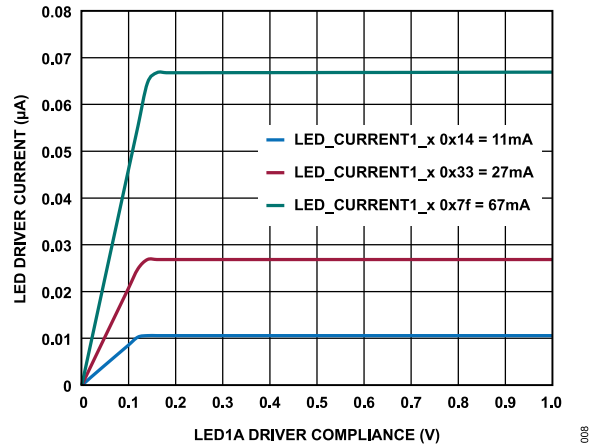


Figure 9. LED Driver Current vs. LED1A Driver Compliance, Low Compliance Mode

TYPICAL PERFORMANCE CHARACTERISTICS

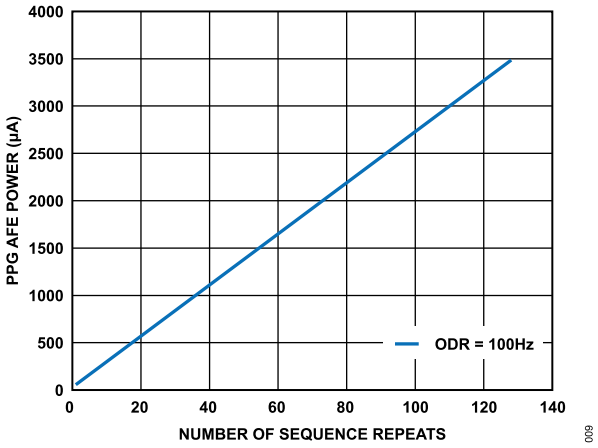


Figure 10. PPG AFE Power vs. Number of Sequence Repeats

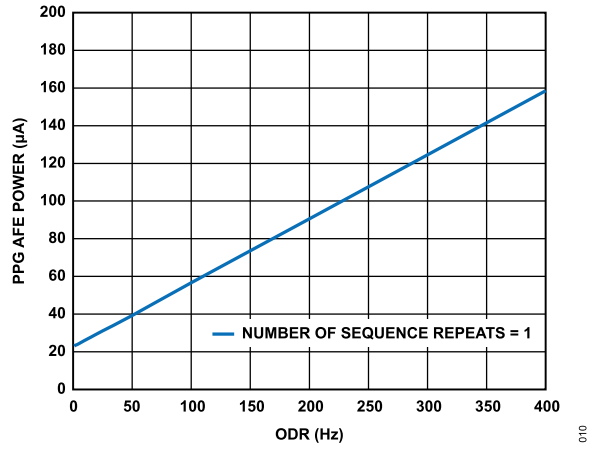


Figure 11. PPG AFE Power vs. ODR

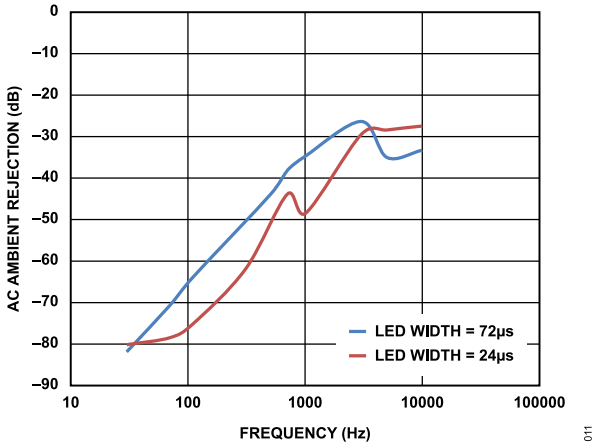


Figure 12. AC Ambient Rejection vs. Frequency

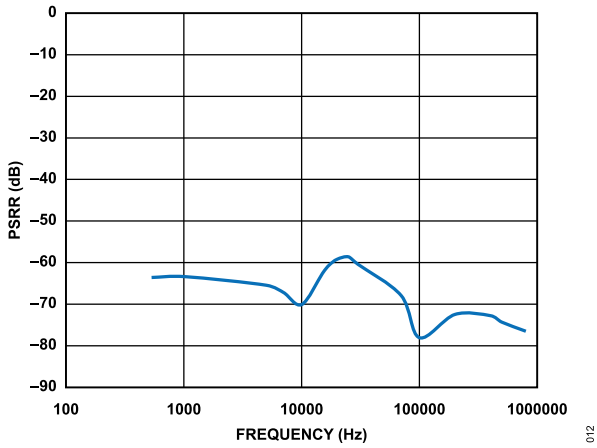


Figure 13. PSRR vs. Frequency, PD Current = 8 µA

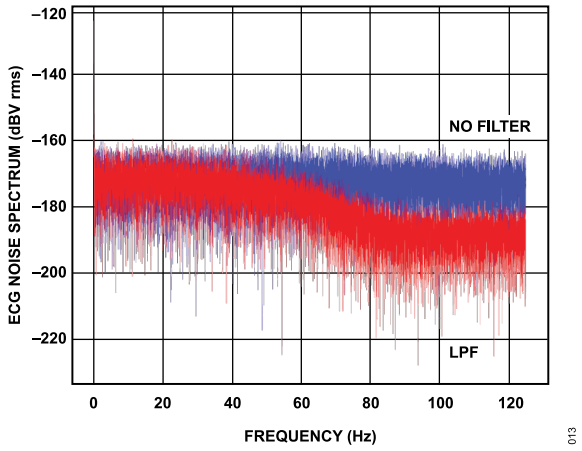


Figure 14. ECG Noise Spectrum vs. Frequency, Input Shorted to Common-Mode Voltage (V_{CM}), Resolution = 286 nV/LSB, Sample Rate = 250 Hz (LPF Is Low Pass Filter)

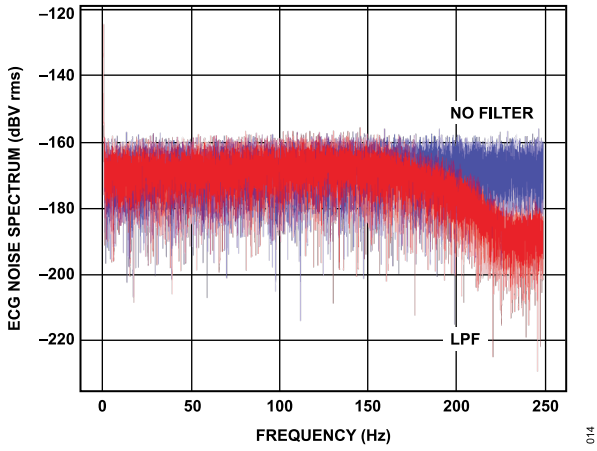


Figure 15. ECG Noise Spectrum vs. Frequency, Input Shorted to V_{CM}, Resolution = 286 nV/LSB, Sample Rate = 500 Hz

TYPICAL PERFORMANCE CHARACTERISTICS

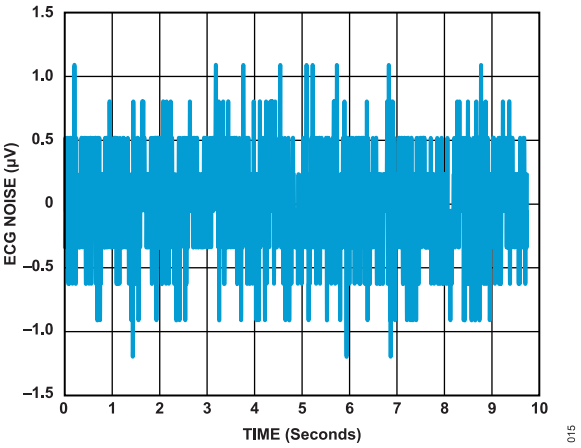


Figure 16. ECG Noise vs. Time, Input Shorted to V_{CM}, Resolution = 286 nV/LSB, Sample Rate = 250 Hz

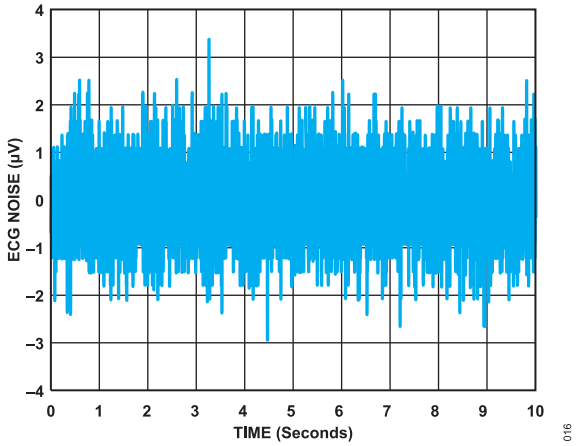


Figure 17. ECG Noise vs. Time, Input Shorted to V_{CM}, Resolution = 286 nV/LSB, Sample Rate = 500 Hz

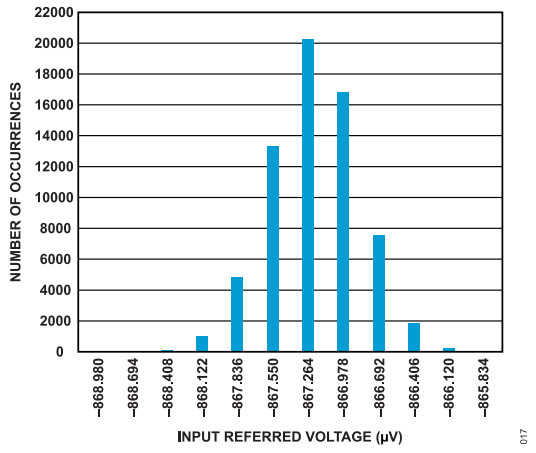


Figure 18. ECG Noise Histogram, Input Shorted to V_{CM}, Resolution = 286 nV/LSB, Sample Rate = 250 Hz

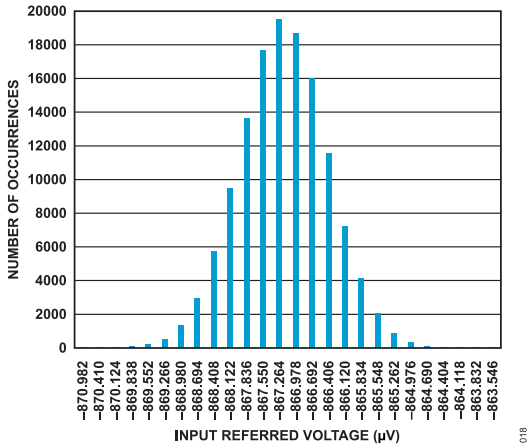


Figure 19. ECG Noise Histogram, Input Shorted to V_{CM}, Resolution = 286 nV/LSB, Sample Rate = 500 Hz

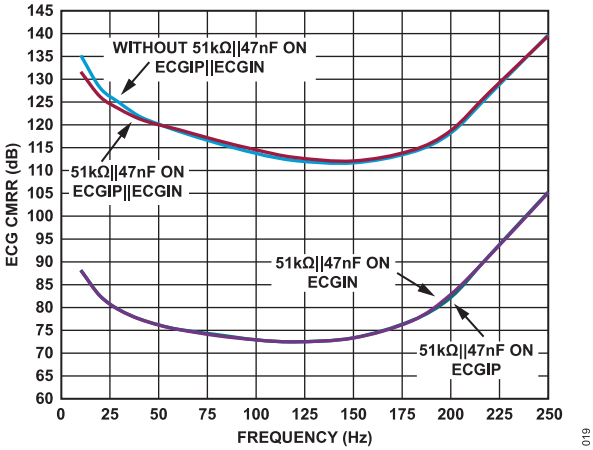


Figure 20. ECG CMRR vs. Frequency, Resolution = 286 nV/LSB, Sample Rate = 500 Hz

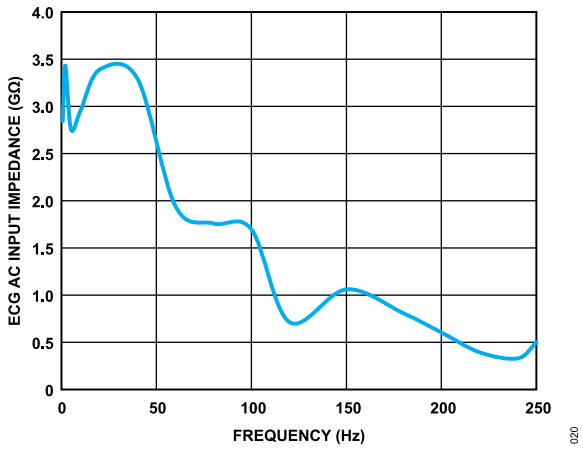


Figure 21. ECG AC Input Impedance vs. Frequency, Resolution = 286 nV/LSB, Sample Rate = 500 Hz

TYPICAL PERFORMANCE CHARACTERISTICS

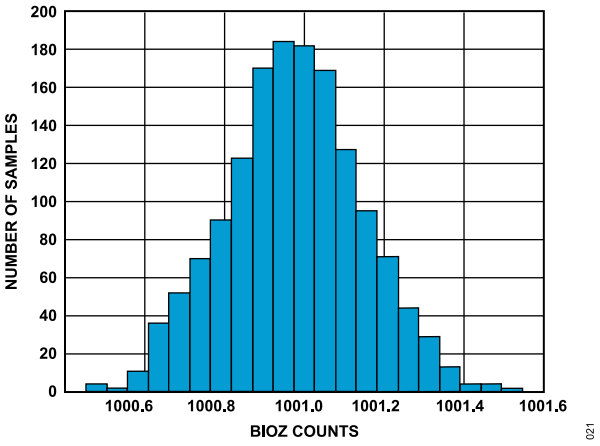


Figure 22. Bioimpedance (BIOZ) Noise Histogram

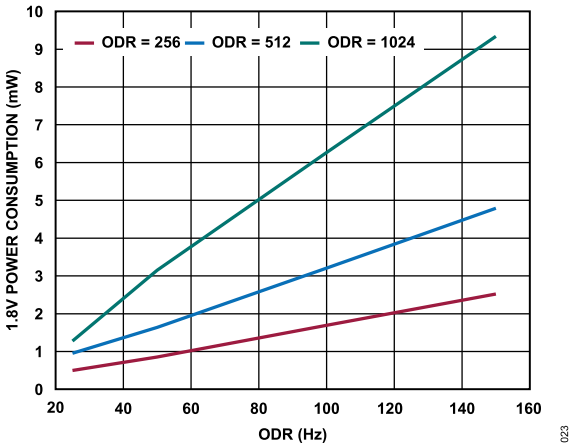


Figure 24. 1.8 V Power Consumption vs. ODR

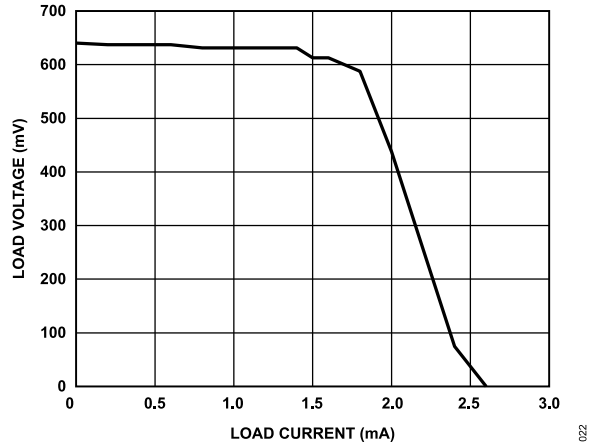


Figure 23. BIOZ Drive Capability

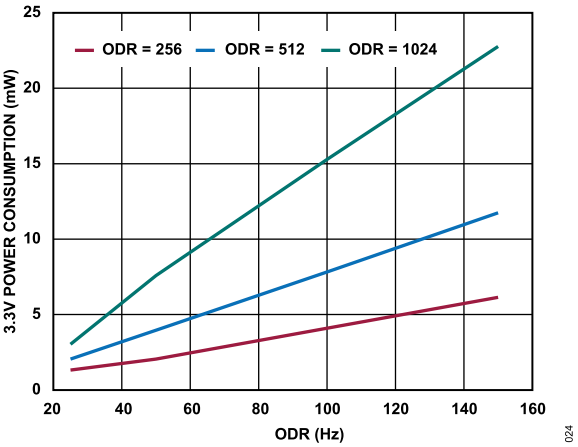


Figure 25. 3.3 V Power Consumption vs. ODR

THEORY OF OPERATION

INTRODUCTION

The ADPD6000 is a multimodal, vital signal monitoring AFE that comprises three high performance signal chains: an optical measurement path (PPG), ECG measurement path, and BIA measurement path.

The PPG measurement path works as a transceiver that supports up to four LEDs and four photodiode inputs. The current on the LEDs is programmable from two 7-bit LED drivers. The receiver path provides two high performance readout channels that can sample simultaneously and can be configured separately. Two high performance current DACs (IDACs) are implemented in each channel to provide first class ambient light suppression and large dynamic range in different application scenarios.

The ECG measurement path offers a high input impedance, low noise, high dynamic range solution to allow high quality ECG signal acquisition in wearable devices. Both DCLO detection and ACLO detection are integrated to guarantee proper detectability.

The stimulus in the BIA path offers a sine wave with various options for frequency, amplitude, and phase to make the ADPD6000 suitable for measurement in different scenarios. A low noise TIA, programmable gain amplifier (PGA), filter, and ADC are integrated in the receiver channel to provide high performance impedance measurement. Direct digital synthesis (DDS) and discrete Fourier transform (DFT) engines are also integrated in this path.

An internal state machine allows flexible control of these three measurement paths. The acquisition data can be stored in a 640-byte FIFO.

TIME SLOT OPERATION

An internal configurable controller handles the operation of the ADPD6000. This controller generates the timing needed to generate sampling regions comprising combinations of the three measurement paths and sleep periods. To facilitate the use of multiple signal chains, multiple time slots handle the access to different transmitters or receivers.

The system is characterized by the ODR, which determines the repetition periodicity of each enabled time slot. The enabled time slots are repeated at the time slot rate configured by the TIMESLOT_PERIOD_x bits.

There are 19 time slots in the ADPD6000, as shown in Figure 26.

Each enabled PPG and BIA time slot is repeated at the time slot rate, followed by an ultra low power sleep period.

ECG_TS is the ECG time slot. The operation of the ECG signal chain is not in time slot fashion. After the ECG time slot turns on, the ECG signal chain runs until the system stops. However, the ECG signal chain output data is synchronized to the FIFO with this time slot rate.

Following the ECG time slot, there are 12 PPG time slots (PPG_TSA to PPG_TSL). Each PPG time slot allows the creation of one or more LED pulses and modulate pulses, as well as the acquisition of the photodiode or other device current based on that stimulus. The operating parameters for each time slot are highly configurable.

The last six time slots are the BIA time slots (BIA_TSA to BIA_TSF). Each BIA time slot allows the excitation voltages, frequencies, and receiver configurations to facilitate accurate body impedance measurement.

Equation 1 determines the sampling rate (time slot rate), as follows:

$$Sampling\ \ Rate = Timer\ \ Clock\ \ Frequency\ (Hz)/TIMESLOT_PERIOD_x \quad (1)$$

Table 9. Sources of Low Frequency Clock (LFCLK) and Timer Clock[1]

LFCLK	Timer Clock	ALT_CLOCKS	TM_CLK_GPIO_SEL
960 kHz internal	960 kHz internal	0	N/A
960 kHz external	960 kHz external	1	N/A
960 kHz internal	960 kHz internal	2	N/A
1 MHz external (divided from 32 MHz)	1 MHz external (divided from 32 MHz)	3	N/A
960 kHz internal	960 kHz external	4	1
960 kHz internal	32 kHz external	4	0

[1] N/A means not applicable.

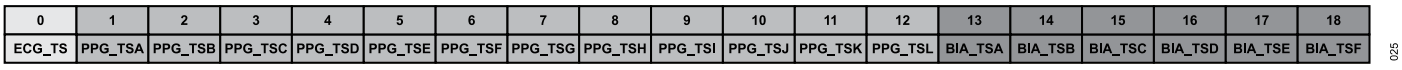


Figure 26. Time Slot Allocation

THEORY OF OPERATION

OPTICAL SIGNAL CHAIN

The optical signal path stimulates up to four LEDs and measures the return signal on up to four separate current inputs. Twelve optical time slots enable 12 separate optical measurements per sampling period.

The analog inputs can be driven single-ended or in differential pairs. The four analog inputs can be multiplexed into a single channel or two independent channels, enabling simultaneous sampling of two sensors.

The optical signal chain consists of a TIA, an integrator that can also be configured as a buffer depending on the register setting, and an ADC. The digital block provides multiple operating modes, programmable timing, and block averaging.

Four independent LED drivers are provided that can each drive up to 200 mA. Two LED drivers can be enabled in any time slot and can be programmed from 1.5 mA to 200 mA monotonically, with a 7-bit register setting. The LED drivers enabled in any time slot can provide a combined maximum LED current of 400 mA.

When making optical measurements, the ADPD6000 provides 100 dB of ac ambient light rejection using a synchronous modulation scheme with pulses as short as 1 µs. Ambient light rejection is automatic without the need of external control loops, dc current subtraction, or digital algorithms.

The LED driver is a current sink and is independent from the LED supply voltage and the LED type. The optical measurement path produces a high SNR for relatively low LED power, while greatly reducing the effect of ambient light on the measured signal.

Analog Signal Path

The analog signal path of the optical signal chain consists of four current inputs that can be configured as single-ended or differential pairs into one of two independent channels. The two channels can be sampled simultaneously for applications that require instantaneous sampling of two sensors.

Analog Input Multiplexer

The optical signal chain supports four analog input pins. Each input can be used as a single-ended input or as part of a differential pair. Figure 27 shows a single representation of the input switch matrix, which allows a programmable connection to the two optical channels. Each pair of inputs has a duplicate of this multiplexer: IN1 and IN2, and IN3 and IN4. The connections are programmable per time slot.

The PAIR12 and PAIR34 bits select whether the matching input pair is used as two single-ended inputs or as a differential pair. This selection is valid for all active time slots. The INP12_x and INP34_x bits specify whether the input pair is enabled during the corresponding time slot and, if enabled, which input is connected to which optical channel.

The sleep conditions are used for any inputs that are not enabled. Sleep conditions are determined by the INP_SLEEP_12 and INP_SLEEP_34 bits, which specify the state for the input pairs during sleep and when the inputs are not active. Inputs are only considered active during the precondition and pulse regions for time slots where they are enabled.

Preconditioning of the sensor connected to the input is provided to set the operating point at the input before sampling. There are several different options for preconditioning determined by the PRECON_x bits. The PRECON_x bits are provided for each time slot to specify the precondition for enabled inputs or input pairs during the corresponding time slot. Preconditioning options include floating the inputs, VC1, VC2, input common-mode voltage (V_{ICM}), internal voltage reference signal for the TIA (TIA_V_{REF}), TIA input, and shorting the input pair. The preconditioning time at the start of each time slot is programmable using the PRE_WIDTH_x bits. The default preconditioning period is 8 µs.

The block diagram in Figure 27 shows the bias levels that can be switched into the input connections during sleep and preconditioning. These connections are not available during the sampling phase of a time slot in which the input is selected.

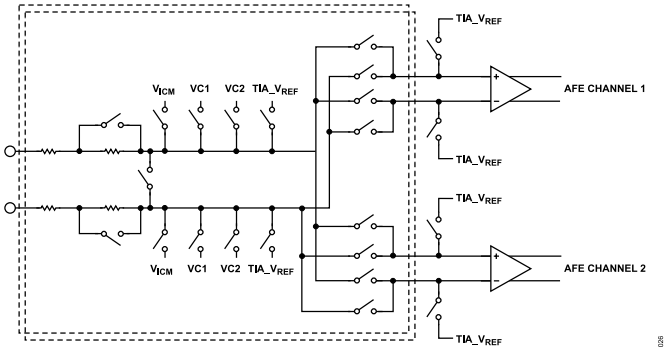


Figure 27. Switch Matrix Block Diagram

Ambient Light Cancellation

The ADPD6000 has three modes to perform ambient light cancellation, as follows:

- Coarse tuning only
- Coarse and fine tuning loop
- External microcontroller unit (MCU) control

Coarse tuning only mode and coarse and fine tuning loop mode are automatically controlled by the ADPD6000 without any software assistance. External MCU control mode allows tuning the ambient light rejection through an external algorithm.

Use the AMBIENT_CANCELLATION_x bits to choose the mode.

Coarse tuning mode works at the beginning of each PPG time slot. This mode measures the ambient light level and sets the ambient DAC code. This circuitry needs 48 µs to complete these activities and determine the baseline of the ambient DAC. Afterward, the

THEORY OF OPERATION

PPG channel can start normal operation–for example, if in digital integration mode, the PPG receiver channel can start to take dark samples. This ambient baseline is used in the time slot if coarse tuning only mode is enabled.

If coarse and fine tuning loop mode is enabled, the coarse tuning circuit works the same way as in coarse tuning mode. However, the ambient DAC code updates after each dark sample measurement.

Select these two modes with the AMBIENT_CANCELLATION_x bits for system level design flexibility.

Coarse loop mode makes the measurement to find the accurate value of the ambient current. Then, the ambient DAC subtracts the ambient current at the beginning of the signal chain so that it does not corrupt the PPG signal measurement.

Both analog integration mode and digital integration mode can perform coarse loop ambient rejection.

The fine tuning loop updates the ambient information after each dark sample measurement. This feature is available only in digital integration mode.

The MCU mode allows the user to subtract the ambient current. The DAC_AMBIENT_CH1_x and DAC_AMBIENT_CH2_x bits are designed to allow the user to fill in the current ambient value, and the AFE then subtracts that value from the signal chain. DAC_AMBIENT_CH1_x and DAC_AMBIENT_CH2_x are 9-bit fields, with each LSB representing a 0.6 µA step in a 0 µA to 300 µA range.

LED DC Cancellation

Besides the ambient DAC, there is another IDAC at the input of each signal chain. This IDAC is used to subtract the unwanted dc component in the reflected LED to increase the dynamic range of the receiver channel.

These two IDACs are controlled by the MCU only. The DAC_LED_DC_CH1_x and DAC_LED_DC_CH2_x bits control the LED dc canceling, 7-bit IDAC with full scale.

The LED dc subtraction feature is available only for digital integration mode.

A certain amount of dc current can be subtracted from the AFE based on the top level optical and system design. DAC_LED_DC_CH1_x and DAC_LED_DC_CH2_x are 7-bit fields, with each LSB representing a 1.5 µA step in a 0 µA to 190 µA range.

LED Drivers

The optical path has two LED drivers, each of which is brought out to two LED driver outputs, providing a total of four LED output drivers. The device can drive up to two LEDs simultaneously, one from each driver pair. The LED output driver is a current sink. Figure 28 shows an example of a single LED driver output pair.

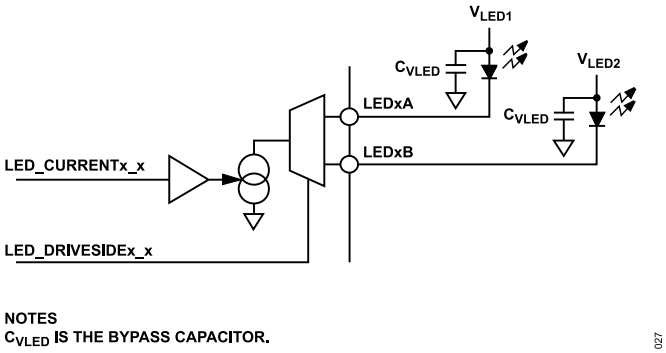


Figure 28. LED Driver Output Pair

The LED driver output pins (LED1A, LED1B, LED2A, and LED2B) have a maximum allowable pin voltage of 3.6 V. Any voltage exposure over this rating affects the reliability of the device operation and, in certain circumstances, causes the device to cease proper operation. The voltage of the LED driver output pins must not be confused with the supply voltages of the LEDs. V_{LEDx} is the voltage applied to the anode of the external LED, whereas the LED output driver pin is connected to the cathode of the external LED. The compliance voltage is the amount of headroom voltage at the LED driver pin, measured with respect to ground, required to maintain the programmed LED current level. The compliance voltage is a function of the current required.

ECG SIGNAL CHAIN

The ECG channel measures the differential voltage across two electrodes to create a lead measurement. The output of this channel is a 24-bit digital word representing the measured ECG voltage. The maximum input differential signal is ±1.2 V, and the LSB size is 286 nV. The output data rate can be 250 SPS, 500 SPS, 1 kSPS, 2 kSPS, or 4 kSPS. This filter selection affects the digital processing but not the analog processing. Additionally, a 4 kHz ac lead off signal is converted by the analog ECG path and extracted in the digital domain.

The ECG channel has a dedicated ADC path with feedback arrangement to remove the dc offset presented by the ECG electrodes. The ECG channel is designed to provide a high quality ECG signal process while suppressing the large dc offset that is caused by the complex system design.

Both DCLO detection and ACLO detection are integrated to accommodate different complex lead contact conditions to provide reliable lead information.

The RLD pin is designed to better bias the human body potential to avoid interference.

ECGIP and ECGIN are the signal inputs for the ECG channel, and they must be connected to the input leads. The RLD pin must be connected to the reference lead.

THEORY OF OPERATION

ECG Main Signal Chain

Figure 29 shows the ECG main signal chain diagram.

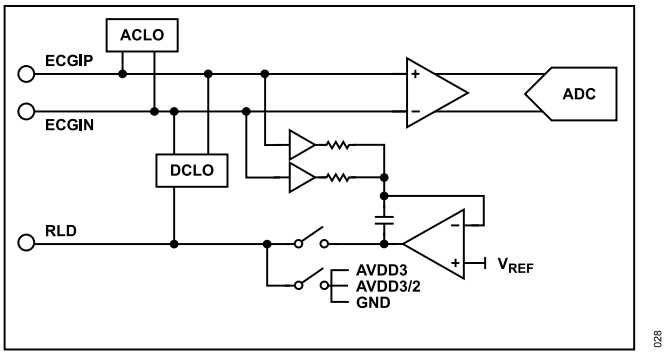


Figure 29. ECG Main Signal Chain Diagram

DCLO Detection

The DCLO circuit injects a small programmable dc current into each input electrode and monitors the resulting electrode voltage. Figure 30 shows the DCLO detection diagram.

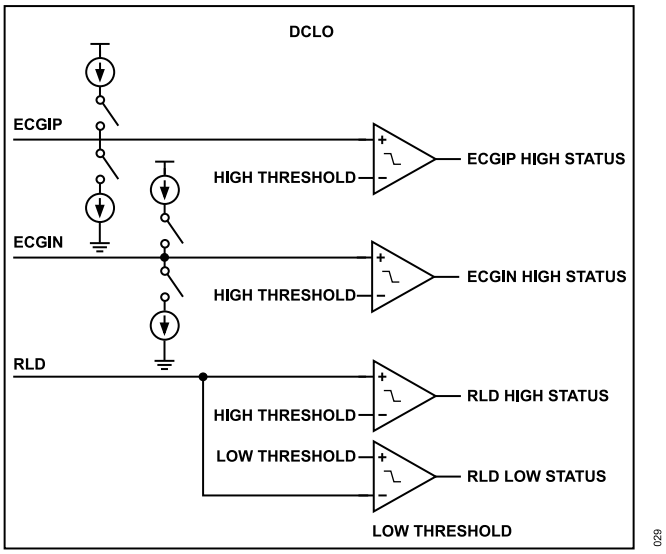


Figure 30. DCLO Detection Diagram

When both ECGIP and ECGIN, are properly connected, the current flow from one of the ECG inputs through the patient and into the other ECG input produces a minimal voltage shift. The fail current magnitude is common across all the ECG electrodes and programmable with a step size of 2 nA over a ±16 nA range using the ECG_DCLO_MAG bit field to change the magnitude.

The polarity of the fail current is independent for each electrode and programmed using ECG_DCLO_POLARITY_IN and ECG_DCLO_POLARITY_IP. When an electrode connection degrades or falls off, the pin voltage of that electrode is pulled high or low depending on the programmed fail current polarity.

The DCLO detection circuit is based on each individual electrode input (ECGIP and ECGIN). The detection circuit is comparator based with independent programmable threshold levels for ECG inputs.

For each input lead (ECGIP and ECGIN), there is only one comparator with a high-side threshold. For the RLD pin, there are two comparators with a high-side threshold and low-side threshold.

These threshold limits are chosen such that all the threshold voltages cover the expected signal range. The window comparator compares the electrode input voltage with the corresponding threshold voltages. Where the voltage change on a particular electrode exceeds one of the programmed threshold voltages for that fail current, the dc resistance of the electrode contact can be determined to flag a lead off.

ACLO Detection

The ECG path has an ACLO detection circuit that can be used for lead off detection with the DCLO detection circuit to deal with different types of lead. Figure 31 shows the ACLO detection diagram.

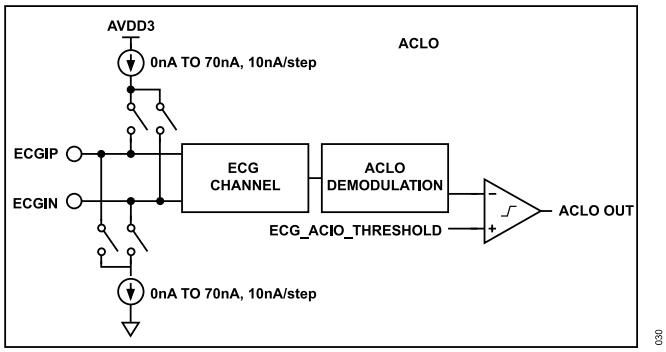


Figure 31. ACLO Detection Diagram

The ACLO method of sensing if the electrodes are connected to the patient is based on injecting ac currents into each ECG electrode and measuring the amplitudes of the resulting voltages through the ECG channel. The ECG channel must be enabled to use the ACLO function.

The magnitude of the ACLO current is programmable through the ECG_ACLO_MAG bit field. The ac current is driven out onto the ECG input paths and establishes a voltage between the ECG channel inputs where it is measured. The measured voltage is synchronously demodulated and sent through a comparator. The user can set the threshold though the ECG_ACLO_THRESHOLD bit field.

ACLO detection functions only on the ECG input pins (ECGIP and ECGIN) and is not supported for the RLD pin. A properly connected electrode has a small signal because the drive current flows into the right leg (RL). An improperly connected or dried out electrode has a larger signal as determined by a capacitive voltage divider.

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Right Leg Driver

The use of a driven reference benefits overall performance by improving common-mode rejection of noise and interference from external sources, such as power line interference (50 Hz/60 Hz) or other patient connected instruments. The drive stage also acts to absorb lead fail currents injected into the ECG electrodes.

The reference electrode drive circuit senses the patient common-mode voltage and drives an inverted version back to the body, creating a negative feedback loop around the patient. The RLD amplifier uses V_{CM} = AVDD3/2, which centers the electrode voltages in the middle of the ADC input range. Each electrode input is buffered and fed to the RLD amplifier through a switch.

The amount of capacitance on the RLD pin affects the RLD amplifier. For best performance, the capacitance on this node must be less than 2.2 nF. In normal operation, the RLD amplifier output is applied to the RL electrode via the RLD pin and associated protection network.

The RLD amplifier can be turned off and the user can drive the RLD pin by selecting a voltage in the ECG_RLD_OUT_SEL bit field.

BIA SIGNAL CHAIN

The BIA signal chain is designed for body impedance measurement. The signal chain consists of a high frequency precision excitation loop and a measurement channel, which enables a wide capability of measurement of the different bioimpedance configurations.

The excitation loop consists of a 12-bit DAC, referred to as the high speed DAC. This DAC is capable of generating high frequency excitation signals up to 250 kHz.

The measurement channel features an ADC with input buffers, a built in antialias filter, and a PGA.

An ultralow leakage, programmable switch matrix connects the sensor to the internal analog excitation and measurement blocks. This matrix provides an interface for connecting external bioimpedance and calibration resistors. Figure 32 shows the block diagram of this BIA signal chain.

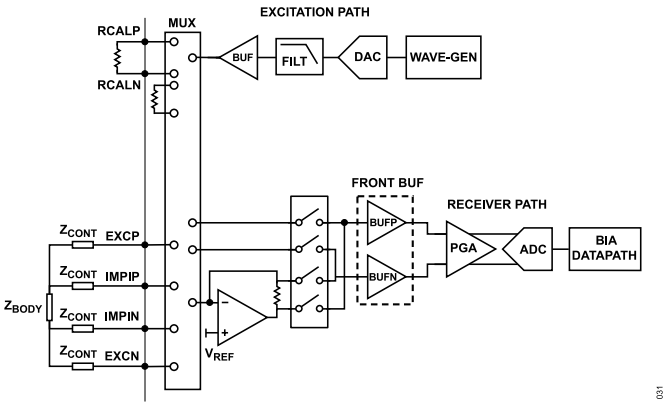


Figure 32. BIA Channel Block Diagram (Z_{CONT} Is Contact Impedance and Z_{BODY} Is Human Body Impedance)

The input multiplexer (mux) of the excitation loop is controlled by the BIOZ_TSW_x, BIOZ_TRSW_x, BIOZ_DSW_x, BIOZ_DRSW_x. The input mux for the measurement path is controlled by the BIOZ_NCHAN_x and BIOZ_PCHAN_x. Table 10 shows the connections of the input mux with the related bit setting. The flexible design of the BIA channel allows different configurations of the measurement.

Table 10. TIA Connections in the BIA Channel

Bit Name	Setting	Connection
BIOZ_TSW_x	0001	IMPIP
	0010	IMPIN
	0100	EXCP
	1000	EXCN
BIOZ_TRSW_x	1	RCALN
BIOZ_RINT_SW_x, Bit 1	1	R_{INT_SN}[1]
BIOZ_DSW_x	0001	IMPIP
	0010	IMPIN
	0100	EXCP
	1000	EXCN
BIOZ_DRSW_x	1	RCALP
BIOZ_RINT_SW_x, Bit 0	1	R_{INT_SP}[1]
BIOZ_PCHAN_x and BIOZ_NCHAN_x	00	TIA
	01	IMPIP and IMPIN
	10	RCALN and RCALP
	11	R_{INT}

[1] R_{INT_SN} and R_{INT_SP} refer to the two terminals of the internal resistor (R_{INT}).

The frequency of the generated sine wave is controlled by BIOZ_SINEFCW_x_x, whereas the amplitude of the sine wave is controlled by BIOZ_SINEAMPLITUDE_x. BIOZ_SINE_PHASE_OFFSET_x is used to control the sine wave phase.

Equation 2 and Equation 3 show how to set the voltage output (V_{OUT}) amplitude and sine wave frequency with these bits, respectively, as follows:

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$$V_{OUT} = 0.8 \times \frac{BIOZ_SINEAMPLITUDE_x}{2^{11}} Vp\text{ - }p \quad (2)$$

$$Frequency = \frac{32M \times BIOZ_SINEFCW_x_x}{2^{26}} Hz \quad (3)$$

BIOZ_DAC_GAIN_x and BIOZ_DAC_OFFSET_x are used to give more flexible control of the generated sine wave for different applications.

The TIA gain can be accessed through BIOZ_TIA_RGAIN_x.

After digitizing the measurement, the ADC output is sent to the datapath of the BIA channel, which includes filters, gain controls, and the DFT path (see the Datapath section for more information). The DFT result is I data and Q data of the received sine wave, and the data format is 18 bits.

When the chain turns on, the DFT path can wait before performing the DFT. The waiting time is controlled by BIOZ_ADC_CONV_DLY_x.

For accurate measurement, the chip must perform ratio measurement. That is, the chip needs to measure the known external resistor at the RCALP and RCALN pins, and then measure the unknown resistor. Use the ratio method to calculate the resistor under test.

FIFO

The FIFO is never written with partial packets of data. If there is not enough room for the data that is written to the FIFO for all enabled time slots and any selected status bytes, no data is written from any of the time slots during that period and the INT_FIFO_OFLOW status bit is set.

The order of samples written to the FIFO (if selected) is dark followed by lit data. Table 11 shows the byte order for multibyte words.

Table 11. Byte Order for FIFO Writes

Size	Byte Order (After Shift)
8	[7:0]
16	[15:8], [7:0]
24	[23:16], [15:8], [7:0]
32	[31:24], [23:16], [15:8], [7:0]

The FIFO size is 640 bytes. When the FIFO is empty, a read operation returns 0xFF and the INT_FIFO_UFLOW status bit is set.

ECG Data Format

The data in the ECG is channel is 24-bit unsigned data with a status byte as a header. Figure 33 shows the data in the ECG channel.

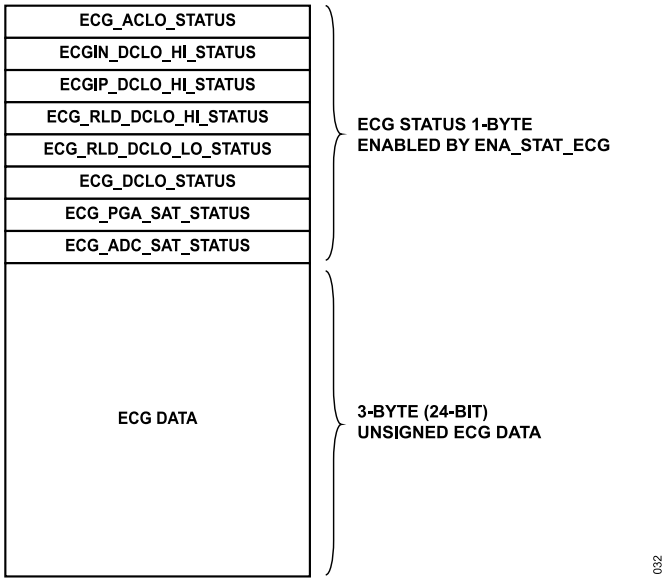


Figure 33. ECG Data Format

If ENA_STAT_ECG is set to 1, the ECG output data is a 4-byte structure, where the highest byte is the ECG related status information. If ENA_STAT_ECG is set to 0, the ECG output data is a 3-byte structure with only ECG channel output data.

PPG Data Format

At the end of each time slot, the selected data is written to the FIFO. The packet can include 0-, 8-, 16-, 24-, or 32-bit data for each of the dark data, signal data, or lit data values. The bit alignment of the data written to the FIFO is selectable with a shift of 0 bits to 31 bits, with saturation provided. Lower bits are ignored. The DARK_SIZE_x, LIT_SIZE_x and SIGNAL_SIZE_x bits select the number of bytes of each field to be written from 0 bytes to 4 bytes. When set to 0, no data is written for that data type. The DARK_SHIFT_x, LIT_SHIFT_x, and SIGNAL_SHIFT_x bits select the number bits to shift the output data to the right before writing the FIFO. If there are any significant bits at more significant bit positions than those selected, the data written to the FIFO is saturated.

The order of samples written to the FIFO (if selected) is signal data followed by dark data and then lit data. If both channels are enabled, all selected Channel 1 data values are written to the FIFO first, followed by the Channel 2 data.

For example, in modes that use dark data, the eight upper bits of the dark data can be stored with 24 appropriately selected bits from the signal data for each time slot. This method detects whether the ambient light is becoming large, while limiting the size of the amount of data transferred.

PPG Data Format shows the PPG data format in the FIFO.

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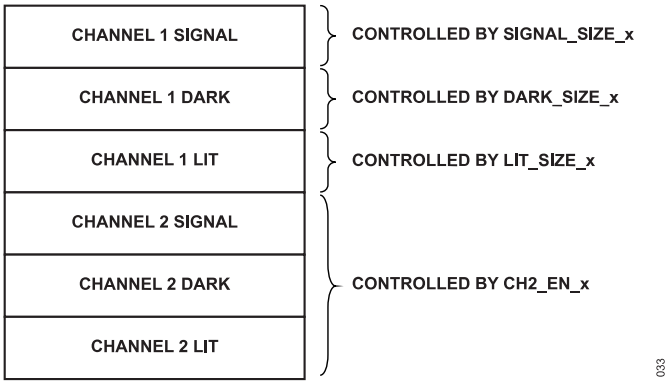


Figure 34. PPG Data Format

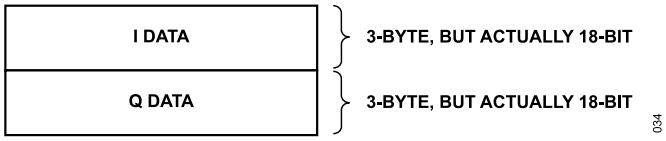


Figure 35. BIA Data Format

Data Arrangement in the FIFO

The data in the FIFO is arranged according to the enabled time slots and follow the same sequence.

For example, Figure 36 shows the data in the FIFO if one ECG time slot, three PPG time slots, and two BIA time slots are enabled.

BIA Data Format

The BIA data format is 3-byte I data followed by 3-byte Q data. Figure 35 shows the BIA data format in the FIFO.

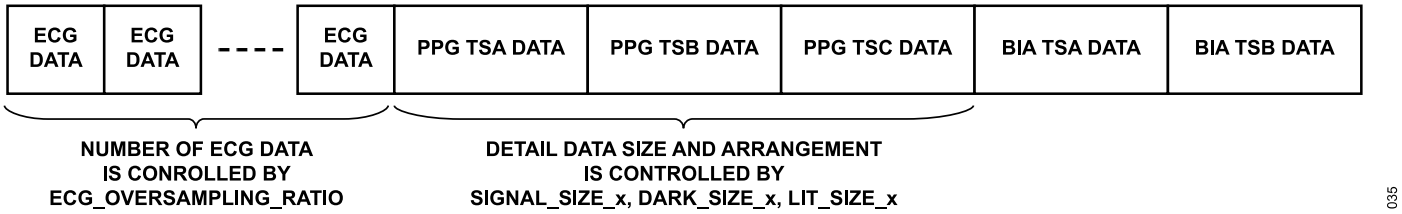


Figure 36. Example of Data Arrangement in the FIFO (TSA Is Time Slot A, TSB Is Time Slot B, and TSC Is Time Slot C)

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CLOCKING

Low Frequency Oscillator

A low frequency oscillator clocks the low speed state machine, which sets the time base used to control the sample timing, wake-up states, and overall operation. There are three options for low frequency oscillator generation. The first option is an internal 960 kHz oscillator. The second option is for the host to provide a low frequency oscillator externally. Finally, the low frequency oscillator can be generated by a divide by 32 of an external high frequency clock source at 32 MHz. When powering up the device, it is expected that the low frequency oscillator be enabled and left running continuously.

To operate with the on-chip low frequency oscillator, use the following writes. Set the OSC_960K_EN bit to 1 to turn on the internal oscillator. The internal 960 kHz clock frequency is set using the 10-bit OSC_960K_FREQ_ADJ bits.

If higher timing precision is required than can be provided by the on-chip low frequency oscillator, the low frequency oscillator can be driven directly from an external source provided on a GPIOx input. To enable an external low frequency clock, use the following writes. Enable one of the GPIOx inputs using the GPIO_PIN_CFGx bits. Next, use the ALT_CLK_GPIO bits to choose the enabled GPIOx input to be used for the external low frequency oscillator. Set the ALT_CLOCKS bits to 0x1 to select an external low frequency oscillator.

In a third method, an external 32 MHz clock is used for both the high frequency clock and to be divided down to generate the low frequency clock. To use this method, follow the previous instructions for an external low frequency clock but set the ALT_CLOCKS bits to 0x3, and a divide by 32 used to generate the low frequency clock so that a 1 MHz clock is generated from the external 32 MHz clock.

High Frequency Oscillator

A 32 MHz high frequency oscillator is generated internally or can be provided externally. This high frequency clock clocks the high speed state machine, which controls the AFE operations during the time slots, such as LED timing, integration times, and BIA excitation frequency.

The high frequency oscillator can be internally generated by setting the ALT_CLOCKS bits to 0x0 or 0x1. When selected, the internal 32 MHz oscillator is enabled automatically by the low speed state machine during the appropriate wake-up time or during the 32 MHz oscillator calibration routine.

The high frequency oscillator can also be driven from an external source. To provide an external 32 MHz high frequency oscillator, enable one of the GPIO inputs using the GPIO_PIN_CFGx bits. Then, use the ALT_CLK_GPIO bits to choose the enabled GPIOx input for the external high frequency oscillator. Finally, write 0x2 or 0x3 to the ALT_CLOCKS bits to select an external high frequency oscillator. Writing 0x2 provides only the high frequency oscillator from the external source, whereas writing 0x3 generates both the low frequency oscillator and high frequency oscillator from the external 32 MHz source. When using an external 32 MHz oscillator, it must be kept running continuously for proper device operation.

TIME STAMP OPERATION

The time stamp feature is useful for calibrating the low frequency oscillator as well as providing the host with timing information during time slot operation. Timestamping is supported by the use of any GPIO as a time stamp request input, the CAPTURE_TIMESTAMP bit to enable capture of the time stamp trigger, a time counter running in the low frequency oscillator domain, and two output registers. The output bits include TIMESTAMP_COUNT_x, which holds the number of low frequency oscillator cycles between time stamp triggers, and TIMESTAMP_SLOT_DELTA, which holds the number of low frequency oscillator cycles remaining to the next time slot start.

The setup for using the time stamp operation is as follows:

1. Set OSC_CAL_ENABLE = 1 to enable the oscillator calibration circuitry.
2. Configure a GPIO to support the time stamp input using the appropriate GPIO_PIN_CFG_x bits. Select the matching GPIOx to provide the time stamp using the TIMESTAMP_ GPIO bits.
3. Configure the ADPD6000 for operation and enable the low frequency oscillator.
4. If the TIMESTAMP_SLOT_DELTA function is desired, start the time slot operation by placing the device in go mode using the OP_MODE bit (see Table 12). For low frequency oscillator calibration, it is only required that the low frequency oscillator is enabled. The device does not have to be in go mode for low frequency oscillator calibration.

Use the following procedure to capture the time stamp:

1. Set the CAPTURE_TIMESTAMP bit to 1 to enable the capture of the time stamp on the next rising edge of the selected GPIOx input.
2. The host provides the initial time stamp trigger on the selected GPIOx at an appropriate time.
3. The CAPTURE_TIMESTAMP bit is cleared when the timestamp signal is captured unless the TIMESTAMP_ ALWAYS_EN bit is set, in which case, the capture of the time stamp is always enabled. Reenable the capture if necessary.
4. The host provides a subsequent time stamp trigger on the selected GPIO at an appropriate time.
5. The number of low frequency oscillator cycles that occurred between time stamp triggers can be read from the TIMESTAMP_COUNT_x bits.

The host must continue to handle the FIFO data normally during time stamp processing.

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If using a dedicated pin for a time stamp that does not have transitions other than the time stamp, set the TIMESTAMP_ ALWAYS_EN bit to avoid automatic clearing of the CAPTURE_ TIMESTAMP bit. This setting removes the need to enable the time stamp capture each time.

The host can also use TIMESTAMP_SLOT_DELTA to determine when the next time slot occurs. TIMESTAMP_SLOT_DELTA can determine the arrival time of the samples currently in the FIFO.

The time stamp trigger is edge sensitive and can be set to either trigger on the rising edge (default) or falling edge using TIMESTAMP_INV.

Low Frequency Oscillator Calibration

The time stamp circuitry can calibrate the 960 kHz low frequency oscillator circuit by adjusting the frequency to match the timing of the time stamp triggers. Simply compare the TIMESTAMP_COUNT_x value in low frequency oscillator cycles to the actual time stamp trigger period and adjust the OSC_960K_FREQ_ADJ value accordingly.

High Frequency Oscillator Calibration

The high frequency oscillator is calibrated by comparing multiples of its cycles with multiple cycles of the low frequency oscillator, which is calibrated to the system time. Calibration of the low frequency oscillator precedes calibration of the high frequency oscillator. The method for calibrating the high frequency oscillator is as follows:

1. Set OSC_CAL_ENABLE = 1 to enable the oscillator calibration circuitry.
2. Write 1 to the OSC_32M_CAL_START bit.
3. The ADPD6000 automatically powers up the high frequency oscillator.
4. The device automatically waits for the high frequency oscillator to be stable.
5. An internal counter automatically counts the number of 32 MHz high frequency oscillations that occur during 128 cycles of the 960 kHz low frequency oscillator.
6. The OSC_32M_CAL_COUNT bits update with the final count.
7. The 32 MHz oscillator automatically powers down following calibration unless time slots are active.
8. The device resets the OSC_32M_CAL_START bit indicating the count has updated.

The OSC_32M_FREQ_ADJ bits adjust the frequency of the 32 MHz oscillator to the desired frequency. When using an external low frequency oscillator, the 32 MHz oscillator calibration is performed with respect to the externally provided low frequency oscillator.

When the calibrations of the low frequency and high frequency oscillators are complete, set CLK_CAL_ENA = 0 to disable the clocking of the oscillator calibration circuitry to reduce the power consumption. CLK_CAL_ENA defaults to 0 so that the calibration circuitry is disabled by default.

EXECUTION MODES

A state machine in the low frequency oscillator clock domain controls sleep times, wake-up cycles, and the start of time slot operations. The low frequency oscillator serves as the time base for all time slot operations, controls the sample rates, and clocks the low frequency state machine. This state machine controls all operations and is controlled by the OP_MODE bit.

Table 12. OP_MODE Bit Setting Descriptions

OP_MODE Setting	Mode	Description
0	Standby	All operations stopped. Time slot actions reset. Low power standby state.
1	Go	Transitioning to this state from standby mode starts time slot operation.

At power-up and following any subsequent reset operations, the ADPD6000 is in standby mode. The user can write 0 to the OP_MODE bit to immediately stop operations and return to standby mode.

The time slots are enabled by the ECG_TIMESLOT_EN, PPG_TIMESLOT_EN, and BIOZ_TIMESLOT_EN bits in the OPMODE register (see Table 1). Set ECG_TIMESLOT_EN to 1 enable the ECG time slot. Set the BIOZ_TIMESLOT_EN value and PPG_TIMESLOT_EN value to enable the corresponding BIOZ time slots and PPG time slots, respectively.

After enabling the desired time slots, set the OP_MODE bit to 1 to start the chip operation.

Register writes that affect operating modes cannot occur during go mode. The user must enter standby mode before changing the control registers. Standby mode resets the digital portion of the ADC, all of the pulse generators, and the state machine.

When OP_MODE is set to 1, the device immediately starts the first wake-up sequence and time slot operations unless using an external synchronization trigger. If using an external synchronization trigger, the device enters the sleep state before the first wake-up and time slot regions begin.

HOST INTERFACE

The ADPD6000 uses an SPI to communicate with other devices. The device also provides numerous FIFO, error, and threshold status bits, each of which can be provided by an interrupt function from a GPIO, read from status registers, or appended as optional status bytes at the end of a FIFO packet.

Interrupt Status Bits

FIFO Threshold Interrupt

The FIFO threshold interrupt status bit, INT_FIFO_TH, is set when the number of bytes in the FIFO exceeds the value stored in the

THEORY OF OPERATION

FIFO_TH register. The INT_FIFO_TH bit is cleared automatically when a FIFO read reduces the number of bytes below the value in the FIFO_TH register, which allows the user to set an appropriate data size for their host needs.

The INT_FIFO_TH bit does not trigger if the FIFO byte count exceeds the threshold in the middle of any write of complete data. Instead, the INT_FIFO_TH bit is set at the next write to the FIFO. For example, if only PPG TSA is running, it only writes 4-byte lit data to the FIFO. Figure 37 shows the data in the FIFO.

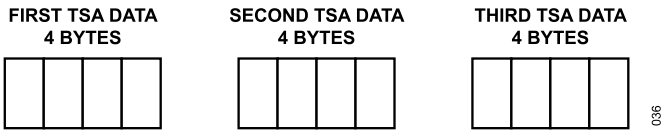


Figure 37. FIFO Threshold Interrupt Example

If the threshold is set as 4, the interrupt triggers at the beginning of the second TSA data write to the FIFO. If the threshold is set as 5, 6, or 7, the INT_FIFO_TH bit does not trigger until the write of the third TSA data. This method can help prevent any partial data read from the FIFO.

Clearing Interrupt Status Bits

All status bits are set regardless of whether the status bit is routed to one of the interrupt outputs, Interrupt X or Interrupt Y. The status bits are independent of the interrupt enable bits. The status bits are always set by the corresponding event. The interrupt bits stay set until they are either manually or automatically cleared.

The user can manually clear a given interrupt by writing a 1 to the matching interrupt status bit. In addition, the data interrupt status bits can be configured to clear automatically. When the INT_ACLEAR_FIFO bit is set, the appropriate interrupt status bit is automatically cleared when any matching FIFO register is read. Automatic clearing of the interrupt status bits removes the need to manually clear these interrupts.

Optional Status Bytes

There is an option to append each data packet with status bits. This option is useful for hosts that cannot spare an interrupt channel to service. The status bytes can each be individually selected in the FIFO_STATUS_BYTES register. Each bit in the FIFO_ STATUS_BYTES register enables a status byte that is appended to the data packet in the FIFO. If any bit in the FIFO_STATUS_ BYTES register is set to 1, the byte that is appended to the data packet contains the status bits.

The 4-bit sequence number cycles from 0 to 15 and is incremented with a wraparound every time the time slot sequence completes. This sequence number can also be made available bitwise on the GPIOx pins.

Interrupt Outputs, Interrupt X and Interrupt Y

The ADPD6000 supports two separate interrupt outputs, Interrupt X and Interrupt Y. Each interrupt has the option to be driven to any of the four GPIOx pins. The two different interrupt outputs can be generated for a host processor if desired. For example, the FIFO threshold interrupt, INT_FIFO_TH, can be routed to Interrupt X and used to drive the direct memory access (DMA) channel of the host, while the INT_FIFO_OFLOW and INT_FIFO_UFLOW interrupts can be routed to Interrupt Y and used to drive an additional host interrupt pin.

For each interrupt, there is an associated Interrupt X and Interrupt Y enable bit. See Table 1 for a full list of available interrupts that can be brought out on Interrupt X and Interrupt Y. The logic for the Interrupt X and Interrupt Y function is a logic AND of the status bit with its matching enable bit. All enabled status bits are then logically OR'ed to create the interrupt function. The enable bits do not affect the status bits.

General-Purpose I/Os

The ADPD6000 provides three general-purpose I/O pins: GPIO0, GPIO1, and GPIO2. These GPIOs can be used as previously described in the Interrupt Outputs, Interrupt X and Interrupt Y section for interrupt outputs or for providing external clock signals to the device. The GPIOs can also be used for many different control signals, as synchronization controls to external devices, as well as test signals that are useful during system debugging. All of the available signals that can be brought out on a GPIOx pin are listed in Table 1.

IOVDD Supply Voltage Consideration

The ADPD6000 can operate with IOVDD as low as 1.7 V and as high as 3.6 V. LOW_IOVDD_EN in Register 0x0057 is set to 0x1 for IOVDD lower than 3 V. 0x1 is the default value for this bit because the typical IOVDD value is 1.8 V.

If 3 V or higher is supplied for IOVDD, the LOW_IOVDD_EN bit must be set to 0x0 for proper operation.

SPI

The ADPD6000 contains an SPI port that operates synchronously with its input clocks.

The ADPD6000 has an internal power-on reset circuit that sets the device into a known idle state during the initial power-up. After the power-on reset is released, approximately 2 µs to 6 µs after the DVDD supply is active, there is an initialization state that sets the register default values. This initialization state lasts approximately 15 µs to 20 µs. The device can then be read and written through the SPI.

The registers are accessed using addresses within a 15-bit address space. Each address references a 15-bit register with one address reserved for the FIFO read accesses. For SPIs, reads and writes

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auto-increment to the next register if additional words are accessed as part of the same access sequence. This automatic address increment occurs for all addresses except the FIFO address, one less than the FIFO address and the last used address, which is 0x351. Reads from the FIFO address continue to access the next byte from the FIFO.

SPI Operations

The SPI single register write operation is shown in Figure 38. The first two bytes contain the 15-bit register address and specify that a write is requested. The remaining two bytes are the 16 data bits to write to the register. The register write occurs only when all 16 bits are shifted in prior to deassertion of the $\overline{CS}$ signal.

In addition, multiple registers can be written if additional 16-bit data is shifted in before deassertion of the $\overline{CS}$ signal. The register address automatically increments to the next register after each 16 bits of data.

The SPI single register read operation is shown in Figure 39. The first two bytes contain the 15-bit register address and specify that a read is requested. Register bits are shifted out starting with the MSB. In addition, multiple registers can be read if additional 16-bit data is shifted out prior to deassertion of the $\overline{CS}$ signal.

It is recommended that reading from the FIFO is performed byte wise. There is no requirement to read multiples of 16 bits.

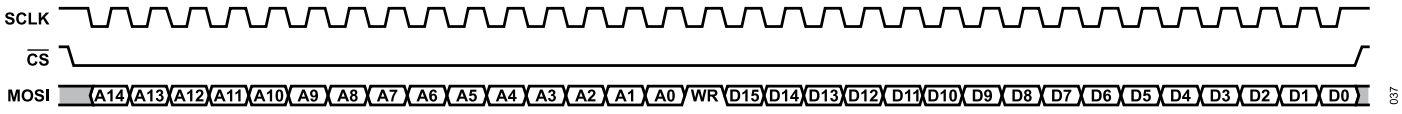


Figure 38. SPI Write Operation

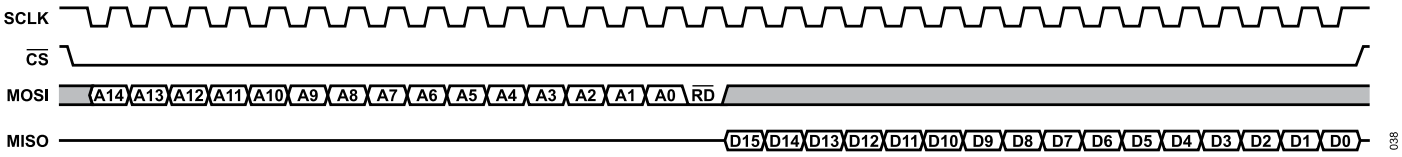


Figure 39. SPI Read Operation

APPLICATIONS INFORMATION

OPTICAL PATH

Digital Integration Mode

The ADPD6000 supports a digital integration mode in the optical path to accommodate sensors that require longer pulses. Digital integration mode allows the system to use a larger LED duty cycle, which may result in the highest achievable levels of SNR.

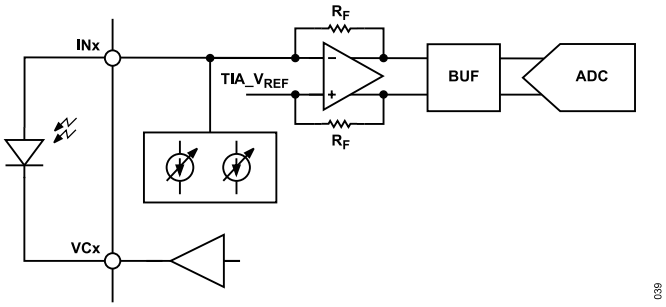


Figure 40. Signal Path for Digital Integration Mode

In digital integration mode, the integrator is configured as a buffer, resulting in the signal path shown in Figure 40. Digital integration regions are configured by the user and separated into lit and dark regions. The LED is pulsed in the lit region, and the LED is off in the dark region. ADC samples are taken at 1 µs intervals within the lit and dark regions and are then digitally integrated. The integration of the ADC samples from the dark region is subtracted from the integration of the ADC samples from the lit region and the result is written into the relevant FIFO. Both signal and dark values can be written to the FIFO.

The ADPD6000 supports one-region and two-region digital integration modes. In one-region digital integration mode, an equal number of dark and lit samples are taken where all of the dark samples are taken in the dark region just prior to the lit region. One-region digital integration mode is shown in the timing diagram in Figure 41.

In two-region digital integration mode, an equal number of dark and lit samples are taken. However, the dark region is split such that half of the samples are taken in the dark region prior to the lit region, and the other half is taken in the dark region following the lit region. The two-region digital integration mode results in higher ambient light rejection than the one-region digital integration mode in situations with a varying ambient light level. A timing diagram for two-region digital integration mode is shown in Figure 42.

The signal data for one-region digital integration mode that reads from the FIFO follows Equation 4:

$$Signal = (I_{PD} \times R_{TIA} \times TIA_Config \times Buf_Gain \times NUM_INT_x \times NUM_REPEAT_x)/(146\mu V/LSB) \quad (4)$$

where:
I_{PD} is the PD current.
TIA_Config is the TIA configuration.
Buf_Gain is the buffer gain.

The signal data for two-region digital integration mode that reads from the FIFO follows Equation 5:

$$Signal = ((I_{PD} \times R_{TIA} \times TIA_Config \times Buf_Gain \times NUM_INT_x \times NUM_REPEAT_x)/(146\mu V/LSB)) \times 2 \quad (5)$$

The AFE_PATH_CFG_x, CHx_TRIM_INT_x, and CHx_TRIM_INT_CAP_x bits need to follow a certain combination in digital integration mode (both one-region mode and two-region mode). Table 13 shows the recommended settings of these bits. The TIA gain setting is independent of these settings.

Table 13. Bit Settings for AFE Path in Digital Integration Mode

Bit Name	Recommended Setting
AFE_INT_C_BUF_x	0x0
AFE_PATH_CFG_x	0x28
CHx_TRIM_INT_x	0x3
CHx_TRIM_INT_CAP_x	0x1

The result of the configurations of the bits in Table 13 is 1× TIA configuration with buffer gain = 2.

Table 14 shows the relevant register settings for the digital integration modes of operation. The MIN_PERIOD_x bits must be set manually with the proper period because the minimum period is not automatically calculated in digital integration mode.

The recommended MIN_PERIOD_x setting for one-region digital integration mode is as follows:

$$MIN_PERIOD_x = NUM_INT_x \times 2 + (2 + t_D) \times 2$$

The recommended MIN_PERIOD_x setting for two-region digital integration mode is as follows:

$$MIN_PERIOD_x = NUM_INT_x \times 4 + t_D \times 2 + 6\mu s$$

The t_D value is the response time of the optical device. The 6 µs time is essential for the ambient fine loop update.

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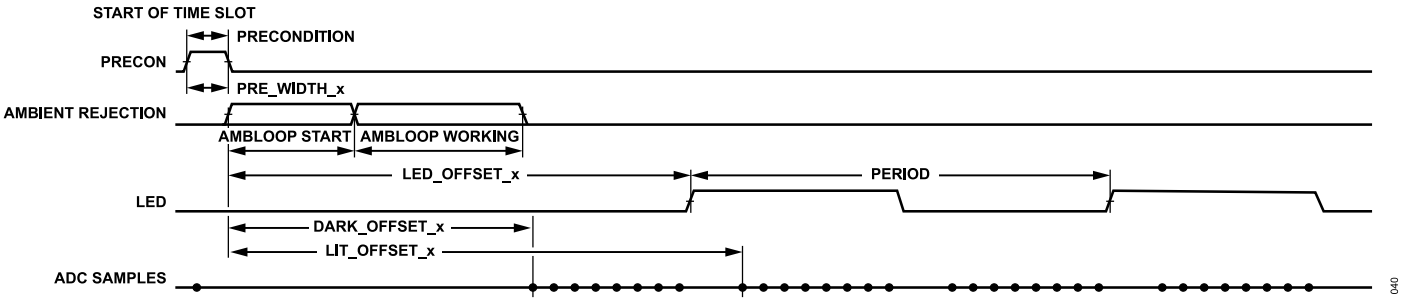


Figure 41. One-Region Digital Integration Mode Timing Diagram

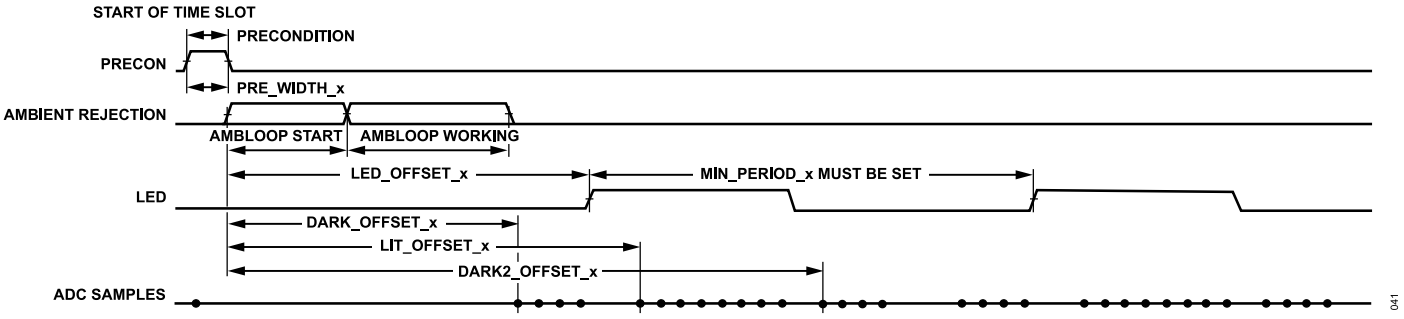


Figure 42. Two-Region Digital Integration Mode Timing Diagram

Table 14. Relevant Settings for Digital Integration Modes

Group	Time Slot A Register Address	Bit Field Name	Description
Signal Path Setup	0x0120, Bits[13:11]	SAMPLE_TYPE_x	Set to 0x2 for one-region digital integration mode. Set to 0x3 for two-region digital integration mode.
	0x0121, Bits[6:0]	AFE_PATH_CFG_x	Set to 0x28 for TIA, buffer, and ADC. Use 1x TIA configuration.
	0x0122, Bits[7:0]	INPxx_x	Enable desired inputs.
	0x0123, Bits[14:12]	PRECON_x	Set to 0x5 to precondition anode of photodiode to TIA_V_{REF}.
	0x0123, Bits[7:6], Bits[1:0]	VCx_SELECT_x	Set to 0x2 to set ~215 mV reverse bias across photodiode.
	0x0124, Bits[5:0]	TIA_GAIN_CHx_x	Select TIA gain.
	0x0124, Bits[9:8]	AFE_TRIM_VREF_x	Set to 0x2 to set TIA_V_{REF} = 0.8855 V.
	0x0124, Bits[12:11], Bits[14:13]	CH1_TRIM_INT_x	Set to 0x3 to set buffer gain = 2.
	0x125, Bits[13:12]	CH1_TRIM_INT_CAP_x	Set to 0x1 to 12.6 pF
Timing	0x012A, Bits[15:8]	NUM_INT_x	Set to the number of desired ADC conversions in the dark and lit regions.
	0x012A, Bits[7:0]	NUM_REPEAT_x	Number of sequence repeats.
	0x012B, Bits[9:0]	MIN_PERIOD_x	Set the period. Automatic period calculation is not supported in digital integration mode.
	0x0138, Bits[8:0]	LIT_OFFSET_x	Set to the time of the first ADC conversion in the lit region.
	0x0139, Bits[6:0]	DARK1_OFFSET_x	Set to the time of the first ADC conversion in the Dark 1 region.
	0x0139, Bits[15:7]	DARK2_OFFSET_x	Set to the time of the first ADC conversion in the Dark 2 region. Only used in two-region digital integration mode.
LED Settings	0x0129, Bits[1:0]	LED_MODEx_x	Select LED mode.
	0x0128, Bit 15 and Bit 7	LED_DRIVESIDEx_x	Select LED for time slot used.
	0x0128, Bits[14:8], Bits[6:0]	LED_CURRENTx_x	Set LED current for selected LED.
	0x012C, Bits[7:0]	LED_OFFSET_x	Sets start time of first LED pulse in 1 µs increments.
	0x012C, Bits[15:8]	LED_WIDTH_x	Sets width of LED pulse in 1 µs increments.

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Timing Recommendations for Digital Integration Mode

When setting the timing for digital integration mode, it is important to place the ADC samples such that the signal being sampled is given time to settle prior to the sample being taken. Settling time of the input signal is affected by photodiode capacitance and TIA settling time.

If automatic ambient light rejection is turned on (AMBIENT_CANCELLATION_x is set to either 1 or 2), some time is needed at the beginning of each time slot to enable the ambient rejection loop. The start-up time of this loop is 18 µs, and the working time of this loop is 30 µs.

The TIA_SAT_DET internal block must be turned on to speed up the TIA settling. Speeding up the TIA settling can help the TIA enter a normal working state quickly to make the automatic ambient rejection loop more accurate.

After the ambient loop completes, the first ADC sample of dark data can be enabled. The DARK1_OFFSET_x setting must be equal or larger than the ambient loop working time (48 µs).

Figure 43 shows an example of the proper placement of the ADC sampling edges.

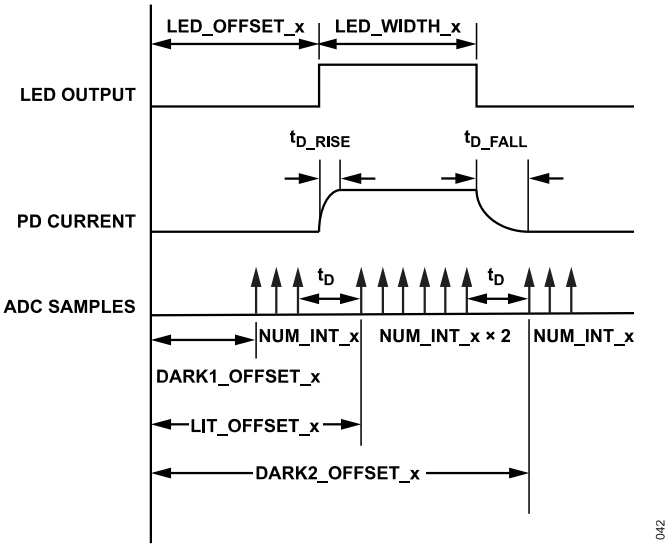


Figure 43. Proper Placement of ADC Sampling Edges in Digital Integration Mode

The recommended DARK1_OFFSET_x setting after the automatic ambient loop completes is 48 µs, or 10 µs if automatic ambient rejection is not turned on.

As shown in Figure 43, different optical devices, including the LED and photodiode, have different response times. t_{D_RISE} is the rising time of the photodiode current, and t_{D_FALL} is the falling time of the photodiode current. t_D is either t_{D_RISE} or t_{D_FALL}, depending on which one is bigger.

See the following equations:

$$LED_OFFSET_x = DARK1_OFFSET_x + (NUM_INT_x + t_D - t_{D_RISE}) \quad (6)$$

$$LIT_OFFSET_x = LED_OFFSET_x + t_{D_RISE} \quad (7)$$

$$DARK2_OFFSET_x = LED_OFFSET_x + LED_WIDTH_x + t_D \quad (8)$$

These values must be characterized in the final application. These settings only apply to two-region digital integration mode.

Table 15. Empirical Values for Two-Region Digital Integration Mode

Optical Device	Green (µs)	Red (µs)	Infrared (µs)
LED_WIDTH_x	24	24	36
PERIOD_x	58	60	138
NUM_INT_x	10	9	13
LED_OFFSET_x	60	59	91
LIT_OFFSET_x	64	65	101
DARK1_OFFSET_x	48	48	48
DARK2_OFFSET_x	90	91	167
t_{D_RISE}	4	6	10
t_{D_FALL}	6	8	40

Optimizing Sampling Sequence

If the empirical value is not appropriate for the measurement, optimize the sampling sequence.

See the following reference method for sweeping the curve (this example is based on TSA Channel 1 in a dark environment):

1. Enable the following settings:
   - One-region digital integration mode
   - 1× TIA configuration
   - AFE_TRIM_VREF_A = 3
   - AMBIENT_CANCELLATION_A = 0
   - NUM_INT_A = 1
   - NUM_REPEAT_A = 1
   - DARK1_OFFSET_A = 10
   - LED_OFFSET_A = 20
   - LED_WIDTH_A = 80
   - LIT_OFFSET_A = 130
   - MIN_PERIOD_A = 160
2. Power on the optical devices and enable TSA Channel 1.
3. Collect about 100 lit data values (remove the first 10 data values) and calculate the mean value.
4. Sweep the LIT_OFFSET_A bit from 130 to 10 and reproduce the result from Step 3.
5. Plot the mean value of the lit data and LIT_OFFSET_A. The response time of the optical device (for example, CT_DBLP3112) is shown in Figure 44.

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When collecting the lit data with the LIT_OFFSET_A bit changing, the data is lower than 16384 (unsaturated).

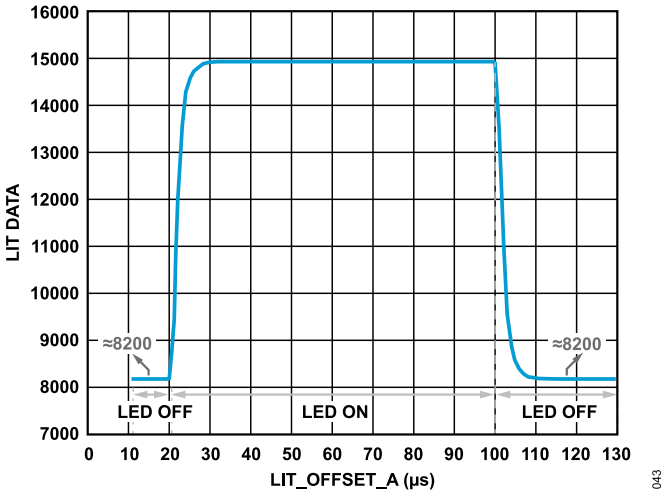


Figure 44. Timing of CT_DBLP3112 (Green LED)

ECG PATH

Figure 45 shows a typical connection diagram for the three-electrode ECG application. Figure 45 captures the external components required around ADPD6000, including current limitation resistors for the ECG channel. These component values were designed by users considering the maximum current of every channel. For example, it is suggested to use 51 kΩ, 51 kΩ, and 330 kΩ on the ECGIP, ECGIN, and RLD channels, respectively, for reference.

The signal data for ECG measurement that is read from FIFO follows Equation 9:

$$Signal = \frac{V_{IN}(V)}{Resolution} + 8,388,608 \quad (LSB) \tag{9}$$

Note that 8,388,608 is the center code of the ADC.

Table 16 shows the relevant register settings for the basic ECG measurement.

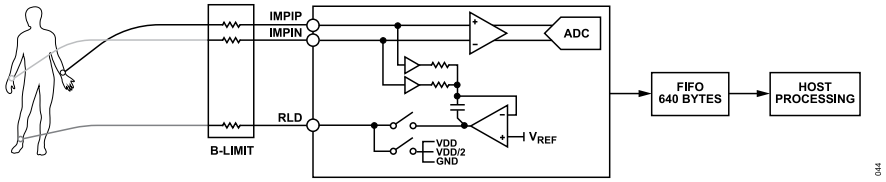


Figure 45. System Overview of ECG Circuit Showing ECG Channel Protection and External Components Requirements

Table 16. Relevant Settings for ECG Measurement

Group	Register Address	Bit Field Name	Description
ECG_ANA_CTRL	0x0100, Bit 10	ECG_INP_CONNECT	ECG input connection. Set 1 to connect the ECG inputs.
	0x0100, Bit 8	ECG_CHAN_RESOLUTION	Set to 0 for 286 nV/LSB, and set to 1 for 572 nV/LSB.
	0x0100, Bits[5:4]	ECG_RLD_OUT_SEL	Set to 0x3 to set regulated common-mode input.
	0x0100, Bit 3	ECG_RLD_SAT_EN	Set to 1 to enable DCLO for RLD.
	0x0100, Bits[2:1]	ECG_RLD_SAT_THRESHOLD	Select the DCLO threshold for RLD.
	0x0100, Bit 0	ECG_RLD_EN	Set to 1 to enable RLD.
ECG_LEADOFF_CTRL	0x0101, Bit 15	ECG_ACLO_EN	Set to 1 to enable the ACLO detector for the ECG inputs.
	0x0101, Bits[14:12]	ECG_ACLO_MAG	Select the ACLO excite current magnitude.
	0x0101, Bits[11:9]	ECG_ACLO_THRESHOLD	Select ACLO threshold for the ECG inputs.
	0x0101, Bit 8	ECG_DCLO_EN	Set to 1 to enable the DCLO detector for the ECG inputs.
	0x0101, Bits[7:4]	ECG_DCLO_MAG	Select the DCLO excite current magnitude.
	0x0101, Bit 3	ECG_DCLO_POLARITY_IN	Select DCLO output current polarity at ECGIN.
	0x0101, Bit 2	ECG_DCLO_POLARITY_IP	Select DCLO output current polarity at ECGIP.
	0x0101, Bits[1:0]	ECG_DCLO_THRESHOLD	Select DCLO threshold for the ECG inputs.
ECG_DIG_CTRL	0x0102, Bits[8:3]	ECG_OVERSAMPLE_RATIO	For ECG only mode, keep the default value. For multimodal, refer to the register description.
	0x0102, Bits[2:0]	ECG_ODR_SEL	Select the ECG ODR.

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Lead Off

DCLO detection uses the ECG_STATUS register to identify the lead connection status. Figure 46 shows an example of DCLO detection. In the case, R1, R2, and R3 are the contact impedances at ECGIP, ECGIN, and RLD, respectively.

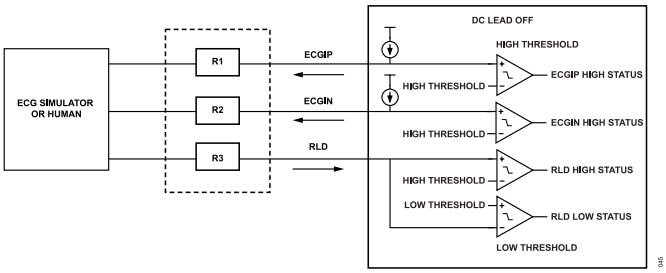


Figure 46. DCLO Detection Example

When using source current at ECGIP and ECGIN, the dc excitation current setting (ECG_DCLO_MAG) follows Equation 10:

If R1= R2 = R3 = 3R,

$$(DCLO\ \ Current\ \ Magnitude > High\ \ Threshold\ \ Voltage)/3R \quad (10)$$

Generally, the DCLO current magnitude setting is rounded up to nearest register value.

Table 17 is the ECG DCLO status truth table.

ACLO threshold selection depends on the particular cable, electrode, or protection scheme because these parameters are typically unique for the specific use case. Identifying the appropriate threshold can start with a high threshold and ratchet it down until a lead off is detected, then increase the threshold by some safety margin.

Table 18 shows the low threshold of electrode difference capacitance for ACLO detection.

Table 17. ECG DCLO Status Truth Table

Status	ECGIN_DCLO_HI_STATUS	ECGIP_DCLO_HI_STATUS	ECG_DCLO_STATUS
All Leads Failed	1	1	1
No Lead Failed	0	0	0
RLD Failed	1	1	1
ECGIN Right Arm (RA) Failed	0	1	1
ECGIP Left Arm (LA) Failed	1	0	1

Table 18. Low Threshold of Electrode Difference Capacitance for ACLO Detection

	ECG_ACLO_MAG						
ECG_ACLO_THRESHOLD	0x1	0x2	0x3	0x4	0x5	0x6	0x7
0x0	0.04 nF	0.08 nF	0.13 nF	0.17 nF	0.21 nF	0.25 nF	0.29 nF
0x1	0.05 nF	0.1 nF	0.14 nF	0.19 nF	0.24 nF	0.29 nF	0.33 nF
0x2	0.06 nF	0.11 nF	0.17 nF	0.22 nF	0.28 nF	0.33 nF	0.39 nF
0x3	0.07 nF	0.13 nF	0.2 nF	0.27 nF	0.33 nF	0.4 nF	0.47 nF
0x4	0.08 nF	0.17 nF	0.25 nF	0.33 nF	0.42 nF	0.5 nF	0.58 nF
0x5	0.11 nF	0.22 nF	0.33 nF	0.44 nF	0.56 nF	0.67 nF	0.78 nF
0x6	0.17 nF	0.33 nF	0.5 nF	0.67 nF	0.83 nF	1 nF	1.17 nF
0x7	0.33 nF	0.67 nF	1 nF	1.33 nF	1.67 nF	2 nF	2.33 nF

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BIA PATH

The BIA path in the ADPD6000 can be used to perform 4-wire impedance measurement on the body. This approach uses a high precision, ac voltage source to excite a sensor with a known ac voltage (VAC). To calculate the impedance, measure the current (I) that flows from the unknown impedance (Z_{UNKOWN}) and the voltage across the unknown impedance ($V_{Z_UNKNOWN}$). Calculate the impedance by using the following equation:

$$|Z_{UNKNOWN}| = \frac{V_{Z_UNKNOWN}}{I} \quad (11)$$

In real-world applications, medical devices must conform to the IEC 60601 standard. This standard limits the amount of dc and ac voltage that can be applied to the human body.

In Figure 47, there are discrete isolation capacitors (C_{ISO1}, C_{ISO2}, C_{ISO3}, and C_{ISO4}) that ensure no dc voltage occurs across the body. R_{LIMIT} limits the current provided to the sensor to conform to the IEC 60601 standard.

$R_{CONTACT}$ represents the resistances of the electrodes connecting to the unknown impedance.

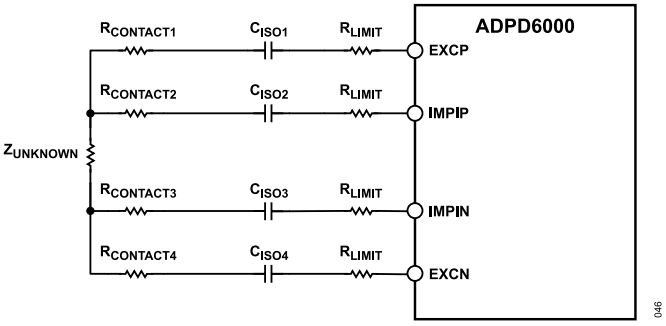


Figure 47. BIA Path Diagram

As shown in Figure 47, a 4-wire bioimpedance solution requires a precision ac voltage source, a high precision current meter, and a precision differential voltage meter.

The ADPD6000 uses a high speed DAC and waveform generator to generate the precision ac voltage. The device uses a high speed, high precision TIA for converting current from the sensor into a voltage measured by the ADC. The TIA channel measures the response current.

The ADC converts the current measurement with a 1 MSPS speed. A DFT is performed on the data. The DFT is implemented on the ADPD6000. The number of DFT points is configurable up to 8192. The ADPD6000 calculates the real and imaginary parts, and the host microcontroller calculates the unknown impedance of the sensor.

There are a number of discrete components needed in the system to guarantee safety and accuracy.

To conform to IEC 60601 standards, limit the amount of ac current entering the human body. The maximum allowable ac current is 500 µA at 50 kHz and 600 µA at 60 kHz. When calculating the R_{LIMIT} resistor value, the maximum output voltage from the ADPD6000 is 0.8 V p-p (0.2828 V rms). Set the maximum allowable ac current to 80% of maximum, or 400 µA rms. The following equation is the result of these values:

$$R_{LIMIT} = \frac{0.2828V\ \ rms}{400\mu A} = 707\Omega \quad (12)$$

As such, a ~1 kΩ R_{LIMIT} is selected and connected to the EXCP pin on the ADPD6000. This calculation ignores C_{ISOx} because of its small size.

To conform to IEC 60601 standards, a 10 µA maximum dc current is allowed to enter the human body. In this application, the dc current is guaranteed to be zero due to the addition of isolation capacitors. A value of 0.47 µF is selected for the isolation capacitors because 0.47 µF is a sufficiently large capacitance that is also available in small packages suitable for wearable electronics.

The ADPD6000 runs the BIA time slot and fills the FIFO with the DFT real and imaginary results for both the voltage and current measurements (four data points in total). The host microcontroller reads the data FIFO and uses the real and imaginary DFT results to calculate the unknown impedance. Calculate the impedance of the sensor by using the following equations:

$$Volage\ \ Measurement\ \ Magnitude = \sqrt{r^2 + i^2} \quad (13)$$

$$Voltage\ \ Measurement\ \ Phase = tan^{-1}\frac{i}{r} \quad (14)$$

To calculate the impedance, use Ohm's law by dividing the voltage magnitude by the current magnitude. Convert the current measurement value into a voltage using R_{TIA}. This gain must be taken into account. Therefore, the equation to determine the unknown impedance is as follows:

$$|Z_{UNKNOWN}| = \frac{Voltage\ \ Magnitude}{Current\ \ Magnitude} \times R_{TIA} \quad (15)$$

MULTIMODAL

Figure 48 shows the basic design reference schematic for PPG, ECG, and BIA multimodal applications.

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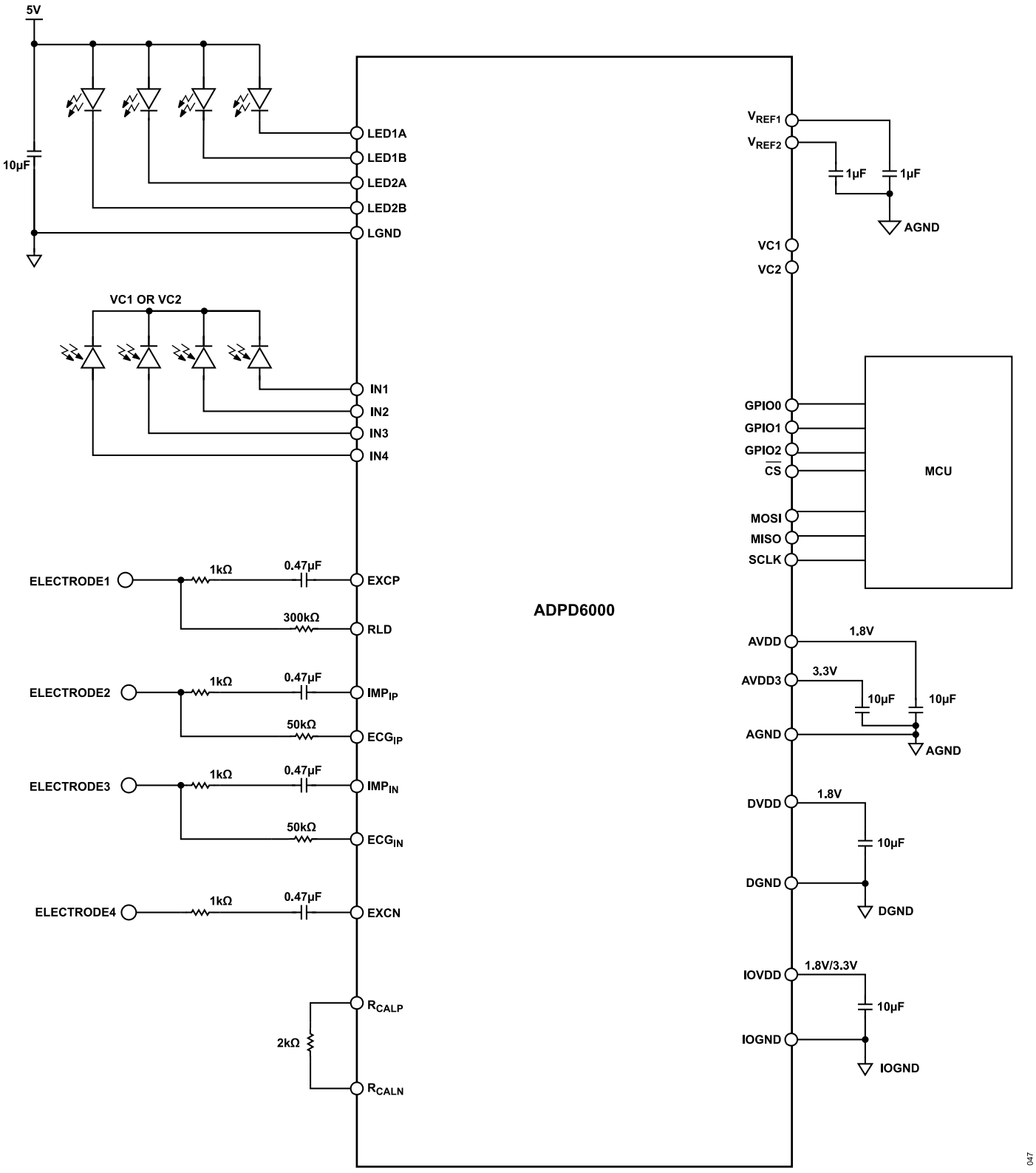


Figure 48. Multimodal Application Reference Schematic

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Recommended Configurations for Multimodal Measurement

The following is one of the recommended configurations for BIOZ, ECG, and PPG operation. The data pattern in the FIFO is ECG × 5 + PPG_A + PPG_B + BIOZ_A + BIOZ_B + BIOZ_C + BIOZ_D = 52 bytes.

```
#System configuration
0006 0034 # FIFO Interrupt Generation Thresh▶
old 52bytes
000F 0002 # Enable Low Frequency Oscillator
960KHz
0009 00B2 # High frequency oscillator Frequen▶
cy control
000B 0206 # Low frequency oscillator Frequency
control
0046 2004 # better ambient setting
004C 400B # lower current setting
005B 0C20 # better ambient settling
000D 2580 # 100Hz ODR = 960k/9600
0020 0022 # All the inputs connected to Cath▶
ode1 when input pair sleep
0021 0000 # Use as two single ended inputs &
Cathode1 set to VDD during sleep

# Slot A with IR LED
0120 1800 # Two region digital integrate mode
0121 4528 # TIA + BUF + ADC (1x TIA config) &
Enable coarse and fine ambient_cancellation
0122 0001 # inp1 to channel 1
0123 5002 # Precondition with AFE_Vref & VC1 =
V_Delta
0124 FAD2 # Enable tia saturation detection,
AFE_Vref = 0.885V tia_gain_ch1&ch2=100k, chan▶
nel1 & channel2 Buffer gain = 2 (Rfb/Rin =
100K/50K)
0125 3000 # Channel1 & channel2 integrator ca▶
pacitor = 12.6pF
0128 8400 # LED current setting
4*1.57mA(=6.3mA) on output 2B
012A 0D02 # num_int=13, num_repeat=2
012B 008A # min_period=138
012C 245B # led_width=36, led_offset=91
0135 0004 # Dark size=0 & Signal size=4
0138 0065 # lit_offset=101
0139 53B0 # dark2_offset=167, dark1_offset=48

# Slot B with Green LED
0140 1800 # Two region digital integrate mode
0141 4528 # TIA + BUF + ADC (1x TIA config) &
Enable coarse and fine ambient_cancellation
0142 0030 # inp4 to channel 1
0143 5002 # Precondition with AFE_Vref & VC1 =
V_Delta
0144 FAD2 # Enable tia saturation detection,
AFE_Vref = 0.885V tia_gain_ch1&ch2=100k, chan▶
nel1 & channel2 Buffer gain = 2 (Rfb/Rin =
100K/50K)
0145 3000 # Channel1 & channel2 integrator ca▶
pacitor = 12.6pF
0148 000B # LED current setting
11*1.57mA(=17mA) on output 1A
014A 0A03 # num_int=10, num_repeat=3
014B 003A # min_period=58
014C 183C # led_width=24, led_offset=60
0155 0004 # Dark size=0 & Signal size=4
0158 0040 # lit_offset=64
0159 2D30 # dark2_offset=90, dark1_offset=48

#ECG setting
001E 0200 # Enable ECG sat status byte
0074 0028 # ECG ACLO LPF coefficient
0077 0100 # ECG PGA power optimization
0100 043F # ECG input connection, resolution
286nV/LSB, RLD output is Regulated common-mode
input; enable RLD DCLO,RLD DCLO threshold
AVDD3V-0.4V/0.4V, enable RLD loop
0101 9FAF # ACLO: enable, excite current 10nA,
threshold max; DCLO: enable, excite current
6nA, threshold AVDD3V-0.4V,ECGIN source, ECGIP
source
0102 0029 # ratio of ECG to PPG ODR is 5,
ECG/PPG = 500Hz/100Hz

# BIOZ Time slot A configure #
02A0 0003 #tia/dacref enable
02A7 320D #exbuf enable
02AA 2E30 #amp/pag enable
02A2 0001 #sinewave frequency is 50kHz
02A1 99A2 #sinewave frequency is 50kHz
02AB 2803 #switch connection to measure exter▶
nal Rcal voltage
02AD 0004 #bypass the SINC filter
02AE 0008 #DFT number is 1024

# BIOZ Time slot B configure #
02C0 0003 #tia/dacref enable
02C7 320D #exbuf enable
02CA 2E30 #amp/pag enable
02C2 0001 #sinewave frequency is 50kHz
02C1 99A2 #sinewave frequency is 50kHz
02CB 0003 #switch connection to measure exter▶
nal Rcal current
02CD 0004 #bypass the SINC filter
02CE 0008 #DFT number is 1024

# BIOZ Time slot C configure #
02E0 0003 #tia/dacref enable
02E7 320D #exbuf enable
02EA 2E30 #amp/pag enable
02E2 0001 #sinewave frequency is 50kHz
```

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```
02E1 99A2 #sinewave frequency is 50kHz
02EB 5610 #switch connection to measure exter▶
nal Rdut voltage
02ED 0004 #bypass the SINC filter
02EE 0008 #DFT number is 1024

# BIOZ Time slot D configure #
0300 0003 #tia/dacref enable
0307 320D #exbuf enable
030A 2E30 #amp/pag enable
0302 0001 #sinewave frequency is 50kHz
0301 99A2 #sinewave frequency is 50kHz
030B 4210 #switch connection to measure exter▶
nal Rdut current
030D 0004 #bypass the SINC filter
030E 0008 #DFT number is 1024
0010 C201 # enable BIOZ timeslot ABCD, PPG
timeslot AB and ECG, go

## Interrupt mapping of fifo_th
0014 8000 # FIFO_th to INX
0022 0003 # GPIO0 output invert
0023 0002 # gpio0 int x
0010 C201 # operation mode set to GO
```

Power-Up Sequencing

Note that the power supplies need to be on and off simultaneously.

FIFO Data Structure

Table 19 shows the data structure in the FIFO for the recommended multimodal measurement configuration. There are 52 bytes for every data pattern.

Table 19. Data Structure in FIFO

Byte Order in FIFO	Description
Byte 0 to Byte 19	ECG data: 20 bytes
Byte 20 to Byte 23	PPG_A data: 4 bytes
Byte 24 to Byte 27	PPG_B data: 4 bytes
Byte 28 to Byte 33	BIOZ_A data: 6 bytes
Byte 34 to Byte 39	BIOZ_B data: 6 bytes
Byte 40 to Byte 45	BIOZ_C data: 6 bytes
Byte 46 to Byte 51	BIOZ_D data: 6 bytes

DESIGN GUIDE

The ADPD6000 is a multimodal, vital sign monitoring AFE. The performance of the device can be adversely impacted by the PCB layout, especially for the analog input interfaces.

Power Rails

For the power supply, decouple the AVDD, AVDD3, DVDD, and IOVDD pins with a 0.1 µF or larger ceramic chip capacitor to the PCB ground plane placed near the power pins. It is recommended that all decoupling capacitors use individual vias to the PCB ground plane to avoid mutual impedance coupling between decoupled supplies when sharing vias.

Optical Channel

For the PPG channel, decouple the VREF1 pin and VREF2 pin to the PCB ground plane with a 1.0 µF ceramic capacitor. The voltage on the VREF1 pin and VREF2 pin is nominally 1.2 V. Therefore, a 6.3 V rated ceramic capacitor is adequate for this purpose. The most critical aspect of the PCB layout of the ADPD6000 is the handling of the IN1, IN2, IN3, and IN4 nodes. Because photodiode input is sensitive to noise, and any parasitic capacitive coupling to the pin can result in additional noise, it is recommended that the photodiode input trace in the layout be as short as possible and fully guarded by the ground plane.

For example, as a 6-layer stack design, the chip is placed in the top layer with optical components in the bottom layer. Therefore, it is recommended that the IN1, IN2, IN3, and IN4 trace length in the top is short to avoid parasitic effects. In the bottom layer, the IN1, IN2, IN3, and IN4 traces and the photodiode anode are fully guarded with the ground shape and trace. VC1, VC2, and the photodiode cathode are also guarded with the ground plane. Layer 5 is filled with a ground plane for reference. Keep the analog input signals away from other digital or noisy signals.

ECG Channel

For the ECG channel, both traces of ECGIP and ECGIN must match to achieve high CMRR performance. Use a differential pair layout for ECGIP and ECGIN and shorten the length of the traces.

BIA Channel

For the BIA channel, minimize the length of the PCB trace for RCALP and RCALN because the RCALP and RCALN value is critical for the BIOZ measurement accuracy. The resistance of the PCB trace is designed to guarantee that the accuracy of the RCALP and RCALN resistance is 0.1%, even including the PCB wire resistance.

REGISTER SUMMARY

Table 20. Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x0000	FIFO_STATUS	[15:8]	CLEAR_FIFO	INT_FIFO_UFLOW	INT_FIFO_OFLOW	INT_FIFO_TH	FIFO_INIT_DONE_STATUS	FIFO_BYTE_COUNT[10:8]			0x0000	R/W
		[7:0]	FIFO_BYTE_COUNT [7:0]									
0x0004	ECG_STATUS	[15:8]	RESERVED								0x00FC	R/W
		[7:0]	ECG_ACLO_STATUS	ECGIN_DCLO_HI_STATUS	ECGIP_DCLO_HI_STATUS	ECG_RLD_DCLO_HI_STATUS	ECG_RLD_DCLO_LO_STATUS	ECG_DCLO_STATUS	ECG_PGA_SAT_STATUS	ECG_ADC_SAT_STATUS		
0x0005	GLOBAL_STATUS	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED							INVALID_CFG_STATUS		
0x0006	FIFO_TH	[15:8]	RESERVED						FIFO_TH[9:8]		0x0000	R/W
		[7:0]	FIFO_TH[7:0]									
0x007	INT_ACLEAR	[15:8]	INT_ACLEAR_FIFO	RESERVED							0x8000	R/W
		[7:0]	RESERVED									
0x0008	CHIP_ID	[15:8]	VERSION								0x00C4	R
		[7:0]	CHIP_ID									
0x0009	OSC32M	[15:8]	RESERVED								0x0080	R/W
		[7:0]	OSC_32M_FREQ_ADJ									
0x000A	OSC32M_CAL	[15:8]	OSC_32M_CAL_START	OSC_32M_CAL_COUNT[14:8]							0x0000	R/W
		[7:0]	OSC_32M_CAL_COUNT[7:0]									
0x000B	OSC960K	[15:8]	CAPTURE_TIMESTAMP	RESERVED				OSC_CAL_ENABLE	OSC_960K_FREQ_ADJ[9:8]		0x02B2	R/W
		[7:0]	OSC_960K_FREQ_ADJ[7:0]									
0x000D	TS_FREQ	[15:8]	TIMESLOT_PERIOD_L[15:8]								0x2580	R/W
		[7:0]	TIMESLOT_PERIOD_L[7:0]									
0x000E	TS_FREQH	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED	TIMESLOT_PERIOD_H								
0x000F	SYS_CTL	[15:8]	SW_RESET	RESERVED				ALT_CLOCKS			0x0000	R/W
		[7:0]	ALT_CLK_GPIO		RESERVED	RESERVED	RESERVED	TM_CLK_GPIO_SEL	OSC_960K_EN	RESERVED		
0x0010	OPMODE	[15:8]	ECG_TIMESLOT_EN	BIOZ_TIMESLOT_EN			PPG_TIMESLOT_EN				0x0000	R/W
		[7:0]	RESERVED					OP_MODE				
0x0011	STAMP_L	[15:8]	TIMESTAMP_COUNT_L[15:8]								0x0000	R
		[7:0]	TIMESTAMP_COUNT_L[7:0]									
0x0012	STAMP_H	[15:8]	TIMESTAMP_COUNT_H[15:8]								0x0000	R
		[7:0]	TIMESTAMP_COUNT_H[7:0]									
0x0013	STAMPDELTA	[15:8]	TIMESTAMP_SLOT_DELTA[15:8]								0x0000	R
		[7:0]	TIMESTAMP_SLOT_DELTA[7:0]									

REGISTER SUMMARY

Table 20. Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x0014	INT_ENABLE_XD	[15:8]	INTX_EN_FIFO_TH	INTX_EN_FIFO_UFLOW	INTX_EN_FIFO_OFLOW	RESERVED					0x0000	R/W
		[7:0]	RESERVED									
0x0015	INT_ENABLE_YD	[15:8]	INTY_EN_FIFO_TH	INTY_EN_FIFO_UFLOW	INTY_EN_FIFO_OFLOW	RESERVED					0x0000	R/W
		[7:0]	RESERVED									
0x001E	FIFO_STATUS_BYTES	[15:8]	RESERVED						ENA_STAT_ECG	ENA_STAT_TSX	0x0200	R/W
		[7:0]	ENA_STAT_TS2	ENA_STAT_TS1	RESERVED							
0x0020	INPUT_SLEEP	[15:8]	RESERVED								0x0000	R/W
		[7:0]	INP_SLEEP_34				INP_SLEEP_12					
0x0021	INPUT_CFG	[15:8]	RESERVED								0x0000	R/W
		[7:0]	VC2_SLEEP		VC1_SLEEP		RESERVED		PAIR34	PAIR12		
0x0022	GPIO_CFG	[15:8]	GPIO_SLEW		GPIO_DRV		RESERVED			GPIO_PIN_CFG2[2]	0x0000	R/W
		[7:0]	GPIO_PIN_CFG2[1:0]		GPIO_PIN_CFG1			GPIO_PIN_CFG0				
0x0023	GPIO01	[15:8]	GPIOOUT1								0x0000	R/W
		[7:0]	GPIOOUT0									
0x0024	GPIO23	[15:8]	RESERVED								0x0000	R/W
		[7:0]	GPIOOUT2									
0x0025	GPIO_IN	[15:8]	RESERVED								0x0000	R
		[7:0]	RESERVED				GPIO_INPUT					
0x0026	GPIO_EXT	[15:8]	RESERVED							GOUT_SLEEP	0x0000	R/W
		[7:0]	TIMESTAMP_INV	TIMESTAMP_ALWAYS_EN	TIMESTAMP_GPIO		RESERVED	EXT_SYNC_EN	EXT_SYNC_GPIO			
0x002F	FIFO_DATA	[15:8]	FIFO_DATA[15:8]								0x0000	R
		[7:0]	FIFO_DATA[7:0]									
0x0046	ADC_CONTROL	[15:8]	RESERVED		ECG_ADC_CTRL	RESERVED					0x2007	R/W
		[7:0]	RESERVED					PPG_ADC_CTRL1	PPG_ADC_CTRL2			
0x004C	GLOBAL_BIAS_CONTROL	[15:8]	RESERVED	TIA_DETECT_CTRL	RESERVED						0x4000	R/W
		[7:0]	RESERVED				GLOBAL_BIAS_TRIM					
0x0057	IO_ADJUST	[15:8]	RESERVED								0x0050	R/W
		[7:0]	RESERVED	LOW_IOVDD_EN	RESERVED		SPI_SLEW		SPI_DRV			
0x005B	PPG_TIA_CONTROL	[15:8]	RESERVED				TIA_CEIL_DETECT_CTRL		RESERVED		0x0020	R/W
		[7:0]	RESERVED	TIA_MODE								
0x0074	ECG_ACLO_CONTROL	[15:8]	RESERVED					ECG_ACLO_LPF_COEF[10:8]			0x0050	R/W
		[7:0]	ECG_ACLO_LPF_COEF[7:0]									

REGISTER SUMMARY

Table 20. Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x0077	ECG_PGA_CONTROL	[15:8]	RESERVED							ECG_PGA_CTRL	0x0000	R/W
		[7:0]	RESERVED									
0x0078	ECG_INPUT_CONTROL	[15:8]	ECG_INPUT_BUF_EN	RESERVED			ECG_INPUT_BUF_CTRL	RESERVED			0x0000	R/W
		[7:0]	RESERVED									
0x0100	ECG_ANA_CTRL	[15:8]	RESERVED					ECG_INP_CONNECT	ECG_SHORT	ECG_CHAN_RESOLUTION	0x0430	R/W
		[7:0]	RESERVED	ECG_RLD_OUT_DISCONNECT	ECG_RLD_OUT_SEL		ECG_RLD_SAT_EN	ECG_RLD_SAT_THRESHOLD		ECG_RLD_EN		
0x0101	ECG_LEADOFF_CTRL	[15:8]	ECG_ACLO_EN	ECG_ACLO_MAG			ECG_ACLO_THRESHOLD			ECG_DCLO_EN	0x0004	R/W
		[7:0]	ECG_DCLO_MAG				ECG_DCLO_POLARITY_IN	ECG_DCLO_POLARITY_IP	ECG_DCLO_THRESHOLD			
0x0102	ECG_DIG_CTRL1	[15:8]	RESERVED							ECG_OVERSAMPLING_RATIO[5]	0x0018	R/W
		[7:0]	ECG_OVERSAMPLING_RATIO[4:0]					ECG_ODR_SEL				
0x0103	ECG_DIG_CTRL2	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED		ECG_ACLO_INV	ECG_BYPASS_EQLZR	ECG_CAL_GAIN					
0x0120	TS_CTRL_A	[15:8]	SUBSAMPLE_A	CH2_EN_A	SAMPLE_TYPE_A			RESERVED	TIMESLOT_OFFSET_A[9:8]		0x0000	R/W
		[7:0]	TIMESLOT_OFFSET_A[7:0]									
0x0121	TS_PATH_A	[15:8]	PRE_WIDTH_A				AMBIENT_CANCELLATION_A		TS_GPIO_A	AFE_INT_C_BUF_A	0x4020	R/W
		[7:0]	RESERVED	AFE_PATH_CFG_A								
0x0122	INPUTS_A	[15:8]	RESERVED								0x0000	R/W
		[7:0]	INP34_A				INP12_A					
0x0123	CATHODE_A	[15:8]	RESERVED	PRECON_A			VC2_PULSE_A		VC2_ALT_A		0x0000	R/W
		[7:0]	VC2_SEL_A		VC1_PULSE_A		VC1_ALT_A		VC1_SEL_A			
0x0124	AFE_TRIM1_A	[15:8]	TIA_CEIL_DETECT_EN_A	CH2_TRIM_INT_A		CH1_TRIM_INT_A		VREF_PULSE_A	AFE_TRIM_VREF_A		0x02C9	R/W
		[7:0]	VREF_PULSE_VAL_A		TIA_GAIN_CH2_A			TIA_GAIN_CH1_A				
0x0125	AFE_TRIM2_A	[15:8]	RESERVED		CH2_TRIM_INT_CAP_A	CH1_TRIM_INT_CAP_A	RESERVED				0x0000	R/W
		[7:0]	RESERVED									
0x0126	AFE_DAC1_A	[15:8]	DAC_AMBIENT_CH1_A[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH1_A[0]	DAC_LED_DC_CH1_A								
0x0127	AFE_DAC2_A	[15:8]	DAC_AMBIENT_CH2_A[8:1]								0x0000	R/W

REGISTER SUMMARY

Table 20. Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
		[7:0]	DAC_AMBIENT_CH2_A[0]	DAC_LED_DC_CH2_A								
0x0128	LED_POW12_A	[15:8]	LED_DRIVESIDE2_A	LED_CURRENT2_A							0x0000	R/W
		[7:0]	LED_DRIVESIDE1_A	LED_CURRENT1_A								
0x0129	LED_MODE_A	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED						LED_MODE2_A	LED_MODE1_A		
0x012A	COUNTS_A	[15:8]	NUM_INT_A								0x0101	R/W
		[7:0]	NUM_REPEAT_A									
0x012B	PERIOD_A	[15:8]	RESERVED	RESERVED	MOD_TYPE_A		RESERVED		MIN_PERIOD_A[9:8]		0x0000	R/W
		[7:0]	MIN_PERIOD_A[7:0]									
0x012C	LED_PULSE1_A	[15:8]	LED_WIDTH_A								0x0210	R/W
		[7:0]	LED_OFFSET_A									
0x012D	LED_PULSE2_A	[15:8]	RESERVED								0x0013	R/W
		[7:0]	LED_SECOND_OFFSET_A									
0x012E	INTEG_WIDTH_A	[15:8]	SINGLE_INTEG_A	RESERVED		CH2_AMP_DISABLE_A		RESERVED		CH1_AMP_DISABLE_A[1]	0x0003	R/W
		[7:0]	CH1_AMP_DISABLE_A[0]	ADC_COUNT_A		INTEG_WIDTH_A						
0x012F	INTEG_OFFSET_A	[15:8]	RESERVED			INTEG_OFFSET_A[7:3]					0x01A0	R/W
		[7:0]	INTEG_OFFSET_A[2:0]			INTEG_FINE_OFFSET_A						
0x0130	MOD_PULSE_A	[15:8]	MOD_WIDTH_A								0x0001	R/W
		[7:0]	MOD_OFFSET_A									
0x0131	PATTERN1_A	[15:8]	LED_DISABLE_A				MOD_DISABLE_A				0x0000	R/W
		[7:0]	SUBTRACT_A				REVERSE_INTEG_A					
0x0133	ADC_OFF1_A	[15:8]	RESERVED		CH1_ADC_ADJUST_A[13:8]						0x0000	R/W
		[7:0]	CH1_ADC_ADJUST_A[7:0]									
0x0134	ADC_OFF2_A	[15:8]	RESERVED		CH2_ADC_ADJUST_A[13:8]						0x0000	R/W
		[7:0]	CH2_ADC_ADJUST_A[7:0]									
0x0135	DATA1_A	[15:8]	DARK_SHIFT_A					DARK_SIZE_A			0x0003	R/W
		[7:0]	SIGNAL_SHIFT_A					SIGNAL_SIZE_A				
0x0136	DATA2_A	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LIT_SHIFT_A					LIT_SIZE_A				
0x0137	DECIMATE_A	[15:8]	RESERVED					DECIMATE_FACTOR_A[6:4]			0x0000	R/W
		[7:0]	DECIMATE_FACTOR_A[3:0]				RESERVED					
0x0138	DIGINT_LIT_A	[15:8]	RESERVED							LIT_OFFSET_A[8]	0x0026	R/W
		[7:0]	LIT_OFFSET_A[7:0]									
0x0139	DIGINT_DARK_A	[15:8]	DARK2_OFFSET_A[8:1]								0x0086	R/W

REGISTER SUMMARY

Table 20. Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
		[7:0]	DARK2_OFFSET_A[0]	DARK1_OFFSET_A								
0x0140	TS_CTRL_B	[15:8]	SUBSAMPLE_B	CH2_EN_B	SAMPLE_TYPE_B			RESERVED	TIMESLOT_OFFSET_B[9:8]		0x0000	R/W
		[7:0]	TIMESLOT_OFFSET_B[7:0]									
0x0141	TS_PATH_B	[15:8]	PRE_WIDTH_B				AMBIENT_CANCELLATION_B		TS_GPIO_B	AFE_INT_C_BUF_B	0x4020	R/W
		[7:0]	RESERVED	AFE_PATH_CFG_B								
0x0142	INPUTS_B	[15:8]	RESERVED								0x0000	R/W
		[7:0]	INP34_B				INP12_B					
0x0143	CATHODE_B	[15:8]	RESERVED	PRECON_B			VC2_PULSE_B		VC2_ALT_B		0x0000	R/W
		[7:0]	VC2_SEL_B		VC1_PULSE_B		VC1_ALT_B		VC1_SEL_B			
0x0144	AFE_TRIM1_B	[15:8]	TIA_CEIL_DETECT_EN_B	CH2_TRIM_INT_B		CH1_TRIM_INT_B		VREF_PULSE_B	AFE_TRIM_VREF_B		0x02C9	R/W
		[7:0]	VREF_PULSE_VAL_B		TIA_GAIN_CH2_B			TIA_GAIN_CH1_B				
0x0145	AFE_TRIM2_B	[15:8]	RESERVED		CH2_TRIM_INT_CAP_B	CH1_TRIM_INT_CAP_B	RESERVED				0x0000	R/W
		[7:0]	RESERVED									
0x0146	AFE_DAC1_B	[15:8]	DAC_AMBIENT_CH1_B[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH1_B[0]	DAC_LED_DC_CH1_B								
0x0147	AFE_DAC2_B	[15:8]	DAC_AMBIENT_CH2_B[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH2_B[0]	DAC_LED_DC_CH2_B								
0x0148	LED_POW12_B	[15:8]	LED_DRIVESIDE2_B	LED_CURRENT2_B							0x0000	R/W
		[7:0]	LED_DRIVESIDE1_B	LED_CURRENT1_B								
0x0149	LED_MODE_B	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED						LED_MODE2_B	LED_MODE1_B		
0x014A	COUNTS_B	[15:8]	NUM_INT_B								0x0101	R/W
		[7:0]	NUM_REPEAT_B									
0x014B	PERIOD_B	[15:8]	RESERVED	RESERVED	MOD_TYPE_B		RESERVED		MIN_PERIOD_B[9:8]		0x0000	R/W
		[7:0]	MIN_PERIOD_B[7:0]									
0x014C	LED_PULSE1_B	[15:8]	LED_WIDTH_B								0x0210	R/W
		[7:0]	LED_OFFSET_B									
0x014D	LED_PULSE2_B	[15:8]	RESERVED								0x0013	R/W
		[7:0]	LED_SECOND_OFFSET_B									
0x014E	INTEG_WIDTH_B	[15:8]	SINGLE_INTEG_B	RESERVED		CH2_AMP_DISABLE_B		RESERVED		CH1_AMP_DISABLE_B[1]	0x0003	R/W

REGISTER SUMMARY

Table 20. Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
		[7:0]	CH1_AMP_DISABLE_B[0]	ADC_COUNT_B		INTEG_WIDTH_B						
0x014F	INTEG_OFFSET_B	[15:8]	RESERVED			INTEG_OFFSET_B[7:3]					0x01A0	R/W
		[7:0]	INTEG_OFFSET_B[2:0]			INTEG_FINE_OFFSET_B						
0x0150	MOD_PULSE_B	[15:8]	MOD_WIDTH_B								0x0001	R/W
		[7:0]	MOD_OFFSET_B									
0x0151	PATTERN1_B	[15:8]	LED_DISABLE_B				MOD_DISABLE_B				0x0000	R/W
		[7:0]	SUBTRACT_B				REVERSE_INTEG_B					
0x0153	ADC_OFF1_B	[15:8]	RESERVED		CH1_ADC_ADJUST_B[13:8]						0x0000	R/W
		[7:0]	CH1_ADC_ADJUST_B[7:0]									
0x0154	ADC_OFF2_B	[15:8]	RESERVED		CH2_ADC_ADJUST_B[13:8]						0x0000	R/W
		[7:0]	CH2_ADC_ADJUST_B[7:0]									
0x0155	DATA1_B	[15:8]	DARK_SHIFT_B					DARK_SIZE_B			0x0003	R/W
		[7:0]	SIGNAL_SHIFT_B					SIGNAL_SIZE_B				
0x0156	DATA2_B	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LIT_SHIFT_B					LIT_SIZE_B				
0x0157	DECIMATE_B	[15:8]	RESERVED					DECIMATE_FACTOR_B[6:4]			0x0000	R/W
		[7:0]	DECIMATE_FACTOR_B[3:0]				RESERVED					
0x0158	DIGINT_LIT_B	[15:8]	RESERVED							LIT_OFFSET_B[8]	0x0026	R/W
		[7:0]	LIT_OFFSET_B[7:0]									
0x0159	DIGINT_DARK_B	[15:8]	DARK2_OFFSET_B[8:1]								0x0086	R/W
		[7:0]	DARK2_OFFSET_B[0]	DARK1_OFFSET_B								
0x0160	TS_CTRL_C	[15:8]	SUBSAMPLE_C	CH2_EN_C	SAMPLE_TYPE_C			RESERVED	TIMESLOT_OFFSET_C[9:8]		0x0000	R/W
		[7:0]	TIMESLOT_OFFSET_C[7:0]									
0x0161	TS_PATH_C	[15:8]	PRE_WIDTH_C				AMBIENT_CANCELLATION_C		TS_GPIO_C	AFE_INT_C_BUF_C	0x4020	R/W
		[7:0]	RESERVED	AFE_PATH_CFG_C								
0x0162	INPUTS_C	[15:8]	RESERVED								0x0000	R/W
		[7:0]	INP34_C				INP12_C					
0x0163	CATHODE_C	[15:8]	RESERVED	PRECON_C			VC2_PULSE_C		VC2_ALT_C		0x0000	R/W
		[7:0]	VC2_SEL_C		VC1_PULSE_C		VC1_ALT_C		VC1_SEL_C			
0x0164	AFE_TRIM1_C	[15:8]	TIA_CEIL_DETECT_EN_C	CH2_TRIM_INT_C		CH1_TRIM_INT_C		VREF_PULSE_C	AFE_TRIM_VREF_C		0x02C9	R/W
		[7:0]	VREF_PULSE_VAL_C		TIA_GAIN_CH2_C			TIA_GAIN_CH1_C				
0x0165	AFE_TRIM2_C	[15:8]	RESERVED		CH2_TRIM_INT_CAP_C	CH1_TRIM_INT_CAP_C	RESERVED				0x0000	R/W
		[7:0]	RESERVED									
0x0166	AFE_DAC1_C	[15:8]	DAC_AMBIENT_CH1_C[8:1]								0x0000	R/W

REGISTER SUMMARY

Table 20. Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
		[7:0]	DAC_AMBIENT_CH1_C[0]	DAC_LED_DC_CH1_C								
0x0167	AFE_DAC2_C	[15:8]	DAC_AMBIENT_CH2_C[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH2_C[0]	DAC_LED_DC_CH2_C								
0x0168	LED_POW12_C	[15:8]	LED_DRIVESIDE2_C	LED_CURRENT2_C							0x0000	R/W
		[7:0]	LED_DRIVESIDE1_C	LED_CURRENT1_C								
0x0169	LED_MODE_C	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED						LED_MODE2_C	LED_MODE1_C		
0x016A	COUNTS_C	[15:8]	NUM_INT_C								0x0101	R/W
		[7:0]	NUM_REPEAT_C									
0x016B	PERIOD_C	[15:8]	RESERVED	RESERVED	MOD_TYPE_C		RESERVED		MIN_PERIOD_C[9:8]		0x0000	R/W
		[7:0]	MIN_PERIOD_C[7:0]									
0x016C	LED_PULSE1_C	[15:8]	LED_WIDTH_C								0x0210	R/W
		[7:0]	LED_OFFSET_C									
0x016D	LED_PULSE2_C	[15:8]	RESERVED								0x0013	R/W
		[7:0]	LED_SECOND_OFFSET_C									
0x016E	INTEG_WIDTH_C	[15:8]	SINGLE_INTEG_C	RESERVED		CH2_AMP_DISABLE_C		RESERVED		CH1_AMP_DISABLE_C[1]	0x0003	R/W
		[7:0]	CH1_AMP_DISABLE_C[0]	ADC_COUNT_C		INTEG_WIDTH_C						
0x016F	INTEG_OFFSET_C	[15:8]	RESERVED			INTEG_OFFSET_C[7:3]					0x01A0	R/W
		[7:0]	INTEG_OFFSET_C[2:0]			INTEG_FINE_OFFSET_C						
0x0170	MOD_PULSE_C	[15:8]	MOD_WIDTH_C								0x0001	R/W
		[7:0]	MOD_OFFSET_C									
0x0171	PATTERN1_C	[15:8]	LED_DISABLE_C				MOD_DISABLE_C				0x0000	R/W
		[7:0]	SUBTRACT_C				REVERSE_INTEG_C					
0x0173	ADC_OFF1_C	[15:8]	RESERVED		CH1_ADC_ADJUST_C[13:8]						0x0000	R/W
		[7:0]	CH1_ADC_ADJUST_C[7:0]									
0x0174	ADC_OFF2_C	[15:8]	RESERVED		CH2_ADC_ADJUST_C[13:8]						0x0000	R/W
		[7:0]	CH2_ADC_ADJUST_C[7:0]									
0x0175	DATA1_C	[15:8]	DARK_SHIFT_C					DARK_SIZE_C			0x0003	R/W
		[7:0]	SIGNAL_SHIFT_C					SIGNAL_SIZE_C				
0x0176	DATA2_C	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LIT_SHIFT_C					LIT_SIZE_C				
0x0177	DECIMATE_C	[15:8]	RESERVED					DECIMATE_FACTOR_C[6:4]			0x0000	R/W
		[7:0]	DECIMATE_FACTOR_C[3:0]				RESERVED					

REGISTER SUMMARY

Table 20. Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x0178	DIGINT_LIT_C	[15:8]	RESERVED							LIT_OFFSET_C[8]	0x0026	R/W
		[7:0]	LIT_OFFSET_C[7:0]									
0x0179	DIGINT_DARK_C	[15:8]	DARK2_OFFSET_C[8:1]								0x0086	R/W
		[7:0]	DARK2_OFFSET_C[0]	DARK1_OFFSET_C								
0x0180	TS_CTRL_D	[15:8]	SUBSAMPLE_D	CH2_EN_D	SAMPLE_TYPE_D			RESERVED	TIMESLOT_OFFSET_D[9:8]		0x0000	R/W
		[7:0]	TIMESLOT_OFFSET_D[7:0]									
0x0181	TS_PATH_D	[15:8]	PRE_WIDTH_D				AMBIENT_CANCELLATION_D		TS_GPIO_D	AFE_INT_C_BUF_D	0x4020	R/W
		[7:0]	RESERVED	AFE_PATH_CFG_D								
0x0182	INPUTS_D	[15:8]	RESERVED								0x0000	R/W
		[7:0]	INP34_D				INP12_D					
0x0183	CATHODE_D	[15:8]	RESERVED	PRECON_D			VC2_PULSE_D		VC2_ALT_D		0x0000	R/W
		[7:0]	VC2_SEL_D		VC1_PULSE_D		VC1_ALT_D		VC1_SEL_D			
0x0184	AFE_TRIM1_D	[15:8]	TIA_CEIL_DETECT_EN_D	CH2_TRIM_INT_D		CH1_TRIM_INT_D		VREF_PULSE_D	AFE_TRIM_VREF_D		0x02C9	R/W
		[7:0]	VREF_PULSE_VAL_D		TIA_GAIN_CH2_D			TIA_GAIN_CH1_D				
0x0185	AFE_TRIM2_D	[15:8]	RESERVED		CH2_TRIM_INT_CAP_D	CH1_TRIM_INT_CAP_D	RESERVED				0x0000	R/W
		[7:0]	RESERVED									
0x0186	AFE_DAC1_D	[15:8]	DAC_AMBIENT_CH1_D[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH1_D[0]	DAC_LED_DC_CH1_D								
0x0187	AFE_DAC2_D	[15:8]	DAC_AMBIENT_CH2_D[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH2_D[0]	DAC_LED_DC_CH2_D								
0x0188	LED_POW12_D	[15:8]	LED_DRIVESIDE2_D	LED_CURRENT2_D							0x0000	R/W
		[7:0]	LED_DRIVESIDE1_D	LED_CURRENT1_D								
0x0189	LED_MODE_D	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED						LED_MODE2_D	LED_MODE1_D		
0x018A	COUNTS_D	[15:8]	NUM_INT_D								0x0101	R/W
		[7:0]	NUM_REPEAT_D									
0x018B	PERIOD_D	[15:8]	RESERVED	RESERVED	MOD_TYPE_D		RESERVED		MIN_PERIOD_D[9:8]		0x0000	R/W
		[7:0]	MIN_PERIOD_D[7:0]									
0x018C	LED_PULSE1_D	[15:8]	LED_WIDTH_D								0x0210	R/W
		[7:0]	LED_OFFSET_D									

REGISTER SUMMARY

Table 20. Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x018D	LED_PULSE2_D	[15:8]	RESERVED								0x0013	R/W
		[7:0]	LED_SECOND_OFFSET_D									
0x018E	INTEG_WIDTH_D	[15:8]	SINGLE_INTEG_D	RESERVED		CH2_AMP_DISABLE_D		RESERVED		CH1_AMP_DISABLE_D[1]	0x0003	R/W
		[7:0]	CH1_AMP_DISABLE_D[0]	ADC_COUNT_D		INTEG_WIDTH_D						
0x018F	INTEG_OFFSET_D	[15:8]	RESERVED			INTEG_OFFSET_D[7:3]					0x01A0	R/W
		[7:0]	INTEG_OFFSET_D[2:0]			INTEG_FINE_OFFSET_D						
0x0190	MOD_PULSE_D	[15:8]	MOD_WIDTH_D								0x0001	R/W
		[7:0]	MOD_OFFSET_D									
0x0191	PATTERN1_D	[15:8]	LED_DISABLE_D				MOD_DISABLE_D				0x0000	R/W
		[7:0]	SUBTRACT_D				REVERSE_INTEG_D					
0x0193	ADC_OFF1_D	[15:8]	RESERVED		CH1_ADC_ADJUST_D[13:8]						0x0000	R/W
		[7:0]	CH1_ADC_ADJUST_D[7:0]									
0x0194	ADC_OFF2_D	[15:8]	RESERVED		CH2_ADC_ADJUST_D[13:8]						0x0000	R/W
		[7:0]	CH2_ADC_ADJUST_D[7:0]									
0x0195	DATA1_D	[15:8]	DARK_SHIFT_D					DARK_SIZE_D			0x0003	R/W
		[7:0]	SIGNAL_SHIFT_D					SIGNAL_SIZE_D				
0x0196	DATA2_D	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LIT_SHIFT_D					LIT_SIZE_D				
0x0197	DECIMATE_D	[15:8]	RESERVED					DECIMATE_FACTOR_D[6:4]			0x0000	R/W
		[7:0]	DECIMATE_FACTOR_D[3:0]				RESERVED					
0x0198	DIGINT_LIT_D	[15:8]	RESERVED							LIT_OFFSET_D[8]	0x0026	R/W
		[7:0]	LIT_OFFSET_D[7:0]									
0x0199	DIGINT_DARK_D	[15:8]	DARK2_OFFSET_D[8:1]								0x0086	R/W
		[7:0]	DARK2_OFFSET_D[0]	DARK1_OFFSET_D								
0x01A0	TS_CTRL_E	[15:8]	SUBSAMPLE_E	CH2_EN_E	SAMPLE_TYPE_E			RESERVED	TIMESLOT_OFFSET_E[9:8]		0x0000	R/W
		[7:0]	TIMESLOT_OFFSET_E[7:0]									
0x01A1	TS_PATH_E	[15:8]	PRE_WIDTH_E				AMBIENT_CANCELLATION_E		TS_GPIO_E	AFE_INT_C_BUF_E	0x4020	R/W
		[7:0]	RESERVED	AFE_PATH_CFG_E								
0x01A2	INPUTS_E	[15:8]	RESERVED								0x0000	R/W
		[7:0]	INP34_E				INP12_E					
0x01A3	CATHODE_E	[15:8]	RESERVED	PRECON_E			VC2_PULSE_E		VC2_ALT_E		0x0000	R/W
		[7:0]	VC2_SEL_E		VC1_PULSE_E		VC1_ALT_E		VC1_SEL_E			
0x01A4	AFE_TRIM1_E	[15:8]	TIA_CEIL_DETECT_EN_E	CH2_TRIM_INT_E		CH1_TRIM_INT_E		VREF_PULSE_E	AFE_TRIM_VREF_E		0x02C9	R/W
		[7:0]	VREF_PULSE_VAL_E		TIA_GAIN_CH2_E			TIA_GAIN_CH1_E				

REGISTER SUMMARY

Table 20. Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x01A5	AFE_TRIM2_E	[15:8]	RESERVED		CH2_TRIM_INT_CAP_E	CH1_TRIM_INT_CAP_E	RESERVED				0x0000	R/W
		[7:0]	RESERVED									
0x01A6	AFE_DAC1_E	[15:8]	DAC_AMBIENT_CH1_E[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH1_E[0]	DAC_LED_DC_CH1_E								
0x01A7	AFE_DAC2_E	[15:8]	DAC_AMBIENT_CH2_E[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH2_E[0]	DAC_LED_DC_CH2_E								
0x01A8	LED_POW12_E	[15:8]	LED_DRIVESIDE2_E	LED_CURRENT2_E							0x0000	R/W
		[7:0]	LED_DRIVESIDE1_E	LED_CURRENT1_E								
0x01A9	LED_MODE_E	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED						LED_MODE2_E	LED_MODE1_E		
0x01AA	COUNTS_E	[15:8]	NUM_INT_E								0x0101	R/W
		[7:0]	NUM_REPEAT_E									
0x01AB	PERIOD_E	[15:8]	RESERVED	RESERVED	MOD_TYPE_E		RESERVED		MIN_PERIOD_E[9:8]		0x0000	R/W
		[7:0]	MIN_PERIOD_E[7:0]									
0x01AC	LED_PULSE1_E	[15:8]	LED_WIDTH_E								0x0210	R/W
		[7:0]	LED_OFFSET_E									
0x01AD	LED_PULSE2_E	[15:8]	RESERVED								0x0013	R/W
		[7:0]	LED_SECOND_OFFSET_E									
0x01AE	INTEG_WIDTH_E	[15:8]	SINGLE_INTEG_E	RESERVED		CH2_AMP_DISABLE_E		RESERVED		CH1_AMP_DISABLE_E[1]	0x0003	R/W
		[7:0]	CH1_AMP_DISABLE_E[0]	ADC_COUNT_E		INTEG_WIDTH_E						
0x01AF	INTEG_OFFSET_E	[15:8]	RESERVED			INTEG_OFFSET_E[7:3]					0x01A0	R/W
		[7:0]	INTEG_OFFSET_E[2:0]			INTEG_FINE_OFFSET_E						
0x01B0	MOD_PULSE_E	[15:8]	MOD_WIDTH_E								0x0001	R/W
		[7:0]	MOD_OFFSET_E									
0x01B1	PATTERN1_E	[15:8]	LED_DISABLE_E				MOD_DISABLE_E				0x0000	R/W
		[7:0]	SUBTRACT_E				REVERSE_INTEG_E					
0x01B3	ADC_OFF1_E	[15:8]	RESERVED		CH1_ADC_ADJUST_E[13:8]						0x0000	R/W
		[7:0]	CH1_ADC_ADJUST_E[7:0]									
0x01B4	ADC_OFF2_E	[15:8]	RESERVED		CH2_ADC_ADJUST_E[13:8]						0x0000	R/W
		[7:0]	CH2_ADC_ADJUST_E[7:0]									
0x01B5	DATA1_E	[15:8]	DARK_SHIFT_E					DARK_SIZE_E			0x0003	R/W
		[7:0]	SIGNAL_SHIFT_E					SIGNAL_SIZE_E				

REGISTER SUMMARY

Table 20. Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x01B6	DATA2_E	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LIT_SHIFT_E					LIT_SIZE_E				
0x01B7	DECIMATE_E	[15:8]	RESERVED					DECIMATE_FACTOR_E[6:4]			0x0000	R/W
		[7:0]	DECIMATE_FACTOR_E[3:0]				RESERVED					
0x01B8	DIGINT_LIT_E	[15:8]	RESERVED							LIT_OFFSET_E[8]	0x0026	R/W
		[7:0]	LIT_OFFSET_E[7:0]									
0x01B9	DIGINT_DARK_E	[15:8]	DARK2_OFFSET_E[8:1]								0x0086	R/W
		[7:0]	DARK2_OFFSET_E[0]	DARK1_OFFSET_E								
0x01C0	TS_CTRL_F	[15:8]	SUBSAMPLE_F	CH2_EN_F	SAMPLE_TYPE_F			RESERVED	TIMESLOT_OFFSET_F[9:8]		0x0000	R/W
		[7:0]	TIMESLOT_OFFSET_F[7:0]									
0x01C1	TS_PATH_F	[15:8]	PRE_WIDTH_F				AMBIENT_CANCELLATION_F		TS_GPIO_F	AFE_INT_C_BUF_F	0x4020	R/W
		[7:0]	RESERVED	AFE_PATH_CFG_F								
0x01C2	INPUTS_F	[15:8]	RESERVED								0x0000	R/W
		[7:0]	INP34_F				INP12_F					
0x01C3	CATHODE_F	[15:8]	RESERVED	PRECON_F			VC2_PULSE_F		VC2_ALT_F		0x0000	R/W
		[7:0]	VC2_SEL_F		VC1_PULSE_F		VC1_ALT_F		VC1_SEL_F			
0x01C4	AFE_TRIM1_F	[15:8]	TIA_CEIL_DETECT_EN_F	CH2_TRIM_INT_F		CH1_TRIM_INT_F		VREF_PULSE_F	AFE_TRIM_VREF_F		0x02C9	R/W
		[7:0]	VREF_PULSE_VAL_F		TIA_GAIN_CH2_F			TIA_GAIN_CH1_F				
0x01C5	AFE_TRIM2_F	[15:8]	RESERVED		CH2_TRIM_INT_CAP_F	CH1_TRIM_INT_CAP_F	RESERVED				0x0000	R/W
		[7:0]	RESERVED									
0x01C6	AFE_DAC1_F	[15:8]	DAC_AMBIENT_CH1_F[8:1]								0x0000	R/W
		[7:0]	dac_ambient_ch1_f[0]	DAC_LED_DC_CH1_F								
0x01C7	AFE_DAC2_F	[15:8]	DAC_AMBIENT_CH2_F[8:1]								0x0000	R/W
		[7:0]	dac_ambient_ch2_f[0]	DAC_LED_DC_CH2_F								
0x01C8	LED_POW12_F	[15:8]	led_drivside2_f	LED_CURRENT2_F							0x0000	R/W
		[7:0]	led_drivside1_f	LED_CURRENT1_F								
0x01C9	LED_MODE_F	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED						LED_MODE2_F	LED_MODE1_F		
0x01CA	COUNTS_F	[15:8]	NUM_INT_F								0x0101	R/W
		[7:0]	NUM_REPEAT_F									
0x01CB	PERIOD_F	[15:8]	RESERVED	RESERVED	MOD_TYPE_F		RESERVED		MIN_PERIOD_F[9:8]		0x0000	R/W
		[7:0]	MIN_PERIOD_F[7:0]									

REGISTER SUMMARY

Table 20. Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x01CC	LED_PULSE1_F	[15:8]	LED_WIDTH_F								0x0210	R/W
		[7:0]	LED_OFFSET_F									
0x01CD	LED_PULSE2_F	[15:8]	RESERVED								0x0013	R/W
		[7:0]	LED_SECOND_OFFSET_F									
0x01CE	INTEG_WIDTH_F	[15:8]	SINGLE_INTEG_F	RESERVED		CH2_AMP_DISABLE_F		RESERVED		CH1_AMP_DISABLE_F[1]	0x0003	R/W
		[7:0]	CH1_AMP_DISABLE_F[0]	ADC_COUNT_F		INTEG_WIDTH_F						
0x01CF	INTEG_OFFSET_F	[15:8]	RESERVED			INTEG_OFFSET_F[7:3]					0x01A0	R/W
		[7:0]	INTEG_OFFSET_F[2:0]			INTEG_FINE_OFFSET_F						
0x01D0	MOD_PULSE_F	[15:8]	MOD_WIDTH_F								0x0001	R/W
		[7:0]	MOD_OFFSET_F									
0x01D1	PATTERN1_F	[15:8]	LED_DISABLE_F				MOD_DISABLE_F				0x0000	R/W
		[7:0]	SUBTRACT_F				REVERSE_INTEG_F					
0x01D3	ADC_OFF1_F	[15:8]	RESERVED		CH1_ADC_ADJUST_F[13:8]						0x0000	R/W
		[7:0]	CH1_ADC_ADJUST_F[7:0]									
0x01D4	ADC_OFF2_F	[15:8]	RESERVED		CH2_ADC_ADJUST_F[13:8]						0x0000	R/W
		[7:0]	CH2_ADC_ADJUST_F[7:0]									
0x01D5	DATA1_F	[15:8]	DARK_SHIFT_F					DARK_SIZE_F			0x0003	R/W
		[7:0]	SIGNAL_SHIFT_F					SIGNAL_SIZE_F				
0x01D6	DATA2_F	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LIT_SHIFT_F					LIT_SIZE_F				
0x01D7	DECIMATE_F	[15:8]	RESERVED					DECIMATE_FACTOR_F[6:4]			0x0000	R/W
		[7:0]	DECIMATE_FACTOR_F[3:0]				RESERVED					
0x01D8	DIGINT_LIT_F	[15:8]	RESERVED							LIT_OFFSET_F[8]	0x0026	R/W
		[7:0]	LIT_OFFSET_F[7:0]									
0x01D9	DIGINT_DARK_F	[15:8]	DARK2_OFFSET_F[8:1]								0x0086	R/W
		[7:0]	DARK2_OFFSET_F[0]	DARK1_OFFSET_F								
0x01E0	TS_CTRL_G	[15:8]	SUBSAMPLE_G	CH2_EN_G	SAMPLE_TYPE_G			RESERVED	TIMESLOT_OFFSET_G[9:8]		0x0000	R/W
		[7:0]	TIMESLOT_OFFSET_G[7:0]									
0x01E1	TS_PATH_G	[15:8]	PRE_WIDTH_G				AMBIENT_CANCELLATION_G		TS_GPIO_G	AFE_INT_C_BUF_G	0x4020	R/W
		[7:0]	RESERVED	AFE_PATH_CFG_G								
0x01E2	INPUTS_G	[15:8]	RESERVED								0x0000	R/W
		[7:0]	INP34_G				INP12_G					
0x01E3	CATHODE_G	[15:8]	RESERVED	PRECON_G			VC2_PULSE_G		VC2_ALT_G		0x0000	R/W
		[7:0]	VC2_SEL_G		VC1_PULSE_G		VC1_ALT_G		VC1_SEL_G			

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Table 20. Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x01E4	AFE_TRIM1_G	[15:8]	TIA_CEIL_DETECT_EN_G	CH2_TRIM_INT_G		CH1_TRIM_INT_G		VREF_PULSE_G	AFE_TRIM_VREF_G		0x02C9	R/W
		[7:0]	VREF_PULSE_VAL_G		TIA_GAIN_CH2_G			TIA_GAIN_CH1_G				
0x01E5	AFE_TRIM2_G	[15:8]	RESERVED		CH2_TRIM_INT_CAP_G	CH1_TRIM_INT_CAP_G	RESERVED				0x0000	R/W
		[7:0]	RESERVED									
0x01E6	AFE_DAC1_G	[15:8]	DAC_AMBIENT_CH1_G[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH1_G[0]	DAC_LED_DC_CH1_G								
0x01E7	AFE_DAC2_G	[15:8]	DAC_AMBIENT_CH2_G[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH2_G[0]	DAC_LED_DC_CH2_G								
0x01E8	LED_POW12_G	[15:8]	LED_DRIVESIDE2_G	LED_CURRENT2_G							0x0000	R/W
		[7:0]	LED_DRIVESIDE1_G	LED_CURRENT1_G								
0x01E9	LED_MODE_G	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED						LED_MODE2_G	LED_MODE1_G		
0x01EA	COUNTS_G	[15:8]	NUM_INT_G								0x0101	R/W
		[7:0]	NUM_REPEAT_G									
0x01EB	PERIOD_G	[15:8]	RESERVED	RESERVED	MOD_TYPE_G		RESERVED		MIN_PERIOD_G[9:8]		0x0000	R/W
		[7:0]	MIN_PERIOD_G[7:0]									
0x01EC	LED_PULSE1_G	[15:8]	LED_WIDTH_G								0x0210	R/W
		[7:0]	LED_OFFSET_G									
0x01ED	LED_PULSE2_G	[15:8]	RESERVED								0x0013	R/W
		[7:0]	LED_SECOND_OFFSET_G									
0x01EE	INTEG_WIDTH_G	[15:8]	SINGLE_INTEG_G	RESERVED		CH2_AMP_DISABLE_G		RESERVED		CH1_AMP_DISABLE_G[1]	0x0003	R/W
		[7:0]	CH1_AMP_DISABLE_G[0]	ADC_COUNT_G		INTEG_WIDTH_G						
0x01EF	INTEG_OFFSET_G	[15:8]	RESERVED			INTEG_OFFSET_G[7:3]					0x01A0	R/W
		[7:0]	INTEG_OFFSET_G[2:0]			INTEG_FINE_OFFSET_G						
0x01F0	MOD_PULSE_G	[15:8]	MOD_WIDTH_G								0x0001	R/W
		[7:0]	MOD_OFFSET_G									
0x01F1	PATTERN1_G	[15:8]	LED_DISABLE_G				MOD_DISABLE_G				0x0000	R/W
		[7:0]	SUBTRACT_G				REVERSE_INTEG_G					
0x01F3	ADC_OFF1_G	[15:8]	RESERVED		CH1_ADC_ADJUST_G[13:8]						0x0000	R/W
		[7:0]	CH1_ADC_ADJUST_G[7:0]									
0x01F4	ADC_OFF2_G	[15:8]	RESERVED		CH2_ADC_ADJUST_G[13:8]						0x0000	R/W

REGISTER SUMMARY

Table 20. Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
		[7:0]	CH2_ADC_ADJUST_G[7:0]									
0x01F5	DATA1_G	[15:8]	DARK_SHIFT_G					DARK_SIZE_G			0x0003	R/W
		[7:0]	SIGNAL_SHIFT_G					SIGNAL_SIZE_G				
0x01F6	DATA2_G	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LIT_SHIFT_G					LIT_SIZE_G				
0x01F7	DECIMATE_G	[15:8]	RESERVED					DECIMATE_FACTOR_G[6:4]			0x0000	R/W
		[7:0]	DECIMATE_FACTOR_G[3:0]				RESERVED					
0x01F8	DIGINT_LIT_G	[15:8]	RESERVED							LIT_OFFSET_G[8]	0x0026	R/W
		[7:0]	LIT_OFFSET_G[7:0]									
0x01F9	DIGINT_DARK_G	[15:8]	DARK2_OFFSET_G[8:1]								0x0086	R/W
		[7:0]	DARK2_OFFSET_G[0]	DARK1_OFFSET_G								
0x0200	TS_CTRL_H	[15:8]	SUBSAMPLE_H	CH2_EN_H	SAMPLE_TYPE_H			RESERVED	TIMESLOT_OFFSET_H[9:8]		0x0000	R/W
		[7:0]	TIMESLOT_OFFSET_H[7:0]									
0x0201	TS_PATH_H	[15:8]	PRE_WIDTH_H				AMBIENT_CANCELLATION_H		TS_GPIO_H	AFE_INT_C_BUF_H	0x4020	R/W
		[7:0]	RESERVED	AFE_PATH_CFG_H								
0x0202	INPUTS_H	[15:8]	RESERVED								0x0000	R/W
		[7:0]	INP34_H				INP12_H					
0x0203	CATHODE_H	[15:8]	RESERVED	PRECON_H			VC2_PULSE_H		VC2_ALT_H		0x0000	R/W
		[7:0]	VC2_SEL_H		VC1_PULSE_H		VC1_ALT_H		VC1_SEL_H			
0x0204	AFE_TRIM1_H	[15:8]	TIA_CEIL_DETECT_EN_H	CH2_TRIM_INT_H		CH1_TRIM_INT_H		VREF_PULSE_H	AFE_TRIM_VREF_H		0x02C9	R/W
		[7:0]	VREF_PULSE_VAL_H		TIA_GAIN_CH2_H			TIA_GAIN_CH1_H				
0x0205	AFE_TRIM2_H	[15:8]	RESERVED		CH2_TRIM_INT_CAP_H	CH1_TRIM_INT_CAP_H	RESERVED				0x0000	R/W
		[7:0]	RESERVED									
0x0206	AFE_DAC1_H	[15:8]	DAC_AMBIENT_CH1_H[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH1_H[0]	DAC_LED_DC_CH1_H								
0x0207	AFE_DAC2_H	[15:8]	DAC_AMBIENT_CH2_H[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH2_H[0]	DAC_LED_DC_CH2_H								
0x0208	LED_POW12_H	[15:8]	LED_DRIVESIDE2_H	LED_CURRENT2_H							0x0000	R/W
		[7:0]	LED_DRIVESIDE1_H	LED_CURRENT1_H								
0x0209	LED_MODE_H	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED						LED_MODE2_H	LED_MODE1_H		
0x020A	COUNTS_H	[15:8]	NUM_INT_H								0x0101	R/W

REGISTER SUMMARY

Table 20. Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
		[7:0]	NUM_REPEAT_H									
0x020B	PERIOD_H	[15:8]	RESERVED	RESERVED	MOD_TYPE_H		RESERVED		MIN_PERIOD_H[9:8]		0x0000	R/W
		[7:0]	MIN_PERIOD_H[7:0]									
0x020C	LED_PULSE1_H	[15:8]	LED_WIDTH_H								0x0210	R/W
		[7:0]	LED_OFFSET_H									
0x020D	LED_PULSE2_H	[15:8]	RESERVED								0x0013	R/W
		[7:0]	LED_SECOND_OFFSET_H									
0x020E	INTEG_WIDTH_H	[15:8]	SINGLE_INTEG_H	RESERVED		CH2_AMP_DISABLE_H		RESERVED		CH1_AMP_DISABLE_H[1]	0x0003	R/W
		[7:0]	CH1_AMP_DISABLE_H[0]	ADC_COUNT_H		INTEG_WIDTH_H						
0x020F	INTEG_OFFSET_H	[15:8]	RESERVED			INTEG_OFFSET_H[7:3]					0x01A0	R/W
		[7:0]	INTEG_OFFSET_H[2:0]			INTEG_FINE_OFFSET_H						
0x0210	MOD_PULSE_H	[15:8]	MOD_WIDTH_H								0x0001	R/W
		[7:0]	MOD_OFFSET_H									
0x0211	PATTERN1_H	[15:8]	LED_DISABLE_H				MOD_DISABLE_H				0x0000	R/W
		[7:0]	SUBTRACT_H				REVERSE_INTEG_H					
0x0213	ADC_OFF1_H	[15:8]	RESERVED		CH1_ADC_ADJUST_H[13:8]						0x0000	R/W
		[7:0]	CH1_ADC_ADJUST_H[7:0]									
0x0214	ADC_OFF2_H	[15:8]	RESERVED		CH2_ADC_ADJUST_H[13:8]						0x0000	R/W
		[7:0]	CH2_ADC_ADJUST_H[7:0]									
0x0215	DATA1_H	[15:8]	DARK_SHIFT_H					DARK_SIZE_H			0x0003	R/W
		[7:0]	SIGNAL_SHIFT_H					SIGNAL_SIZE_H				
0x0216	DATA2_H	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LIT_SHIFT_H					LIT_SIZE_H				
0x0217	DECIMATE_H	[15:8]	RESERVED					DECIMATE_FACTOR_H[6:4]			0x0000	R/W
		[7:0]	DECIMATE_FACTOR_H[3:0]				RESERVED					
0x0218	DIGINT_LIT_H	[15:8]	RESERVED							LIT_OFFSET_H[8]	0x0026	R/W
		[7:0]	LIT_OFFSET_H[7:0]									
0x0219	DIGINT_DARK_H	[15:8]	DARK2_OFFSET_H[8:1]								0x0086	R/W
		[7:0]	DARK2_OFFSET_H[0]	DARK1_OFFSET_H								
0x0220	TS_CTRL_I	[15:8]	SUBSAMPLE_I	CH2_EN_I	SAMPLE_TYPE_I			RESERVED	TIMESLOT_OFFSET_I[9:8]		0x0000	R/W
		[7:0]	TIMESLOT_OFFSET_I[7:0]									
0x0221	TS_PATH_I	[15:8]	PRE_WIDTH_I				AMBIENT_CANCELLATION_I		TS_GPIO_I	AFE_INT_C_BUF_I	0x4020	R/W
		[7:0]	RESERVED	AFE_PATH_CFG_I								
0x0222	INPUTS_I	[15:8]	RESERVED								0x0000	R/W
		[7:0]	INP34_I				INP12_I					

REGISTER SUMMARY

Table 20. Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x0223	CATHODE_I	[15:8]	RESERVED	PRECON_I			VC2_PULSE_I		VC2_ALT_I		0x0000	R/W
		[7:0]	VC2_SEL_I		VC1_PULSE_I		VC1_ALT_I		VC1_SEL_I			
0x0224	AFE_TRIM1_I	[15:8]	TIA_CEIL_DETECT_EN_I	CH2_TRIM_INT_I		CH1_TRIM_INT_I		VREF_PULSE_I	AFE_TRIM_VREF_I		0x02C9	R/W
		[7:0]	VREF_PULSE_VAL_I		TIA_GAIN_CH2_I			TIA_GAIN_CH1_I				
0x0225	AFE_TRIM2_I	[15:8]	RESERVED		CH2_TRIM_INT_CAP_I	CH1_TRIM_INT_CAP_I	RESERVED				0x0000	R/W
		[7:0]	RESERVED									
0x0226	AFE_DAC1_I	[15:8]	DAC_AMBIENT_CH1_I[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH1_I[0]	DAC_LED_DC_CH1_I								
0x0227	AFE_DAC2_I	[15:8]	DAC_AMBIENT_CH2_I[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH2_I[0]	DAC_LED_DC_CH2_I								
0x0228	LED_POW12_I	[15:8]	LED_DRIVESIDE2_I	LED_CURRENT2_I							0x0000	R/W
		[7:0]	LED_DRIVESIDE1_I	LED_CURRENT1_I								
0x0229	LED_MODE_I	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED						LED_MODE2_I	LED_MODE1_I		
0x022A	COUNTS_I	[15:8]	NUM_INT_I								0x0101	R/W
		[7:0]	NUM_REPEAT_I									
0x022B	PERIOD_I	[15:8]	RESERVED	RESERVED	MOD_TYPE_I		RESERVED		MIN_PERIOD_I[9:8]		0x0000	R/W
		[7:0]	MIN_PERIOD_I[7:0]									
0x022C	LED_PULSE1_I	[15:8]	LED_WIDTH_I								0x0210	R/W
		[7:0]	LED_OFFSET_I									
0x022D	LED_PULSE2_I	[15:8]	RESERVED								0x0013	R/W
		[7:0]	LED_SECOND_OFFSET_I									
0x022E	INTEG_WIDTH_I	[15:8]	SINGLE_INTEG_I	RESERVED		CH2_AMP_DISABLE_I		RESERVED		CH1_AMP_DISABLE_I[1]	0x0003	R/W
		[7:0]	CH1_AMP_DISABLE_I[0]	ADC_COUNT_I		INTEG_WIDTH_I						
0x022F	INTEG_OFFSET_I	[15:8]	RESERVED			INTEG_OFFSET_I[7:3]					0x01A0	R/W
		[7:0]	INTEG_OFFSET_I[2:0]			INTEG_FINE_OFFSET_I						
0x0230	MOD_PULSE_I	[15:8]	MOD_WIDTH_I								0x0001	R/W
		[7:0]	MOD_OFFSET_I									
0x0231	PATTERN1_I	[15:8]	LED_DISABLE_I				MOD_DISABLE_I				0x0000	R/W
		[7:0]	SUBTRACT_I				REVERSE_INTEG_I					

REGISTER SUMMARY

Table 20. Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x0233	ADC_OFF1_I	[15:8]	RESERVED		CH1_ADC_ADJUST_I[13:8]						0x0000	R/W
		[7:0]	CH1_ADC_ADJUST_I[7:0]									
0x0234	ADC_OFF2_I	[15:8]	RESERVED		CH2_ADC_ADJUST_I[13:8]						0x0000	R/W
		[7:0]	CH2_ADC_ADJUST_I[7:0]									
0x0235	DATA1_I	[15:8]	DARK_SHIFT_I					DARK_SIZE_I			0x0003	R/W
		[7:0]	SIGNAL_SHIFT_I					SIGNAL_SIZE_I				
0x0236	DATA2_I	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LIT_SHIFT_I					LIT_SIZE_I				
0x0237	DECIMATE_I	[15:8]	RESERVED					DECIMATE_FACTOR_I[6:4]			0x0000	R/W
		[7:0]	DECIMATE_FACTOR_I[3:0]				RESERVED					
0x0238	DIGINT_LIT_I	[15:8]	RESERVED							LIT_OFFSET_I[8]	0x0026	R/W
		[7:0]	LIT_OFFSET_I[7:0]									
0x0239	DIGINT_DARK_I	[15:8]	DARK2_OFFSET_I[8:1]								0x0086	R/W
		[7:0]	DARK2_OFFSET_I[0]	DARK1_OFFSET_I								
0x0240	TS_CTRL_J	[15:8]	SUBSAMPLE_J	CH2_EN_J	SAMPLE_TYPE_J			RESERVED	TIMESLOT_OFFSET_J[9:8]		0x0000	R/W
		[7:0]	TIMESLOT_OFFSET_J[7:0]									
0x0241	TS_PATH_J	[15:8]	PRE_WIDTH_J				AMBIENT_CANCELLATION_J		TS_GPIO_J	AFE_INT_C_BUF_J	0x4020	R/W
		[7:0]	RESERVED	AFE_PATH_CFG_J								
0x0242	INPUTS_J	[15:8]	RESERVED								0x0000	R/W
		[7:0]	INP34_J				INP12_J					
0x0243	CATHODE_J	[15:8]	RESERVED	PRECON_J			VC2_PULSE_J		VC2_ALT_J		0x0000	R/W
		[7:0]	VC2_SEL_J		VC1_PULSE_J		VC1_ALT_J		VC1_SEL_J			
0x0244	AFE_TRIM1_J	[15:8]	TIA_CEIL_DETECT_EN_J	CH2_TRIM_INT_J		CH1_TRIM_INT_J		VREF_PULSE_J	AFE_TRIM_VREF_J		0x02C9	R/W
		[7:0]	VREF_PULSE_VAL_J		TIA_GAIN_CH2_J			TIA_GAIN_CH1_J				
0x0245	AFE_TRIM2_J	[15:8]	RESERVED		CH2_TRIM_INT_CAP_J	CH1_TRIM_INT_CAP_J	RESERVED				0x0000	R/W
		[7:0]	RESERVED									
0x0246	AFE_DAC1_J	[15:8]	DAC_AMBIENT_CH1_J[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH1_J[0]	DAC_LED_DC_CH1_J								
0x0247	AFE_DAC2_J	[15:8]	DAC_AMBIENT_CH2_J[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH2_J[0]	DAC_LED_DC_CH2_J								
0x0248	LED_POW12_J	[15:8]	LED_DRIVESIDE2_J	LED_CURRENT2_J							0x0000	R/W
		[7:0]	LED_DRIVESIDE1_J	LED_CURRENT1_J								
0x0249	LED_MODE_J	[15:8]	RESERVED								0x0000	R/W

REGISTER SUMMARY

Table 20. Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
		[7:0]	RESERVED						LED_MODE2_J	LED_MODE1_J		
0x024A	COUNTS_J	[15:8]	NUM_INT_J								0x0101	R/W
		[7:0]	NUM_REPEAT_J									
0x024B	PERIOD_J	[15:8]	RESERVED	RESERVED	MOD_TYPE_J		RESERVED		MIN_PERIOD_J[9:8]		0x0000	R/W
		[7:0]	MIN_PERIOD_J[7:0]									
0x024C	LED_PULSE1_J	[15:8]	LED_WIDTH_J								0x0210	R/W
		[7:0]	LED_OFFSET_J									
0x024D	LED_PULSE2_J	[15:8]	RESERVED								0x0013	R/W
		[7:0]	LED_SECOND_OFFSET_J									
0x024E	INTEG_WIDTH_J	[15:8]	SINGLE_INTEG_J	RESERVED		CH2_AMP_DISABLE_J		RESERVED		CH1_AMP_DISABLE_J[1]	0x0003	R/W
		[7:0]	CH1_AMP_DISABLE_J[0]	ADC_COUNT_J		INTEG_WIDTH_J						
0x024F	INTEG_OFFSET_J	[15:8]	RESERVED			INTEG_OFFSET_J[7:3]					0x01A0	R/W
		[7:0]	INTEG_OFFSET_J[2:0]			INTEG_FINE_OFFSET_J						
0x0250	MOD_PULSE_J	[15:8]	MOD_WIDTH_J								0x0001	R/W
		[7:0]	MOD_OFFSET_J									
0x0251	PATTERN1_J	[15:8]	LED_DISABLE_J				MOD_DISABLE_J				0x0000	R/W
		[7:0]	SUBTRACT_J				REVERSE_INTEG_J					
0x0253	ADC_OFF1_J	[15:8]	RESERVED		CH1_ADC_ADJUST_J[13:8]						0x0000	R/W
		[7:0]	CH1_ADC_ADJUST_J[7:0]									
0x0254	ADC_OFF2_J	[15:8]	RESERVED		CH2_ADC_ADJUST_J[13:8]						0x0000	R/W
		[7:0]	CH2_ADC_ADJUST_J[7:0]									
0x0255	DATA1_J	[15:8]	DARK_SHIFT_J					DARK_SIZE_J			0x0003	R/W
		[7:0]	SIGNAL_SHIFT_J					SIGNAL_SIZE_J				
0x0256	DATA2_J	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LIT_SHIFT_J					LIT_SIZE_J				
0x0257	DECIMATE_J	[15:8]	RESERVED					DECIMATE_FACTOR_J[6:4]			0x0000	R/W
		[7:0]	DECIMATE_FACTOR_J[3:0]				RESERVED					
0x0258	DIGINT_LIT_J	[15:8]	RESERVED							LIT_OFFSET_J[8]	0x0026	R/W
		[7:0]	LIT_OFFSET_J[7:0]									
0x0259	DIGINT_DARK_J	[15:8]	DARK2_OFFSET_J[8:1]								0x0086	R/W
		[7:0]	DARK2_OFFSET_J[0]	DARK1_OFFSET_J								
0x0260	TS_CTRL_K	[15:8]	SUBSAMPLE_K	CH2_EN_K	SAMPLE_TYPE_K			RESERVED	TIMESLOT_OFFSET_K[9:8]		0x0000	R/W
		[7:0]	TIMESLOT_OFFSET_K[7:0]									
0x0261	TS_PATH_K	[15:8]	PRE_WIDTH_K				AMBIENT_CANCELLATION_K		TS_GPIO_K	AFE_INT_C_BUF_K	0x4020	R/W

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Table 20. Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
		[7:0]	RESERVED	AFE_PATH_CFG_K								
0x0262	INPUTS_K	[15:8]	RESERVED								0x0000	R/W
		[7:0]	INP34_K				INP12_K					
0x0263	CATHODE_K	[15:8]	RESERVED	PRECON_K			VC2_PULSE_K		VC2_ALT_K		0x0000	R/W
		[7:0]	VC2_SEL_K		VC1_PULSE_K		VC1_ALT_K		VC1_SEL_K			
0x0264	AFE_TRIM1_K	[15:8]	TIA_CEIL_DETECT_EN_K	CH2_TRIM_INT_K		CH1_TRIM_INT_K		VREF_PULSE_K	AFE_TRIM_VREF_K		0x02C9	R/W
		[7:0]	VREF_PULSE_VAL_K		TIA_GAIN_CH2_K			TIA_GAIN_CH1_K				
0x0265	AFE_TRIM2_K	[15:8]	RESERVED		CH2_TRIM_INT_CAP_K	CH1_TRIM_INT_CAP_K	RESERVED				0x0000	R/W
		[7:0]	RESERVED									
0x0266	AFE_DAC1_K	[15:8]	DAC_AMBIENT_CH1_K[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH1_K[0]	DAC_LED_DC_CH1_K								
0x0267	AFE_DAC2_K	[15:8]	DAC_AMBIENT_CH2_K[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH2_K[0]	DAC_LED_DC_CH2_K								
0x0268	LED_POW12_K	[15:8]	LED_DRIVESIDE2_K	LED_CURRENT2_K							0x0000	R/W
		[7:0]	LED_DRIVESIDE1_K	LED_CURRENT1_K								
0x0269	LED_MODE_K	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED						LED_MODE2_K	LED_MODE1_K		
0x026A	COUNTS_K	[15:8]	NUM_INT_K								0x0101	R/W
		[7:0]	NUM_REPEAT_K									
0x026B	PERIOD_K	[15:8]	RESERVED	RESERVED	MOD_TYPE_K		RESERVED		MIN_PERIOD_K[9:8]		0x0000	R/W
		[7:0]	MIN_PERIOD_K[7:0]									
0x026C	LED_PULSE1_K	[15:8]	LED_WIDTH_K								0x0210	R/W
		[7:0]	LED_OFFSET_K									
0x026D	LED_PULSE2_K	[15:8]	RESERVED								0x0013	R/W
		[7:0]	LED_SECOND_OFFSET_K									
0x026E	INTEG_WIDTH_K	[15:8]	SINGLE_INTEG_K	RESERVED		CH2_AMP_DISABLE_K		RESERVED		CH1_AMP_DISABLE_K[1]	0x0003	R/W
		[7:0]	CH1_AMP_DISABLE_K[0]	ADC_COUNT_K		INTEG_WIDTH_K						
0x026F	INTEG_OFFSET_K	[15:8]	RESERVED			INTEG_OFFSET_K[7:3]					0x01A0	R/W
		[7:0]	INTEG_OFFSET_K[2:0]			INTEG_FINE_OFFSET_K						

REGISTER SUMMARY

Table 20. Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x0270	MOD_PULSE_K	[15:8]	MOD_WIDTH_K								0x0001	R/W
		[7:0]	MOD_OFFSET_K									
0x0271	PATTERN1_K	[15:8]	LED_DISABLE_K				MOD_DISABLE_K				0x0000	R/W
		[7:0]	SUBTRACT_K				REVERSE_INTEG_K					
0x0273	ADC_OFF1_K	[15:8]	RESERVED		CH1_ADC_ADJUST_K[13:8]						0x0000	R/W
		[7:0]	CH1_ADC_ADJUST_K[7:0]									
0x0274	ADC_OFF2_K	[15:8]	RESERVED		CH2_ADC_ADJUST_K[13:8]						0x0000	R/W
		[7:0]	CH2_ADC_ADJUST_K[7:0]									
0x0275	DATA1_K	[15:8]	DARK_SHIFT_K					DARK_SIZE_K			0x0003	R/W
		[7:0]	SIGNAL_SHIFT_K					SIGNAL_SIZE_K				
0x0276	DATA2_K	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LIT_SHIFT_K					LIT_SIZE_K				
0x0277	DECIMATE_K	[15:8]	RESERVED					DECIMATE_FACTOR_K[6:4]			0x0000	R/W
		[7:0]	DECIMATE_FACTOR_K[3:0]				RESERVED					
0x0278	DIGINT_LIT_K	[15:8]	RESERVED							LIT_OFFSET_K[8]	0x0026	R/W
		[7:0]	LIT_OFFSET_K[7:0]									
0x0279	DIGINT_DARK_K	[15:8]	DARK2_OFFSET_K[8:1]								0x0086	R/W
		[7:0]	DARK2_OFFSET_K[0]	DARK1_OFFSET_K								
0x0280	TS_CTRL_L	[15:8]	SUBSAMPLE_L	CH2_EN_L	SAMPLE_TYPE_L			RESERVED	TIMESLOT_OFFSET_L[9:8]		0x0000	R/W
		[7:0]	TIMESLOT_OFFSET_L[7:0]									
0x0281	TS_PATH_L	[15:8]	PRE_WIDTH_L				AMBIENT_CANCELLATION_L		TS_GPIO_L	AFE_INT_C_BUF_L	0x4020	R/W
		[7:0]	RESERVED	AFE_PATH_CFG_L								
0x0282	INPUTS_L	[15:8]	RESERVED								0x0000	R/W
		[7:0]	INP34_L				INP12_L					
0x0283	CATHODE_L	[15:8]	RESERVED	PRECON_L			VC2_PULSE_L		VC2_ALT_L		0x0000	R/W
		[7:0]	VC2_SEL_L		VC1_PULSE_L		VC1_ALT_L		VC1_SEL_L			
0x0284	AFE_TRIM1_L	[15:8]	TIA_CEIL_DETECT_EN_L	CH2_TRIM_INT_L		CH1_TRIM_INT_L		VREF_PULSE_L	AFE_TRIM_VREF_L		0x02C9	R/W
		[7:0]	VREF_PULSE_VAL_L		TIA_GAIN_CH2_L			TIA_GAIN_CH1_L				
0x0285	AFE_TRIM2_L	[15:8]	RESERVED		CH2_TRIM_INT_CAP_L	CH1_TRIM_INT_CAP_L	RESERVED				0x0000	R/W
		[7:0]	RESERVED									
0x0286	AFE_DAC1_L	[15:8]	DAC_AMBIENT_CH1_L[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH1_L[0]	DAC_LED_DC_CH1_L								
0x0287	AFE_DAC2_L	[15:8]	DAC_AMBIENT_CH2_L[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH2_L[0]	DAC_LED_DC_CH2_L								

REGISTER SUMMARY

Table 20. Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x0288	LED_POW12_L	[15:8]	LED_DRIVESIDE2_L	LED_CURRENT2_L							0x0000	R/W
		[7:0]	LED_DRIVESIDE1_L	LED_CURRENT1_L								
0x0289	LED_MODE_L	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED						LED_MODE2_L	LED_MODE1_L		
0x028A	COUNTS_L	[15:8]	NUM_INT_L								0x0101	R/W
		[7:0]	NUM_REPEAT_L									
0x028B	PERIOD_L	[15:8]	RESERVED	RESERVED	MOD_TYPE_L		RESERVED		MIN_PERIOD_L[9:8]		0x0000	R/W
		[7:0]	MIN_PERIOD_L[7:0]									
0x028C	LED_PULSE1_L	[15:8]	LED_WIDTH_L								0x0210	R/W
		[7:0]	LED_OFFSET_L									
0x028D	LED_PULSE2_L	[15:8]	RESERVED								0x0013	R/W
		[7:0]	LED_SECOND_OFFSET_L									
0x028E	INTEG_WIDTH_L	[15:8]	SINGLE_INTEG_L	RESERVED		CH2_AMP_DISABLE_L		RESERVED		CH1_AMP_DISABLE_L[1]	0x0003	R/W
		[7:0]	CH1_AMP_DISABLE_L[0]	ADC_COUNT_L		INTEG_WIDTH_L						
0x028F	INTEG_OFFSET_L	[15:8]	RESERVED			INTEG_OFFSET_L[7:3]					0x01A0	R/W
		[7:0]	INTEG_OFFSET_L[2:0]			INTEG_FINE_OFFSET_L						
0x0290	MOD_PULSE_L	[15:8]	MOD_WIDTH_L								0x0001	R/W
		[7:0]	MOD_OFFSET_L									
0x0291	PATTERN1_L	[15:8]	LED_DISABLE_L				MOD_DISABLE_L				0x0000	R/W
		[7:0]	SUBTRACT_L				REVERSE_INTEG_L					
0x0293	ADC_OFF1_L	[15:8]	RESERVED		CH1_ADC_ADJUST_L[13:8]						0x0000	R/W
		[7:0]	CH1_ADC_ADJUST_L[7:0]									
0x0294	ADC_OFF2_L	[15:8]	RESERVED		CH2_ADC_ADJUST_L[13:8]						0x0000	R/W
		[7:0]	CH2_ADC_ADJUST_L[7:0]									
0x0295	DATA1_L	[15:8]	DARK_SHIFT_L					DARK_SIZE_L			0x0003	R/W
		[7:0]	SIGNAL_SHIFT_L					SIGNAL_SIZE_L				
0x0296	DATA2_L	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LIT_SHIFT_L					LIT_SIZE_L				
0x0297	DECIMATE_L	[15:8]	RESERVED					DECIMATE_FACTOR_L[6:4]			0x0000	R/W
		[7:0]	DECIMATE_FACTOR_L[3:0]				RESERVED					
0x0298	DIGINT_LIT_L	[15:8]	RESERVED							LIT_OFFSET_L[8]	0x0026	R/W
		[7:0]	LIT_OFFSET_L[7:0]									
0x0299	DIGINT_DARK_L	[15:8]	DARK2_OFFSET_L[8:1]								0x0086	R/W
		[7:0]	DARK2_OFFSET_L[0]	DARK1_OFFSET_L								

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Table 20. Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x02A0	BIOZ_AFECON_A	[15:8]	RESERVED				BIOZ_TIMESLOT_OFFSET_A[9:6]				0x0000	R/W
		[7:0]	BIOZ_TIMESLOT_OFFSET_A[5:0]						BIOZ_TIAEN_A	BIOZ_DACREFEN_A		
0x02A1	BIOZ_WGFCW_LOW_A	[15:8]	BIOZ_SINEFCW_L_A[15:8]								0x0000	R/W
		[7:0]	BIOZ_SINEFCW_L_A[7:0]									
0x02A2	BIOZ_WGFCW_HI_A	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED				BIOZ_SINEFCW_H_A					
0x02A3	BIOZ_WGPHASE_LOW_A	[15:8]	BIOZ_SINE_PHASE_OFFSET_L_A[15:8]								0x0000	R/W
		[7:0]	BIOZ_SINE_PHASE_OFFSET_L_A[7:0]									
0x02A4	BIOZ_WGPHASE_HI_A	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED				BIOZ_SINE_PHASE_OFFSET_H_A					
0x02A5	BIOZ_WGOFFSET_A	[15:8]	RESERVED				BIOZ_SINE_OFFSET_A[11:8]				0x0000	R/W
		[7:0]	BIOZ_SINE_OFFSET_A[7:0]									
0x02A6	BIOZ_WGAMPLITUDE_A	[15:8]	RESERVED					BIOZ_SINEAMPLITUDE_A[10:8]			0x0600	R/W
		[7:0]	BIOZ_SINEAMPLITUDE_A[7:0]									
0x02A7	BIOZ_DACCON_A	[15:8]	RESERVED		BIOZ_EXBUFEN_A	BIOZ_DACBUFBW_A			BIOZ_BW250KEN_A	BIOZ_BW50KEN_A	0x0120D	R/W
		[7:0]	BIOZ_RATE_DIV_A									
0x02A8	BIOZ_DACGAIN_A	[15:8]	RESERVED			BIOZ_DACGAIN_EN_A	BIOZ_DAC_GAIN_A[11:8]				0x1800	R/W
		[7:0]	BIOZ_DAC_GAIN_A[7:0]									
0x02A9	BIOZ_DACOFFSET_A	[15:8]	RESERVED			BIOZ_DACOFFSET_EN_A	BIOZ_DAC_OFFSET_A[11:8]				0x1000	R/W
		[7:0]	BIOZ_DAC_OFFSET_A[7:0]									
0x02AA	BIOZ_ANA_CTRL1_A	[15:8]	BIOZ_TIA_RGAIN_A			BIOZ_TIA_CGAIN_A				BIOZ_RX_LPMODE_A	0x2E3E	R/W
		[7:0]	BIOZ_TIA_LPMODE_A	BIOZ_EXCBUF_LPMODE_A	BIOZ_CHOP_OFF_IN_A		BIOZ_AMP_OFF_A		BIOZ_PGA_PD_A	BIOZ_DAC_RCF_LOWBW_EN_A		
0x02AB	BIOZ_ANA_CTRL2_A	[15:8]	RESERVED	BIOZ_CM_SW_A	BIOZ_NCHAN_A		BIOZ_PCHAN_A		BIOZ_TSW_A[3:2]		0x0000	R/W
		[7:0]	BIOZ_TSW_A[1:0]		BIOZ_DSW_A				BIOZ_TRSW_A	BIOZ_DRSW_A		
0x02AC	BIOZ_ANA_CTRL3_A	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED						BIOZ_RINT_SW_A			
0x02AD	BIOZ_ADCFILTERCON_A	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED		BIOZ_AVRGNUM_A		BIOZ_AVRGEN_A	BIOZ_SINC3BYP_A	BIOZ_SINC3OSR_A			
0x02AE	BIOZ_DFTCON_A	[15:8]	RESERVED								0x0009	R/W

REGISTER SUMMARY

Table 20. Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
		[7:0]	RESERVED		BIOZ_WG_DFT_DIFF_PHASE_EN_A	BIOZ_HANNINGEN_A	BIOZ_DFTNUM_A					
0x02AF	BIOZ_ADC_CONV_DLY_A	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED					BIOZ_ADC_CONV_DLY_A				
0x02B0	BIOZ_DFTPHASE_LOW_A	[15:8]	BIOZ_DFT_PHASE_OFFSET_L_A[15:8]								0x0000	R/W
		[7:0]	BIOZ_DFT_PHASE_OFFSET_L_A[7:0]									
0x02B1	BIOZ_DFTPHASE_HI_A	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED				BIOZ_DFT_PHASE_OFFSET_H_A					
0x02C0	BIOZ_AFECON_B	[15:8]	RESERVED				BIOZ_TIMESLOT_OFFSET_B[9:6]				0x0000	R/W
		[7:0]	BIOZ_TIMESLOT_OFFSET_B[5:0]						BIOZ_TIAEN_B	BIOZ_DACREFEN_B		
0x02C1	BIOZ_WGFCW_LOW_B	[15:8]	BIOZ_SINEFCW_L_B[15:8]								0x0000	R/W
		[7:0]	BIOZ_SINEFCW_L_B[7:0]									
0x02C2	BIOZ_WGFCW_HI_B	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED				BIOZ_SINEFCW_H_B					
0x02C3	BIOZ_WGPHASE_LOW_B	[15:8]	BIOZ_SINE_PHASE_OFFSET_L_B[15:8]								0x0000	R/W
		[7:0]	BIOZ_SINE_PHASE_OFFSET_L_B[7:0]									
0x02C4	BIOZ_WGPHASE_HI_B	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED				BIOZ_SINE_PHASE_OFFSET_H_B					
0x02C5	BIOZ_WGOFFSET_B	[15:8]	RESERVED				BIOZ_SINE_OFFSET_B[11:8]				0x0000	R/W
		[7:0]	BIOZ_SINE_OFFSET_B[7:0]									
0x02C6	BIOZ_WGAMPLITUDE_B	[15:8]	RESERVED					BIOZ_SINEAMPLITUDE_B[10:8]			0x0600	R/W
		[7:0]	BIOZ_SINEAMPLITUDE_B[7:0]									
0x02C7	BIOZ_DACCON_B	[15:8]	RESERVED		BIOZ_EXBUFEN_B	BIOZ_DACBUFBW_B			BIOZ_BW250KEN_B	BIOZ_BW50KEN_B	0x120D	R/W
		[7:0]	BIOZ_RATE_DIV_B									
0x02C8	BIOZ_DACGAIN_B	[15:8]	RESERVED			BIOZ_DACGAIN_EN_B	BIOZ_DAC_GAIN_B[11:8]				0x1800	R/W
		[7:0]	BIOZ_DAC_GAIN_B[7:0]									
0x02C9	BIOZ_DACOFFSET_B	[15:8]	RESERVED			BIOZ_DACOFFSET_EN_B	BIOZ_DAC_OFFSET_B[11:8]				0x1000	R/W
		[7:0]	BIOZ_DAC_OFFSET_B[7:0]									
0x02CA	BIOZ_ANA_CTRL1_B	[15:8]	BIOZ_TIA_RGAIN_B			BIOZ_TIA_CGAIN_B				BIOZ_RX_LPMODE_B	0x2E3E	R/W
		[7:0]	BIOZ_TIA_LPMODE_B	BIOZ_EXCBUF_LPMODE_B	BIOZ_CHOP_OFF_IN_B		BIOZ_AMP_OFF_B		BIOZ_PGA_PD_B	BIOZ_DAC_RCF_LOWBW_EN_B		

REGISTER SUMMARY

Table 20. Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x02CB	BIOZ_ANA_CTRL2_B	[15:8]	RESERVED	BIOZ_CM_SW_B	BIOZ_NCHAN_B		BIOZ_PCHAN_B		BIOZ_TSW_B[3:2]		0x0000	R/W
		[7:0]	BIOZ_TSW_B[1:0]		BIOZ_DSW_B				BIOZ_TRSW_B	BIOZ_DRSW_B		
0x02CC	BIOZ_ANA_CTRL3_B	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED						BIOZ_RINT_SW_B			
0x02CD	BIOZ_ADCFILTERCON_B	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED		BIOZ_AVRGNUM_B		BIOZ_AVRGEN_B	BIOZ_SINC3BYP_B	BIOZ_SINC3OSR_B			
0x02CE	BIOZ_DFTCON_B	[15:8]	RESERVED								0x0009	R/W
		[7:0]	RESERVED		BIOZ_WG_DFT_DIFF_PHASE_EN_B	BIOZ_HANNINGEN_B	BIOZ_DFTNUM_B					
0x02CF	BIOZ_ADC_CONV_DLY_B	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED					BIOZ_ADC_CONV_DLY_B				
0x02D0	BIOZ_DFTPHASE_LOW_B	[15:8]	BIOZ_DFT_PHASE_OFFSET_L_B[15:8]								0x0000	R/W
		[7:0]	BIOZ_DFT_PHASE_OFFSET_L_B[7:0]									
0x02D1	BIOZ_DFTPHASE_HI_B	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED				BIOZ_DFT_PHASE_OFFSET_H_B					
0x02E0	BIOZ_AFECON_C	[15:8]	RESERVED				BIOZ_TIMESLOT_OFFSET_C[9:6]				0x0000	R/W
		[7:0]	BIOZ_TIMESLOT_OFFSET_C[5:0]						BIOZ_TIAEN_C	BIOZ_DACREFEN_C		
0x02E1	BIOZ_WGFCW_LOW_C	[15:8]	BIOZ_SINEFCW_L_C[15:8]								0x0000	R/W
		[7:0]	BIOZ_SINEFCW_L_C[7:0]									
0x02E2	BIOZ_WGFCW_HI_C	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED				BIOZ_SINEFCW_H_C					
0x02E3	BIOZ_WGPHASE_LOW_C	[15:8]	BIOZ_SINE_PHASE_OFFSET_L_C[15:8]								0x0000	R/W
		[7:0]	BIOZ_SINE_PHASE_OFFSET_L_C[7:0]									
0x02E4	BIOZ_WGPHASE_HI_C	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED				BIOZ_SINE_PHASE_OFFSET_H_C					
0x02E5	BIOZ_WGOFFSET_C	[15:8]	RESERVED				BIOZ_SINE_OFFSET_C[11:8]				0x0000	R/W
		[7:0]	BIOZ_SINE_OFFSET_C[7:0]									
0x02E6	BIOZ_WGAMPLITUDE_C	[15:8]	RESERVED					BIOZ_SINEAMPLITUDE_C[10:8]			0x0600	R/W
		[7:0]	BIOZ_SINEAMPLITUDE_C[7:0]									
0x02E7	BIOZ_DACCON_C	[15:8]	RESERVED		BIOZ_EXBUFEN_C	BIOZ_DACBUFBW_C			BIOZ_BW250KEN_C	BIOZ_BW50KEN_C	0x120D	R/W
		[7:0]	BIOZ_RATE_DIV_C									

REGISTER SUMMARY

Table 20. Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x02E8	BIOZ_DACGAIN_C	[15:8]	RESERVED			BIOZ_DACGAIN_EN_C	BIOZ_DAC_GAIN_C[11:8]				0x1800	R/W
		[7:0]	BIOZ_DAC_GAIN_C[7:0]									
0x02E9	BIOZ_DACOFFSET_C	[15:8]	RESERVED			BIOZ_DACOFFSET_EN_C	BIOZ_DAC_OFFSET_C[11:8]				0x1000	R/W
		[7:0]	BIOZ_DAC_OFFSET_C[7:0]									
0x02EA	BIOZ_ANA_CTRL1_C	[15:8]	BIOZ_TIA_RGAIN_C			BIOZ_TIA_CGAIN_C				BIOZ_RX_LPMODE_C	0x2E3E	R/W
		[7:0]	BIOZ_TIA_LPMODE_C	BIOZ_EXCBUF_LPMODE_C	BIOZ_CHOP_OFF_IN_C		BIOZ_AMP_OFF_C		BIOZ_PGA_PD_C	BIOZ_DAC_RCF_LOWBW_EN_C		
0x02EB	BIOZ_ANA_CTRL2_C	[15:8]	RESERVED	BIOZ_CM_SW_C	BIOZ_NCHAN_C		BIOZ_PCHAN_C		BIOZ_TSW_C[3:2]		0x0000	R/W
		[7:0]	BIOZ_TSW_C[1:0]		BIOZ_DSW_C				BIOZ_TRSW_C	BIOZ_DRSW_C		
0x02EC	BIOZ_ANA_CTRL3_C	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED						BIOZ_RINT_SW_C			
0x02ED	BIOZ_ADCFILTERCON_C	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED		BIOZ_AVRGNUM_C		BIOZ_AVRGEN_C	BIOZ_SINC3BYP_C	BIOZ_SINC3OSR_C			
0x02EE	BIOZ_DFTCON_C	[15:8]	RESERVED								0x0009	R/W
		[7:0]	RESERVED		BIOZ_WG_DFT_DIFF_PHASE_EN_C	BIOZ_HANNINGEN_C	BIOZ_DFTNUM_C					
0x02EF	BIOZ_ADC_CONV_DLY_C	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED					BIOZ_ADC_CONV_DLY_C				
0x02F0	BIOZ_DFTPHASE_LOW_C	[15:8]	BIOZ_DFT_PHASE_OFFSET_L_C[15:8]								0x0000	R/W
		[7:0]	BIOZ_DFT_PHASE_OFFSET_L_C[7:0]									
0x02F1	BIOZ_DFTPHASE_HI_C	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED				BIOZ_DFT_PHASE_OFFSET_H_C					
0x300	BIOZ_AFECON_D	[15:8]	RESERVED				BIOZ_TIMESLOT_OFFSET_D[9:6]				0x0000	R/W
		[7:0]	BIOZ_TIMESLOT_OFFSET_D[5:0]						BIOZ_TIAEN_D	BIOZ_DACREFEN_D		
0x301	BIOZ_WGFCW_LOW_D	[15:8]	BIOZ_SINEFCW_L_D[15:8]								0x0000	R/W
		[7:0]	BIOZ_SINEFCW_L_D[7:0]									
0x302	BIOZ_WGFCW_HI_D	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED				BIOZ_SINEFCW_H_D					
0x303	BIOZ_WGPHASE_LOW_D	[15:8]	BIOZ_SINE_PHASE_OFFSET_L_D[15:8]								0x0000	R/W

REGISTER SUMMARY

Table 20. Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
		[7:0]	BIOZ_SINE_PHASE_OFFSET_L_D[7:0]									
0x304	BIOZ_WGPHASE_HI_D	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED				BIOZ_SINE_PHASE_OFFSET_H_D					
0x305	BIOZ_WGOFFSET_D	[15:8]	RESERVED				BIOZ_SINE_OFFSET_D[11:8]				0x0000	R/W
		[7:0]	BIOZ_SINE_OFFSET_D[7:0]									
0x306	BIOZ_WGAMPLITUDE_D	[15:8]	RESERVED					BIOZ_SINEAMPLITUDE_D[10:8]			0x0600	R/W
		[7:0]	BIOZ_SINEAMPLITUDE_D[7:0]									
0x307	BIOZ_DACCON_D	[15:8]	RESERVED		BIOZ_EXBUFEN_D	BIOZ_DACBUFBW_D			BIOZ_BW250KEN_D	BIOZ_BW50KEN_D	0x120D	R/W
		[7:0]	BIOZ_RATE_DIV_D									
0x308	BIOZ_DACGAIN_D	[15:8]	RESERVED			BIOZ_DACGAIN_EN_D	BIOZ_DAC_GAIN_D[11:8]				0x1800	R/W
		[7:0]	BIOZ_DAC_GAIN_D[7:0]									
0x309	BIOZ_DACOFFSET_D	[15:8]	RESERVED			BIOZ_DACOFFSET_EN_D	BIOZ_DAC_OFFSET_D[11:8]				0x1000	R/W
		[7:0]	BIOZ_DAC_OFFSET_D[7:0]									
0x30A	BIOZ_ANA_CTRL1_D	[15:8]	BIOZ_TIA_RGAIN_D			BIOZ_TIA_CGAIN_D				BIOZ_RX_LPMODE_D	0x2E3E	R/W
		[7:0]	BIOZ_TIA_LPMODE_D	BIOZ_EXCBUF_LPMODE_D	BIOZ_CHOP_OFF_IN_D		BIOZ_AMP_OFF_D		BIOZ_PGA_PD_D	BIOZ_DAC_RCF_LOWBW_EN_D		
0x030B	BIOZ_ANA_CTRL2_D	[15:8]	RESERVED	BIOZ_CM_SW_D	BIOZ_NCHAN_D		BIOZ_PCHAN_D		BIOZ_TSW_D[3:2]		0x0000	R/W
		[7:0]	BIOZ_TSW_D[1:0]		BIOZ_DSW_D				BIOZ_TRSW_D	BIOZ_DRSW_D		
0x030C	BIOZ_ANA_CTRL3_D	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED						BIOZ_RINT_SW_D			
0x030D	BIOZ_ADCFILTERCON_D	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED		BIOZ_AVRGNUM_D		BIOZ_AVRGEN_D	BIOZ_SINC3BYP_D	BIOZ_SINC3OSR_D			
0x030E	BIOZ_DFTCON_D	[15:8]	RESERVED								0x0009	R/W
		[7:0]	RESERVED		BIOZ_WG_DFT_DIFF_PHASE_EN_D	BIOZ_HANNINGEN_D	BIOZ_DFTNUM_D					
0x030F	BIOZ_ADC_CONV_DLY_D	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED					BIOZ_ADC_CONV_DLY_D				
0x0310	BIOZ_DFTPHASE_LOW_D	[15:8]	BIOZ_DFT_PHASE_OFFSET_L_D[15:8]								0x0000	R/W
		[7:0]	BIOZ_DFT_PHASE_OFFSET_L_D[7:0]									
0x0311	BIOZ_DFTPHASE_HI_D	[15:8]	RESERVED								0x0000	R/W

REGISTER SUMMARY

Table 20. Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
		[7:0]	RESERVED				BIOZ_DFT_PHASE_OFFSET_H_D					
0x0320	BIOZ_AFECON_E	[15:8]	RESERVED				BIOZ_TIMESLOT_OFFSET_E[9:6]				0x0000	R/W
		[7:0]	BIOZ_TIMESLOT_OFFSET_E[5:0]						BIOZ_TIAEN_E	BIOZ_DACREFEN_E		
0x0321	BIOZ_WGFCW_LOW_E	[15:8]	BIOZ_SINEFCW_L_E[15:8]								0x0000	R/W
		[7:0]	BIOZ_SINEFCW_L_E[7:0]									
0x0322	BIOZ_WGFCW_HI_E	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED				BIOZ_SINEFCW_H_E					
0x0323	BIOZ_WGPHASE_LOW_E	[15:8]	BIOZ_SINE_PHASE_OFFSET_L_E[15:8]								0x0000	R/W
		[7:0]	BIOZ_SINE_PHASE_OFFSET_L_E[7:0]									
0x0324	BIOZ_WGPHASE_HI_E	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED				BIOZ_SINE_PHASE_OFFSET_H_E					
0x0325	BIOZ_WGOFFSET_E	[15:8]	RESERVED				BIOZ_SINE_OFFSET_E[11:8]				0x0000	R/W
		[7:0]	BIOZ_SINE_OFFSET_E[7:0]									
0x0326	BIOZ_WGAMPLITUDE_E	[15:8]	RESERVED					BIOZ_SINEAMPLITUDE_E[10:8]			0x0600	R/W
		[7:0]	BIOZ_SINEAMPLITUDE_E[7:0]									
0x0327	BIOZ_DACCON_E	[15:8]	RESERVED		BIOZ_EXBUFEN_E	BIOZ_DACBUFBW_E			BIOZ_BW250KEN_E	BIOZ_BW50KEN_E	0x120D	R/W
		[7:0]	BIOZ_RATE_DIV_E									
0x0328	BIOZ_DACGAIN_E	[15:8]	RESERVED			BIOZ_DACGAIN_EN_E	BIOZ_DAC_GAIN_E[11:8]				0x1800	R/W
		[7:0]	BIOZ_DAC_GAIN_E[7:0]									
0x0329	BIOZ_DACOFFSET_E	[15:8]	RESERVED			BIOZ_DACOFFSET_EN_E	BIOZ_DAC_OFFSET_E[11:8]				0x1000	R/W
		[7:0]	BIOZ_DAC_OFFSET_E[7:0]									
0x032A	BIOZ_ANA_CTRL1_E	[15:8]	BIOZ_TIA_RGAIN_E			BIOZ_TIA_CGAIN_E				BIOZ_RX_LPMODE_E	0x2E3E	R/W
		[7:0]	BIOZ_TIA_LPMODE_E	BIOZ_EXCBUF_LPMODE_E	BIOZ_CHOP_OFF_IN_E		BIOZ_AMP_OFF_E		BIOZ_PGA_PD_E	BIOZ_DAC_RCF_LOWBW_EN_E		
0x032B	BIOZ_ANA_CTRL2_E	[15:8]	RESERVED	BIOZ_CM_SW_E	BIOZ_NCHAN_E		BIOZ_PCHAN_E		BIOZ_TSW_E[3:2]		0x0000	R/W
		[7:0]	BIOZ_TSW_E[1:0]		BIOZ_DSW_E				BIOZ_TRSW_E	BIOZ_DRSW_E		
0x032C	BIOZ_ANA_CTRL3_E	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED						BIOZ_RINT_SW_E			
0x032D	BIOZ_ADCFILTERCON_E	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED		BIOZ_AVRGNUM_E		BIOZ_AVRGEN_E	BIOZ_SINC3BYP_E	BIOZ_SINC3OSR_E			

REGISTER SUMMARY

Table 20. Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x032E	BIOZ_DFTCON_E	[15:8]	RESERVED								0x0009	R/W
		[7:0]	RESERVED		BIOZ_WG_DFT_DIFF_PHASE_EN_E	BIOZ_HANNINGEN_E	BIOZ_DFTNUM_E					
0x032F	BIOZ_ADC_CONV_DLY_E	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED					BIOZ_ADC_CONV_DLY_E				
0x0330	BIOZ_DFTPHASE_LOW_E	[15:8]	BIOZ_DFT_PHASE_OFFSET_L_E[15:8]								0x0000	R/W
		[7:0]	BIOZ_DFT_PHASE_OFFSET_L_E[7:0]									
0x0331	BIOZ_DFTPHASE_HI_E	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED				BIOZ_DFT_PHASE_OFFSET_H_E					
0x0340	BIOZ_AFECON_F	[15:8]	RESERVED				BIOZ_TIMESLOT_OFFSET_F[9:6]				0x0000	R/W
		[7:0]	BIOZ_TIMESLOT_OFFSET_F[5:0]						BIOZ_TIAEN_F	BIOZ_DACREFEN_F		
0x0341	BIOZ_WGFCW_LOW_F	[15:8]	BIOZ_SINEFCW_L_F[15:8]								0x0000	R/W
		[7:0]	BIOZ_SINEFCW_L_F[7:0]									
0x0342	BIOZ_WGFCW_HI_F	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED				BIOZ_SINEFCW_H_F					
0x0343	BIOZ_WGPHASE_LOW_F	[15:8]	BIOZ_SINE_PHASE_OFFSET_L_F[15:8]								0x0000	R/W
		[7:0]	BIOZ_SINE_PHASE_OFFSET_L_F[7:0]									
0x0344	BIOZ_WGPHASE_HI_F	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED				BIOZ_SINE_PHASE_OFFSET_H_F					
0x0345	BIOZ_WGOFFSET_F	[15:8]	RESERVED				BIOZ_SINE_OFFSET_F[11:8]				0x0000	R/W
		[7:0]	BIOZ_SINE_OFFSET_F[7:0]									
0x0346	BIOZ_WGAMPLITUDE_F	[15:8]	RESERVED					BIOZ_SINEAMPLITUDE_F[10:8]			0x0600	R/W
		[7:0]	BIOZ_SINEAMPLITUDE_F[7:0]									
0x0347	BIOZ_DACCON_F	[15:8]	RESERVED		BIOZ_EXBUFEN_F	BIOZ_DACBUFBW_F			BIOZ_BW250KEN_F	BIOZ_BW50KEN_F	0x120D	R/W
		[7:0]	BIOZ_RATE_DIV_F									
0x0348	BIOZ_DACGAIN_F	[15:8]	RESERVED			BIOZ_DACGAIN_EN_F	BIOZ_DAC_GAIN_F[11:8]				0x1800	R/W
		[7:0]	BIOZ_DAC_GAIN_F[7:0]									
0x0349	BIOZ_DACOFFSET_F	[15:8]	RESERVED			BIOZ_DACOFFSET_EN_F	BIOZ_DAC_OFFSET_F[11:8]				0x1000	R/W
		[7:0]	BIOZ_DAC_OFFSET_F[7:0]									
0x034A	BIOZ_ANA_CTRL1_F	[15:8]	BIOZ_TIA_RGAIN_F			BIOZ_TIA_CGAIN_F				BIOZ_RX_LPMODE_F	0x2E3E	R/W

REGISTER SUMMARY

Table 20. Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
		[7:0]	BIOZ_TIA_LPMODE_F	BIOZ_EXCBUF_LPMODE_F	BIOZ_CHOP_OFF_IN_F		BIOZ_AMP_OFF_F		BIOZ_PGA_PD_F	BIOZ_DAC_RCF_LOWBW_EN_F		
0x034B	BIOZ_ANA_CTRL2_F	[15:8]	RESERVED	BIOZ_CM_SW_F	BIOZ_NCHAN_F		BIOZ_PCHAN_F		BIOZ_TSW_F[3:2]		0x0000	R/W
		[7:0]	BIOZ_TSW_F[1:0]		BIOZ_DSW_F				BIOZ_TRSW_F	BIOZ_DRSW_F		
0x034C	BIOZ_ANA_CTRL3_F	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED						BIOZ_RINT_SW_F			
0x034D	BIOZ_ADCFILTERCON_F	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED		BIOZ_AVRGNUM_F		BIOZ_AVRGEN_F	BIOZ_SINC3BYP_F	BIOZ_SINC3OSR_F			
0x034E	BIOZ_DFTCON_F	[15:8]	RESERVED								0x0009	R/W
		[7:0]	RESERVED		BIOZ_WG_DFT_DIFF_PHASE_EN_F	BIOZ_HANNINGEN_F	BIOZ_DFTNUM_F					
0x034F	BIOZ_ADC_CONV_DLY_F	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED					BIOZ_ADC_CONV_DLY_F				
0x0350	BIOZ_DFTPHASE_LOW_F	[15:8]	BIOZ_DFT_PHASE_OFFSET_L_F[15:8]								0x0000	R/W
		[7:0]	BIOZ_DFT_PHASE_OFFSET_L_F[7:0]									
0x0351	BIOZ_DFTPHASE_HI_F	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED				BIOZ_DFT_PHASE_OFFSET_H_F					

REGISTER DETAILS

Table 21. Register Details

Reg	Name	Bits	Bit Name	Description	Reset	Access
0x0000	FIFO_STATUS	15	CLEAR_FIFO	Clear FIFO. Write a 1 to empty the FIFO while not operating. This resets FIFO_BYTE_COUNT and also clears the INT_FIFO_OFLOW, INT_FIFO_UFLOW, and INT_FIFO_TH status bits. After the FIFO is cleared, CLEAR_FIFO must be set to 0 for the FIFO function.	0x0	R0/W
		14	INT_FIFO_UFLOW	FIFO underflow error. This bit is set when the FIFO is read while empty. Write 1 to this bit to clear the interrupt. This bit is also cleared if the FIFO is cleared using the CLEAR_FIFO bit.	0x0	R/W1C
		13	INT_FIFO_OFLOW	FIFO overflow error. This bit is set when data is not written to the FIFO due to a lack of space. Write 1 to this bit to clear the interrupt. This bit is also cleared if the FIFO is cleared with the CLEAR_FIFO bit.	0x0	R/W1C
		12	INT_FIFO_TH	FIFO_TH interrupt status. This bit is set during a FIFO write when the number of bytes in the FIFO exceed the FIFO_TH register value. Write 1 to this bit to clear this interrupt. This bit can also be automatically cleared when the FIFO data register is read if the INT_ACLEAR_FIFO bit is set.	0x0	R/W1C
		11	FIFO_INIT_DONE_STATUS	FIFO initialization process is finished. Note that this bit is a status bit and is not sent to the interrupt. This bit is set after the FIFO self initialization process.	0x0	R
		[10:0]	FIFO_BYTE_COUNT	Number of bytes in FIFO. This field indicates the number of bytes in the FIFO.	0x0	R
0x0004	ECG_STATUS	[15:8]	RESERVED	Reserved.	0x0	R
		7	ECG_ACLO_STATUS	ECG ACLO status bit. Write 1 to this bit to clear this status.	0x1	R/W1C
		6	ECGIN_DCLO_HI_STATUS	ECGIN DCLO HI status bit. Write 1 to this bit to clear this status.	0x1	R/W1C
		5	ECGIP_DCLO_HI_STATUS	ECGIP DCLO HI status bit. Write 1 to this bit to clear this status.	0x1	R/W1C
		4	ECG_RLD_DCLO_HI_STATUS	ECG RLD DCLO HI status bit. Write 1 to this bit to clear this status.	0x1	R/W1C
		3	ECG_RLD_DCLO_LO_STATUS	ECG RLD DCLO LO status bit. Write 1 to this bit to clear this status.	0x1	R/W1C
		2	ECG_DCLO_STATUS	ECG DCLO status bit. Write 1 to this bit to clear this status.	0x1	R/W1C
		1	ECG_PGA_SAT_STATUS	ECG PGA saturation status bit. Write 1 to this bit to clear this status.	0x0	R/W1C
		0	ECG_ADC_SAT_STATUS	ECG ADC saturation status bit. Write 1 to this bit to clear this status.	0x0	R/W1C
0x0005	GLOBAL_STATUS	[15:1]	RESERVED	Reserved.	0x0	R
		0	INVALID_CFG_STATUS	Status bit indicating that TIMESLOT_PERIOD_x is not configured properly. Write 1 to this bit to clear this status.	0x0	R/W1C
0x0006	FIFO_TH	[15:10]	RESERVED	Reserved.	0x0	R
		[9:0]	FIFO_TH	FIFO interrupt generation threshold. This bit generates the FIFO interrupt during a FIFO write when the number of bytes in the FIFO exceeds this value.	0x0	R/W
0x0007	INT_ACLEAR	15	INT_ACLEAR_FIFO	FIFO threshold interrupt automatic clear enable. Set this bit to enable automatic clearing of the FIFO_TH bit interrupt each time the FIFO is read.	0x1	R/W
		[14:0]	RESERVED	Reserved.	0x0	R
0x0008	CHIP_ID	[15:8]	RESERVED	Reserved.	0x0	R
		[7:0]	CHIP_ID	Chip ID.	0xC4	R
0x0009	OSC32M	[15:8]	RESERVED	Reserved.	0x0	R
		[7:0]	OSC_32M_FREQ_ADJ	High frequency oscillator frequency control. 0x00 is the lowest frequency, and 0xFF is maximum frequency.	0x80	R/W

REGISTER DETAILS

Table 21. Register Details

Reg	Name	Bits	Bit Name	Description	Reset	Access
0x000A	OSC32M_CAL	15	OSC_32M_CAL_START	Start high frequency oscillator calibration cycle. Writing a 1 to this bit causes the high frequency oscillator calibration cycle to occur. 32 MHz oscillator cycles are counted during 128 low frequency oscillator cycles if using the 1 MHz low frequency oscillator, or 4 low frequency oscillator cycles if using the 32 kHz low frequency oscillator. The OSC_32M_CAL_COUNT bits are updated with the count. The calibration circuit clears the OSC_32M_CAL_START bit when the calibration cycle is completed. Silicon Version 0 counts 32 low frequency oscillator cycles if using the 32 kHz low frequency oscillator.	0x0	R/W
		[14:0]	OSC_32M_CAL_COUNT	High frequency oscillator calibration count. These bits contain the total number of 32 MHz cycles that occurred during the last high frequency oscillator calibration cycle.	0x0	R
0x000B	OSC960K	15	CAPTURE_TIMESTAMP	Enable time stamp capture. This bit field is used to activate the time stamp capture function. When set, the next rising edge on the time stamp input (defaults to GPIO0) causes a time stamp capture. This bit is cleared when the time stamp occurs.	0x0	R/W
		[14:11]	RESERVED	Reserved.	0x0	R
		10	OSC_CAL_ENABLE	Enable clock calibration clocking. Writing a 1 to this bit enables the clocking of the low frequency and high frequency calibration circuits.	0x0	R/W
		[9:0]	OSC_960K_FREQ_ADJ	Low frequency oscillator frequency control. 0x000 is the lowest frequency, and 0x3FF is maximum frequency.	0x2B2	R/W
0x000D	TS_FREQ	[15:0]	TIMESLOT_PERIOD_L	Lower 16 bits of time slot period in low frequency oscillator cycles. The time slot rate is (timer clock frequency)/(TIMESLOT_PERIOD_x). The default value operates at 100 Hz when using the 960 kHz clock. If the timer clock is set as an external source from the GPIO, either 960 kHz or 32 kHz, TM_CLK_GPIO_SEL must be configured to match the real clock frequency.	0x2580	R/W
0x000E	TS_FREQH	[15:7]	RESERVED	Reserved.	0x0	R
		[6:0]	TIMESLOT_PERIOD_H	Upper seven bits of time slot period in low frequency oscillator cycles. The time slot rate is (timer clock frequency)/(TIMESLOT_PERIOD_x). The default value operates at 100 Hz when using the 960 kHz clock. If the timer clock is set to be an external source from the GPIO, either 960 kHz or 32 kHz, TM_CLK_GPIO_SEL must be configured to match the real clock frequency.	0x0	R/W
0x000F	SYS_CTL	15	SW_RESET	Software Reset. Write 1 to this bit to assert a software reset. This resets the chip to its default values and stops all AFE operations. The software reset does not reset the SPI (or optional I^2C) port.	0x0	R0/W
		[14:11]	RESERVED	Reserved.	0x0	R
		[10:8]	ALT_CLOCKS	External clock select. 000: use internal clocks. 001: use GPIO for low frequency oscillator (960 kHz). Timer clock also uses this as the source. 010: use GPIO for high frequency oscillator (32 MHz). 011: use GPIO for high frequency oscillator (32 MHz), and generate low frequency oscillator (1 MHz) from high frequency oscillator. This feature must be disabled when the ECG is enabled. 100: use GPIO for timer clock, 32 kHz or 960 kHz.	0x0	R/W
		[7:6]	ALT_CLK_GPIO	Alternate clock GPIO select.	0x0	R/W

REGISTER DETAILS

Table 21. Register Details

Reg	Name	Bits	Bit Name	Description	Reset	Access
				00: use GPIO0 for alternate clock. 01: use GPIO1 for alternate clock. 10: use GPIO2 for alternate clock. 11: reserved.		
		[5:3]	RESERVED	Reserved.	0x0	R
		2	TM_CLK_GPIO_SEL	Select low frequency clock between 960 kHz and 32 kHz. This bit must be used when ALT_CLOCKS is 3'b100. 0: use the 32 kHz external source from GPIO as the timer clock. 1: use the 960 kHz external source from GPIO as the low frequency clock.	0x0	R/W
		1	OSC_960K_EN	Enable low frequency oscillator. This bit turns on the 960 kHz low frequency oscillator, which must be left running during all operations using this oscillator.	0x0	R/W
		0	RESERVED	Reserved.	0x0	R
0x0010	OPMODE	15	ECG_TIMESLOT_EN	ECG time slot enable control. 0: disable ECG time slot. 1: enable ECG time slot.	0x0	R/W
		[14:12]	BIOZ_TIMESLOT_EN	BIOZ time slot enable control. 000: no BIOZ time slot. 001: BIOZ Time Slot Sequence A only. 010: BIOZ Time Slot Sequence AB. 011: BIOZ Time Slot Sequence ABC. 100: BIOZ Time Slot Sequence ABCD. 101: BIOZ Time Slot Sequence ABCDE. 110: BIOZ Time Slot Sequence ABCDEF. 111: Reserved.	0x0	R/W
		[11:8]	PPG_TIMESLOT_EN	PPG Timeslot enable control. 0000: no PPG time slot. 0001: PPG Time Slot Sequence A. 0010: PPG Time Slot Sequence AB. 0011: PPG Time Slot Sequence ABC. 0100: PPG Time Slot Sequence ABCD. 0101: PPG Time Slot Sequence ABCDE. 0110: PPG Time Slot Sequence ABCDEF. 0111: PPG Time Slot Sequence ABCDEFG. 1000: PPG Time Slot Sequence ABCDEFGH. 1001: PPG Time Slot Sequence ABCDEFGHI. 1010: PPG Time Slot Sequence ABCDEFGHIJ. 1011: PPG Time Slot Sequence ABCDEFGHIJK. 1100: PPG Time Slot Sequence ABCDEFGHIJKL.	0x0	R/W
		[7:3]	RESERVED	Reserved.	0x0	R
		[2:0]	OP_MODE	Operating mode selection. 000: standby. 001: operate selected time slots.	0x0	R/W
0x0011	STAMP_L	[15:0]	TIMESTAMP_COUNT_L	Count at last time stamp. Lower 16 bits.	0x0	R
0x0012	STAMP_H	[15:0]	TIMESTAMP_COUNT_H	Count at last time stamp. Upper 16 bits.	0x0	R
0x0013	STAMPDELTA	[15:0]	TIMESTAMP_SLOT_DELTA	Count remaining until next time slot start.	0x0	R
0x0014	INT_ENABLE_XD	15	INTX_EN_FIFO_TH	INT_FIFO_TH interrupt enable. Write a 1 to this bit to enable drive of the FIFO threshold status on Interrupt X.	0x0	R/W

REGISTER DETAILS

Table 21. Register Details

Reg	Name	Bits	Bit Name	Description	Reset	Access
		14	INTX_EN_FIFO_UFLOW	INT_FIFO_UFLOW interrupt enable for Interrupt X. Write a 1 to this bit to enable drive of the FIFO underflow status on Interrupt X.	0x0	R/W
		13	INTX_EN_FIFO_OFLOW	INTO_FIFO_OFLOW interrupt enable for Interrupt X. Write a 1 to this bit to enable drive of the FIFO overflow status on Interrupt X.	0x0	R/W
		[12:0]	RESERVED	Reserved.	0x0	R
0x0015	INT_ENABLE_YD	15	INTY_EN_FIFO_TH	INT_FIFO_TH interrupt enable. Write a 1 to this bit to enable drive of the FIFO threshold status on Interrupt Y.	0x0	R/W
		14	INTY_EN_FIFO_UFLOW	INT_FIFO_UFLOW interrupt enable for Interrupt Y. Write a 1 to this bit to enable drive of the FIFO underflow status on Interrupt Y.	0x0	R/W
		13	INTY_EN_FIFO_OFLOW	INT_FIFO_OFLOW interrupt enable for Interrupt Y. Write a 1 to this bit to enable drive of the FIFO overflow status on Interrupt Y.	0x0	R/W
		[12:0]	RESERVED	Reserved.	0x0	R
0x001E	FIFO_STATUS_BYTES	[15:10]	RESERVED	Reserved.	0x0	R
		9	ENA_STAT_ECG	Enable ECG status byte.	0x1	R/W
		8	ENA_STAT_TSX	Enable Channel 1 and Channel 2 TIA interrupt status byte, upper. This byte contains the interrupt status for the Channel 1 and Channel 2 interrupts for Time Slot I through Time Slot L.	0x0	R/W
		7	ENA_STAT_TS2	Enable Channel 2 TIA interrupt status byte, lower. This byte contains the interrupt status for the Channel 2 interrupts for Time Slot A through Time Slot H.	0x0	R/W
		6	ENA_STAT_TS1	Enable Channel 1 TIA interrupt status byte, lower. This byte contains the interrupt status for the Channel 1 interrupts for Time Slot A through Time Slot H.	0x0	R/W
		[5:0]	RESERVED	Reserved.	0x0	R
0x0020	INPUT_SLEEP	[15:8]	RESERVED	Reserved.	0x0	R
		[7:4]	INP_SLEEP_34	Input pair sleep state for IN3 and IN4 inputs. 0x0: both inputs float. 0x1: floating short of IN3 to IN4. Only if PAIR34 is set to 1. 0x2: IN3 and IN4 connected to VC1. Shorted together if PAIR34 is set to 1. 0x3: IN3 and IN4 connected to VC2. Shorted together if PAIR34 is set to 1. 0x4: IN3 connected to VC1. IN4 floating. 0x5: IN3 connected to VC1. IN4 connected to VC2. 0x6: IN3 connected to VC1. IN4 floating. 0x7: IN3 connected to VC2. IN4 connected to VC1. 0x8: IN3 floating. IN4 connected to VC1. 0x9: IN3 floating. IN4 connected to VC2.	0x0	R/W
		[3:0]	INP_SLEEP_12	Input pair sleep state for IN1 and IN2 inputs. 0x0: both inputs float. 0x1: floating short of IN1 and IN2. Only if PAIR12 is set to 1. 0x2: IN1 and IN2 connected to VC1. Shorted together if PAIR12 is set to 1. 0x3: IN1 and IN2 connected to VC2. Shorted together if PAIR12 is set to 1. 0x4: IN1 connected to VC1. IN2 floating. 0x5: IN1 connected to VC1. IN2 connected to VC2. 0x6: IN1 connected to VC2. IN2 floating.	0x0	R/W

REGISTER DETAILS

Table 21. Register Details

Reg	Name	Bits	Bit Name	Description	Reset	Access
				0x7: IN1 connected to VC2. IN2 connected to VC1. 0x8: IN1 floating. IN2 connected to VC1. 0x9: IN1 floating. IN2 connected to VC2.		
0x0021	INPUT_CFG	[15:8]	RESERVED	Reserved.	0x0	R
		[7:6]	VC2_SLEEP	VC2 sleep state. 00: VC2 set to AVDD during sleep. 01: VC2 set to GND during sleep. 10: VC2 floating during sleep.	0x0	R/W
		[5:4]	VC1_SLEEP	VC1 sleep state. 00: VC1 set to AVDD during sleep. 01: VC1 set to GND during sleep. 10: VC1 floating during sleep.	0x0	R/W
		[3:2]	RESERVED	Reserved.	0x0	R
		1	PAIR34	Input pair configuration. 0: use as two single-ended inputs. 1: use as a differential pair.	0x0	R/W
		0	PAIR12	Input pair configuration. 0: use as two single-ended inputs. 1: use as a differential pair.	0x0	R/W
0x0022	GPIO_CFG	[15:14]	GPIO_SLEW	Slew control for GPIOx pins. 00: slowest. 01: slow. 10: fastest. 11: fast.	0x0	R/W
		[13:12]	GPIO_DRV	Drive control for GPIOx pins. 00: medium. 01: weak. 10: strong. 11: strong.	0x0	R/W
		[11:9]	RESERVED	Reserved.	0x0	R/W
		[8:6]	GPIO_PIN_CFG2	GPIO2 pin configuration. 000: disabled (tristate, input buffer off). 001: enabled input. 010: output–normal. 011: output–inverted. 100: pull-down only–normal. 101: pull-down only–inverted. 110: pull-up only–normal. 111: pull-up only–inverted.	0x0	R/W
		[5:3]	GPIO_PIN_CFG1	GPIO1 pin configuration. 000: disabled (tristate, input buffer off). 001: enabled Input. 010: output–normal. 011: output–inverted. 100: pull-down only–normal. 101: pull-down only–inverted. 110: pull-up only–normal. 111: pull-up only–inverted.	0x0	R/W

REGISTER DETAILS

Table 21. Register Details

Reg	Name	Bits	Bit Name	Description	Reset	Access
		[2:0]	GPIO_PIN_CFG0	GPIO0 pin configuration. 000: disabled (tristate, input buffer off). 001: enabled input. 010: output–normal. 011: output–inverted. 100: pull-down only–normal. 101: pull-down only–inverted. 110: pull-up only–normal. 111: pull-up only–inverted.	0x0	R/W
0x0023	GPIO01	[15:8]	GPIOOUT1	GPIO1 output signal select. 0x00: Output Logic 0. 0x01: Output Logic 1. 0x02: Interrupt X. 0x03: Interrupt Y. 0x08: LED1x amplifier enable. 0x09: LED2x amplifier enable. 0x0C: any LED amplifier enable. 0x0F: 32 MHz oscillator output divided by 64 (500 kHz). 0x10: time slot specific output pattern defined by TS_GPIO_X and TS_GPIO_SLEEP bits. 0x16: low frequency oscillator output. 0x17: 32 MHz oscillator output. 0x18: 32 MHz oscillator output divided by 32 (1 MHz). 0x20: Time Slot A active. 0x21: Time Slot B active. 0x22: Time Slot C active. 0x23: Time Slot D active. 0x24: Time Slot E active. 0x25: Time Slot F active. 0x26: Time Slot G active. 0x27: Time Slot H active. 0x28: Time Slot I active. 0x29: Time Slot J active. 0x2A: Time Slot K active. 0x2B: Time Slot L active. 0x31: Time Slot A LED pulse. 0x32: Time Slot B LED pulse. 0x33: Time Slot C LED pulse. 0x34: Time Slot D LED pulse. 0x35: Time Slot E LED pulse. 0x36: Time Slot F LED pulse. 0x37: Time Slot G LED pulse. 0x38: Time Slot H LED pulse. 0x39: Time Slot I LED pulse. 0x3A: Time Slot J LED pulse. 0x3B: Time Slot K LED pulse. 0x3C: Time Slot L LED pulse. 0x3F: Time Slot x LED pulse. 0x40: Time Slot A modulation pulse.	0x0	R/W

REGISTER DETAILS

Table 21. Register Details

Reg	Name	Bits	Bit Name	Description	Reset	Access
				0x41: Time Slot B modulation pulse. 0x42: Time Slot C modulation pulse. 0x43: Time Slot D modulation pulse. 0x44: Time Slot E modulation pulse. 0x45: Time Slot F modulation pulse. 0x46: Time Slot G modulation pulse. 0x47: Time Slot H modulation pulse. 0x48: Time Slot I modulation pulse. 0x49: Time Slot J modulation pulse. 0x4A: Time Slot K modulation pulse. 0x4B: Time Slot L modulation pulse. 0x4F: Time Slot x modulation pulse. 0x50: output data cycle occurred in Time Slot A. 0x51: output data cycle occurred in Time Slot B. 0x52: output data cycle occurred in Time Slot C. 0x53: output data cycle occurred in Time Slot D. 0x54: output data cycle occurred in Time Slot E. 0x55: output data cycle occurred in Time Slot F. 0x56: output data cycle occurred in Time Slot G. 0x57: output data cycle occurred in Time Slot H. 0x58: output data cycle occurred in Time Slot I. 0x59: output data cycle occurred in Time Slot J. 0x5A: output data cycle occurred in Time Slot K. 0x5B: output data cycle occurred in Time Slot L. 0x5F: output data cycle occurred in any time slot.		
		[7:0]	GPIOOUT0	GPIO0 output signal select. Output options are identical to those described in GPIOOUT1.	0x0	R/W
0x0024	GPIO23	[15:8]	RESERVED	Reserved.	0x0	R/W
		[7:0]	GPIOOUT2	GPIO2 output signal select. Output options are identical to those described in GPIOOUT1.	0x0	R/W
0x0025	GPIO_IN	[15:4]	RESERVED	Reserved.	0x0	R
		[3:0]	GPIO_INPUT	GPIO input value (if enabled).	0x0	R
0x0026	GPIO_EXT	[15:9]	RESERVED	Reserved.	0x0	R
		8	GOUT_SLEEP	Time slot specific GPIO signal sleep value.	0x0	R/W
		7	TIMESTAMP_INV	Time stamp trigger invert. 0: time stamp trigger is rising edge. 1: time stamp trigger is falling edge.	0x0	R/W
		6	TIMESTAMP_ALWAYS_EN	Enable time stamp always on. When set, do not automatically clear TIMESTAMP_CAPTURE. This bit provides an always activated time stamp.	0x0	R/W
		[5:4]	TIMESTAMP_GPIO	Timestamp GPIO select. 00: use GPIO0 for time stamp (default). 01: use GPIO1 for time stamp. 10: use GPIO2 for time stamp.	0x0	R/W
		3	RESERVED	Reserved.	0x0	R
		2	EXT_SYNC_EN	External sync enable. When enabled, use the GPIO selected by EXT_SYNC_GPIO to trigger samples rather than the period counter.	0x0	R/W
		[1:0]	EXT_SYNC_GPIO	External sync GPIO select.	0x0	R/W

REGISTER DETAILS

Table 21. Register Details

Reg	Name	Bits	Bit Name	Description	Reset	Access
				00: use GPIO0 for external sync (default). 01: use GPIO1 for external sync. 10: use GPIO2 for external sync.		
0x002F	FIFO_DATA	[15:0]	FIFO_DATA	FIFO data port.	0x0	R
0x0046	ADC_CONTROL	[15:14]	RESERVED	Reserved.	0x0	R
		13	ECG_ADC_CTRL	Must write 1.	0x1	R/W
		[12:3]	RESERVED	Reserved.	0x0	R
		2	PPG_ADC_CTRL1	Must write 1.	0x1	R/W
		[1:0]	PPG_ADC_CTRL2	Set to 0x0 when PPG is enabled for better ambient rejection.	0x3	R/W
0x004C	GLOBAL_BIAS_CONTROL	[15]	RESERVED	Reserved.	0x0	R
		14	TIA_DETECT_CTRL	Must write 1.	0x1	R/W
		[13:4]	RESERVED	Reserved.	0x0	R
		[3:0]	GLOBAL_BIAS_TRIM	Set to 0xB for lower global current bias.	0x0	R/W
0x0057	IO_ADJUST	[15:7]	RESERVED	Reserved.	0x0	R
		6	LOW_IOVDD_EN	Set to 0x0 if IOVDD of 3 V or higher is used. Default value of 0x1 is used for IOVDD lower than 3 V, because the typical value of IOVDD is 1.8 V.	0x1	R/W
		[5:4]	RESERVED	Reserved.	0x1	R/W
		[3:2]	SPI_SLEW	Slew control for SPI pins. 00: slowest. 01: slow. 10: fastest. 11: fast.	0x0	R/W
		[1:0]	SPI_DRV	Drive control for SPI pins. 00: medium. 01: weak. 10: strong. 11: strong.	0x0	R/W
0x005B	PPG_TIA_CONTROL	[15:12]	RESERVED	Reserved.	0x0	R
		[11:10]	TIA_DETECT_CTRL	Set to 0x3 when PPG is enabled for better ambient rejection.	0x0	R/W
		[9:7]	RESERVED	Reserved.	0x0	R
		[6:0]	TIA_MODE	Must write 0x20.	0x20	R/W
0x0074	ECG_ACLO_CONTROL	[15:11]	RESERVED	Reserved.	0x0	R
		[10:0]	ECG_ACLO_LPF_COEF	Set to 0x28 when ECG is enabled.	0x50	R/W
0x0077	ECG_PGA_CONTROL	[15:9]	RESERVED	Reserved.	0x0	R
		8	ECG_PGA_CTRL	Set to 0x1 when ECG is enabled for power optimization.	0x0	R/W
		[7:0]	RESERVED	Reserved.	0x0	R
0x0078	ECG_INPUT_CONTROL	15	ECG_INPUT_BUF_EN	Set to 0x1 to enable the ECG input buffer.	0x0	R/W
		[14:12]	RESERVED	Reserved.	0x0	R
		11	ECG_INPUT_BUF_CTRL	Set to 0x1 when ECG input buffer is enabled.	0x0	R/W
		[10:0]	RESERVED	Reserved.	0x0	R
0x0100	ECG_ANA_CTRL	[15:11]	RESERVED	Reserved.	0x0	R
		10	ECG_INP_CONNECT	ECG input connection. Set 1 to connect the ECG inputs.	0x1	R/W
		9	ECG_SHORT	ECG short switches. When set 1, the ECG_SHORT bits internally short the inputs of ECG. The feature can be used for ECG noise measurements.	0x0	R/W
		8	ECG_CHAN_RESOLUTION	Select ECG channel resolution.	0x0	R
				0: 288 nV/LSB.		

REGISTER DETAILS

Table 21. Register Details

Reg	Name	Bits	Bit Name	Description	Reset	Access
				1: 576 nV/LSB		
		7	RESERVED	Reserved.	0x0	R
		6	ECG_RLD_OUT_DISCONNECT	Disconnect the RLD output for test mode.	0x0	R/W
		[5:4]	ECG_RLD_OUT_SEL	Select the RLD output. 00: AGND. 01: AVDD3 10: AVDD3/2. 11: Regulated common-mode input.	0x3	R/W
		3	ECG_RLD_SAT_EN	Enable dc lead off for the RLD pin. 0: dc lead off for RLD is disabled. 1: dc lead off for RLD is enabled.	0x0	R/W
		[2:1]	ECG_RLD_SAT_THRESHOLD	DC lead off threshold selection for the RLD. 00: high threshold = AVDD3 − 0.1 V, low threshold = 0.1 V. 01: high threshold = AVDD3 − 0.2 V, low threshold = 0.2 V. 10: high threshold = AVDD3 − 0.3 V, low threshold = 0.3 V. 11: high threshold = AVDD3 − 0.4 V, low threshold = 0.4 V.	0x0	R/W
		0	ECG_RLD_EN	Enable the RLD circuit.	0x0	R/W
0x0101	ECG_LEADOFF_CTRL	15	ECG_ACLO_EN	Enable the AC lead off detector for the ECG inputs.	0x0	R/W
		[14:12]	ECG_ACLO_MAG	AC lead off excite current magnitude. 000: 0 nA. 001: 10 nA. 010: 20 nA. 011: 30 nA. 100: 40 nA. 101: 50 nA. 110: 60 nA. 111: 70 nA.	0x0	R/W
		[11:9]	ECG_ACLO_THRESHOLD	AC lead off threshold selection for the ECG inputs.	0x0	R/W
		8	ECG_DCLO_EN	Enable the dc lead off detector for the ECG inputs.	0x0	R/W
		[7:4]	ECG_DCLO_MAG	DC lead off excite current magnitude. 0000: 0 nA. 0001: Reserved. 0010: Reserved. 0011: Reserved. 0100: Reserved. 0101: Reserved. 0110: Reserved. 0111: Reserved. 1000: 2 nA. 1001: 4 nA. 1010: 6 nA. 1011: 8 nA. 1100: 10 nA. 1101: 12 nA. 1110: 14 nA. 1111: 16 nA.	0x0	R/W
		3	ECG_DCLO_POLARITY_IN	DC lead off output current polarity at ECGIN. 0: sink current.	0x0	R/W

REGISTER DETAILS

Table 21. Register Details

Reg	Name	Bits	Bit Name	Description	Reset	Access
				1: source current.		
		2	ECG_DCLO_POLARITY_IP	DC lead off output current polarity at ECGIP. 0: sink current. 1: source current.	0x1	R/W
		[1:0]	ECG_DCLO_THRESHOLD	DC lead off threshold selection for the ECG inputs. 00: high threshold = AVDD3 − 0.1 V. 01: high threshold = AVDD3 − 0.2 V. 10: high threshold = AVDD3 − 0.3 V. 11: high threshold = AVDD3 − 0.4 V.	0x0	R/W
0x0102	ECG_DIG_CTRL1	[15:9]	RESERVED	Reserved.	0x0	R
		[8:3]	ECG_OVERSAMPLING_RATIO	This field must be configured as ratio = ECG_ODR_SEL/(960 kHz/TIMESLOT_PERIOD_x) if using an internal low frequency oscillator, or ratio = ECG_ODR_SEL/(external sync rate) if using external triggers. The result is rounded up to the nearest integer.	0x3	R/W
		[2:0]	ECG_ODR_SEL	ECG ODR. 000: 250 Ω. 001: 500 Ω. 010: 1 kΩ. 011: 2 kΩ. 100: 4 kΩ.	0x0	R/W
0x0103	ECG_DIG_CTRL2	[15:6]	RESERVED	Reserved.	0x0	R
		5	ECG_ACLO_INV	The polarity of the ACLO signal can be inverted, and this can be used to have the signal inverted on every other channel. When set (1), ACLO is inverted, when cleared (0), ACLO is not inverted.	0x0	R/W
		4	ECG_BYPASS_EQLZR	Bypass equalizer filter in ECG postprocessing path.	0x0	R/W
		[3:0]	ECG_CAL_GAIN	Calibrated gain ECG. 0000: 1.0000. 0001: 1.0039. 0010: 1.0078. 0011: 1.0117. 0100: 1.0156. 0101: 1.0195. 0110: 1.0234. 0111: 1.0273. 1000: 0.9688. 1001: 0.9727. 1010: 0.9766. 1011: 0.9805. 1100: 0.9844. 1101: 0.9883. 1110: 0.9922. 1111: 0.9961.	0x0	R/W
0x0120	TS_CTRL_A	15	SUBSAMPLE_x	Subsample using DECIMATE_FACTOR_x. When this bit is set, operate the time slot only once per (DECIMATE_FACTOR_X + 1) time slot sequences. This subsampling aligns to other time slots using the same decimate factor. Subsampling skips DECMATE_FACTOR_x times and then executes the time slot.	0x0	R/W
0x0140 0x0160	TS_CTRL_B TS_CTRL_C	14	CH2_EN_x	Channel 2 enable. 0: Channel 2 disabled.	0x0	R/W

REGISTER DETAILS

Table 21. Register Details

Reg	Name	Bits	Bit Name	Description	Reset	Access
0x0180	TS_CTRL_D			1: Channel 2 enabled.		
0x01A0	TS_CTRL_E	[13:11]	SAMPLE_TYPE_x	Time slot sampling type.	0x0	R/W
0x01C0	TS_CTRL_F			000: normal sampling mode.		
0x01E0	TS_CTRL_G			001: two phase normal sampling mode.		
0x0200	TS_CTRL_H			010: on-region digital integrate mode.		
0x0220	TS_CTRL_I			011: two-region digital integrate mode.		
0x0240	TS_CTRL_J			100: reserved		
0x0260	TS_CTRL_K			101: reserved.		
0x0280	TS_CTRL_L			110: reserved.		
				111: reserved.		
		10	RESERVED	Reserved	0x0	R/W
		[9:0]	TIMESLOT_OFFSET_x	Time Slot X offset in 64 × 960 kHz or 64 × (external 960 kHz) cycles.	0x0	R/W
0x0121	TS_PATH_A	[15:12]	PRE_WIDTH_x	Precondition duration for this time slot. This value is in 2 µs increments. A value of 0 skips the precondition state.	0x4	R/W
0x0141	TS_PATH_B	[11:10]	AMBIENT_CANCELLATION_x	Select the control type for the ambient cancellation DAC.	0x0	R/W
0x0161	TS_PATH_C			00: disable the ambient cancellation loop.		
0x0181	TS_PATH_D			01: enable coarse and fine loop.		
0x01A1	TS_PATH_E			10: enable coarse loop only.		
0x01C1	TS_PATH_F			11: enable MCU control.		
0x01E1	TS_PATH_G	9	TS_GPIO_x	Timeslot specific GPIO value for this time slot.	0x0	R/W
0x0201	TS_PATH_H	8	AFE_INT_C_BUF_x	Convert integrator to buffer.	0x0	R/W
0x0221	TS_PATH_I	7	RESERVED	Reserved.	0x0	R
0x0241	TS_PATH_J	[6:0]	AFE_PATH_CFG_x	Bypass and input mux select. Integrator is either an integrator or buffer based on mode and AFE_INT_C_BUF for the active time slot.	0x20	R/W
0x0261	TS_PATH_K			0x20: TIA, integrator/buffer, and ADC (2× TIA configuration).		
0x0281	TS_PATH_L			0x28: TIA, buffer, and ADC (1× TIA configuration).		
				0x31: TIA, integrator, and ADC (1× TIA configuration).		
				0x35: integrator and ADC.		
				0x41: ADC.		
0x0122	INPUTS_A	[15:8]	RESERVED	Reserved.	0x0	R
0x0142	INPUTS_B	[7:4]	INP34_x	IN3 and IN4 input pair enable.	0x0	R/W
0x0162	INPUTS_C			0000: input pair disabled. IN3 and IN4 disconnected.		
0x0182	INPUTS_D			0001: IN3 connected to Channel 1. IN4 disconnected.		
0x01A2	INPUTS_E			0010: IN3 connected to Channel 2. IN4 disconnected.		
0x01C2	INPUTS_F			0011: IN4 connected to Channel 1. IN3 disconnected.		
0x01E2	INPUTS_G			0100: IN4 connected to Channel 2. IN3 disconnected.		
0x0202	INPUTS_H			0101: IN3 connected to Channel 1. IN4 connected to Channel 2.		
0x0222	INPUTS_I			0110: IN4 connected to Channel 1. IN3 connected to Channel 2.		
0x0242	INPUTS_J			0111: IN3 and IN4 connected to Channel 1. Single-ended or differential, based on PAIR34. None to channel 2.		
0x0262	INPUTS_K			1000: IN3 and IN4 connected to Channel 2. Single-ended or differential, based on PAIR34.		
0x0282	INPUTS_L	[3:0]	INP12_x	IN1 and IN2 input pair enable.	0x0	R/W
				0000: input pair disabled. IN1 and IN2 disconnected.		
				0001: IN1 connected to Channel 1. IN2 disconnected.		
				0010: IN1 connected to Channel 2. IN2 disconnected.		
				0011: IN2 connected to Channel 1. IN1 disconnected.		

REGISTER DETAILS

Table 21. Register Details

Reg	Name	Bits	Bit Name	Description	Reset	Access
				0100: IN2 connected to Channel 2. IN1 disconnected. 0101: IN1 connected to Channel 1. IN2 connected to Channel 2. 0110: IN2 connected to Channel 1. IN1 connected to Channel 2. 0111: IN1 and IN2 connected to Channel 1. Single-ended or differential, based on PAIR12. 1000: IN1 and IN2 connected to Channel 2. Single-ended or differential, based on PAIR12.		
0x0123	CATHODE_A	15	RESERVED	Reserved.	0x0	R
0x0143 0x0163 0x0183 0x01A3 0x01C3 0x01E3 0x0203 0x0223	CATHODE_B CATHODE_C CATHODE_D CATHODE_E CATHODE_F CATHODE_G CATHODE_H CATHODE_I	[14:12]	PRECON_x	Precondition value for enabled inputs during this time slot. 000: float inputs. 001: precondition to VC1. 010: precondition to VC2. 011: precondition to V_{ICM}. 100: precondition with TIA input. 101: precondition with TIA_V_{REF}. 110: Precondition by shorting differential pair.	0x0	R/W
0x0243 0x0263 0x0283	CATHODE_J CATHODE_K CATHODE_L	[11:10]	VC2_PULSE_x	VC2 pulse control. 00: no pulsing. 01: alternate odd/even time slots. 10: pulse to alternate value using modulate pulse. 11: leave VC2 floating.	0x0	R/W
		[9:8]	VC2_ALT_x	VC2 alternate pulsed state for this time slot. 00: AVDD. 01: TIA_V_{REF}. 10: TIA_V_{REF} + 215 mV (V_DELTA). 11: GND.	0x0	R/W
		[7:6]	VC2_SEL_x	VC2 active state for this time slot. 00: AVDD. 01: TIA_V_{REF}. 10: V_DELTA. 11: GND.	0x0	R/W
		[5:4]	VC1_PULSE_x	VC1 pulse control. 00: no pulsing. 01: alternate odd/even times lots. 10: pulse to alternate value using modulate pulse. 11: leave VC1 floating.	0x0	R/W
		[3:2]	VC1_ALT_x	VC1 alternate pulsed state for Time Slot x. 00: AVDD. 01: TIA_V_{REF}. 10: V_DELTA. 11: GND.	0x0	R/W
		[1:0]	VC1_SEL_x	VC1 active state for Time Slot x. 00: AVDD. 01: TIA_V_{REF}. 10: V_DELTA. 11: GND.	0x0	R/W
0x0124	AFE_TRIM1_A	15	TIA_CEIL_DETECT_EN_x	Enable TIA saturation detection. Set to 1 to enable TIA saturation detection circuitry. Enables Channel 1 and also Channel 2 if Channel 2 is enabled.	0x0	R/W

REGISTER DETAILS

Table 21. Register Details

Reg	Name	Bits	Bit Name	Description	Reset	Access
0x0144	AFE_TRIM1_B	[14:13]	CH2_TRIM_INT_x	Channel 2 integrator resistor or buffer gain. 00: R_{IN} = 400 kΩ or buffer gain = 1 (R_F/R_{IN} = 200 kΩ/200 kΩ). 01: R_{IN} = 200 kΩ or buffer gain = 2 (R_F/R_{IN} = 200 kΩ/100 kΩ). 10: R_{IN} = 100 kΩ or buffer gain = 1 (R_F/R_{IN} = 100 kΩ/100 kΩ). 11: R_{IN} = 50 kΩ or buffer gain = 2 (R_F/R_{IN} = 100 kΩ/50 kΩ).	0x0	R/W
0x0164	AFE_TRIM1_C					
0x0184	AFE_TRIM1_D					
0x01A4	AFE_TRIM1_E					
0x01C4	AFE_TRIM1_F					
0x01E4	AFE_TRIM1_G	[12:11]	CH1_TRIM_INT_x	Channel 1 integrator resistor or buffer gain. 00: R_{IN} = 400 kΩ or buffer gain = 1 (R_F/R_{IN} = 200 kΩ/200 kΩ). 01: R_{IN} = 200 kΩ or buffer gain = 2 (R_F/R_{IN} = 200 kΩ/100 kΩ). 10: R_{IN} = 100 kΩ or buffer gain = 1 (R_F/R_{IN} = 100 kΩ/100 kΩ). 11: R_{IN} = 50 kΩ or buffer gain = 2 (R_F/R_{IN} = 100 kΩ/50 kΩ).	0x0	R/W
0x0204	AFE_TRIM1_H					
0x0224	AFE_TRIM1_I					
0x0244	AFE_TRIM1_J					
0x0264	AFE_TRIM1_K					
0x0284	AFE_TRIM1_L	10	VREF_PULSE_x	TIA_V_{REF} pulse control. 0: no pulsing. 1: pulse TIA_V_{REF} based on modulate pulse.	0x0	R/W
		[9:8]	AFE_TRIM_VREF_x	Voltage trim for ref buffer. 00: TIA_V_{REF} = 0.8855 V, P_D reverse bias = 600 mV. 01: TIA_V_{REF} = 0.8855 V, P_D reverse bias = 400 mV 10: TIA_V_{REF} = 0.8855 V, P_D reverse bias = 200 mV 11: TIA_V_{REF} = 1.265 V, P_D reverse bias = 200 mV	0x2	R/W
		[7:6]	VREF_PULSE_VAL_x	TIA_V_{REF} pulse alternate value. 00: modulate TIA_V_{REF} = 0.8855 V, P_D reverse bias = 600 mV. 01: modulate TIA_V_{REF} = 0.8855 V, P_D reverse bias = 400 mV. 10: modulate TIA_V_{REF} = 0.8855 V, P_D reverse bias = 200 mV. 11: modulate TIA_V_{REF} = 1.265 V, P_D reverse bias = 200 mV.	0x3	R/W
		[5:3]	TIA_GAIN_CH2_x	TIA resistor gain setting for Channel 2. 000: 400 kΩ. 001: 200 kΩ. 010: 100 kΩ. 011: 50 kΩ. 100: 25 kΩ. 101: 12.5 kΩ.	0x1	R/W
		[2:0]	TIA_GAIN_CH1_x	TIA resistor gain setting for Channel 1. 000: 400 kΩ. 001: 200 kΩ. 010: 100 kΩ. 011: 50 kΩ. 100: 25 kΩ. 101: 12.5 kΩ.	0x1	R/W
0x0125	AFE_TRIM2_A	[15:14]	RESERVED	Reserved.	0x0	R
0x0145	AFE_TRIM2_B	13	CH2_TRIM_INT_CAP_x	Channel2 integrator capacitor. 0: 6.3 pF. 1: 12.6 pF.	0x0	R/W
0x0165	AFE_TRIM2_C					
0x0185	AFE_TRIM2_D					
0x01A5	AFE_TRIM2_E	12	CH1_TRIM_INT_CAP_x	Channel1 integrator capacitor. 0: 6.3 pF. 1: 12.6 pF.	0x0	R/W
0x01C5	AFE_TRIM2_F					
0x01E5	AFE_TRIM2_G					
0x0205	AFE_TRIM2_H	[11:0]	RESERVED	Reserved.	0x0	R
0x0225	AFE_TRIM2_I					
0x0245	AFE_TRIM2_J					
0x0265	AFE_TRIM2_K					

REGISTER DETAILS

Table 21. Register Details

Reg	Name	Bits	Bit Name	Description	Reset	Access
0x0285	AFE_TRIM2_L					
0x0126	AFE_DAC1_A	[15:7]	DAC_AMBIENT_CH1_x	Channel 1 ambient cancellation DAC code from 0 µA to 300 µA with 0.6 µA/LSB step.	0x0	R/W
0x0146	AFE_DAC1_B	[6:0]	DAC_LED_DC_CH1_x	Channel 1 LED dc offset cancellation DAC code from 0 µA to 190 µA with 1.5 µA/LSB step. Set to 0 to disable.	0x0	R/W
0x0166	AFE_DAC1_C					
0x0186	AFE_DAC1_D					
0x01A6	AFE_DAC1_E					
0x01C6	AFE_DAC1_F					
0x01E6	AFE_DAC1_G					
0x0206	AFE_DAC1_H					
0x0226	AFE_DAC1_I					
0x0246	AFE_DAC1_J					
0x0266	AFE_DAC1_K					
0x0286	AFE_DAC1_L					
0x0127	AFE_DAC2_A	[15:7]	DAC_AMBIENT_CH2_x	Channel 2 ambient cancellation DAC code from 0 µA to 300 µA with 0.6 µA/LSB step.	0x0	R/W
0x0147	AFE_DAC2_B	[6:0]	DAC_LED_DC_CH2_x	Channel 2 LED dc offset cancellation DAC code from 0 µA to 190 µA with 1.5 µA/LSB step. Set to 0 to disable.	0x0	R/W
0x0167	AFE_DAC2_C					
0x0187	AFE_DAC2_D					
0x01A7	AFE_DAC2_E					
0x01C7	AFE_DAC2_F					
0x01E7	AFE_DAC2_G					
0x0207	AFE_DAC2_H					
0x0227	AFE_DAC2_I					
0x0247	AFE_DAC2_J					
0x0267	AFE_DAC2_L					
0x0287	AFE_DAC2_L					
0x0128	LED_POW12_A	15	LED_DRIVESIDE2_x	LED output select for LED2x. 0: drive LED on Output LED2A. 1: drive LED on Output LED2B.	0x0	R/W
0x0148	LED_POW12_B					
0x0168	LED_POW12_C					
0x0188	LED_POW12_D	[14:8]	LED_CURRENT2_x	LED current setting for LED2A or LED2B output. Set to 0 to disable. Output current varies monotonically from 1.57 mA to 200 mA for values between 0x01 and 0x7F.	0x0	R/W
0x01A8	LED_POW12_E	7	LED_DRIVESIDE1_x	LED output select for LED1x. 0: drive LED on Output LED1A. 1: drive LED on Output LED2B.	0x0	R/W
0x01C8	LED_POW12_F					
0x01E8	LED_POW12_G					
0x0208	LED_POW12_H	[6:0]	LED_CURRENT1_x	LED current setting for LED1A or LED1B output. Set to 0 to disable. Output current varies monotonically from 1.57 mA to 200 mA for values between 0x01 and 0x7F.	0x0	R/W
0x0228	LED_POW12_I					
0x0248	LED_POW12_J					
0x0268	LED_POW12_K					
0x0288	LED_POW12_L					
0x0129	LED_MODE_A	[15:2]	RESERVED	Reserved.	0x0	R
0x0149	LED_MODE_B	1	LED_MODE2_x	Choose the operation mode of LED2x. 0: high SNR mode. 1: low compliance mode.	0x0	R/W
0x0169	LED_MODE_C					
0x0189	LED_MODE_D					

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Table 21. Register Details

Reg	Name	Bits	Bit Name	Description	Reset	Access
0x01A9 0x01C9 0x01E9 0x0209 0x0229 0x0249 0x0269 0x0289	LED_MODE_E LED_MODE_F LED_MODE_G LED_MODE_H LED_MODE_I LED_MODE_J LED_MODE_K LED_MODE_L	0	LED_MODE1_x	Choose the operation mode of LED1x 0: high SNR mode.	0x0	R/W
0x012A	COUNTS_A	[15:8]	NUM_INT_x	Number of ADC cycles or acquisition width. Number of analog integration cycles per ADC conversion or the acquisition width for digital integration. A setting of 0 is not allowed.	0x1	R/W
0x014A 0x016A 0x018A 0x01AA 0x01CA 0x01EA 0x020A 0x022A 0x024A 0x026A 0x028A	COUNTS_B COUNTS_C COUNTS_D COUNTS_E COUNTS_F COUNTS_G COUNTS_H COUNTS_I COUNTS_J COUNTS_K COUNTS_L	[7:0]	NUM_REPEAT_x	Number of sequence repeats. Total number of pulses = NUM_INT_x × NUM_REPEAT_x. A setting of 0 is not allowed.	0x1	R/W
0x012B	PERIOD_A	15	RESERVED	Reserved.	0x0	R
0x014B 0x016B 0x018B	PERIOD_B PERIOD_C PERIOD_D	14	RESERVED	Reserved	0x0	R/W
0x01AB 0x01CB 0x01EB 0x020B	PERIOD_E PERIOD_F PERIOD_G PERIOD_H	[13:12]	MOD_TYPE_x	Modulation connection type. 00: TIA is continuously connected to input after precondition. No connection modulation. 01: float type operation. Pulse connection from input to TIA with modulate pulse, floating between pulses. 10: nonfloat type connection modulation. Pulse connection from input to TIA. Connect to precondition value between pulses.	0x0	R/W
0x022B	PERIOD_I	[11:10]	RESERVED	Reserved.	0x0	R
0x024B 0x026B 0x028B	PERIOD_J PERIOD_K PERIOD_L	[9:0]	MIN_PERIOD_x	Minimum period for pulse repetition. Override for the automatically calculated period. Used in float type operations to set the floating time of second and subsequent floats using the following formula: *Float Time = MIN_PERIOD_x − MOD_WIDTH_x*.	0x0	R/W
0x012C	LED_PULSE1_A	[15:8]	LED_WIDTH_x	LED pulse width.	0x2	R/W
0x014C 0x016C 0x018C 0x01AC 0x01CC 0x01EC 0x020C	LED_PULSE1_B LED_PULSE1_C LED_PULSE1_D LED_PULSE1_E LED_PULSE1_F LED_PULSE1_G LED_PULSE1_H	[7:0]	LED_OFFSET_x	LED pulse offset.	0x10	R/W

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Table 21. Register Details

Reg	Name	Bits	Bit Name	Description	Reset	Access
0x022C	LED_PULSE1_I					
0x024C	LED_PULSE1_J					
0x026C	LED_PULSE1_K					
0x028C	LED_PULSE1_L					
0x12D	LED_PULSE2_A	[15:8]	RESERVED	Reserved.	0x0	R
0x014D	LED_PULSE2_B	[7:0]	LED_SECOND_OFFSET_x	LED pulse offset for the second LED phase.	0x13	R/W
0x016D	LED_PULSE2_C					
0x018D	LED_PULSE2_D					
0x01AD	LED_PULSE2_E					
0x01CD	LED_PULSE2_F					
0x01ED	LED_PULSE2_G					
0x020D	LED_PULSE2_H					
0x022D	LED_PULSE2_I					
0x024D	LED_PULSE2_J					
0x026D	LED_PULSE2_K					
0x028D	LED_PULSE2_L					
0x012E	INTEG_WIDTH_A	15	SINGLE_INTEG_x	Use single integrator pulse. 0: use both generated integrator clocks. 1: skip the second integrator clock.	0x0	R/W
0x014E	INTEG_WIDTH_B					
0x016E	INTEG_WIDTH_C					
0x018E	INTEG_WIDTH_D	[14:13]	RESERVED	Reserved.	0x0	R
0x01AE	INTEG_WIDTH_E	[12:11]	CH2_AMP_DISABLE_x	Amplifier disables for power control. Set the appropriate bit to disable the Channel 2 amplifier in Time Slot x. 0: TIA. 1: integrator.	0x0	R/W
0x01CE	INTEG_WIDTH_F	[10:9]	RESERVED	Reserved.	0x0	R
0x01EE	INTEG_WIDTH_G	[8:7]	CH1_AMP_DISABLE_x	Amplifier disables for power control. Set the appropriate bit to disable the Channel 1 amplifier in Time Slot x. 0: TIA. 1: integrator.	0x0	R/W
0x020E	INTEG_WIDTH_H	[6:5]	ADC_COUNT_x	ADC conversions per pulse. Number of conversions = ADC_COUNT + 1.	0x0	R/W
0x022E	INTEG_WIDTH_I	[4:0]	INTEG_WIDTH_x	Integrator clock width.	0x3	R/W
0x024E	INTEG_WIDTH_J					
0x026E	INTEG_WIDTH_K					
0x028E	INTEG_WIDTH_L					
0x012F	INTEG_OFFSET_A	[15:13]	RESERVED	Reserved.	0x0	R
0x014F	INTEG_OFFSET_B	[12:5]	INTEG_OFFSET_x	Integrator clock coarse offset.	0xD	R/W
0x016F	INTEG_OFFSET_C	[4:0]	INTEG_FINE_OFFSET_x	Integrator clock fine offset.	0x0	R/W
0x018F	INTEG_OFFSET_D					
0x01AF	INTEG_OFFSET_E					
0x01CF	INTEG_OFFSET_F					
0x01EF	INTEG_OFFSET_G					
0x020F	INTEG_OFFSET_H					
0x022F	INTEG_OFFSET_I					
0x024F	INTEG_OFFSET_J					
0x026F	INTEG_OFFSET_K					
0x028F	INTEG_OFFSET_L					
0x130	MOD_PULSE_A	[15:8]	MOD_WIDTH_x	Modulation pulse width. 0 = disable.	0x0	R/W

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Table 21. Register Details

Reg	Name	Bits	Bit Name	Description	Reset	Access
0x0150	MOD_PULSE_B	[7:0]	MOD_OFFSET_x	Modulation pulse offset.	0x1	R/W
0x0170	MOD_PULSE_C					
0x0190	MOD_PULSE_D					
0x01B0	MOD_PULSE_E					
0x01D0	MOD_PULSE_F					
0x01F0	MOD_PULSE_G					
0x0210	MOD_PULSE_H					
0x0230	MOD_PULSE_I					
0x0250	MOD_PULSE_J					
0x0270	MOD_PULSE_K					
0x0290	MOD_PULSE_L					
0x0131	PATTERN1_A	[15:12]	LED_DISABLE_x	Four-pulse LED disable pattern. Set to 1 to disable the LED pulse in the matching position in a group of four pulses. The LSB maps to the first pulse.	0x0	R/W
0x0151	PATTERN1_B	[11:8]	MOD_DISABLE_x	Four-pulse modulation disable pattern. Set to 1 to disable the modulation pulse in the matching position in a group of four pulses. The LSB maps to the first pulse.	0x0	R/W
0x0171	PATTERN1_C	[7:4]	SUBTRACT_x	Four-pulse subtract pattern. Set to 1 to negate the math operation in the matching position in a group of four pulses. The LSB maps to the first pulse.	0x0	R/W
0x0191	PATTERN1_D	[3:0]	REVERSE_INTEG_x	Four-pulse integration reverse pattern. Set to 1 to reverse the integrator pos/neg pulse order in the matching position in a group of four pulses. The LSB maps to the first pulse.	0x0	R/W
0x01B1	PATTERN1_E					
0x01D1	PATTERN1_F					
0x01F1	PATTERN1_G					
0x0211	PATTERN1_H					
0x0231	PATTERN1_I					
0x0251	PATTERN1_J					
0x0271	PATTERN1_K					
0x0291	PATTERN1_L					
0x0133	ADC_OFF1_A	[15:14]	RESERVED	Reserved.	0x0	R
0x0153	ADC_OFF1_B	[13:0]	CH1_ADC_ADJUST_x	Adjustment to ADC value. This value is subtracted from the ADC value for Channel 1.	0x0	R/W
0x0173	ADC_OFF1_C					
0x0193	ADC_OFF1_D					
0x01B3	ADC_OFF1_E					
0x01D3	ADC_OFF1_F					
0x01F3	ADC_OFF1_G					
0x0213	ADC_OFF1_H					
0x0233	ADC_OFF1_I					
0x0253	ADC_OFF1_J					
0x0273	ADC_OFF1_K					
0x0293	ADC_OFF1_L					
0x0134	ADC_OFF2_A	[15:14]	RESERVED	Reserved.	0x0	R/W
0x0154	ADC_OFF2_B	[13:0]	CH2_ADC_ADJUST_x	Adjustment to ADC value. This value is subtracted from the ADC value for Channel 2.	0x0	R/W
0x0174	ADC_OFF2_C					
0x0194	ADC_OFF2_D					
0x01B4	ADC_OFF2_E					

REGISTER DETAILS

Table 21. Register Details

Reg	Name	Bits	Bit Name	Description	Reset	Access
0x01D4	ADC_OFF2_F					
0x01F4	ADC_OFF2_G					
0x0214	ADC_OFF2_H					
0x0234	ADC_OFF2_I					
0x0254	ADC_OFF2_J					
0x0274	ADC_OFF2_K					
0x0294	ADC_OFF2_L					
0x0135	DATA1_A	[15:11]	DARK_SHIFT_x	Dark data shift.	0x0	R/W
0x0155	DATA1_B	[10:8]	DARK_SIZE_x	Dark data size.	0x0	R/W
0x0175	DATA1_C	[7:3]	SIGNAL_SHIFT_x	Signal data shift.	0x0	R/W
0x0195	DATA1_D	[2:0]	SIGNAL_SIZE_x	Signal data size.	0x3	R/W
0x01B5	DATA1_E					
0x01D5	DATA1_F					
0x01F5	DATA1_G					
0x0215	DATA1_H					
0x0235	DATA1_I					
0x0255	DATA1_J					
0x0275	DATA1_K					
0x0295	DATA1_L					
0x0136	DATA2_A	[15:8]	RESERVED	Reserved.	0x0	R
0x0156	DATA2_B	[7:3]	LIT_SHIFT_x	Lit data shift.	0x0	R/W
0x0176	DATA2_C	[2:0]	LIT_SIZE_x	Lit data size.	0x0	R/W
0x0196	DATA2_D					
0x01B6	DATA2_E					
0x01D6	DATA2_F					
0x01F6	DATA2_G					
0x0216	DATA2_H					
0x0236	DATA2_I					
0x0256	DATA2_J					
0x0276	DATA2_K					
0x0296	DATA2_L					
0x0137	DECIMATE_A	[15:11]	RESERVED	Reserved.	0x0	R
0x0157	DECIMATE_B	[10:4]	DECIMATE_FACTOR_x	Decimate sample divider. Output data rate is sample rate/ (DECIMATE_FACTOR_x + 1).	0x0	R/W
0x0177	DECIMATE_C	[3:0]	RESERVED	Reserved.	0x0	R
0x0197	DECIMATE_D					
0x01B7	DECIMATE_E					
0x01D7	DECIMATE_F					
0x01F7	DECIMATE_G					
0x0217	DECIMATE_H					
0x0237	DECIMATE_I					
0x0257	DECIMATE_J					
0x0277	DECIMATE_K					
0x0297	DECIMATE_L					
0x0138	DIGINT_LIT_A	[15:9]	RESERVED	Reserved.	0x0	R
0x0158	DIGINT_LIT_B	[8:0]	LIT_OFFSET_x	Acquisition window lit offset for Time Slot x.	0x26	R/W
0x0178	DIGINT_LIT_C					
0x0198	DIGINT_LIT_D					

REGISTER DETAILS

Table 21. Register Details

Reg	Name	Bits	Bit Name	Description	Reset	Access
0x01B8	DIGINT_LIT_E					
0x01D8	DIGINT_LIT_F					
0x01F8	DIGINT_LIT_G					
0x0218	DIGINT_LIT_H					
0x0238	DIGINT_LIT_I					
0x0258	DIGINT_LIT_J					
0x0278	DIGINT_LIT_K					
0x0298	DIGINT_LIT_L					
0x0139	DIGINT_DARK_A	[15:7]	DARK2_OFFSET_x	Acquisition window Dark Offset 2 for Time Slot x.	0x1	R/W
0x0159	DIGINT_DARK_B	[6:0]	DARK1_OFFSET_x	Acquisition window Dark Offset 1 for Time Slot x.	0x6	R/W
0x0179	DIGINT_DARK_C					
0x0199	DIGINT_DARK_D					
0x01B9	DIGINT_DARK_E					
0x01D9	DIGINT_DARK_F					
0x01F9	DIGINT_DARK_G					
0x0219	DIGINT_DARK_H					
0x0239	DIGINT_DARK_I					
0x0259	DIGINT_DARK_J					
0x0279	DIGINT_DARK_K					
0x0299	DIGINT_DARK_L					
0x02A0	BIOZ_AFECON_A	[15:12]	RESERVED	Reserved.	0x0	R
0x02C0	BIOZ_AFECON_B	[11:2]	BIOZ_TIMESLOT_OFFSET_x	BIOZ Time Slot X offset in 64 × 960 kHz or 64 × (external 960 kHz) cycles.	0x0	R/W
0x02E0	BIOZ_AFECON_C	1	BIOZ_TIAEN_x	High power TIA enable. Enable high power TIA.	0x0	R/W
0x0300	BIOZ_AFECON_D	0	BIOZ_DACREFEN_x	DAC reference enable. 0: disable DAC reference block. 1: enable DAC reference block.	0x0	R/W
0x0320	BIOZ_AFECON_E					
0x0340	BIOZ_AFECON_F					
0x02A1	BIOZ_WGFCW_LOW_A	[15:0]	BIOZ_SINEFCW_L_x	Sinusoid generator frequency control word. BIOZ_SINEFCW_H_x and BIOZ_SINEFCW_L_x constitute BIOZ_SINEFCW_x_x, Bits[19:0]. BIOZ_SINEFCW_x_x, Bits[19:0] = 2^{26} × F/32e6, where F is frequency value (Hz) of sinusoid. To get an accurate DFT result and avoid spectral leakage, use F/(DFT_FS/N) as an integer (N is the number of DFT input data, and DFT_FS is DFT input data rate). DFT_FS can be different due to different input data sources.	0x0	R/W
0x02C1	BIOZ_WGFCW_LOW_B					
0x02E1	BIOZ_WGFCW_LOW_C					
0x0301	BIOZ_WGFCW_LOW_D					
0x0321	BIOZ_WGFCW_LOW_E					
0x0341	BIOZ_WGFCW_LOW_F					
0x02A2	BIOZ_WGFCW_HI_A	[15:4]	RESERVED	Reserved.	0x0	R
0x02C2	BIOZ_WGFCW_HI_B	[3:0]	BIOZ_SINEFCW_H_x	Sinusoid generator frequency control word. BIOZ_SINEFCW_H_x and BIOZ_SINEFCW_L_x constitute BIOZ_SINEFCW_x_x, Bits[19:0]. BIOZ_SINEFCW_x_x, Bits[19:0] = 2^{26} × F/32e6, where F is the frequency value (Hz) of sinusoid. To get an accurate DFT result and avoid spectral leakage, use F/(DFT_FS/N) as an integer (N is the number of DFT input data, and DFT_FS is the DFT input data rate). DFT_FS can be different due to different input data sources.	0x0	R/W
0x02E2	BIOZ_WGFCW_HI_C					

REGISTER DETAILS

Table 21. Register Details

Reg	Name	Bits	Bit Name	Description	Reset	Access
0x0302	BIOZ_WGFCW_HI_D					
0x0322	BIOZ_WGFCW_HI_E					
0x0342	BIOZ_WGFCW_HI_F					
0x02A3	BIOZ_WGPHASE_LOW_A	[15:0]	BIOZ_SINE_PHASE_OFFSET_L_x	Sinusoid phase offset. BIOZ_SINE_PHASE_OFFSET_H_x and BIOZ_SINE_PHASE_OFFSET_L_x constitute BIOZ_SINE_PHASE_OFFSET_x_x, Bits[19:0]. BIOZ_SINE_PHASE_OFFSET_x_x, Bits[19:0] = Phase (degree)/360 × 2^{20}. For example, to get a 45° phase offset, BIOZ_SINE_PHASE_OFFSET_x_x, Bits[19:0] = 45/360 × 2^{20}.	0x0	R/W
0x02C3	BIOZ_WGPHASE_LOW_B					
0x02E3	BIOZ_WGPHASE_LOW_C					
0x0303	BIOZ_WGPHASE_LOW_D					
0x0323	BIOZ_WGPHASE_LOW_E					
0x0343	BIOZ_WGPHASE_LOW_F					
0x02A4	BIOZ_WGPHASE_HI_A	[15:4]	RESERVED	Reserved.	0x0	R
0x02C4	BIOZ_WGPHASE_HI_B	[3:0]	BIOZ_SINE_PHASE_OFFSET_H_x	Sinusoid phase offset. BIOZ_SINE_PHASE_OFFSET_H_x and BIOZ_SINE_PHASE_OFFSET_L_x constitute BIOZ_SINE_PHASE_OFFSET_x_x, Bits[19:0]. BIOZ_SINE_PHASE_OFFSET_x_x, Bits[19:0] = Phase (degree)/360 × 2^{20}. For example, to get 45° phase offset, BIOZ_SINE_PHASE_OFFSET_x_x, Bits[19:0] = 45/360 × 2^{20}.	0x0	R/W
0x02E4	BIOZ_WGPHASE_HI_C					
0x0304	BIOZ_WGPHASE_HI_D					
0x0324	BIOZ_WGPHASE_HI_E					
0x0344	BIOZ_WGPHASE_HI_F					
0x02A5	BIOZ_WGOFFSET_A	[15:12]	RESERVED	Reserved.	0x0	R
0x02C5	BIOZ_WGOFFSET_B	[11:0]	BIOZ_SINE_OFFSET_x	Sinusoid offset. Added to the waveform generator output in sinusoid mode. Signed number represented in twos complement format.	0x0	R/W
0x02E5	BIOZ_WGOFFSET_C					
0x0305	BIOZ_WGOFFSET_D					
0x0325	BIOZ_WGOFFSET_E					
0x0345	BIOZ_WGOFFSET_F					
0x02A6	BIOZ_WGAMPLITUDE_A	[15:11]	RESERVED	Reserved.	0x0	R
0x02C6	BIOZ_WGAMPLITUDE_B	[10:0]	BIOZ_SINEAMPLITUDE_x	Sinusoid amplitude. Unsigned number. Scales the waveform generator in sinusoid mode. Gain coefficient = SINEAMPLITUDE, Bits[10:0]/2^{11}.	0x600	R/W
0x02E6	BIOZ_WGAMPLITUDE_C					
0x0306	BIOZ_WGAMPLITUDE_D					
0x0326	BIOZ_WGAMPLITUDE_E					
0x0346	BIOZ_WGAMPLITUDE_F					
0x02A7	BIOZ_DACCON_A	[15:14]	RESERVED	Reserved.	0x0	R
0x02C7	BIOZ_DACCON_B	13	BIOZ_EXBUFEN_x	Enable excitation buffer. Enable excitation buffer to drive the resistance under measurement. 0: disable. 1: enable.	0x0	R/W
0x02E7	BIOZ_DACCON_C					
0x0307	BIOZ_DACCON_D					
0x0327	BIOZ_DACCON_E	[12:10]	BIOZ_DACBUFBW_x	DAC reconstruction filter power consumption tuning. 001: 30 µA. 010: 40 µA. 100: 111 µA.	0x4	R/W
0x0347	BIOZ_DACCON_F					
		9	BIOZ_BW250KEN_x	Reconstruction filter cutoff frequency of 250 kHz.	0x1	R/W

REGISTER DETAILS

Table 21. Register Details

Reg	Name	Bits	Bit Name	Description	Reset	Access
				0: disable 250 kHz cutoff frequency. 1: enable 250 kHz cutoff frequency.		
		8	BIOZ_BW50KEN_x	Reconstruction filter cutoff frequency of 50 kHz. 0: disable 50 kHz cutoff frequency. 1: enable 50 kHz cutoff frequency.	0x0	R/W
		[7:0]	BIOZ_RATE_DIV_x	DAC update rate. DAC update rate = 32 MHz/ BIOZ_RATE_DIV_x.	0xD	R/W
0x02A8	BIOZ_DACGAIN_A	[15:13]	RESERVED	Reserved.	0x0	R
0x02C8	BIOZ_DACGAIN_B	12	BIOZ_DACGAIN_EN_x	Enable DAC gain. 0: disable DAC gain correction. 1: perform DAC gain correction.	0x1	R/W
0x02E8	BIOZ_DACGAIN_C					
0x0308	BIOZ_DACGAIN_D					
0x0328	BIOZ_DACGAIN_E	[11:0]	BIOZ_DAC_GAIN_x	DAC gain correction factor. Unsigned number. 0x000: maximum negative gain adjustment occurs. 0x001: $1/2^{11}$. 0x800: no gain adjustment. 0xFFF: maximum positive gain adjustment occurs.	0x800	R/W
0x0348	BIOZ_DACGAIN_F					
0x02A9	BIOZ_DACOFFSET_A	[15:13]	RESERVED	Reserved.	0x0	R
0x02C9	BIOZ_DACOFFSET_B	12	BIOZ_DACOFFSET_EN_x	Bypass DAC offset. Use the DAC offset calculated during the calibration routine. 0: bypass DAC offset correction. 1: perform DAC offset correction.	0x1	R/W
0x02E9	BIOZ_DACOFFSET_C					
0x0309	BIOZ_DACOFFSET_D					
0x0329	BIOZ_DACOFFSET_E	[11:0]	BIOZ_DAC_OFFSET_x	DAC offset correction factor. Signed number represented in twos complement format with 0.5 LSB precision. Used when attenuator is disabled. Maximum positive adjustment. Results in positive full scale/2^{10} − 0.5 LSB adjustment. 0.5. results in 0.5 LSB adjustment 0. no offset adjustment. −0.5. results in −0.5 LSB adjustment. -2^{10}. maximum negative adjustment. Results in negative full scale/2 adjustment.	0x0	R/W
0x0349	BIOZ_DACOFFSET_F					
0x02AA	BIOZ_ANA_CTRL1_A	[15:13]	BIOZ_TIA_RGAIN_x	Control signal for HPTIA feedback resistor. 000: 1 kΩ. 001: 2 kΩ. 010: 3 kΩ. 011: 4 kΩ. 100: 6 kΩ. 101: 8 kΩ. 110: 10 kΩ.	0x1	R/W
0x02CA	BIOZ_ANA_CTRL1_B					
0x02EA	BIOZ_ANA_CTRL1_C					
0x030A	BIOZ_ANA_CTRL1_D					
0x032A	BIOZ_ANA_CTRL1_E					
0x034A	BIOZ_ANA_CTRL1_F					
		[12:9]	BIOZ_TIA_CGAIN_x	Control signal for HPTIA feedback capacitor. 0000: off. 0001: 1 pF. 0010: 2 pF. 0011: 3 pF. 0100: 4 pF (default value for low power). 0101: 5 pF. 0110: 6 pF. 0111: 7 pF (default value for high power). 1000: 8 pF. 1001: 9 pF.	0x7	R/W

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Table 21. Register Details

Reg	Name	Bits	Bit Name	Description	Reset	Access
				1010: 10 pF. 1011: 11 pF. 1100: 12 pF. 1101: 13 pF. 1110: 14 pF. 1111: 15 pF.		
		8	BIOZ_RX_LPMODE_x	Low power mode enable for ADC receiver channel. 0: high power mode. 1: low power mode.	0x0	R/W
		7	BIOZ_TIA_LPMODE_x	Low power mode enable for TIA. 0: high power mode. 1: low power mode.	0x0	R/W
		6	BIOZ_EXCBUF_LPMODE_x	Low power mode enable for excitation buffer. 0: high power mode. 1: low power mode.	0x0	R/W
		[5:4]	BIOZ_CHOP_OFF_IN_x	Disable chop off front buffer and PGA. 00: enable front buffer and PGA chopping. 01: only enable PGA chopping. 10: only enable front buffer chopping. 11: disable front buffer and PGA chopping.	0x3	R/W
		[3:2]	BIOZ_AMP_OFF_x	Disable front buffer. 00: enable all. 01: only enable Buffer_p 10: only enable Buffer_n. 11: disable Buffer_p and Buffer_n.	0x3	R/W
		1	BIOZ_PGA_PD_x	PGA P_D control. 0: enable. 1: disable.	0x1	R/W
		0	BIOZ_DAC_RCF_LOWBW_EN_x	DAC RC filters bandwidth tuning. High to set bandwidth reduced to 80% of its original value. 0: disable. 1: enable.	0x0	R/W
0x02AB	BIOZ_ANA_CTRL2_A	15	RESERVED	Reserved.	0x0	R
0x02CB	BIOZ_ANA_CTRL2_B	14	BIOZ_CM_SW_x	Weak V_{CM} driven for IMPIP and IMPIN. 0: disable weak V_{CM} driven. 1: weak CM driven IMPIP and IMPIN.	0x0	R/W
0x02EB	BIOZ_ANA_CTRL2_C					
0x030B	BIOZ_ANA_CTRL2_D					
0x032B	BIOZ_ANA_CTRL2_E	[13:12]	BIOZ_NCHAN_x	N-channel selection. 00: connect HPTIA_n to Buffer_p. 01: connect IMPIN to Buffer_n. 10: connect RCALN to Buffer_n. 11: connect R_{INT_SN} to Buffer_n.	0x0	R/W
0x034B	BIOZ_ANA_CTRL2_F					
		[11:10]	BIOZ_PCHAN_x	P-channel selection. 00: connect HPTIA_p to Buffer_p. 01: connect IMPIP to Buffer_p. 10: connect RCALP to Buffer_p. 11: connect R_{INT_SP} to Buffer_p.	0x0	R/W
		[9:6]	BIOZ_TSW_x	Switch mux for TIA input. 0001: connect TIA input to IMPIP.	0x0	R/W

REGISTER DETAILS

Table 21. Register Details

Reg	Name	Bits	Bit Name	Description	Reset	Access
				0010: connect TIA input to IMPIN. 0100: connect TIA input to EXCP. 1000: connect TIA input to EXCN.		
		[5:2]	BIOZ_DSW_x	Switch mux for excitation buffer output. 0001: connect excitation buffer output to IMPIP. 0010: connect excitation buffer output to IMPIN. 0100: connect excitation buffer output to EXCP. 1000: connect excitation buffer output to EXCN.	0x0	R/W
		1	BIOZ_TRSW_x	T switch in mux for RCALx. 0: disconnect RCALx to HPTIA. 1: connect RCALx to HPTIA.	0x0	R/W
		0	BIOZ_DRSW_x	D switch in mux for RCALx. 0: disconnect RCALx to excitation buffer. 1: connect RCALx to excitation buffer.	0x0	R/W
0x02AC	BIOZ_ANA_CTRL3_A	[15:2]	RESERVED	Reserved.	0x0	R
0x02CC 0x02EC 0x030C 0x032C 0x034C	BIOZ_ANA_CTRL3_B BIOZ_ANA_CTRL3_C BIOZ_ANA_CTRL3_D BIOZ_ANA_CTRL3_E BIOZ_ANA_CTRL3_F	[1:0]	BIOZ_RINT_SW_x	Support internal calibration resistor. Set to 0x11 to enable the internal calibration resolution. 00: floating internal calibration resistance. 11: connect internal calibration resistance to excitation buffer and HPTIA.	0x0	R/W
0x02AD	BIOZ_ADCFILTERCON_A	[15:6]	RESERVED	Reserved.	0x0	R
0x02CD 0x02ED 0x030D 0x032D 0x034D	BIOZ_ADCFILTERCON_B BIOZ_ADCFILTERCON_C BIOZ_ADCFILTERCON_D BIOZ_ADCFILTERCON_E BIOZ_ADCFILTERCON_F	[5:4]	BIOZ_AVRGNUM_x	Sets number of samples used by the averaging function. 00: Two ADC samples. 01: Four ADC samples. The number of input data for one average is four. 10: Eight ADC samples. The number of input data for one average is eight. 11: 16 ADC samples. The number of input data for one average is 16.	0x0	R/W
		3	BIOZ_AVRGEN_x	Average function enable. Enable average operation of SINC3 filter output 0: disable. SINC3 filter result fed to the next stage directly. 1: enable. Averaged result fed to the next stage.	0x0	R/W
		2	BIOZ_SINC3BYP_x	Bypass SINC3 filter. 0: enable SINC3 filter. 1: bypass SINC3 filter.	0x0	R/W
		[1:0]	BIOZ_SINC3OSR_x	SINC3 filter oversampling rate. 00: oversampling rate of five. 01: oversampling rate of four. 10: oversampling rate of two. 11: oversampling rate of five.	0x0	R/W
0x02AE	BIOZ_DFTCON_A	[15:6]	RESERVED	Reserved.	0x0	R
0x02CE 0x02EE 0x030E	BIOZ_DFTCON_B BIOZ_DFTCON_C BIOZ_DFTCON_D	5	BIOZ_WG_DFT_DIFF_PHASE_EN_x	Wave generator block sine wave and DFT block sine wave use a different offset. 0: use the same offset. 1: use the different offset.	0x0	R/W
0x032E	BIOZ_DFTCON_E	4	BIOZ_HANNINGEN_x	Enable Hanning window.	0x0	R/W

REGISTER DETAILS

Table 21. Register Details

Reg	Name	Bits	Bit Name	Description	Reset	Access
0x034E	BIOZ_DFTCON_F			0: disable. 1: enable.		
		[3:0]	BIOZ_DFTNUM_x	ADC samples used. DFT number can be four up to 8192. 0000: DFT point number is four. 0001: DFT point number is eight. 0010: DFT point number is 16. 0011: DFT point number is 32. 0100: DFT point number is 64. 0101: DFT point number is 128. 0110: DFT point number is 256. 0111: DFT point number is 512. 1000: DFT point number is 1024. 1001: DFT point number is 2048. 1010: DFT point number is 4096. 1011: DFT point number is 8192.	0x9	R/W
0x02AF	BIOZ_ADC_CONV_DLY_A	[15:3]	RESERVED	Reserved.	0x0	R
0x02CF 0x02EF 0x030F 0x032F 0x034F	BIOZ_ADC_CONV_DLY_B BIOZ_ADC_CONV_DLY_C BIOZ_ADC_CONV_DLY_D BIOZ_ADC_CONV_DLY_E BIOZ_ADC_CONV_DLY_F	[2:0]	BIOZ_ADC_CONV_DLY_x	Delay between ADC enable and SINC3 enable. Default value is ~25 µs. 000: 25 µs. 001: 50 µs. 010: 100 µs. 011: 200 µs. 100: 400 µs. 101: 800 µs. 110: 1.6 ms. 111: 3.2 ms.	0x0	R/W
0x02B0 0x02D0 0x02F0 0x0310 0x0330 0x0350	BIOZ_DFTPHASE_LOW_A BIOZ_DFTPHASE_LOW_B BIOZ_DFTPHASE_LOW_C BIOZ_DFTPHASE_LOW_D BIOZ_DFTPHASE_LOW_E BIOZ_DFTPHASE_LOW_F	[15:0]	BIOZ_DFT_PHASE_OFFSET_L_x	DFT_PHASE_OFFSET, Bits[19:0] = Phase (degree)/360 × 2^{20}. For example, to get 45° phase offset, DFTOFFSET, Bits[19:0] = 45/360 × 2^{20}.	0x0	R/W
0x02B1	BIOZ_DFTPHASE_HI_A	[15:4]	RESERVED	Reserved.	0x0	R
0x02D1 0x02F1 0x0311 0x0331 0x0351	BIOZ_DFTPHASE_HI_B BIOZ_DFTPHASE_HI_C BIOZ_DFTPHASE_HI_D BIOZ_DFTPHASE_HI_E BIOZ_DFTPHASE_HI_F	[3:0]	BIOZ_DFT_PHASE_OFFSET_H_x	DFT_PHASE_OFFSET, Bits[19:0] = Phase (degree)/360 × 2^{20}. For example, to get 45° phase offset, DFTOFFSET, Bits[19:0] = 45/360 × 2^{20}.	0x0	R/W

OUTLINE DIMENSIONS

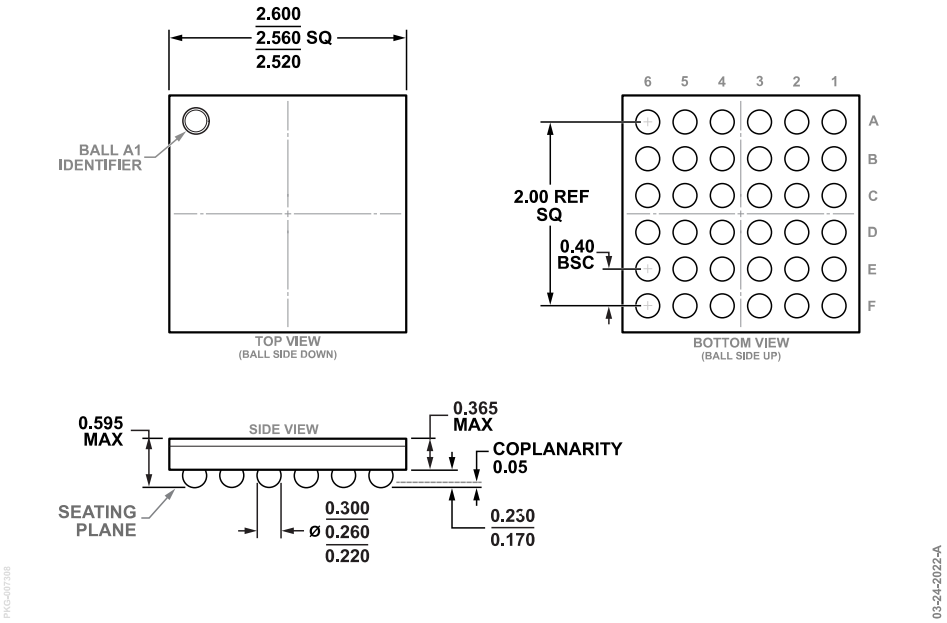


Figure 49. 36-Ball Wafer Level Chip Scale Package [WLCSP]
with Backside Coating
(CB-36-10)
Dimensions shown in millimeters

Updated: April 22, 2022

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADPD6000BCBZR7	-40°C to +85°C	CHIPS W/SOLDER BUMPS/WLCSP	Reel, 1500	CB-36-10

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Description
EVAL-ADPD6000Z	Evaluation Board

[1] Z = RoHS Compliant Part.

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