ANALOG DEVICES

EVAL-ADE9000EBZ User Guide
UG-1082

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Evaluating the ADE9000 High Performance, Multiphase Energy, Power Quality Monitoring IC

FEATURES
Full featured evaluation board for the ADE9000
PC control in conjunction with the EVAL-SDP-CB1Z system demonstration platform (SDP)
PC software for control and data analysis (time and frequency domain)
Standalone capability

EVALUATION KIT CONTENTS
EVAL-ADE9000EBZ evaluation board

ADDITIONAL EQUIPMENT NEEDED
EVAL-SDP-CB1Z (must be ordered separately)
Includes a mini USB cable
Current transformers or Rogowski coils for 3-phase current channels and the neutral channel
Precision current and voltage signal source
PC running Windows XP SP2, Windows Vista, or Windows 7 with USB 2.0 port

DOCUMENTS NEEDED
ADE9000 data sheet
EVAL-ADE9000EBZ user guide

SOFTWARE NEEDED
EVAL-ADE9000EBZ evaluation software

ONLINE RESOURCES
Design and integration files
Schematics, layout files, and bill of materials

GENERAL DESCRIPTION
The EVAL-ADE9000EBZ evaluation board allows the performance of the ADE9000 energy monitoring IC to be evaluated in a context very similar to an actual power quality monitor. The kit requires purchasing a second board: the controller board for the system demonstration platform (EVAL-SDP-CB1Z) and current sensors. The ADE9000 evaluation kit includes evaluation software, written in LabVIEW®, which provides access to the registers and features of the device using a PC interface.

Consult the ADE9000 data sheet in conjunction with this user guide when using the evaluation board.

TYPICAL EVALUATION BOARD SETUP

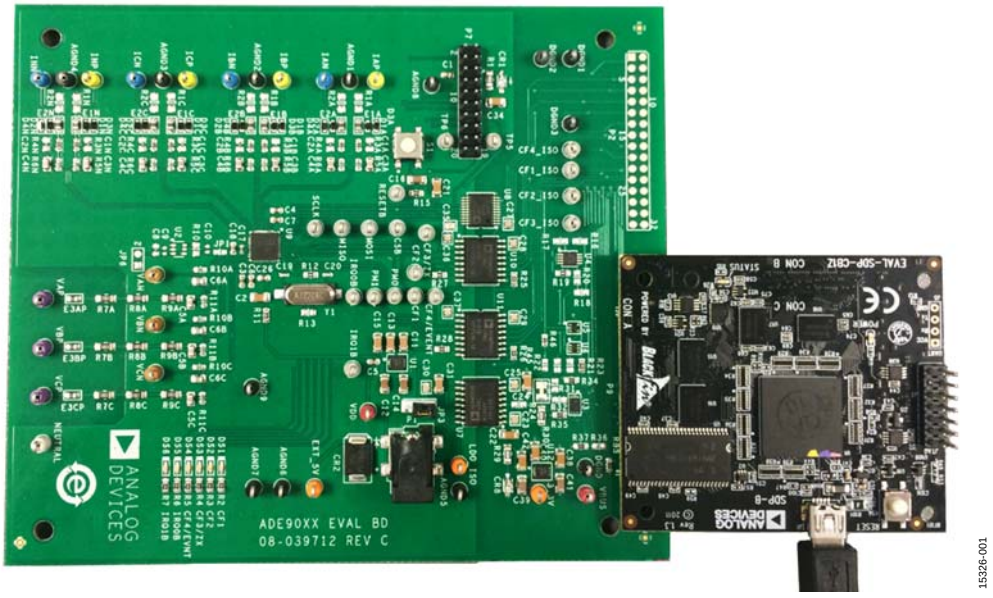


Figure 1. EVAL-ADE9000EBZ (Left) Connected to EVAL-SDP-CB1Z SDP Interface Board (Right)

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REVISION HISTORY

1/2017—Revision 0: Initial Version

EVALUATION BOARD CONNECTION DIAGRAM

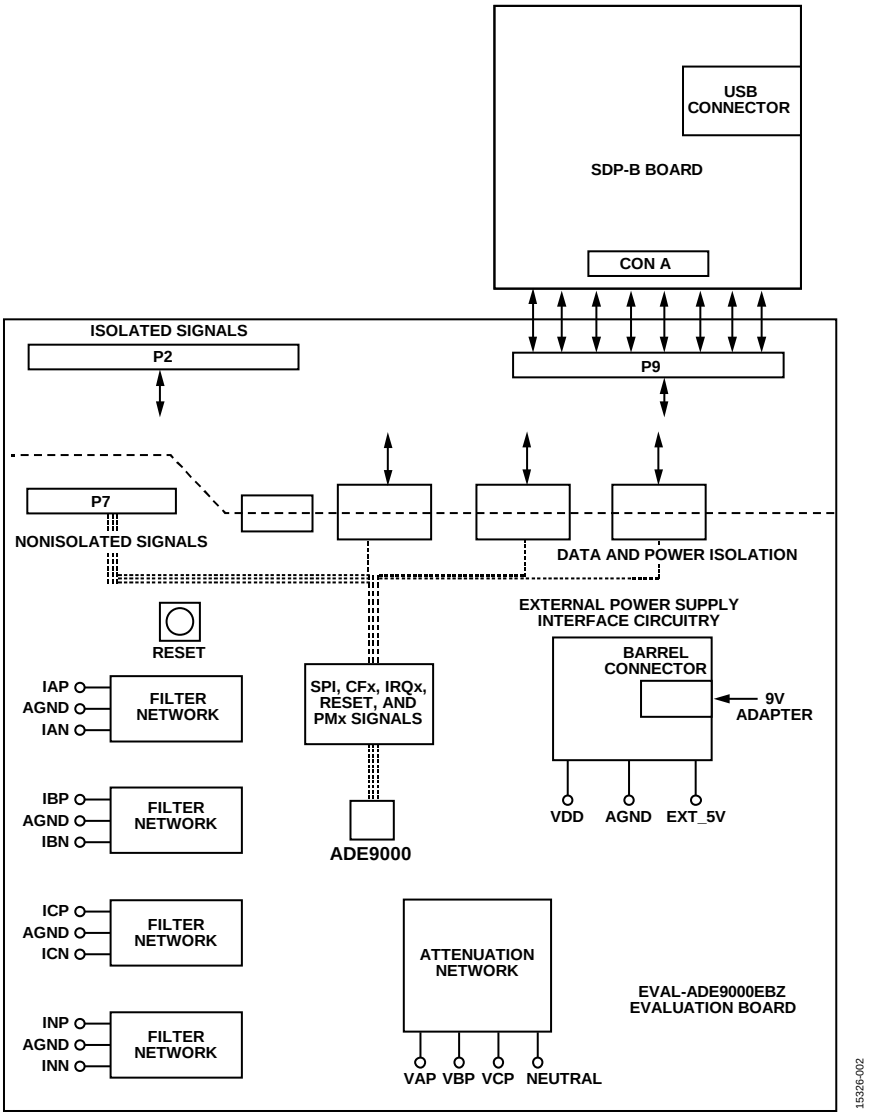


Figure 2. Evaluation Board Connection Diagram

EVALUATION BOARD HARDWARE

OVERVIEW

The EVAL-ADE9000EBZ and the SDP-B (also referred to as the EVAL-SDP-CB1Z or the Blackfin® SDP board) boards are both required to evaluate the ADE9000.

When ordering the EVAL-ADE9000EBZ evaluation board, order the EVAL-SDP-CB1Z; the evaluation kit and the SDP-B board are purchased and packaged separately, but must be used together.

The EVAL-ADE9000EBZ board is connected to the SDP-B board using the 120-pin connector, P9, on the EVAL-ADE9000EBZ evaluation board. The SDP-B board consists of an ADSP-BF527 microcontroller that handles all the communications from the PC to the ADE9000 device that populates the evaluation board.

POWERING UP THE EVALUATION BOARDS

The ADE9000 can be powered through the USB of the SDP-B board or an external power supply.

Power the ADE9000 externally by connecting a 3.3 V supply to the VDD test point, or a 5 V to 16 V dc supply to the EXT_5V test point or barrel jack. When using an external supply, connect Pin 1 and Pin 2 at J3. Connect Pin 2 and Pin 3 to power the ADE9000 with internal isolated power from the SDP-B board.

ANALOG INPUTS

Current and voltage signals are connected at the test pins placed on the evaluation board. All analog input signals are filtered using the on-board antialiasing filters before the signals are connected to the ADE9000. The components used on the board are the recommended values to be used with the ADE9000.

CURRENT SENSE INPUTS: IAP, IAN, IBP, IBN, ICP, ICN, INP, AND INN TEST PINS

Figure 3 shows the structure used for the Phase A current channel in the evaluation board. The same signal path is used for the other current channels. Therefore, the explanation in this section applies to other current channels on the evaluation board, such as Phase B, Phase C, and the neutral phase.

E1A and E2A are ferrite beads that filter any high frequency noise present on the wires. Immediately following the ferrite beads, there are four protection diodes per current channel used for overcurrent protection. The antialiasing filter network appears after the protection network.

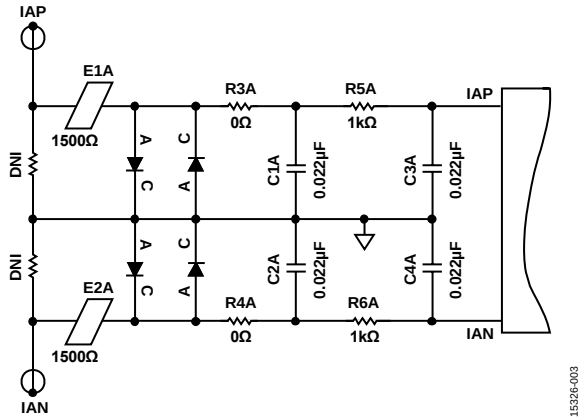


Figure 3. Phase A Current Input Structure on the Evaluation Board

USING CURRENT SENSE TRANSFORMERS

Figure 4 shows an example of a current transformer sensor configuration. When using current sense transformers, populate the R1A and R2A burden resistors according to the full-scale current and the current transformer (CT) turns ratio of the application. The CT turns ratio and the burden resistor values must be chosen such that the IAP pin to AGND pin and IAN pin to AGND pin potentials do not exceed ±0.5 V peak. The C1A and C2A capacitors are not populated when the current transformer is used. An example burden resistor calculation, where the maximum expected current at current transformer primary is 50 A rms, the CT turns ratio is 3000:1, and the secondary current at 50 A is as follows,

$$I_{SECONDARY} = \frac{50}{3000} = 16.66\ \text{mA}$$

To allow headroom, the input signal into the current channel analog-to-digital converter (ADC) at maximum current is set at half of full scale. Because the full-scale differential input is ±0.707 V rms, the total burden resistor, R_B, can be calculated as

$$R_B = \left(\frac{0.707}{2} \times \frac{1}{16.66\ mA}\right) = 21.2\ \Omega$$

Because the total burden resistor is split to have a differential configuration,

$$R1A = R2A = \frac{R_B}{2} = \frac{21.2}{2} = 10.6\,\Omega$$

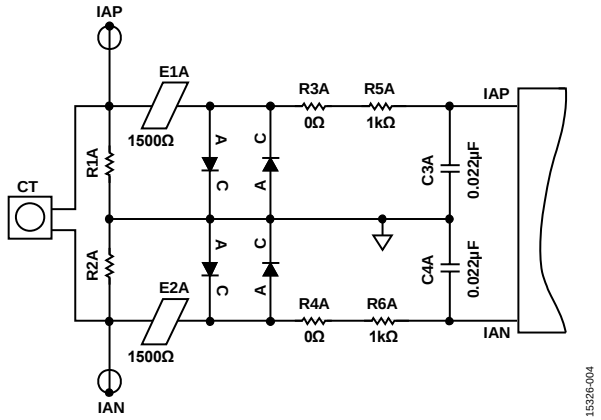


Figure 4. Example of a Current Transformer Connection

USING ROGOWSKI COILS

Figure 5 shows an example of a configuration using a Rogowski coil current sensor. The R1A and R2A burden resistors are not used in this configuration, and are therefore removed from the board. Because Rogowski coil sensors have a gain that increases with frequency (20 dB/decade), the high frequency components of the current signal are amplified by a larger factor. Therefore, two stages of resistor capacitor (RC) filtering are required to attenuate the high frequency components and to avoid aliasing. The R3A and R4A resistors must be 100 Ω and are used in conjunction with the 22 nF C1A and C2A capacitors to form a low-pass filter with a cutoff frequency of 72 kHz. This first stage is followed by the 1 kΩ/22 nF RC filter combination that provides a cutoff frequency of 7.2 kHz. The Rogowski coil must be chosen such that the IAP to AGND and IAN to AGND potentials do not exceed ±0.5 V peak.

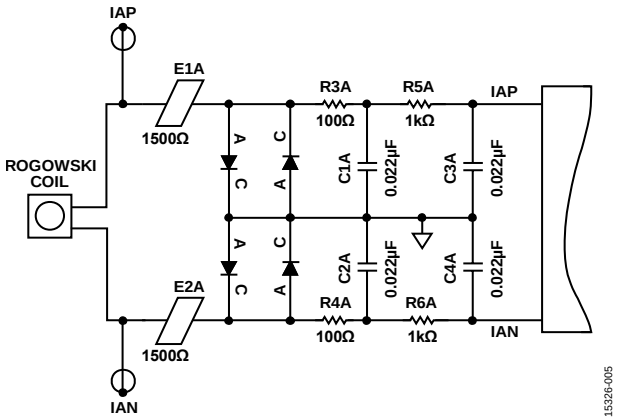


Figure 5. Example of a Rogowski Coil Connection

PHASE VOLTAGE SENSE INPUTS: VAP AND VAN, VBP AND VBN, AND VCP AND VCN TEST PINS

Figure 6 shows the Phase A voltage channel signal path on the evaluation board. The same signal path is also replicated on the Phase B and Phase C channels; therefore, the description in this section applies to the Phase B and Phase C channels.

E3AP is a ferrite bead that filters any high frequency noise present on the wires. There are three 330 kΩ resistors connected in series, forming an attenuation network with a 1 kΩ resistor, R11A. This setup provides an attenuation ratio of 990:1. The R11A and C5A RC combination and the R10A and C6A RC combination have the same cutoff frequency as that of the RC filters used on the current channels. This matching is essential to avoid large phase errors between the voltage and current signals. If a different attenuation ratio is preferred, replace the R7A, R8A, and R9A resistors with alternate resistors. The resistors must be chosen such that the maximum signal at the VAP pin is ±0.5 V peak with respect to the AGND pin. The Phase A line is connected to the VAP test point and the neutral line (in the case of the 3-phase, 4-wire wye configuration) is connected to the NEUTRAL test point. The NEUTRAL test point is tied to the AGND potential of the ADE9000.

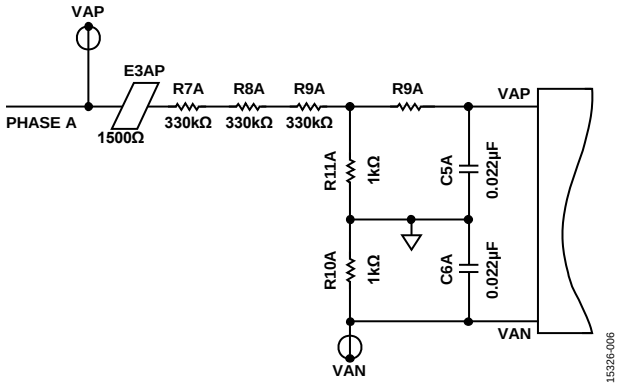


Figure 6. Phase A Voltage Input Structure on the Evaluation Board

SETTING UP THE EVALUATION BOARD AS AN ENERGY METER

Figure 7 shows a typical setup for the EVAL-ADE9000EBZ evaluation board. In this example, an energy meter for a 3-phase, 4-wire, wye distribution system is shown. Current transformers sense the phase currents and are connected as shown in Figure 7. The line voltages are connected directly to the board as shown.

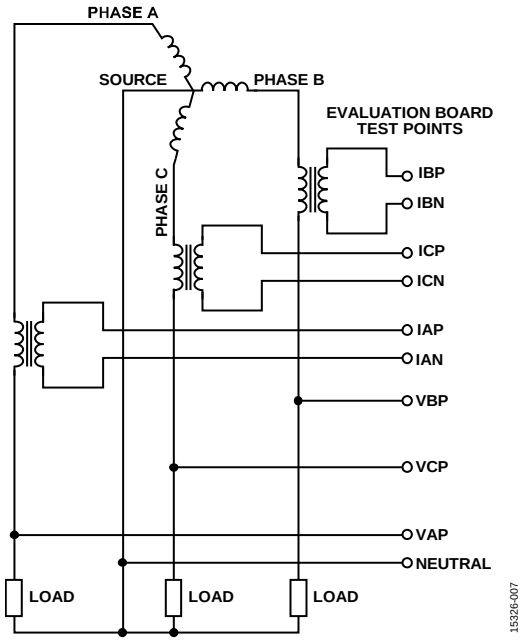


Figure 7. Typical Setup for the EVAL-ADE9000EBZ for 3-Phase, 4-Wire, Wye Distribution System

Figure 8 shows a typical setup for the EVAL-ADE9000EBZ evaluation board as an energy meter for a 3-phase, 3-wire, delta distribution system. The Phase B voltage is considered a reference and therefore is tied to the NEUTRAL test point on the evaluation board.

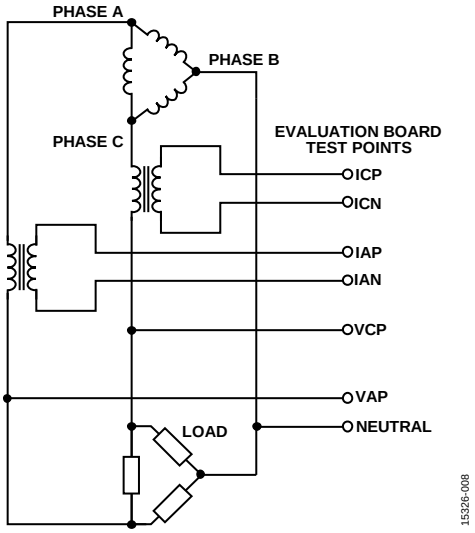


Figure 8. Typical Setup for the EVAL-ADE9000EBZ for a 3-Phase, 3-Wire, Delta Distribution System

USING THE EVALUATION BOARD WITH ANOTHER MICROCONTROLLER

It is possible to manage the ADE9000 evaluation board with a different microcontroller mounted on another board. The evaluation board can be connected to this second board through the P2 connector. The SDP-B board in this case is unused and not connected. If nonisolated signals are to be used with the external microcontroller, the P7 connector can be used. In this case, the U7, U8, U10, and U11 isolators must be removed from the EVAL-ADE9000EBZ evaluation board. Note that the P2 and P9 connectors have isolated signals, whereas the P7 connector is nonisolated. It is necessary to have isolation on the host side if signals from the P7 connector are used.

EVALUATION BOARD SOFTWARE

The EVAL-ADE9000EBZ is supported by Windows®-based software that allows the user to access all the functionality of the ADE9000. The software communicates with the SDP-B board using the USB. The SDP-B microcontroller communicates with the ADE9000 placed on the evaluation board to process the requests sent from the PC.

INSTALLING THE DRIVERS

Make sure to have administrator privileges to install and run the evaluation software. Disconnect the SDP-B board.

1. Install SDPDriversNET.exe located in the **SDP Drivers** folder. This installs the SDP drivers and the .NET framework required to install LabVIEW run-time engine. .NET 3.5 or higher is required to install LabVIEW run-time engine.
2. Connect the USB cable from the PC to the SDP-B board. Windows detects the device and locates the correct driver automatically.

INSTALLING AND UNINSTALLING THE EVAL-ADE9000EBZ SOFTWARE

The ADE9000 evaluation software is supplied with the evaluation software package. It contains an installer to install the EVAL-ADE9000EBZ evaluation software. The program to be installed is a LabVIEW-based program that runs on the PC.

When running the software on a PC that does not have LabVIEW 2014 for the first time, run the installer. The installer installs a LabVIEW run-time engine that enables the PC to open the evaluation software executable without any issues. This installer is available in the **LabVIEW\InstallationFiles** folder. If LabVIEW 2014 is available on the PC, the executable can be directly opened from the **Executable** folder.

To install and launch the EVAL-ADE9000EBZ evaluation software, use the following procedure:

1. Double click **InstallationFiles\setup.exe** to launch the setup program that automatically installs all the software components, including the uninstall program, and creates the required directories.
2. To launch the software, click **Start, All Programs, ADE9000** and click **ADE9000_Evaluation_Software**. When the software runs for the first time, right-click **ADE9000_Evaluation_Software.exe** and select **run as the administrator**.

Both the EVAL-ADE9000EBZ evaluation software program and the run-time engine are uninstalled using the **Add/Remove Programs** option in the Control Panel.

Before installing a new version of the EVAL-ADE9000EBZ evaluation software, use the following procedure:

1. Uninstall the previous version of the evaluation software.
2. Select the add/remove programs option in the Windows Control Panel.
3. Select the program to uninstall and click **Add/Remove**.

MAIN WINDOW

When the software executable opens, the main window of the evaluation software appears, as shown in Figure 9. When opened for the first time, the software searches for two files: the register file, **ADE9000_reg_map.bin,** and the SDP microcontroller code file, **ADE9000.ldr**. These files can be found in the **\Executable\data** folder. After manually choosing the location of these files the first time, the **ADE9000coms.ini** file is updated with their file paths. This update allows the software to find the files correctly during the next run.

The software recognizes the device on the evaluation board, (the ADE9000) and displays the device features in the **IC being evaluated:** box of the window. The SDP code version and the version register value of the IC are displayed in their corresponding boxes in the window.

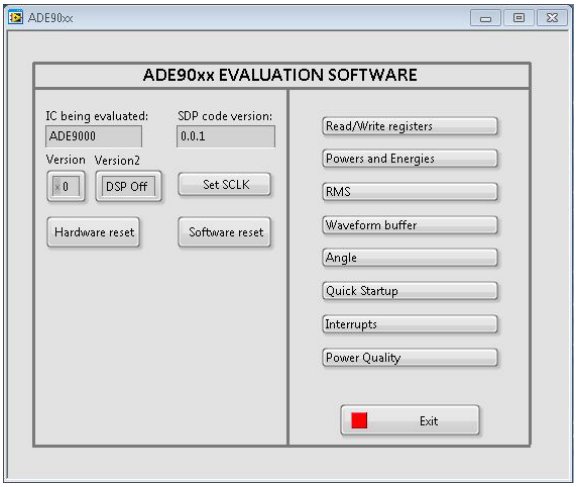


Figure 9. Main Window of the Evaluation Software

Three different operations can be performed using the options present in the left pane of the main window (see Figure 9). These operations are enacted using the following buttons:

1. **Set SCLK**. Click this option to open the **Select SPI Frequency** window, as shown in Figure 10. Set the serial peripheral interface (SPI) clock frequency for communication between the ADE9000 and the SDP-B board using this window. Enter the intended SCLK frequency value on the SCLK control and click **Check if Valid.** The **Check if Valid** option rounds off the clock frequency to the closest setting that is possible in the SDP-B board. Finally, click **Set SCLK** to set the SCLK frequency in the SDP-B board. The window closes automatically. The default SPI clock rate is 10 MHz.
2. **Software reset**. Click this option to perform a software reset on the ADE9000. A dialog box appears confirming the completion of the reset operation.
3. **Hardware reset**. Click this option to perform a hardware reset on the ADE9000. A dialog box appears confirming the completion of the reset operation.

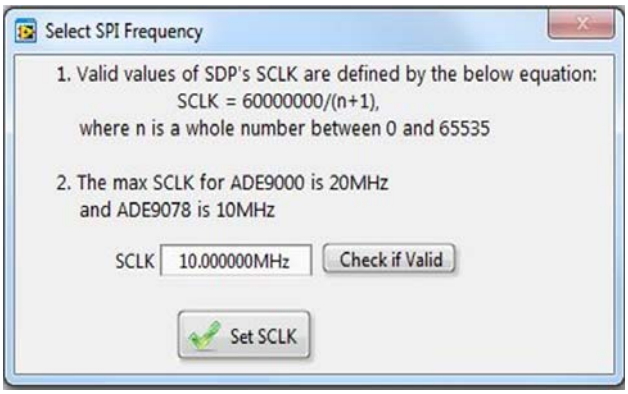


*Figure 10. **Set SCLK** Option on the SDP-B Board*

EVALUATION SOFTWARE FUNCTIONS

The right pane of the main window (see Figure 9) consists of eight options, each of which can be used to evaluate a particular functionality of the ADE9000. The functionalities that can be evaluated are represented by the following options:

- **Read/Write registers**
- **Powers and Energies**
- **RMS**
- **Waveform buffer**
- **Angle**
- **Quick Startup**
- **Interrupts**
- **Power Quality**

Clicking any of these eight options opens a corresponding window. To close any of these windows, the same option must be clicked again in the main window. Multiple windows can be left open on the monitor to evaluate different features at the same time.

READ/WRITE REGISTERS OPTION

The first option in the right pane of the main window is **Read/Write registers**. Click this option to open the **Read/Write registers** window, as shown in Figure 11. There are four tabs available within this window: **Single access**, **Sequential access**, **All register access**, and **Read on Interrupt**.

Each tab helps perform read/write operations to the ADE9000 at different capacities.

Single Access Tab

The **Single access** tab contains a **Name** selection box. Click the down arrow in the selection box to open a list of all the registers within ADE9000. Any of the registers can be selected for communication purposes. After the registers are selected, the **Address** box and **Length** box are updated on the screen. Alternatively, the address of the register can be written first, which updates the register name and the length fields. The individual bit fields within the register can be accessed via the **Bitfield** box. Data can be written to and read from the IC using the **Write** and **Read** options. The white boxes in the window denote the description of the register and the corresponding bit fields. Figure 11 shows the window when the **Single access** tab is selected.

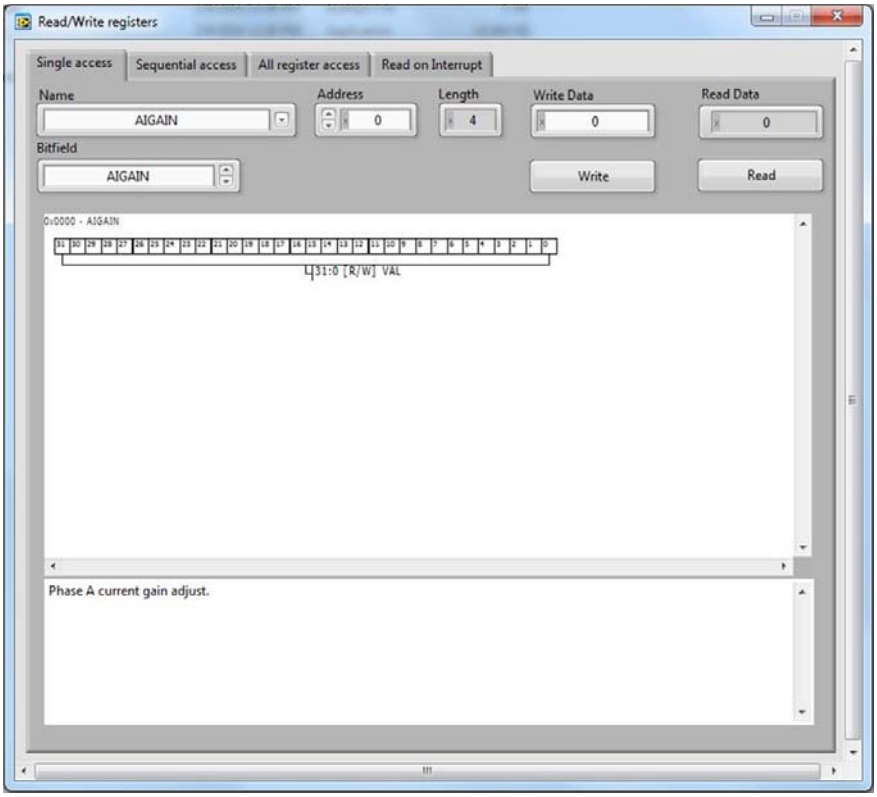


*Figure 11. **Single access** Tab in the **Read/Write registers** Window*

Sequential Access Tab

The **Sequential access** tab allows the user to perform read or write operations on four different registers, in a particular order. The **Enable** checkboxes at the beginning of each of the steps (Step 1 through Step 4) can be selected to enable that particular step. When all the required settings are entered, click **Execute Sequence** to perform the operations in sequence. Figure 12 shows the window when the **Sequential access** tab is selected.

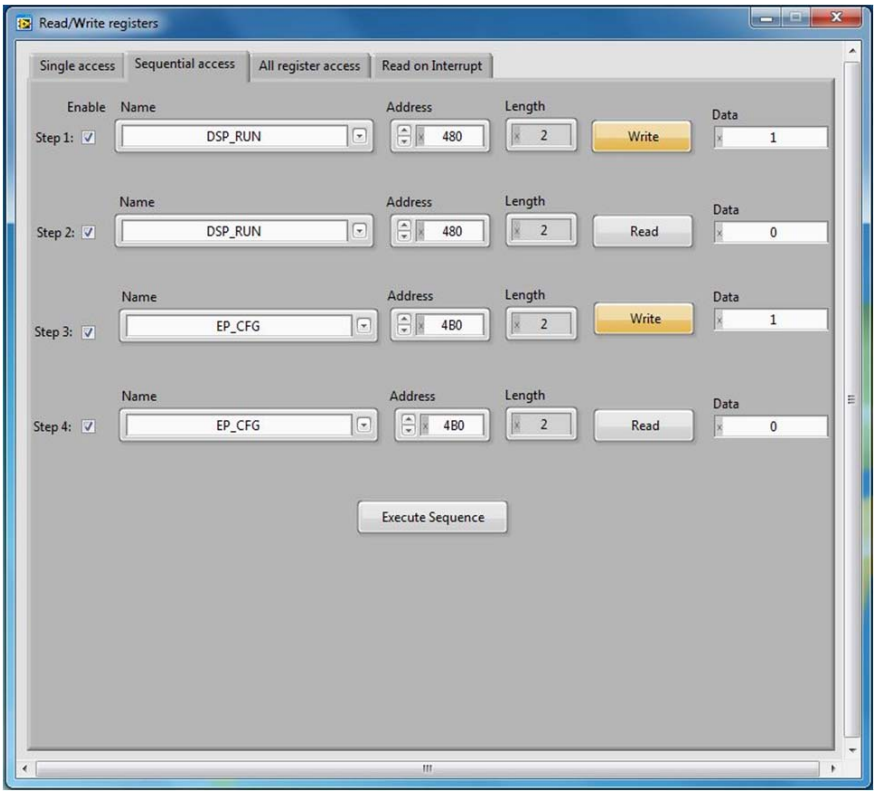


*Figure 12. **Sequential access** Tab in the **Read/Write registers** Window*

All Register Access Tab

The **All register access** tab allows the user to read from all the registers on the device and to write all writable registers by clicking a single option. Click **Read and display all registers** to read the registers and output the results to the **Register values** table. Enter the file path for saving the register values and click **Save data to file** to generate a text file with all the register values. Any notes for reference can be added to the file using the **Notes** field. The saved text file can also be edited and used to write back to the registers. When attempting to write back to the registers, edit the hexadecimal register value in the text file and specify the file path next to the **Read from file and update display** option (perform this action before clicking this option). Click **Read from file and update display** to update the table in the window with the values from the file. At this point, clicking the **Write register values from display** option writes to all the writable registers within the ADE9000. Figure 13 shows the window with the **All register access** tab selected.

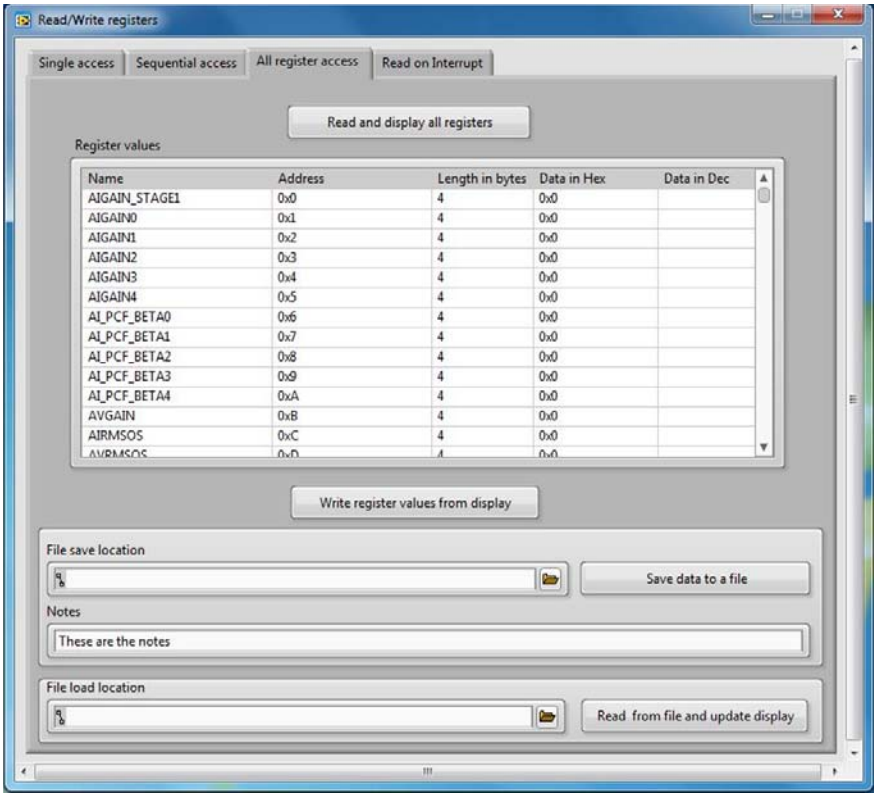


*Figure 13. **All register access** Tab in the **Read/Write registers** Window*

Read on Interrupt Tab

The **Read on Interrupt** tab allows the user to read any particular register on any particular interrupt event. Examples of cases where using this tab may be useful are as follows:

- Reading the AVRMS register result on each DREADY interrupt.
- Reading the AWATTHR_HI register result at every EGYRDY interrupt.

The register and the interrupt can be selected from their respective boxes in the window. The number of desired register reads is entered in the **No. of interrupts** field. Click **Read on interrupts** at this point to perform the read operation. The results are available in the **Read-back values** table. Click **Save data to a file** to save the readback values. Figure 14 shows the window when the **Read on Interrupt** tab is selected.

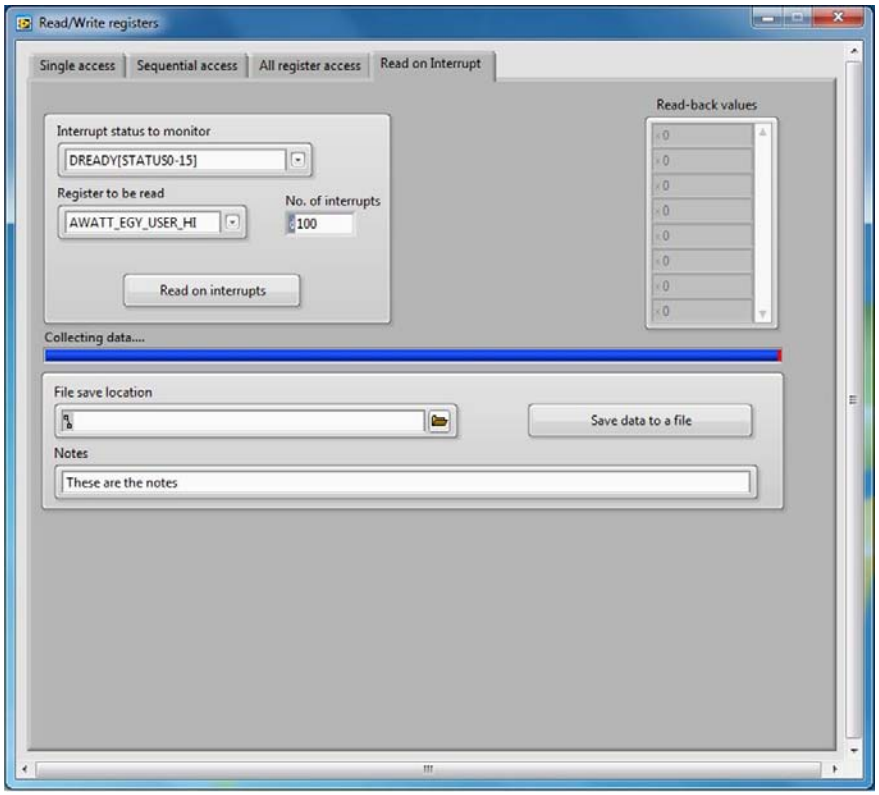


*Figure 14. **Read on Interrupt** Tab in the **Read/Write registers** Window*

POWERS AND ENERGIES

The next functionality available in the evaluation software is powers and energies, located in the **Powers and Energies** window. This window contains the **Powers, Energies,** and **CF** tabs.

Powers Tab

The **Powers** tab allows the user to read from all the instantaneous powers and accumulated powers available in the ADE9000.

Before evaluating the accumulated powers, it is recommended to set the **Power update rate (ms)** field and click **Set**. This action writes to the PWR_TIME register accordingly. Figure 15 shows the window when the **Powers** tab is selected in the evaluation software. The signal path for the independent current and voltage channels is found in the RMS Window section. Note that the **update continuously** option must be disabled before writing a value to any register.

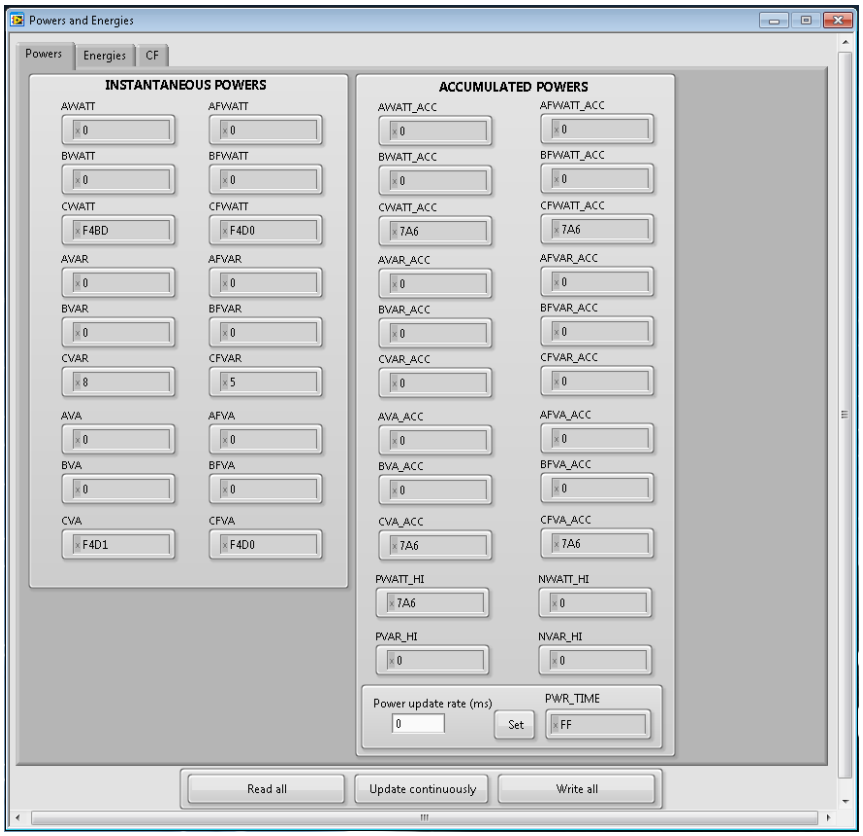


*Figure 15. **Powers** Tab in the **Powers and Energies** Window*

Energies Tab

The **Energies** tab allows the user to set the EP_CFG register and the EGY_TIME register correctly and to read the energy results from the ADE9000. Figure 16 shows the **Energies** tab. In the **ENERGY SETTINGS** pane, there are different options available for the user, such as the **Accumulation Setting**, which, when turned on, can be further specified using the **Sample-based** or **Half-Line Cycle** options. Select the **Enable accumulation** box to overwrite the user energy register at every EGYRDY bit interval (EGY_LD_ACCUM = 1). After all inputs are populated, click **Set** to write to the registers appropriately. Then, select the **Enable energy/power calculations** box and click **Set**. The **ENERGY** pane displays the energy results. Note that the **Update continuously** option must be disabled before writing a value to any register.

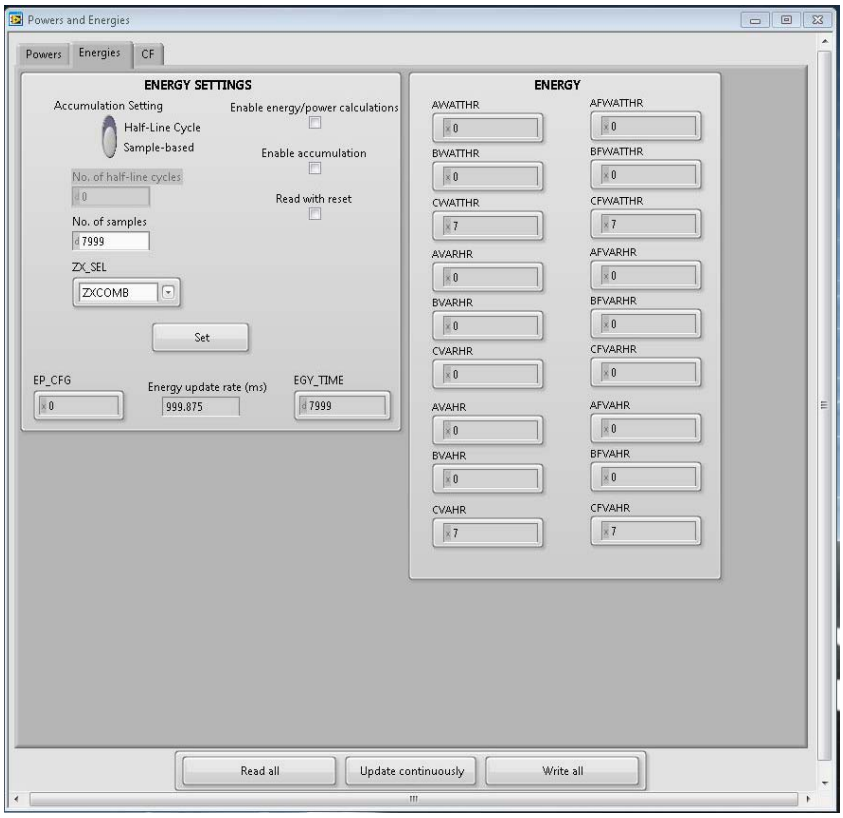


*Figure 16. **Energies** Tab in the **Powers and Energies** Window*

CF Tab

The **CF** tab allows the user to configure the CF1 to CF4 pins of the ADE9000. There is a wide range of configurability available in the ADE9000 with respect to the functionality of the CF1 to CF4 pins. Some of the major settings that affect the CF1 to CF4 pins results include the phases enabled in each CF1 to CF4 pin, the type of energy represented, and the **CF1DEN** to **CF4DEN** register values. These settings can be set using the **CF** tab, as shown in Figure 17. There are additional functionalities muxed onto the CF3 and CF4 pins, which can also be controlled using this tab. Common threshold settings such as **WTHR**, **VARTHR**, and **VATHR** can also be set in the **COMMON SETTINGS** pane of the **CF** tab. The CF1 to CF4 low pulse widths can be fixed at a particular value by enabling the corresponding check boxes for each of the CF1 to CF4 pins and setting a value for the **CF_LTMR[18:0]** bit field to execute this pulse width setting.

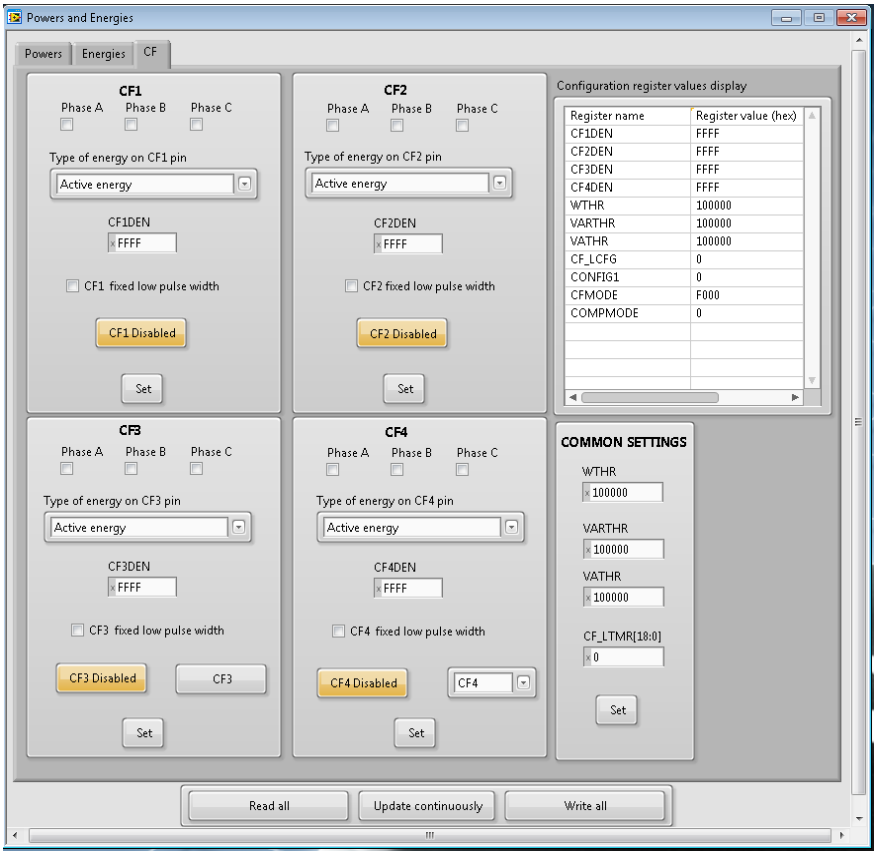


*Figure 17. **CF** Tab in the **Powers and Energies** Window*

RMS WINDOW

The **RMS** window allows the user to visualize the datapath inside the ADE9000, configure the high-pass filter, integrator, programmable gain amplifier (PGA) gain levels, ADC_REDIRECT register values, VCONSEL and ICONSEL settings, and view the results. To perform the configuration changes, enter the changes to the respective boxes in the window and click **Write**, located in the bottom right corner of the signal path, as shown in Figure 19. The different gain and offset registers can also be accessed via the tabs within this window.

There are several tabs within the **RMS** window. The first tab is the **Continuous monitor** tab, shown in Figure 18. The current and voltage rms results are shown separately on the screen.

There are individual tabs present for each of the voltage and current channels. Under each of these tabs, there are multiple subtabs. The **IA** and **VA** tabs are shown in Figure 19 and Figure 20, respectively. The VB and VC datapaths are very similar to the VA datapath; the IB and IC datapaths are very similar to the IA datapath. To enable or disable the **Multi-point Gain and Phase** calibration, click **Disabled**. The state of this option controls the multi-point gain and phase register accessibility.

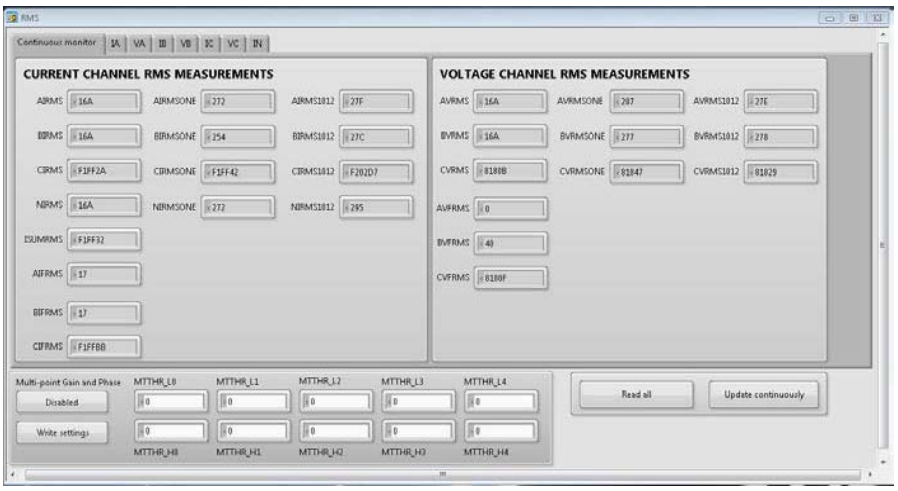


*Figure 18. **Continuous monitor** Tab in the **RMS** Window*

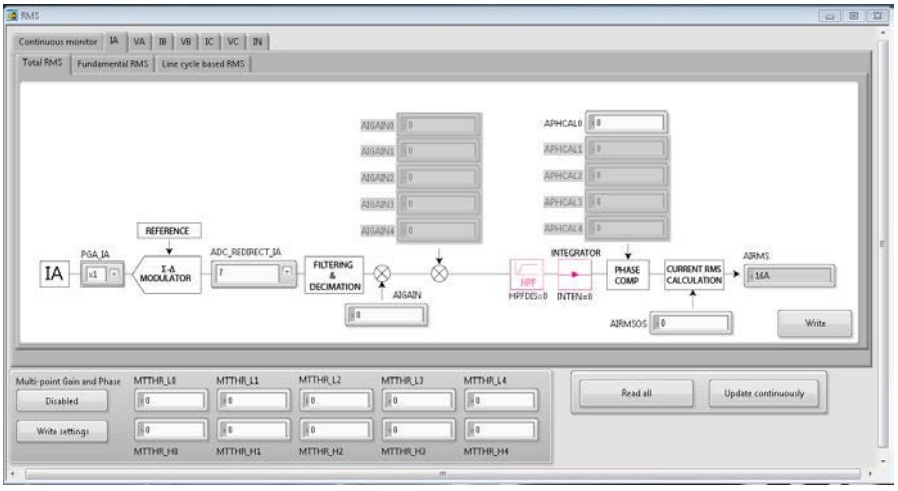


*Figure 19. **IA** Tab (**Total RMS** Subtab) in the **RMS** Window*

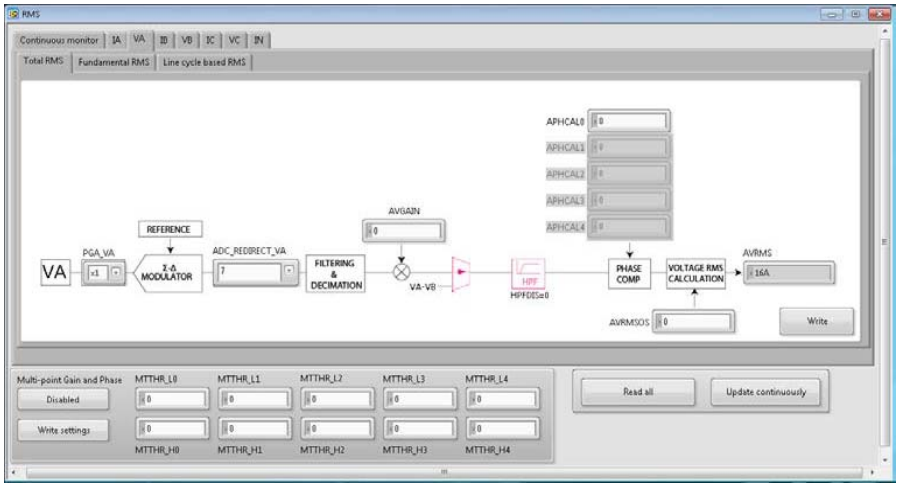


*Figure 20. **VA** Tab (**Total RMS** Subtab) in the **RMS** Window*

WAVEFORM BUFFER WINDOW

The **Waveform Buffer** window has two panes. The upper pane of the window controls the different settings of the waveform buffer. Settings such as the operation mode, specifying which channels burst, the source of the waveforms, and the number of samples to be collected are selected from this upper pane of the window. After all the settings are entered, click **Run** to start the filling process of the buffer. When the filling is complete, the buffer samples are plotted in the time domain under the **Waveforms** tab. Figure 21 shows the **Waveform Buffer** window with the **Waveforms** tab selected.

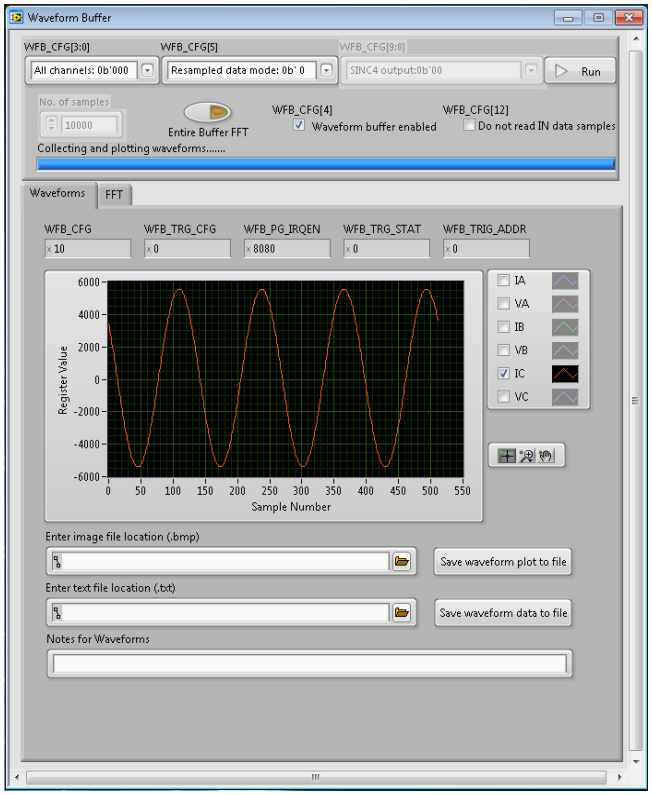


*Figure 21. **Waveforms** Tab in the **Waveform Buffer** Window*

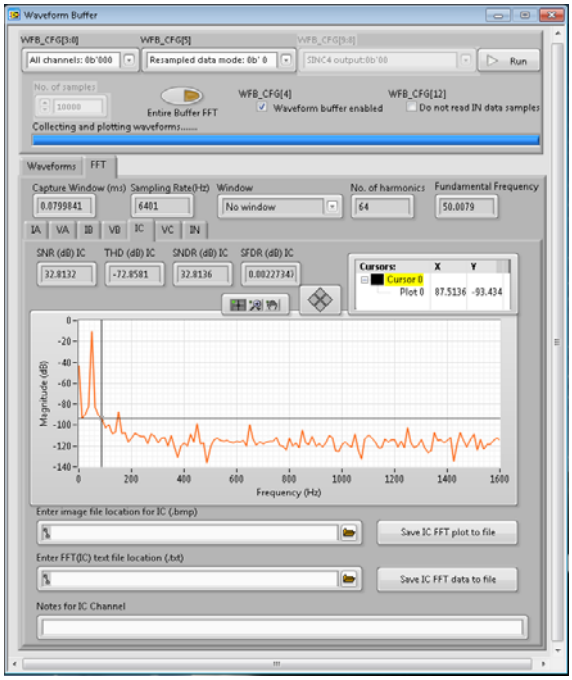


*Figure 22. **FFT** Tab in the **Waveform Buffer** Window*

When the **FFT** tab is selected, the window appears as shown in Figure 22. The FFT of all the waveforms is computed and plotted automatically based on the waveforms. The window allows the user to save the waveform and FFT data into a text file. The waveform and FFT display images can be saved to a .bmp file as well.

ANGLE WINDOW

The **Angle** window is shown in Figure 23. This window allows the user to visualize the angles of three voltage and three current channels with respect to each other. In the **Angle register readings** pane, all nine angle register values are displayed. Using these register results, the angles are computed in degrees and displayed in their respective boxes. The dial to the right of the screen provides a phasor-like representation of the six signals.

The frequency values are displayed below the dial. These values are computed from the **COM PERIOD** and **APERIOD** register values. The **Angle** window does not require the user to perform a write. The user can save the values in the window to a file, perform a single read of the screen quantities, or perform a continuous update of the quantities using the respective options in the window.

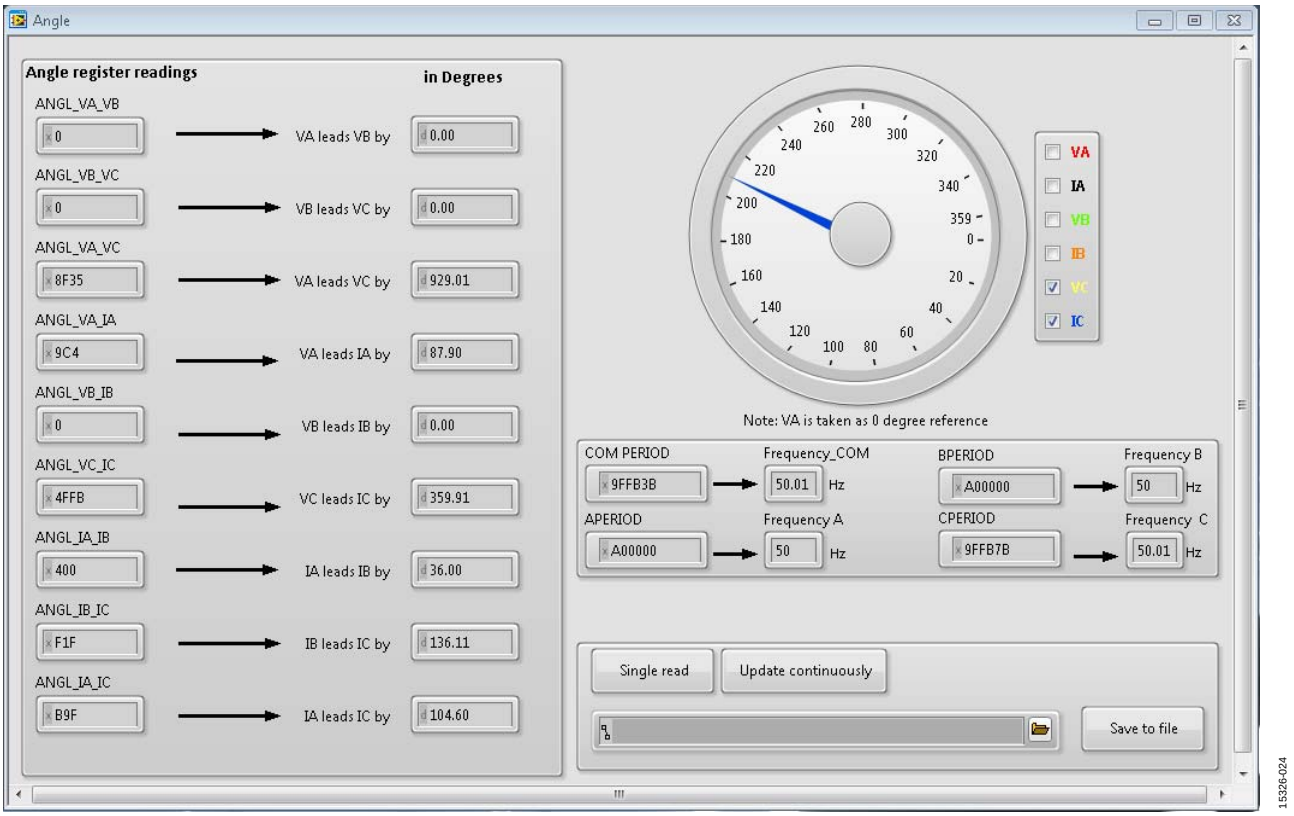


*Figure 23. **Angle** Window*

QUICK STARTUP WINDOW

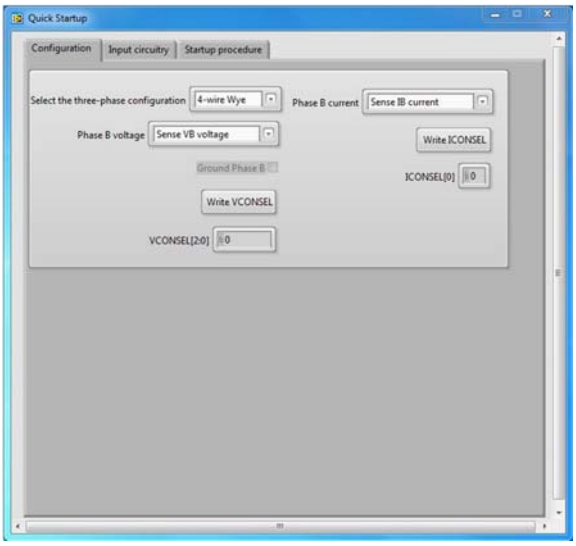
There are three tabs within the **Quick Startup** window: the **Configuration** tab, the **Input circuitry** tab, and the **Startup procedure** tab. The **Startup procedure** tab is the main tab that performs the quick start-up routine, as well as all the necessary initializations. However, before the start-up routine and the initializations, make sure that the inputs are operating in the correct 3-phase configuration and that they are not overranging the ADCs.

The **Configuration** tab accepts the user response on a few parameters and selects the appropriate **VCONSEL[2:0]** and **ICONSEL[0]** settings for the user. The **Input circuitry** tab can be used as a quick calculator for determining if the input signal exceeds the current channel and the voltage channel ADCs inside the ADE9000. By feeding in the system parameters and input signals, along with the PGA setting, the software calculates the signal level at the ADCs. If the signal level exceeds the full-scale range of the ADCs, the indicator turns red. This indication signals to the user that the system parameters must be adjusted.

The **Startup procedure** tab performs the following initialization steps, which must be completed sequentially (see Figure 26):

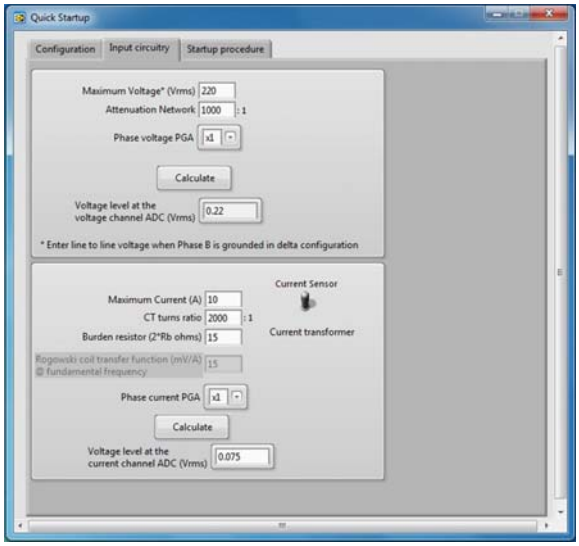
1. Sets the PGA for all channels.
2. Sets SELFREQ and VLEVEL.
3. Enables the integrator and sets **DICOEFF**. This step is skipped for everything except the di/dt sensor.
4. Enables the DSP.
5. Disables the CF1 to CF4 pin outputs, enables the energy and powers functionality, and reads all the energy registers on reset.
6. Performs a quick gain calibration and obtains calibration conversion constants, such as V/LSB, A/LSB, and Wh/LSB.
7. Obtains the CF1DEN to CF4DEN values from the **Meter constant** and writes these values to the registers.
8. Enables the CF1 and CF2 pins and configures them such that the CF1 pin denotes the sum of all the total active energy of the phases and the CF2 pin denotes the sum of all the total reactive energy phases.

These steps must be performed sequentially. The user must click the options in each step to perform the operation.



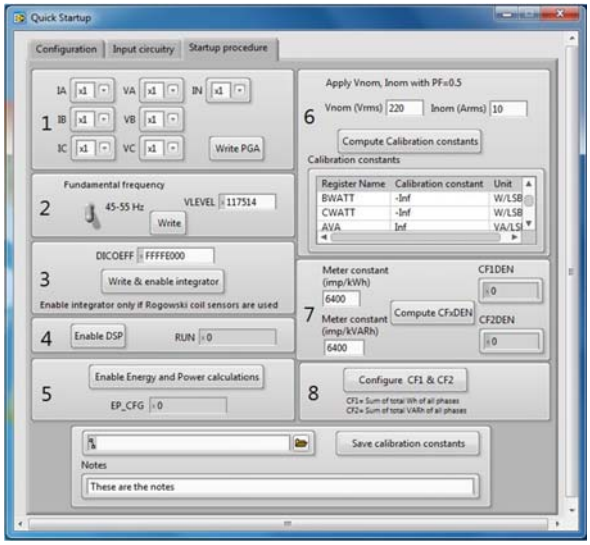
15326-025

*Figure 24. **Configuration** Tab in the **Quick Startup** Window*



15326-026

*Figure 25. **Input Circuitry** Tab in the **Quick Startup** Window*



15326-027

*Figure 26. **Startup Procedure** Tab in the **Quick Startup** Window*

INTERRUPTS WINDOW

The **Interrupts** window displays the status of all the interrupt events. The individual bits of the **STATUS0** and **STATUS1** registers are shown as green LEDs in the window (see Figure 27). If the LED is lit, it indicates that the corresponding status bit is set to 1. Next to each of the LEDs, a checkbox represents the corresponding **MASK0** and **MASK1** bits. If the **MASK1** and **MASK0** bits must be set, select the corresponding checkbox and click **Write Mask Registers**. Click **Write '1' to all set status bits** to reset all status bits simultaneously. If specific values must be written to the status bits, write to the bits using the controls under the **Write to STATUSx registers** option on the screen.

To view the $\overline{\text{IRQ0}}$ and $\overline{\text{IRQ1}}$ pin logic level, click **Check $\overline{\text{IRQx}}$ pin logic state**. If the LED is lit, this means that the pin is in a logic low state. Click **Auto Clear** to reset the interrupts available on the pins on the fly. The $\overline{\text{IRQ0}}$ and $\overline{\text{IRQ1}}$ pins can be monitored on a scope to understand the rate at which the interrupts are being set. The **Route all events to $\overline{\text{IRQ1}}$ pin** option sets the configuration bit that routes all interrupt events to be accessible via the $\overline{\text{IRQ1}}$ pin.

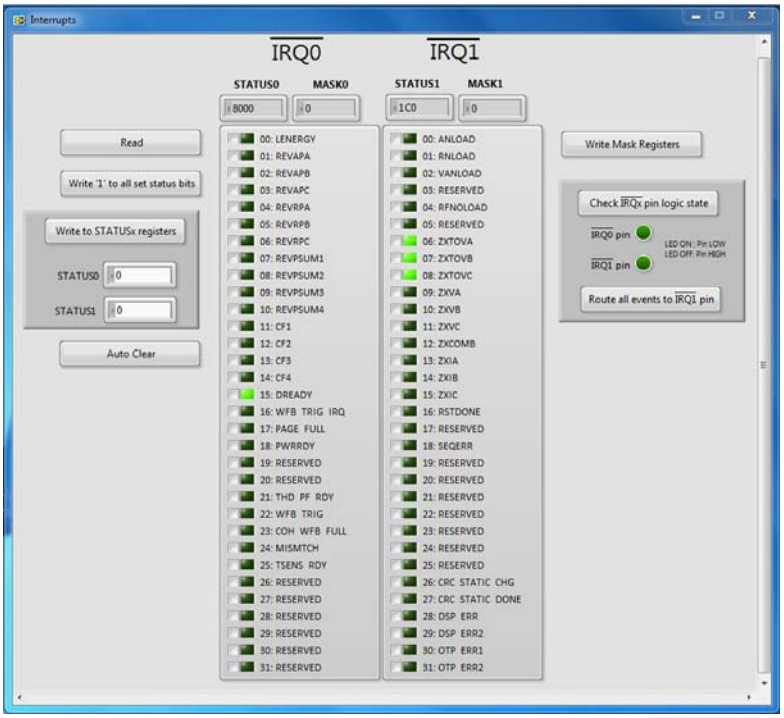


*Figure 27. **Interrupts** Window*

POWER QUALITY WINDOW

The **Power Quality** window allows the user to access all the power quality features of the ADE9000. The window is subdivided into the **Voltage monitor**, **Current monitor**, and **Power Factor and THD** tabs.

Voltage Monitor Tab

The **Voltage monitor** tab is shown in Figure 28. This tab evaluates the **DIP**, **SWELL**, **ZX & ZXTOUT**, **VPEAK**, and **PHASE SEQUENCE ERROR DETECTION** features. This tab allows the user to configure all the control inputs for the features and to monitor the status bits as LEDs. The corresponding mask bits can also be set using the checkboxes in the tab.

Current Monitor Tab

The **Current monitor** tab is shown in Figure 29. This tab is organized in the same way as the **Voltage monitor** tab. The **IPEAK**, **ZX**, and **OI** power quality features are accessible in this tab.

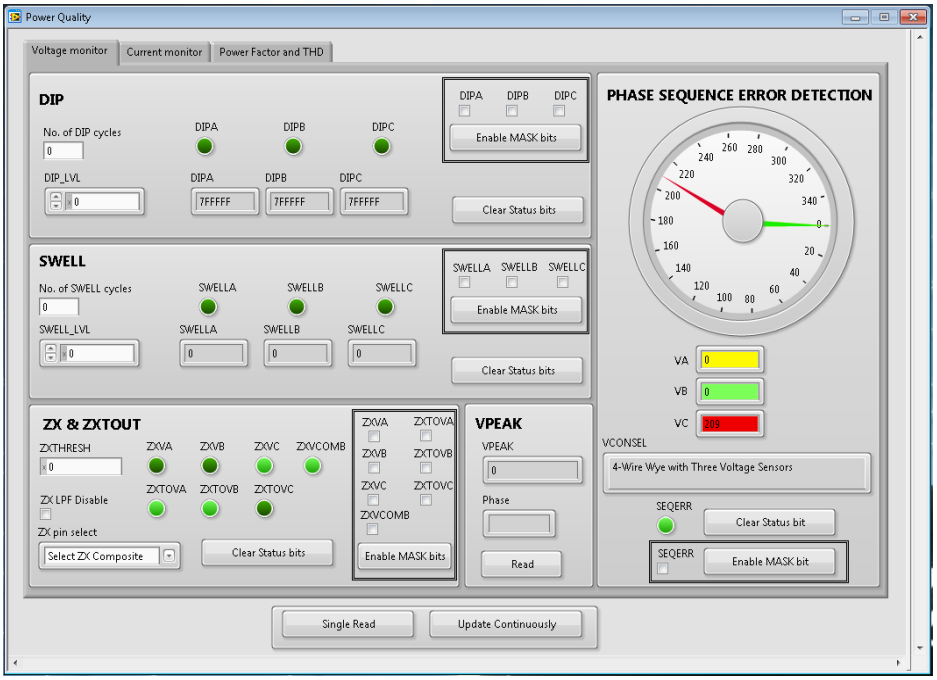


*Figure 28. **Voltage monitor** Tab in the **Power Quality** Window*

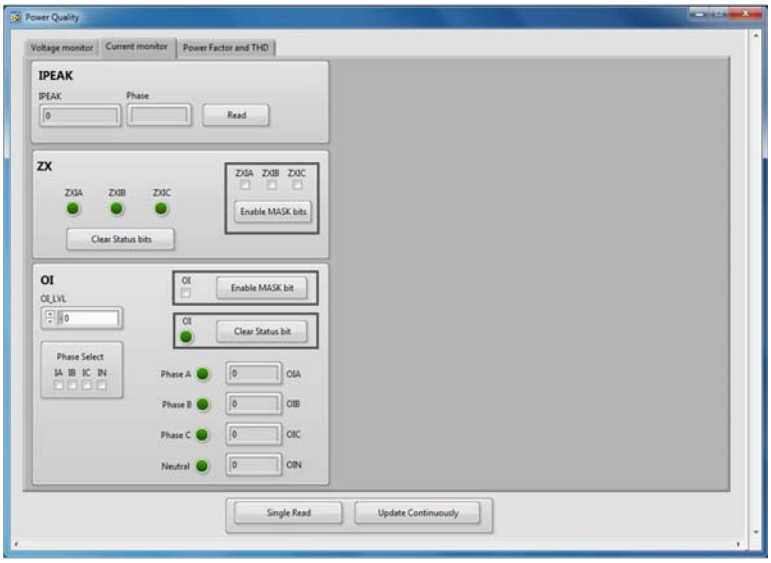


*Figure 29. **Current monitor** Tab in the **Power Quality** Window*

Power Factor and THD Tab

The **Power Factor and THD** tab is shown in Figure 30. This window reads all the power factor and total harmonic distortion (THD) register results from the device, converts these results to meaningful results, and displays them.

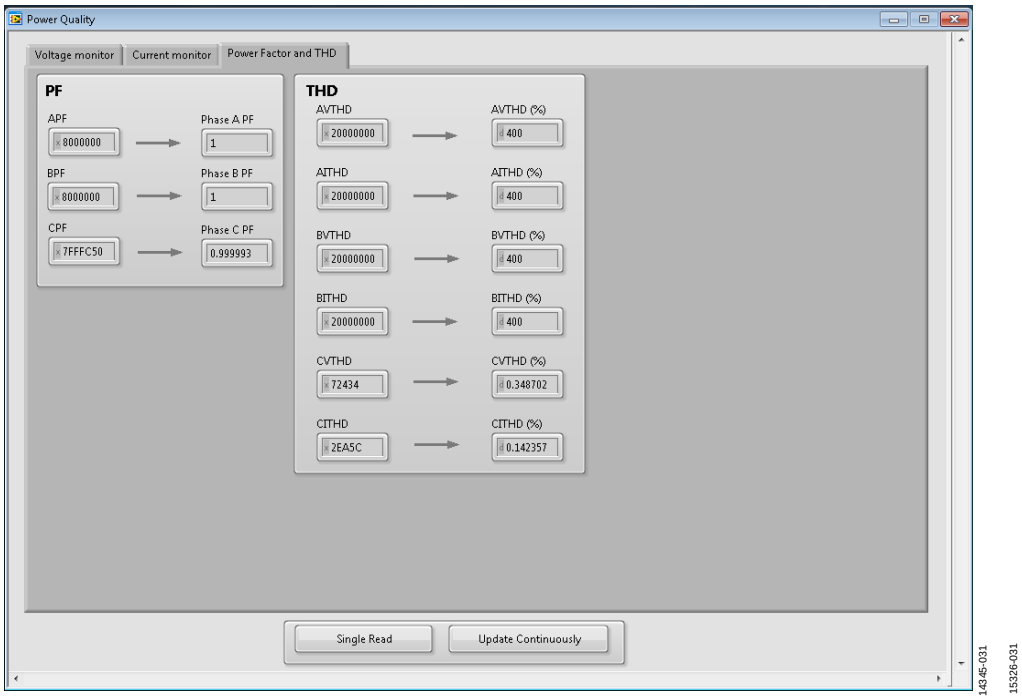


*Figure 30. **Power Factor and THD** Tab in the **Power Quality** Window*

TROUBLESHOOTING

If the software does not detect the SDP-B board, the message shown in Figure 31 is displayed.

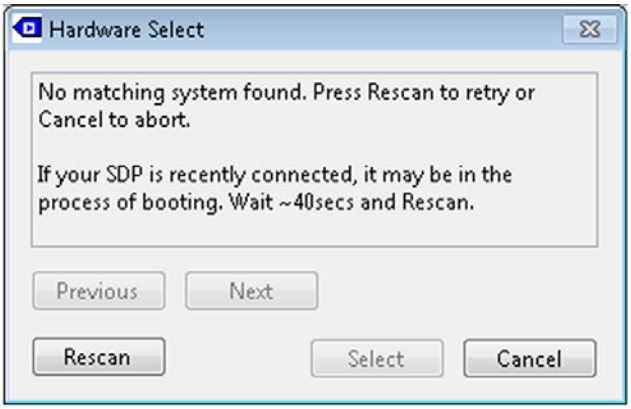


*Figure 31. **Hardware Select** Message*

If this message appears, take the following steps:

1. Verify that the SDP-B board is connected to the PC using the USB cable. The window in Figure 32 appears on the task bar; Windows then installs any other necessary drivers.
2. After the installation is complete, click **Rescan**.
3. When another window appears, check if the LED on the board is flashing; if so, click **Select**.

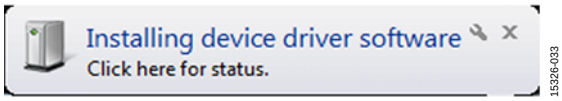


*Figure 32. **Installing device driver software** Message*

EVALUATION BOARD SCHEMATICS AND ARTWORK

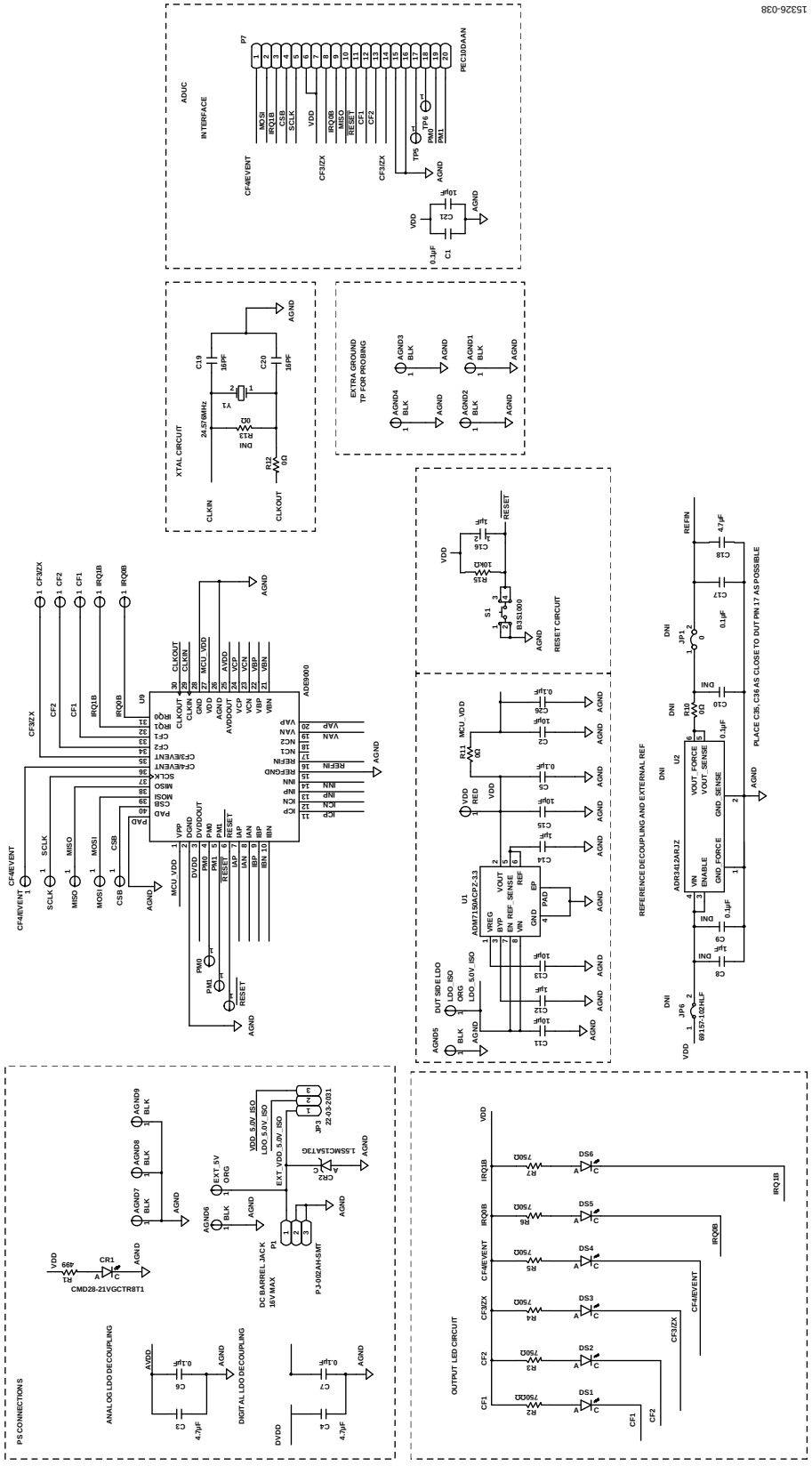


Figure 33. Evaluation Board Schematic—ADE9000

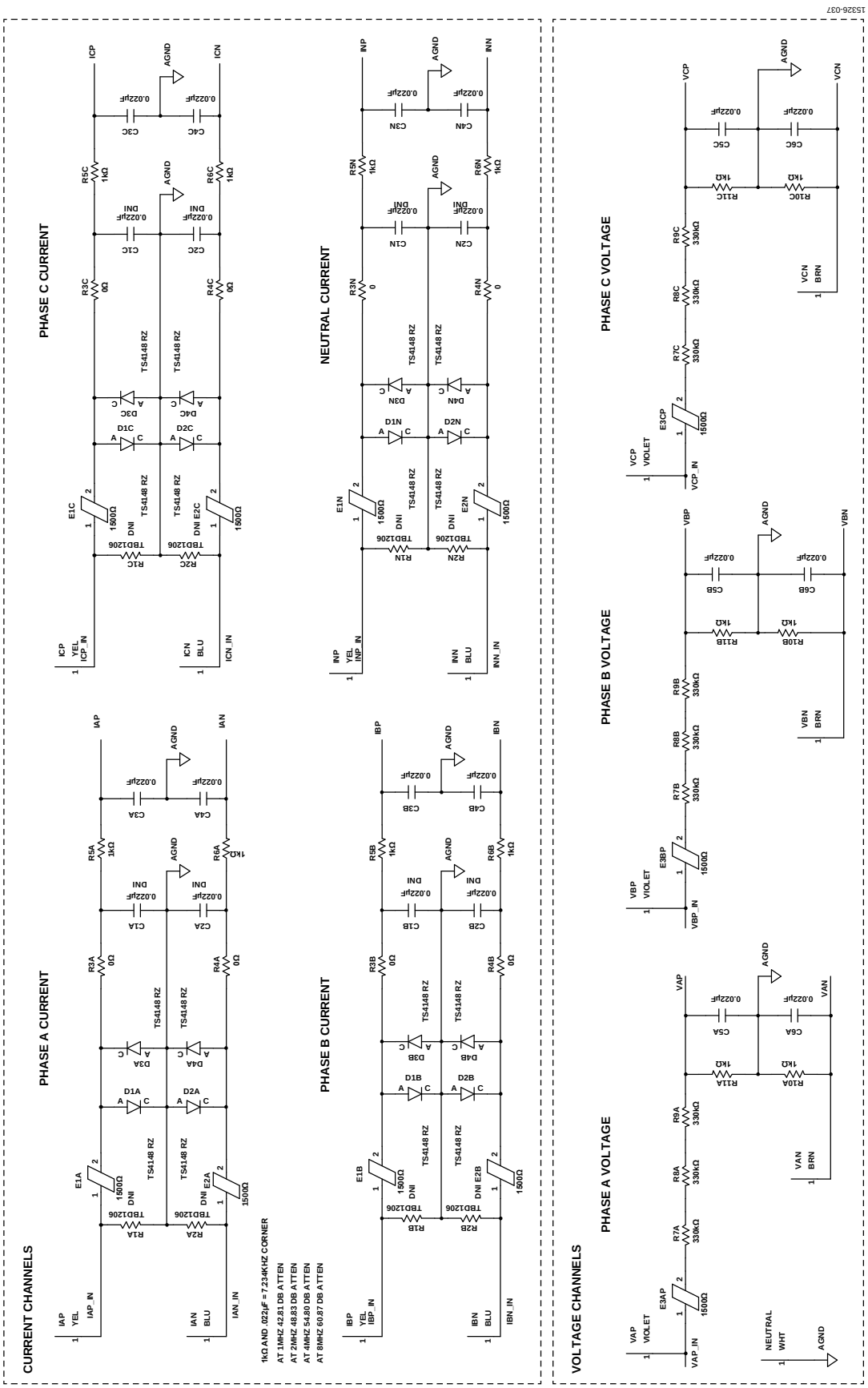


Figure 34. Evaluation Board Schematic—Current and Voltage Channels

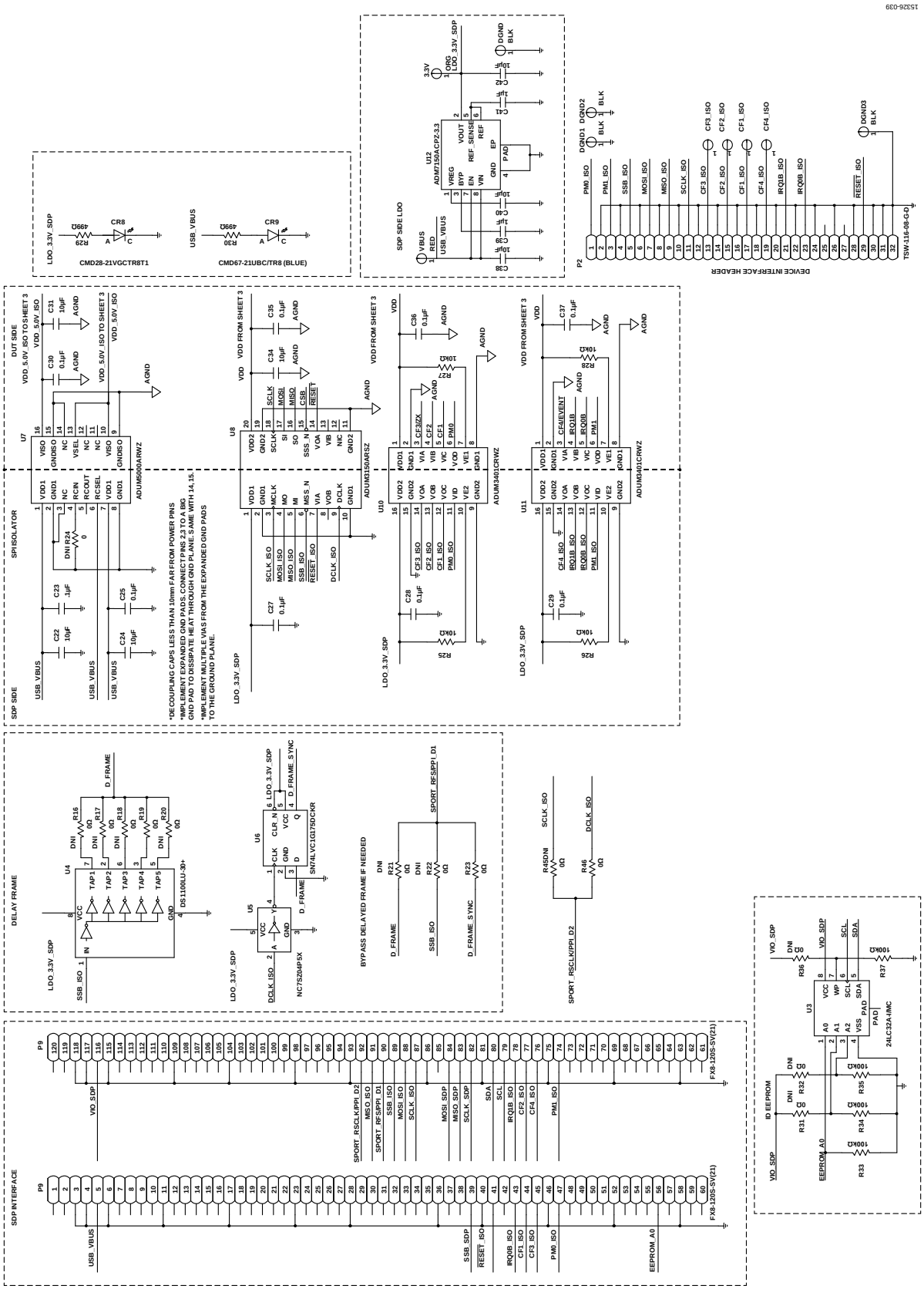


Figure 35. Evaluation Board Schematic—SDP-B Interface and Isolation

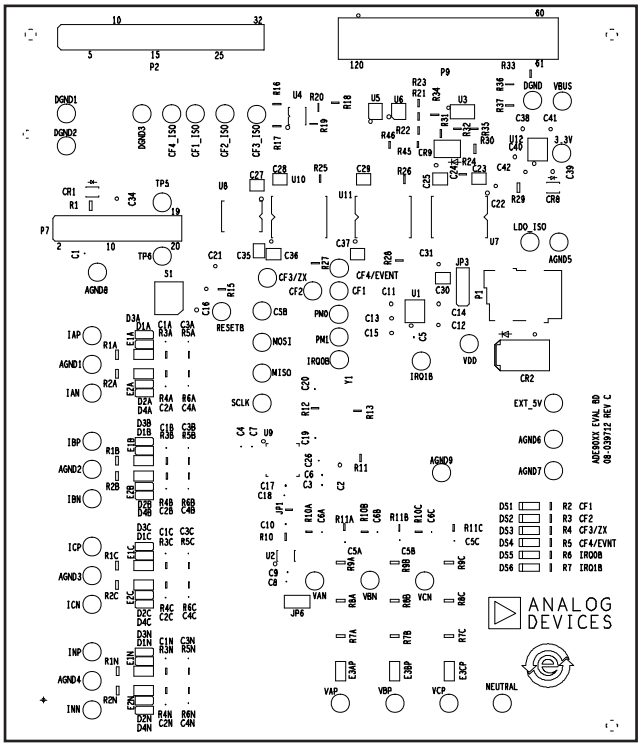


Figure 36. Evaluation Board Silkscreen

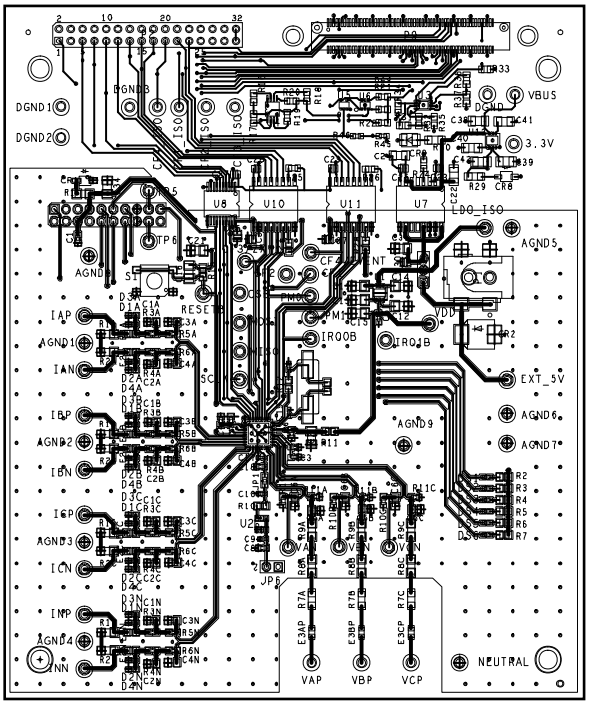


Figure 37. Layout of the Top Layer of the Evaluation Board

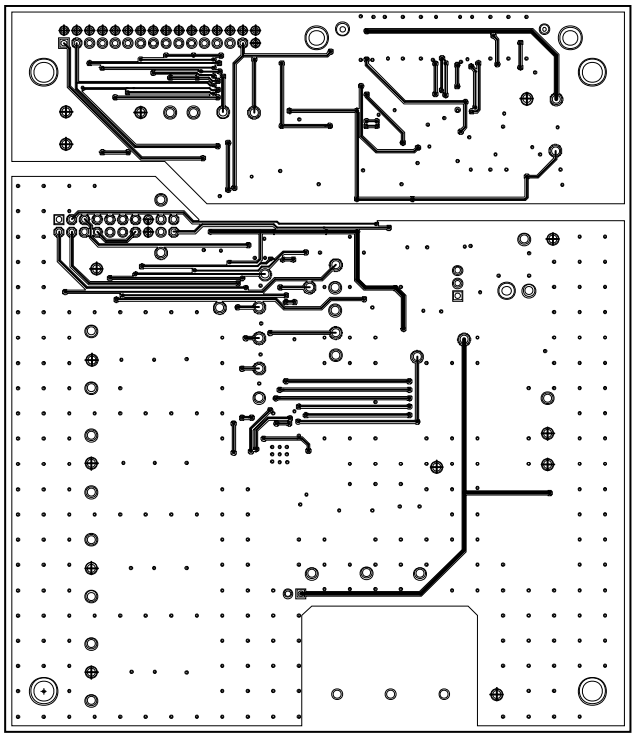


Figure 38. Layout of the Bottom Layer of the Evaluation Board

ORDERING INFORMATION

BILL OF MATERIALS

Table 1.

Qty	Reference Designator	Description	Value[1]	Tolerance (Ω)[1]	Voltage (V)[1]	Part Number
1	Not applicable	Printed circuit board (PCB)	N/A	N/A	N/A	08_039712c
3	3.3 V, EXT_5V, LDO_ISO	Connector; PCB test point, orange	Orange	N/A	N/A	TP104-01-03
13	DGND, AGND1 to AGND9, DGND1 to DGND3	Connector; PCB test point, black	Black	N/A	N/A	TP-104-01-00
5	C1, C5 to C7, C26	Capacitor, ceramic, chip, X8R	0.1 µF	10	25	C1608X8R1E104K
12	C2, C11, C13, C15, C21, C22, C24, C31, C34, C38, C40, C42	Capacitor, ceramic, monolithic, X7R	10 µF	10	25	GRM31CR71E106KA12L
5	C12, C14, C16, C39, C41	Capacitor, ceramic, chip, 1206, X7R	1 µF	10	35	GMK316B7105KL-T
1	C17	Capacitor, ceramic, X7R, 0402	0.1 µF	10	16	GRM155R71C-104KA88D
3	C3, C4, C18	Capacitor, monolithic, ceramic, X5R	4.7 µF	10	6.3	GRM188R60J-475KE19
2	C19, C20	Capacitor, chip, monolithic, ceramic, C0G, 0402	16 pF	5	50	GJM1555C1H160JB01D
9	C23, C25, C27 to C30, C35 to C37	Capacitor, ceramic, X7R	0.1 µF	10	10	0306ZC104KAT2A
14	C3A to C6A, C3B to C6B, C3C to C6C, C3N, C4N	Capacitor, ceramic, multilayer, C0G	0.022 µF	5	50	C2012C0G1H223J
19	CF1, CF2, $\overline{CS}$, PM0, PM1, TP5, TP6, MISO, MOSI, SCLK, $\overline{IRQ0}$, $\overline{IRQ1}$, CF3/ZX, $\overline{RESET}$, CF1_ISO to CF4_ISO, CF4/EVENT	Connector; PCB test point, gray	Gray	N/A	N/A	TP104-01-08
2	CR1, CR8	Diode, LED, green, SMD	CMD28-21VGCTR8T1	N/A	2.1	CMD28-21VGCTR8T1
1	CR2	Diode, Zener TVS	1.5SMC15AT3G	N/A	15	1.5SMC15AT3G
1	CR9	LED, blue, surface-mount	CMD67-21UBC/TR8 (blue)	N/A	4.5	CMD67-21UBC/TR8
16	D1A to D4A, D1B to D4B, D1C to D4C, D1N to D4N	Diode, high speed switching	TS4148 RZ	N/A	100	TS4148 RZ
6	DS1 to DS6	LED red, surface-mount	LNJ208R8ARA (red)	N/A	2.5	LNJ208R8ARA
11	E1A, E1B, E1C, E1N, E2A, E2B, E2C, E2N, E3AP, E3BP, E3CP	Inductor, chip, ferrite bead, 0805	1500 Ω	25	N/A	BLM21BD152SN1D
4	IAN, IBN, ICN, INN	Connector; PCB test point, blue	Blue	N/A	N/A	TP104-01-06
4	IAP, IBP, ICP, INP	Connector; PCB test point, yellow	Yellow	N/A	N/A	TP-104-01-04
1	JP3	Connector; PCB header, 2.54 mm, 3 position, vertical	22-03-2031	N/A	N/A	22-03-2031
1	NEUTRAL	Connector; PCB test point, white	White	N/A	N/A	TP-104-01-09
1	P1	Connector; PCB, use E022246 for 4-pin power jack from the CN4P_V6 folder	PJ-002AH-SMT	N/A	N/A	PJ-002AH-SMT
1	P7	Connector; PCB BERG header, ST male, 20-pin	PEC10DAAN	N/A	N/A	PEC10DAAN

Qty	Reference Designator	Description	Value[1]	Tolerance (Ω)[1]	Voltage (V)[1]	Part Number
1	P9	Connector; PCB, board to board receptacle, ST, 0.6 mm pitch	FX8-120S-SV(21)	N/A	N/A	FX8-120S-SV(21)
3	R1, R29, R30	Resistor, precision, thick film, chip, R1206	499	1	N/A	ERJ-8ENF4990V
6	R10A, R10B, R10C, R11A, R11B, R11C	Resistor, film, SMD, 0603	1 kΩ	0.1	N/A	ERA-3YEB102V
4	R11, R12, R19, R23	Resistor, thick film, chip	0		N/A	ERJ-6GEY0R00V
5	R15, R25 to R28	Resistor, precision, thick film, chip, R0805	10 kΩ	1	N/A	ERJ-6ENF1002V
6	R2 to R7	Resistor, precision, thick film, chip, R0805	750	1	N/A	ERJ-6ENF7500V
4	R33 to R35, R37	Resistor, precision, thick film, chip, R0805	100 kΩ	1	N/A	ERJ-6ENF1003V
9	R3A, R3B, R3C, R3N, R46, R4A, R4B, R4C, R4N	Resistor, film, SMD, 0603	0	5	N/A	ERJ-3GEY0R00V
8	R5A, R5B, R5C, R5N, R6A, R6B, R6C, R6N	Resistor, precision, thick film, chip, R0603	1 kΩ	1	N/A	ERJ-3EKF1001V
9	R7A to R9A, R7B to R9B, R7C to R9C	Resistor, high voltage, thin film, flat chip	33 kΩ	0.1	N/A	TNPV1206330KBEEN
1	S1	SW SM mechanical keyswitch	B3S1000	N/A	N/A	B3S1000
2	U1, U12	Analog Devices, Inc. IC, 800 mA, ultralow noise, high PSRR, RF linear regulator (3.3 V output)	N/A	N/A	N/A	ADM7150ACPZ-3.3
2	U10, U11	Analog Devices IC, quad-channel digital isolator	N/A	N/A	2.7 to 5.5	ADuM3401CRWZ
1	U3	IC, 32 kB, I^2C serial EEPROM	24LC32A-I/MC	N/A	N/A	24LC32A-I/MC
1	U4	IC, 3.3 V to 5-tap economy timing element	DS1100LU-30+	N/A	N/A	DS1100LU-30+
1	U5	IC, tiny logic UHS inverter	NC7SZ04P5X	N/A	N/A	NC7SZ04P5X
1	U6	IC-TTL, single D-type flip-flop with asynchronous clear	SN74LVC1G175DCKR	N/A	N/A	SN74LVC1G175-DCKR
1	U7	Analog Devices IC, 2.5 kV, isolated dc-to-dc converter	N/A	N/A	N/A	ADuM5000ARWZ
1	U8	Analog Devices IC, 3.75 kV, 6-channel, SPIsolator® digital isolator for SPI with delay clock	N/A	N/A	N/A	ADuM3150ARSZ
1	U9	Analog Devices IC, high performance, polyphase, energy metering AFE	N/A	N/A	N/A	ADE9000
3	VAN, VBN, VCN	Connector; PCB test point, brown	Brown	N/A	N/A	TP104-01-01
3	VAP, VBP, VCP	Connector; PCB test point, violet	Violet	N/A	N/A	TP104-01-07
2	VDD, VBUS	Connector; PCB test point, red	Red	N/A	N/A	TP-104-01-02
1	Y1	IC, crystal SMD, low profile	24.576 MHz	N/A	N/A	ABLS-24.576MHZ-8-L4Q-F-T

[1] N/A means not applicable.

NOTES

I^2C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).



ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Legal Terms and Conditions
By using the evaluation board discussed herein (together with any tools, components documentation or support materials, the "Evaluation Board"), you are agreeing to be bound by the terms and conditions set forth below ("Agreement") unless you have purchased the Evaluation Board, in which case the Analog Devices Standard Terms and Conditions of Sale shall govern. Do not use the Evaluation Board until you have read and agreed to the Agreement. Your use of the Evaluation Board shall signify your acceptance of the Agreement. This Agreement is made by and between you ("Customer") and Analog Devices, Inc. ("ADI"), with its principal place of business at One Technology Way, Norwood, MA 02062, USA. Subject to the terms and conditions of the Agreement, ADI hereby grants to Customer a free, limited, personal, temporary, non-exclusive, non-sublicensable, non-transferable license to use the Evaluation Board FOR EVALUATION PURPOSES ONLY. Customer understands and agrees that the Evaluation Board is provided for the sole and exclusive purpose referenced above, and agrees not to use the Evaluation Board for any other purpose. Furthermore, the license granted is expressly made subject to the following additional limitations: Customer shall not (i) rent, lease, display, sell, transfer, assign, sublicense, or distribute the Evaluation Board; and (ii) permit any Third Party to access the Evaluation Board. As used herein, the term "Third Party" includes any entity other than ADI, Customer, their employees, affiliates and in-house consultants. The Evaluation Board is NOT sold to Customer; all rights not expressly granted herein, including ownership of the Evaluation Board, are reserved by ADI. CONFIDENTIALITY. This Agreement and the Evaluation Board shall all be considered the confidential and proprietary information of ADI. Customer may not disclose or transfer any portion of the Evaluation Board to any other party for any reason. Upon discontinuation of use of the Evaluation Board or termination of this Agreement, Customer agrees to promptly return the Evaluation Board to ADI. ADDITIONAL RESTRICTIONS. Customer may not disassemble, decompile or reverse engineer chips on the Evaluation Board. Customer shall inform ADI of any occurred damages or any modifications or alterations it makes to the Evaluation Board, including but not limited to soldering or any other activity that affects the material content of the Evaluation Board. Modifications to the Evaluation Board must comply with applicable law, including but not limited to the RoHS Directive. TERMINATION. ADI may terminate this Agreement at any time upon giving written notice to Customer. Customer agrees to return to ADI the Evaluation Board at that time. LIMITATION OF LIABILITY. THE EVALUATION BOARD PROVIDED HEREUNDER IS PROVIDED "AS IS" AND ADI MAKES NO WARRANTIES OR REPRESENTATIONS OF ANY KIND WITH RESPECT TO IT. ADI SPECIFICALLY DISCLAIMS ANY REPRESENTATIONS, ENDORSEMENTS, GUARANTEES, OR WARRANTIES, EXPRESS OR IMPLIED, RELATED TO THE EVALUATION BOARD INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, TITLE, FITNESS FOR A PARTICULAR PURPOSE OR NONINFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS. IN NO EVENT WILL ADI AND ITS LICENSORS BE LIABLE FOR ANY INCIDENTAL, SPECIAL, INDIRECT, OR CONSEQUENTIAL DAMAGES RESULTING FROM CUSTOMER'S POSSESSION OR USE OF THE EVALUATION BOARD, INCLUDING BUT NOT LIMITED TO LOST PROFITS, DELAY COSTS, LABOR COSTS OR LOSS OF GOODWILL. ADI'S TOTAL LIABILITY FROM ANY AND ALL CAUSES SHALL BE LIMITED TO THE AMOUNT OF ONE HUNDRED US DOLLARS ($100.00). EXPORT. Customer agrees that it will not directly or indirectly export the Evaluation Board to another country, and that it will comply with all applicable United States federal laws and regulations relating to exports. GOVERNING LAW. This Agreement shall be governed by and construed in accordance with the substantive laws of the Commonwealth of Massachusetts (excluding conflict of law rules). Any legal action regarding this Agreement will be heard in the state or federal courts having jurisdiction in Suffolk County, Massachusetts, and Customer hereby submits to the personal jurisdiction and venue of such courts. The United Nations Convention on Contracts for the International Sale of Goods shall not apply to this Agreement and is expressly disclaimed.

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