



EV-AD4020-REF-DGNZ Reference Design Board User Guide UG-1280

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20-Bit, High Accuracy Data Acquisition Reference Design Board

FEATURES

- 20-bit, high accuracy data acquisition reference design board
- Versatile analog signal conditioning circuitry
- On-board reference, reference buffers, and ADC drivers
- PC software for control and data analysis of time and frequency domain, including INL and DNL capability
- Software programmable gain options (1, 2, 5 and 10)
- Single-ended and fully differential bipolar input ranges: $\pm 10\text{ V}$ to $\pm 1\text{ V}$
- Active filtering and overranging option
- Averaging capability (102 dB at 900 kSPS)
- Compatible with [SDP-H1](#) controller board

EVALUATION BOARD KIT CONTENTS

- EV-AD4020-REF-DGNZ reference design board
- 12 V wall adapter power supply
- Standard USB A to mini B USB cable

EQUIPMENT NEEDED

- [SDP-H1](#) controller board
- High precision signal source
- Cable with SMA input to evaluation board
- PC running Windows® operating system
- Band-pass filter suitable for 20-bit testing (value based on signal frequency)

SOFTWARE NEEDED

- [AD4020](#) Reference Design Software
- [ADI SDP Drivers](#)

GENERAL DESCRIPTION

The EV-AD4020-REF-DGNZ reference design board incorporates a unique Analog Devices, Inc., programmable gain instrumentation amplifier (PGIA) designed using off the shelf, discrete components, a 20-bit, 1.8 MSPS, successive approximation register (SAR) analog-to-digital converter (ADC), a 5 V reference, a reference buffer, and on-board power supply circuitry. The EV-AD4020-REF-DGNZ reference design board is optimized for 20-bit precision and offers superior linearity with a typical integral nonlinearity (INL) of ± 2 ppm, low offset and gain error drift, and trackable noise and distortion (over -115 dB) performance at a full speed of 1.8 MSPS for all gain options. The EV-AD4020-REF-DGNZ reference design board is suitable for use in high end data acquisition instruments and automated test equipment applications that typically require high input impedance and have varying common-mode voltages present. The EV-AD4020-REF-DGNZ reference design board can resolve either bipolar or unipolar, single-ended or fully differential input ranges up to $\pm 10\text{ V}$ with four software programmable gain options of 1, 2, 5, and 10. In addition, the EV-AD4020-REF-DGNZ reference design board allows higher order antialiasing filtering and overrange calibration options in the PGIA.

The EV-AD4020-REF-DGNZ reference design board (see Figure 1) is compatible with the Analog Devices [EVAL-SDP-CH1Z](#) system demonstration platform ([SDP-H1](#)) controller board, and interfaces to the [SDP-H1](#) controller board via a 120-pin connector. The JP1 and JP2 Subminiature Version A (SMA) connectors are provided for connecting the low noise analog signal source.

For full details on the [AD4020](#), see the [AD4020](#) data sheet, which must be consulted in conjunction with this user guide when using the EV-AD4020-REF-DGNZ reference design board.

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REVISION HISTORY

5/2019—Revision 0: Initial Version

REFERENCE DESIGN BOARD PHOTOGRAPH



Figure 1.

16786-001

REFERENCE DESIGN BOARD HARDWARE

POWER SUPPLIES

The [SDP-H1](#) controller board supplies 12 V to power the necessary rails for the EV-AD4020-REF-DGNZ reference design board (see Table 1).

Table 1. Power Supplies Provided on the Board

Power Supply (V)	Function
5, 7 (default)	Reference, amplifiers rails
-1 (default)	Amplifiers rail
-15, +15	Amplifiers rails
1.8, 3.3	ADC power

Each supply is decoupled where it enters the board, and again where it connects to each device. A single ground plane is used on this board to minimize the effect of high frequency noise interference.

A benchtop power supply powers the EV-AD4020-REF-DGNZ reference design board. The P1 and P3 screw terminals are provided for this function. When benchtop power is used, the on-board power supplies are no longer required. Soldier links JP4 Pin 2, JP4 Pin 3, JP5 Pin 1, and JP5 Pin 2 must be changed, as well.

SDP-H1 CONTROLLER BOARD

The EV-AD4020-REF-DGNZ reference design board uses serial port interface (SPI), and is connected to the high speed [SDP-H1](#) controller board. The [SDP-H1](#) controller board requires a power supply from a 12 V wall adapter. The [SDP-H1](#) controller board has a Xilinx® Spartan 6 and an [ADSP-BF527](#) processor with connectivity to the PC through a USB 2.0 high speed port. The [SDP-H1](#) controller boards allows the configuration and capture of data on daughter boards from the PC via the USB.

The [SDP-H1](#) controller board has a field programmable gate array (FPGA) mezzanine card (FMC), low pin count (LPC) connector with fully differential low voltage differential signaling (LVDS), and single-ended, low voltage complimentary metal-oxide semiconductor (LVCMOS) support. The [SDP-H1](#) has the same 120- or 160-pin connector found on the [SDP-B](#) controller board, which exposes the Blackfin® processor peripherals. This connector provides a configurable, serial, parallel I²C and SPI, and general-purpose input/output (GPIO) communication lines to the attached daughter board.

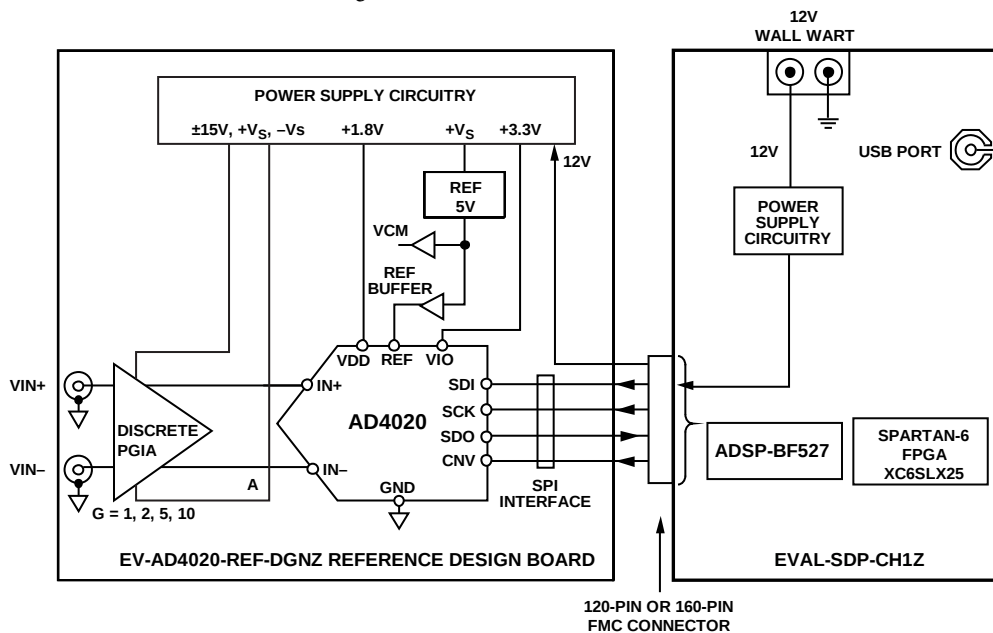


Figure 2. Simplified Evaluation Board Block Diagram

ANALOG INPUTS

The analog inputs to the EV-AD4020-REF-DGNZ reference design board are SMA connectors J1 and J2. These inputs are fed to a high impedance input amplifier with programmable gain settings set by a multiplexer.

The EV-AD4020-REF-DGNZ reference design board is factory configured for providing either a single-ended path or a fully differential path.

For dynamic performance, a fast Fourier transform (FFT) test can be performed by applying a low distortion ac source.

For low frequency testing, the audio precision source (such as the Audio Precision SYS-2700 series) can be used directly because of the isolated outputs on the signal source. Set the outputs for balanced and floating ground. Different precision sources can be used with additional filtering.

Table 2. Jumper Detail with Factory Default Setting

Link	Default	Function	Comment
JP1	Pin 1 to Pin 2	VDD supply	Change Pin 2 to Pin 3 when using VDD bench
JP2	Pin 1 to Pin 2	V_DRIVE (VIO)	Change Pin 2 to Pin 3 when using V_DRIVE bench
JP3	Pin 1 to Pin 2	U7 frequency select	Change Pin 2 to Pin 3 when using low frequency
JP4	Pin 1 to Pin 2	+VS	Change Pin 2 to Pin 3 when using +VS bench
JP5	Pin 2 to Pin 3	–VS	Change Pin 1 to Pin 2 when using –VS bench
JP6	Pin 1 to Pin 2	15 V	Not applicable
JP7	Pin 1 to Pin 2	–15 V	Not applicable
JP8	Insert 0 Ω	Voltage reference	Change link to JP9 when using external VREF
JP9	Open	VREF bench	Insert 0 Ω when using external VREF and JP8 is open

REFERENCE DESIGN BOARD SOFTWARE QUICK START PROCEDURES

SOFTWARE INSTALLATION PROCEDURES

Download the [AD4020](#) reference design software from the following location: C:\Program Files\Analog Devices\AD40XX Evaluation Software\EVAL-AD40XX. This location contains the executable software and example files.

Install the [AD4020](#) reference design software before connecting the [SDP-H1](#) controller board to the USB port of the PC to ensure that the [SDP-H1](#) controller board is recognized when it connects to the PC.

Proceed through the installation, allowing the [AD4020](#) reference design software and drivers to be placed in the appropriate locations. Connect the [SDP-H1](#) controller board to the PC only after the [AD4020](#) reference design software and drivers are installed.

Installing the [AD4020](#) Reference Design Software

To install the [AD4020](#) reference design software, take the following steps:

1. Start the Windows operating system and download the software.
2. Unzip the downloaded file. Run the **setup.exe** file.
3. The [AD4020](#) reference design software installation window opens, as shown in Figure 3.

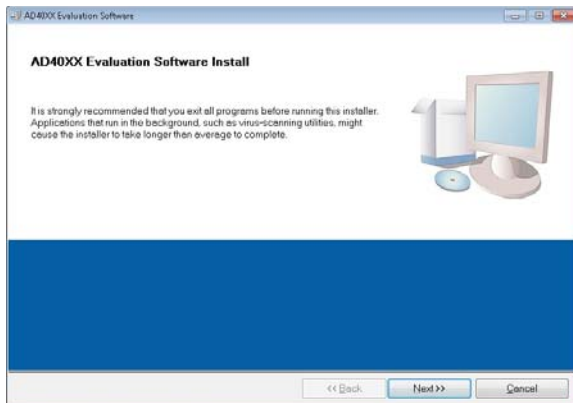


Figure 3. [AD4020](#) Reference Design Software Installation Window

4. Click **Browse** and choose the folder location for installation, and then click **Next>>**. The default folder is shown in Figure 4.

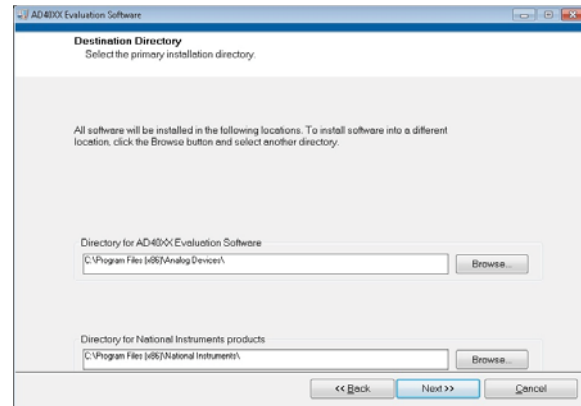


Figure 4. Destination Directory

5. Select **I accept the License Agreement** to accept the National Instruments software license agreement, and then click **Next>>** (see Figure 5).

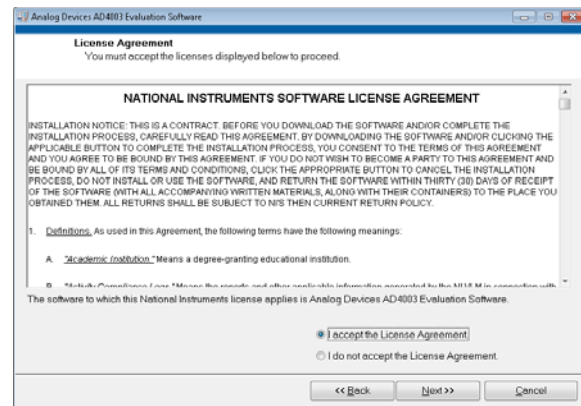


Figure 5. License Agreement

6. Click **Next>>** again to install the [AD4020](#) reference design software (see Figure 6).

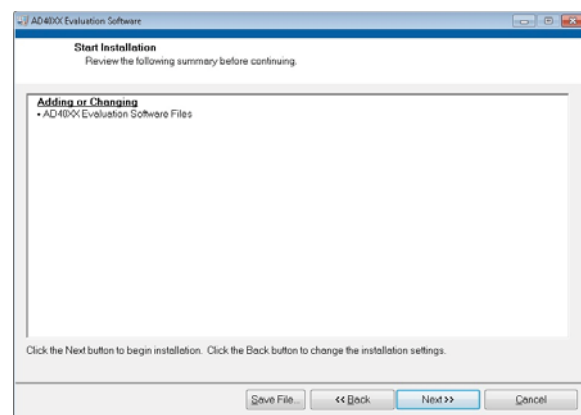


Figure 6. Start Installation

7. A pop-up window opens and displays a bar showing the installation progress, as shown in Figure 7.

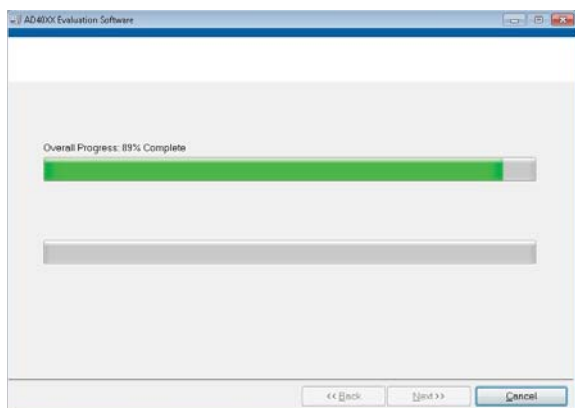


Figure 7. Overall Progress

8. After the installation progress reaches 100%, click **Next>>** to complete the installation (see Figure 8).

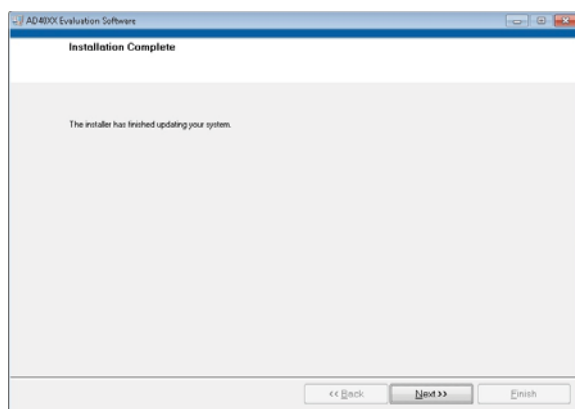


Figure 8. AD4020 Reference Design Software Installation Complete

Installing the ADI SDP Drivers

The ADI SDP drivers related to the SDP-H1 controller board must be installed for the EV-AD4020-REF-DGNZ reference design board to function properly. To install the drivers, take the following steps:

1. After the AD4020 reference design software installation is complete, click **Next>>**, as shown in Figure 8. This command starts the SDP-H1 driver installation, as shown in Figure 9.

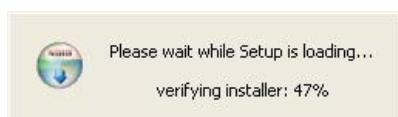


Figure 9. Beginning of SDP-H1 Driver Installation

2. The ADI SDP drivers Setup Wizard opens. Click **Next>>** to install the ADI SDP drivers (see Figure 10).



Figure 10. ADI SDP Drivers Setup Wizard

3. Click **Browse** and choose the installation location, and then click **Install**. The default folder is shown in Figure 11.

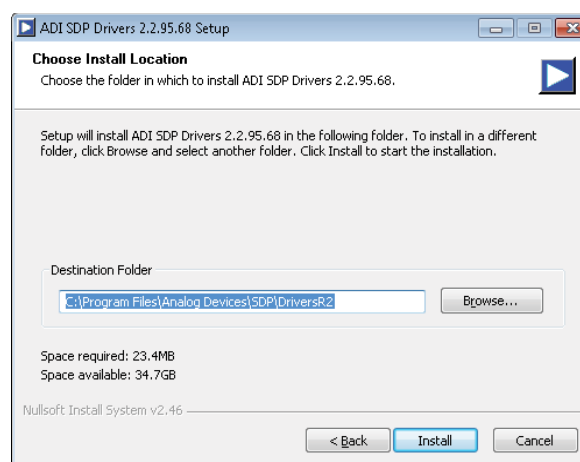


Figure 11. Choose Installation Location

4. The installation begins and a progress bar is displayed (see Figure 12).

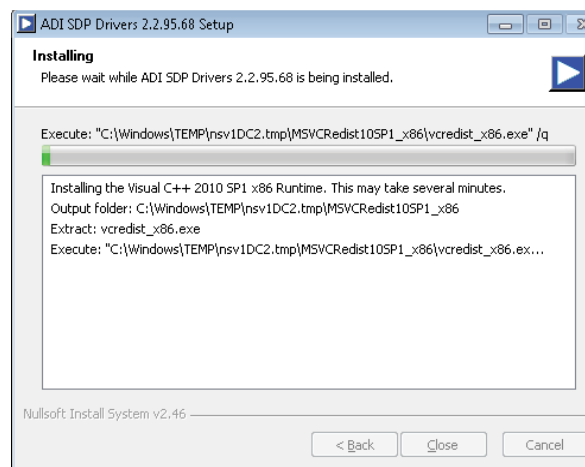


Figure 12. ADI SDP Drivers Installing

- When the progress bar is completed, click **C**lose to finish the installation (see Figure 13).

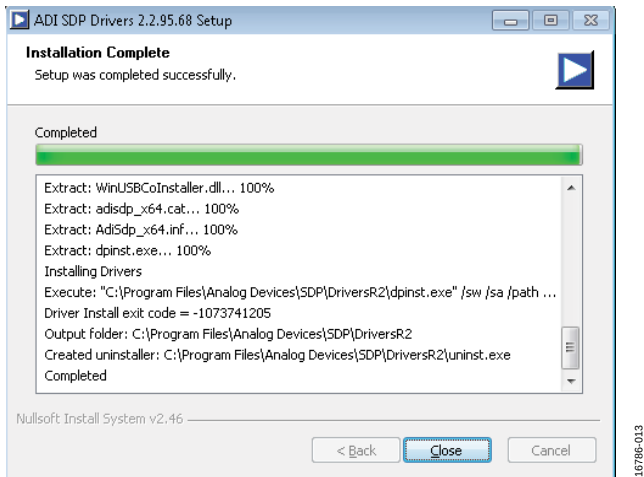


Figure 13. ADI SDP Drivers Installation Complete

BOARD OPERATION AND CONNECTION SEQUENCE

- Connect the **SDP-H1** controller board to the EV-AD4020-REF-DGNZ reference design board with the J5 connector. Screw the J5 connector into place as required. The **AD4020** reference design software is configured to find the evaluation board on either connector of the **SDP-H1** controller board.
- Power up the **SDP-H1** controller board with the appropriate power supply, as described in the Power Supplies section.
- Connect the **SDP-H1** controller board to the PC with the USB cable provided in the evaluation board kit.
- When the **SDP-H1** controller board is first plugged in via the USB cable, allow the new found hardware wizard to run. Look at the **Device Manager** of the PC to ensure that the **ADI SDP drivers** and the **SDP-H1** controller board are connected properly. **Analog Devices System Development Platform (32 MB)** appears under **ADI Development Tools** (see Figure 14).

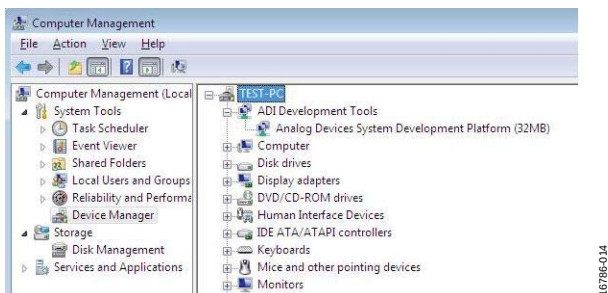


Figure 14. Device Manager

- Click **Start**, then click **All Programs**, and then click **Analog Devices\AD4020 Reference Design Software** to start the **AD4020** reference design software.
- Apply the signal source and capture the data.

RUNNING THE SOFTWARE WITH THE HARDWARE CONNECTED

To run the **AD4020** reference design software with the EV-AD4020-REF-DGNZ reference design board and the **SDP-H1** controller board connected together, take the following steps:

- Click **Start > All Programs > Analog Devices > AD4020 Reference Design Software** to launch the software. To uninstall the program, click **Start > Control Panel > Programs and Features > AD4020 Reference Design Software**.

After the **AD4020** reference design software starts, it automatically seeks to find the hardware connected. When no hardware is connected, the **AD4020** reference design software displays a connectivity error when started (see Figure 15). If this error occurs, connect the EV-AD4020-REF-DGNZ reference design board to the **SDP-H1** controller board, and connect the **SDP-H1** controller board to the USB port of the PC. Wait a few seconds, and then click **Rescan** and follow the instructions.

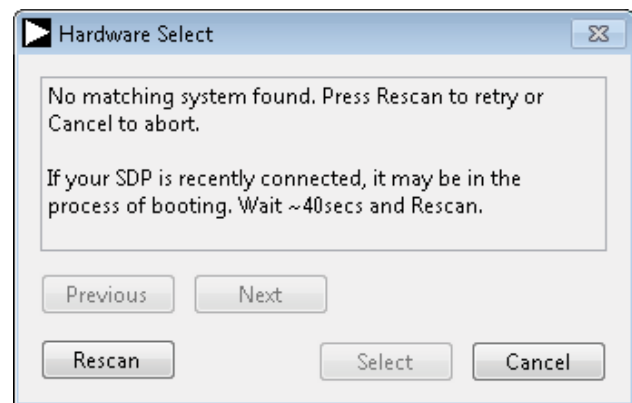


Figure 15. SDP-H1 Board Not Connected to USB Port Error Rescan

- If **Cancel** is clicked, a message appears, as shown in Figure 16.

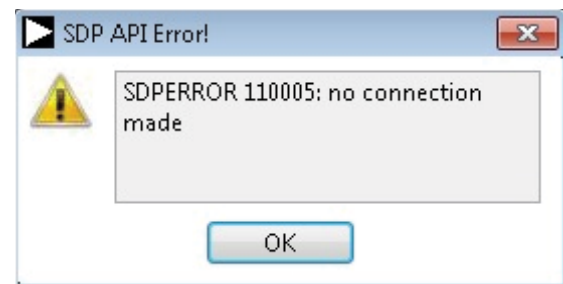


Figure 16. SDP-H1 Board Not Connected to USB Port Error

3. After **Rescan** is clicked, the [AD4020](#) reference design software connects to the board and displays the message shown in Figure 17.

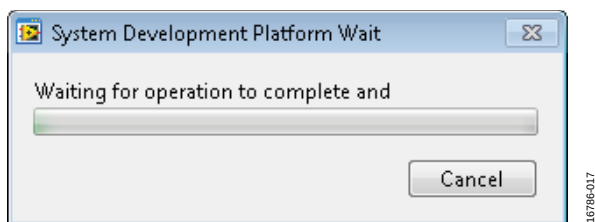


Figure 17. [AD4020](#) Reference Design Software Connects to [SDP-H1](#) Board

4. When the EV-AD4020-REF-DGNZ reference design board is detected, the software panel opens and the [AD4020](#) reference design software looks for the hardware connected to the PC. The [AD4020](#) reference design software detects the generic device attached to the PC and the product panel launches, as shown in Figure 23.

SOFTWARE OPERATION

DESCRIPTION OF THE USER PANEL

The **File** menu (Label 1 in Figure 23) provides the following commands:

- **Save Captured Data** allows the user to save the current captured data for later analysis, and the file format is .csv. The user is prompted to select or enter the path of the file in the **Save As** window (see Figure 18). Save the file to an appropriate folder location.
- **Load Captured Data** opens the **Load File** window where the user is prompted to load previously captured data in .csv format for analysis.
- **Take Screenshot** allows the user to save the current screen capture as a .jpg.
- **Print Screenshot** allows the user to save the current screen capture as a .pdf.
- **Exit** stops running the AD4020 reference design software.

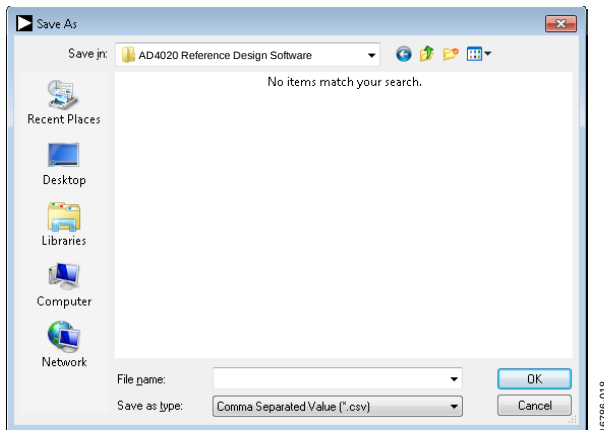


Figure 18. Save As Window

The **Edit** menu (Label 1 in Figure 23) provides the **Reinitialize to Default Values** command to reset the AD4020 reference design software to the initial state.

The **Help** menu (Label 1 in Figure 23) provides the following four options that offer specific information:

- **Analog Devices Website**
- **User Guide**
- **Context Help**
- **About**

When hardware is connected to the USB port, the AD4020 reference design software automatically detects which generic board is connected and displays this board in the **Eval Board Connected** dropdown menu (Label 2 in Figure 23).

The **Throughput** pane (Label 3 in Figure 23) is where the user enters the throughput value. The default throughput (sampling frequency) is 1.75 MSPS. The minimum throughput is 10 kSPS. When the user enters a value larger than the ability of the existing device, the software reverts to the maximum throughput.

Clicking on the **Voltage Reference** dropdown menu (Label 4 in Figure 23) allows the user to select a reference value. By default, the reference is 5 V (on-board reference). The minimum and maximum voltage calculations are based on the reference voltage. When the user changes the reference voltage, they must change the input accordingly.

Click **Single Capture** (Label 5 in Figure 23) to perform a single capture of data, and click **Continuous Capture** (Label 5 in Figure 23) to perform a continuous stream capture from the ADC.

Select a value from the **Samples** dropdown menu (Label 6 in Figure 23) to analyze data according to the number of samples. The maximum number of samples the AD4020 reference design software can support is 524,288.

Five capture tabs (Label 7 in Figure 23) display the data in the following formats: waveform, histogram, FFT, INL/DNL, and summary.

Click **Enable Status Bits** (Label 8 in Figure 23) to enable the status header content. Status bits can be clocked out at the end of the conversion data using six extra clocks when the status header content is enabled. Click **Enable Status Bits** (Label 8 in Figure 23) to enable the six status bits. Click **Single Capture** or **Continuous Capture** (Label 5 in Figure 23) to display the content of the six status bits in the **Status Header** pane (Label 13 in Figure 23). The overvoltage clamp flag status bit updates on a per conversion basis.

Click **Span Compression** (Label 9 in Figure 23) to enable the ADC span compression feature. In single-supply applications, the use of span compression increases the headroom and footroom available to the ADC driver by reducing the input range by 10% from the top and bottom of the range while still accessing all available ADC codes.

Click **High-Z Mode** (Label 10 in Figure 23) to enable the internal high-Z mode. Enabling this mode allows a low input current for the ADC and improves total harmonic distortion (THD) performance using low power and bandwidth precision ADC drivers for slow, dc type signals.

Click **Turbo Mode** (Label 11 in Figure 23) to enable turbo mode and run the ADC at a full throughput of 1.8 MSPS.

Click **Read Register** (Label 12 in Figure 23) to see if any easy to use features are enabled. The easy to use features include span compression, high-Z mode, turbo mode, an overvoltage condition (sticky bit), and the status bits.

When the **Busy** indicator (Label 14 in Figure 23) is illuminated, the user must wait until the AD4020 reference design software completes the data analysis to ensure complete data capture.

Within any of the chart panels, the tools shown in Figure 19, Figure 20, and Figure 21 allow user control of the different chart displays.



Figure 19. Controlling the Cursor Tool



Figure 20. Zooming In and Out Tool



Figure 21. Panning Tool

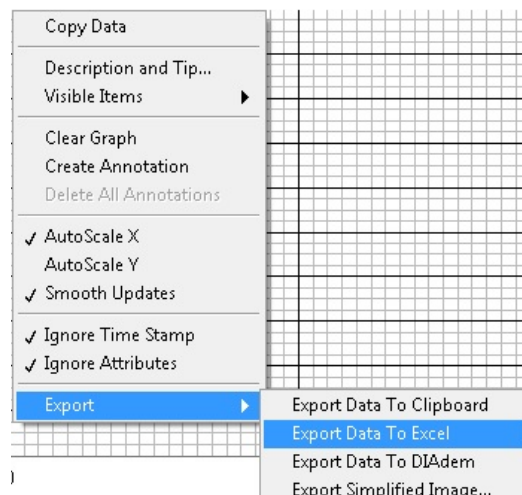


Figure 22. Export Raw Data or Image

The AD4020 reference design software allows the user to export the raw data or image. Right click any of the five capture tabs (**Waveform**, **Histogram**, **FFT**, **INL/DNL** or **Summary**) to open the menu shown in Figure 22. Choose to export raw data in Excel format or save an image of the data in .bmp, .eps, or .emf format.

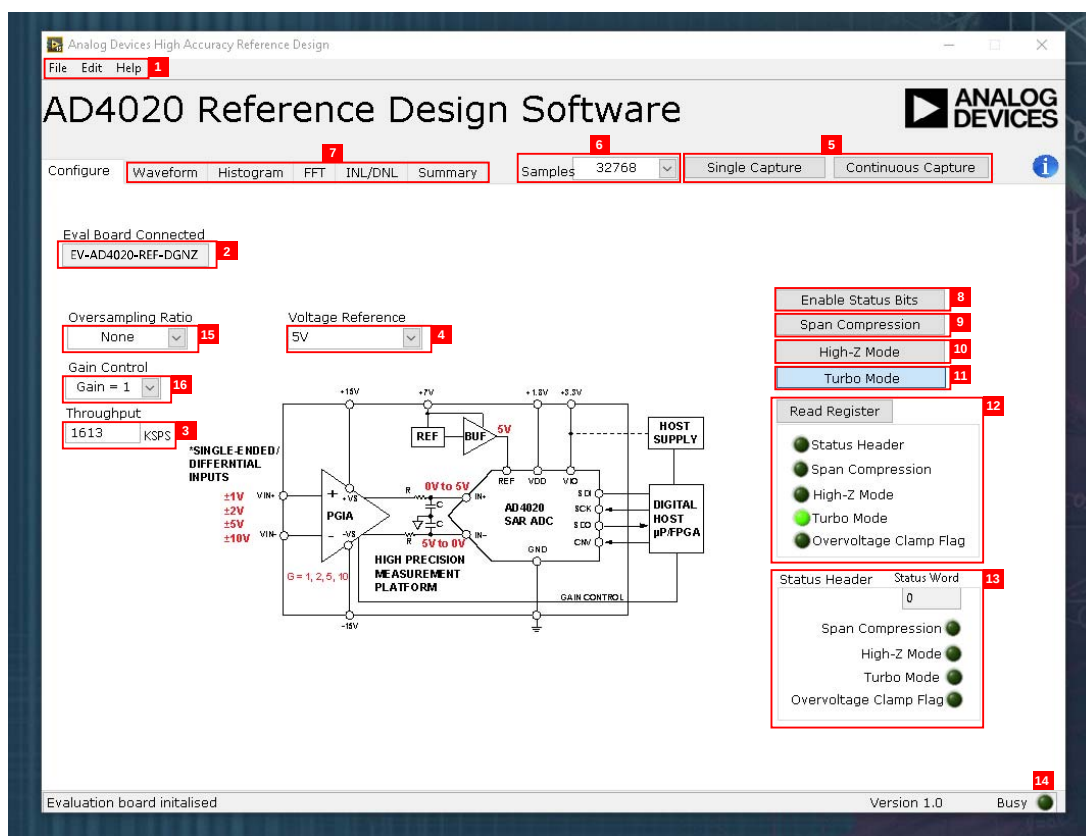


Figure 23. AD4020 Reference Design Software Setup Screen

WAVEFORM CAPTURE

Figure 24 shows the waveform capture feature. The input signal is a 1 kHz sine wave. The waveform analysis reports the amplitudes recorded from the captured signal in addition to the frequency of the signal tone.

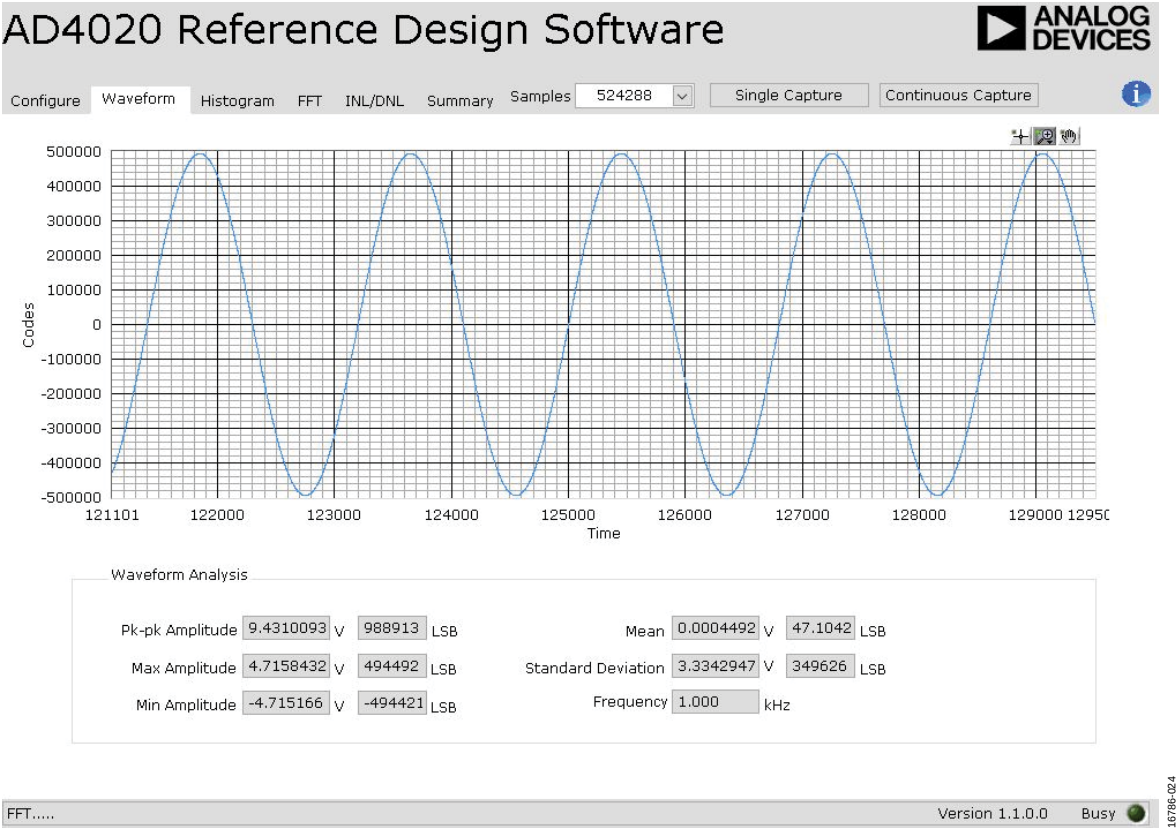


Figure 24. Waveform Capture Data Display

HISTOGRAM AC TESTING

The ac testing histogram tests the ADC for the code distribution of the ac input. The histogram test computes the mean, minimum, and maximum amplitudes, and the LSB size of the converter. Raw data is captured and passed to the PC for statistical computations.

To perform a histogram test, click the **Histogram** tab, and then click **Single Capture** or **Continuous Capture** stream. An ac histogram requires a quality signal source applied to the J6 and J10 input connectors. Figure 25 shows the histogram for a 1 kHz sine wave applied to the ADC input, and shows the different measured values for the data captured.

HISTOGRAM DC TESTING

The histogram is more commonly used for dc testing. The dc testing histogram tests the ADC for the code distribution of the dc input, computes the mean and standard deviation or the transition noise of the converter, and displays the results. Raw data is captured and passed to the PC for statistical computations.

To perform a histogram test, click the **Histogram** tab, and then click **Start Stream**. A histogram test can be performed without an external source using the reference voltage (V_{REF}) divided by 2 (10 k Ω resistor divider) at the ADC input. To test other dc values, apply a source to the J6 and J10 input connectors. Filter the signal to make the dc source noise compatible with that of the ADC when required.

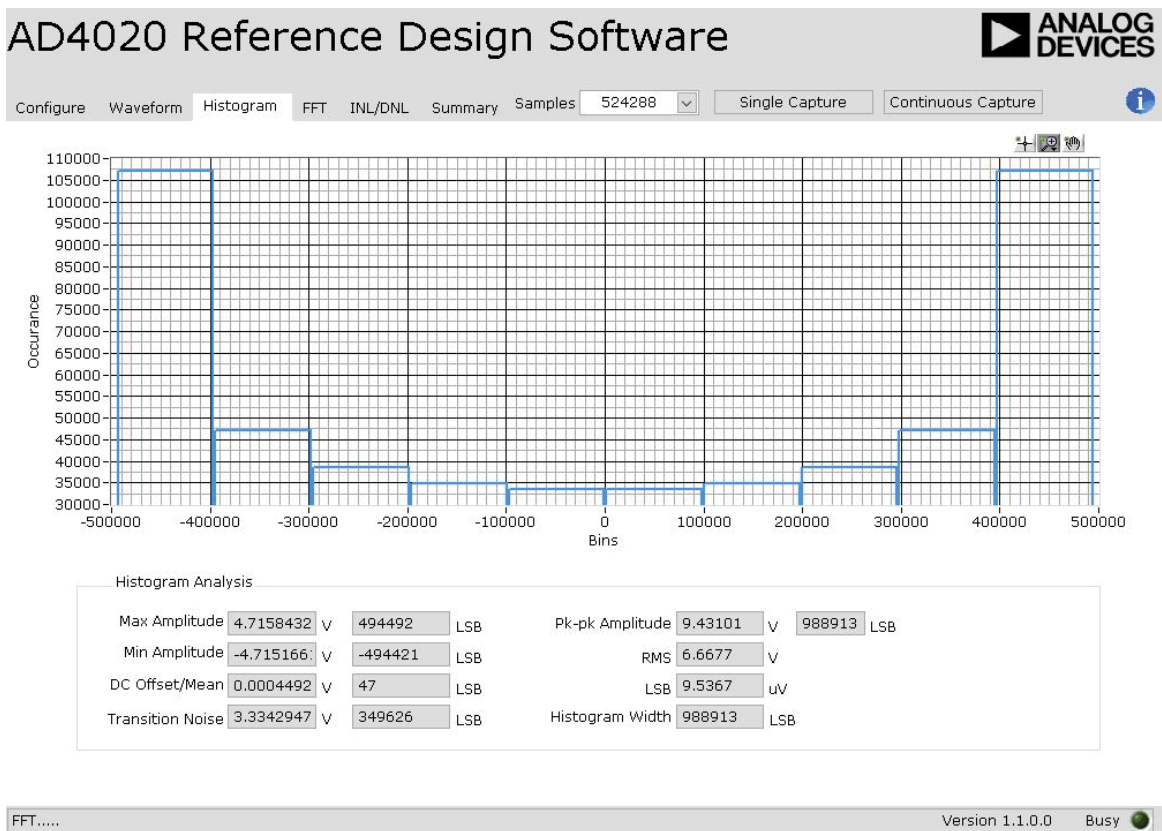


Figure 25. Histogram Captured for Sine Wave

FFT CAPTURE AC TESTING

The traditional ac characteristics of the converter are displayed on the **FFT** tab (see Figure 26). Raw data is captured and passed to the PC in the same way it is in the histogram test, where the FFT is performed displaying signal-to-noise ratio (SNR), signal-to-noise-and-distortion ratio (SINAD), THD, and spurious-free dynamic range (SFDR). The time domain displays the data as well.

To perform an ac test, apply a sinusoidal signal to the EV-AD4020-REF-DGNZ reference design board at the J6 and J10 SMA inputs. Low distortion (better than 100 dB) is required to allow true evaluation of the device. Filter the input signal from the ac source using a band-pass filter. Ensure that the center

frequency of the band-pass filter matches the test frequency of interest. If using a low frequency band-pass filter when the full-scale input range is more than a few volts peak-to-peak, use the on-board amplifiers to amplify the signal, thus preventing the filter from distorting the input signal.

Figure 26 displays the FFT of the captured data that includes the following:

- The spectrum information
- The fundamental frequency and amplitude in addition to the second to fifth harmonics
- The performance data (SNR, dynamic range, THD, SINAD, and noise performance).

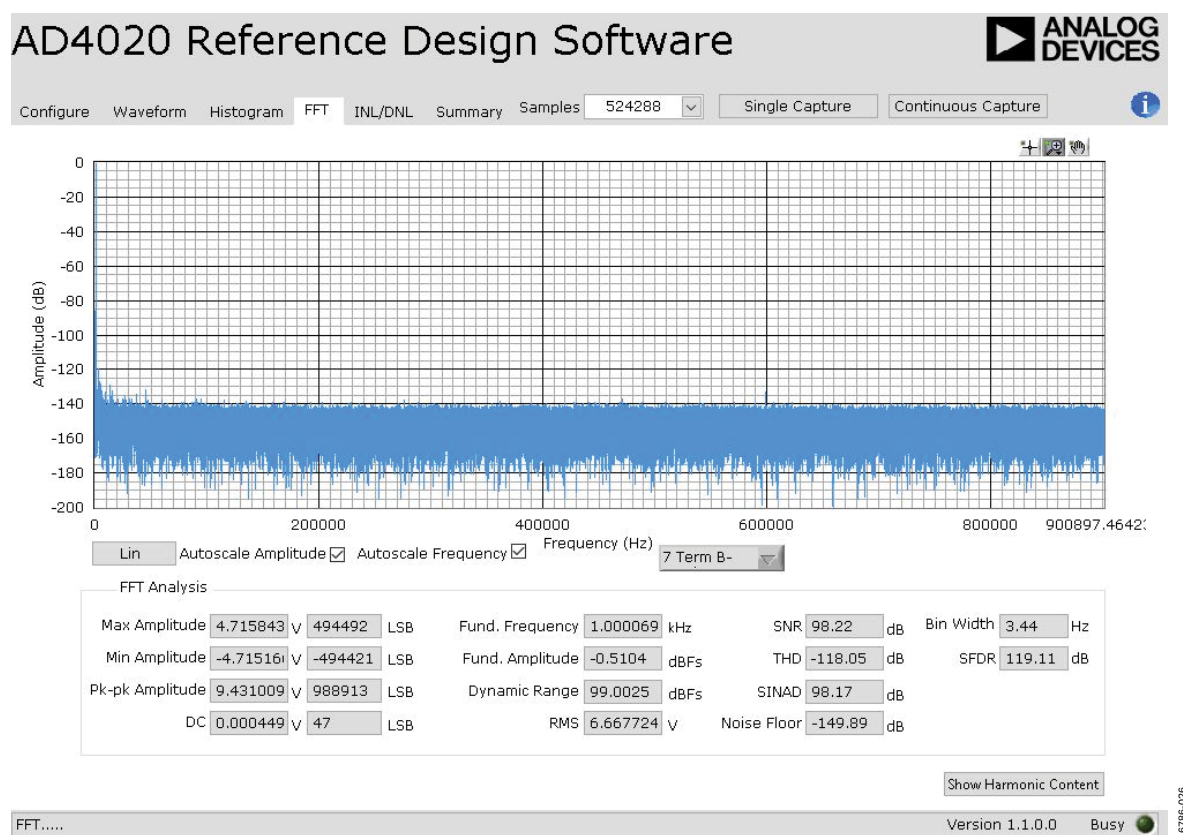


Figure 26. **FFT** Tab (AD4020 Running in Turbo Mode)

INL/DNL CAPTURE LINEARITY TESTING

The INL/DNL tab (see Figure 27) displays linearity analysis. The INL/DNL parameter is defined as the maximum deviation from the ideal slope of the ADC, and is measured from the center of the step performance.

To perform a linearity test, apply a sinusoidal signal with 0.5 dB above full scale to the EV-AD4020-REF-DGNZ reference

design board at the J1 and J2 SMA inputs. Set the number of hits per code and adjust to the desired accuracy. Using a large number of hits per code results in significant test time.

Figure 27 displays captured data that includes $\pm$ INL position and $\pm$ DNL position.

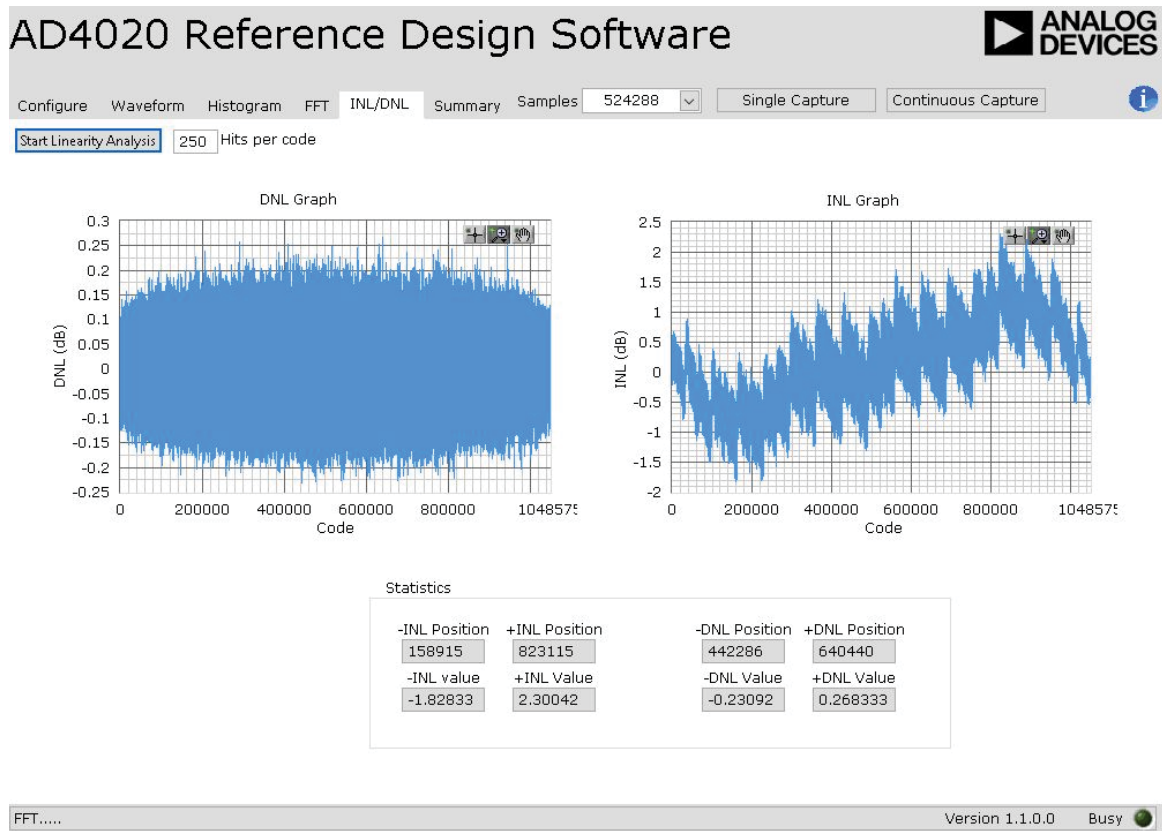


Figure 27. INL/DNL Testing

OFFSET ERROR TESTING

The offset error is the difference between the ideal code and the output code where both inputs are tied to GND. The input offset error can be positive (IN+) or negative (IN-). Use the following equation to test for the offset error:

$$\text{Offset Error} = \frac{V_{\text{CODE}} \text{ ADC}}{IN+ - IN-}$$

where:

$V_{\text{CODE}} \text{ ADC}$ is the ADC output code.

$IN+$ is the positive input.

$IN-$ is the negative input.

GAIN ERROR TESTING

The gain error is the deviation of the difference between the actual levels of the first and last transition from the difference between the ideal levels of the first and last transition.

To perform a gain error test, apply a sinusoidal signal with -0.5 dB above full scale to the EV-AD4020-REF-DGNZ reference design board at the J1 and J2 SMA inputs with 1 kHz input tone,

$$\text{Actual Gain} = \frac{\text{Maxcode} - \text{Mincode}}{V_{IN+} - (V_{IN-})}$$

$$\text{Ideal Gain} = \frac{V_{\text{CODE}} \text{ ADC}}{IN+ - IN-}$$

$$\text{Gain Error} = \left(\frac{\text{Actual Gain}}{\text{Ideal Gain}} \right) \times 100$$

where:

Maxcode is the maximum output.

Mincode is the minimum output.

Actual Gain is the actual input voltage over the ideal output.

Ideal Gain is the ideal input voltage over the ideal output.

COMMON-MODE REJECTION RATIO TESTING

The common-mode rejection ratio (CMRR) is the ratio of the power in the ADC output at the frequency (f) to the power of a 200 mV p-p sine wave applied to the common-mode voltage ($IN+$ and $IN-$) when both inputs are tied together,

$$A_{\text{DIFF}} = \frac{\Delta \text{Output Code}}{\Delta \text{Differential Voltage}}$$

$$A_{\text{CM}} = \frac{\Delta \text{Output Code}}{\Delta \text{Common - Mode Voltage}}$$

where:

A_{DIFF} is the differential gain.

A_{CM} is the common gain.

Because the output code is very small with respect to common-mode voltage, the CMRR is generally a large number and is expressed on a logarithmic scale,

$$\text{CMRR}_{\text{ADC}} = 20 \log \left(\frac{A_{\text{DIFF}}}{A_{\text{CM}}} \right)$$

where CMRR_{ADC} is the common-mode voltage when both inputs are tied together.

TROUBLESHOOTING

SOFTWARE

To troubleshoot the [AD4020](#) reference design software, ensure that each of the following steps have been taken:

- Always allow the [AD4020](#) reference design software installation to be fully complete before connecting the hardware to the PC. Note that the [AD4020](#) reference design software is a two-part installation consisting of the [AD4020](#) reference design software and the [SDP-H1](#) drivers. A restart is recommended after installation is finished.
- When the [SDP-H1](#) controller board is first plugged in via the USB cable provided, allow the new found hardware wizard to run, which can take some time. Let the wizard run before starting the [AD4020](#) reference design software.
- If the EV-AD4020-REF-DGNZ reference design board does not appear to be functioning, ensure that the EV-AD4020-REF-DGNZ reference design board is connected to the [SDP-H1](#) controller board, and that the EV-AD4020-REF-DGNZ reference design board is recognized in the **Eval Board Connected** box, as shown in Figure 23.
- When the [SDP-H1](#) controller board connects to a slower USB port where it cannot read as quickly as required, a timeout error occurs. In this case, do not read continuously or alternatively in order to lower the number of samples taken.

HARDWARE

When the [AD4020](#) reference design software does not read any data back, try any of the following options to troubleshoot:

- Ensure that the power is applied within the power ranges described in the Power Supplies section.
- Using a voltmeter, measure to ensure that the voltage is correct at each of the test points (+V_s, -V_s, 1P8V_VDD, VDD_1P8V, +3P3V, +5 V, REF1) and common-mode voltages (REF/2) at IN+ and IN-. The [SDP-H1](#) controller board LED1 must be illuminated.
- Launch the [AD4020](#) reference design software and read the data. If no data is read back, exit the [AD4020](#) reference design software.
- Power-down the board and relaunch the [AD4020](#) reference design software.
- If no data is read back, confirm that the EV-AD4020-REF-DGNZ reference design board is connected to the [SDP-H1](#) controller board and that the board is being recognized in the **Eval Board Connected** pane, as shown in Figure 23.

When the user is working with the [AD4020](#) reference design software in standalone mode or offline mode with no hardware connected, and later chooses to connect hardware, close and relaunch the [AD4020](#) reference design software.

REFERENCE DESIGN BOARD ARTWORK

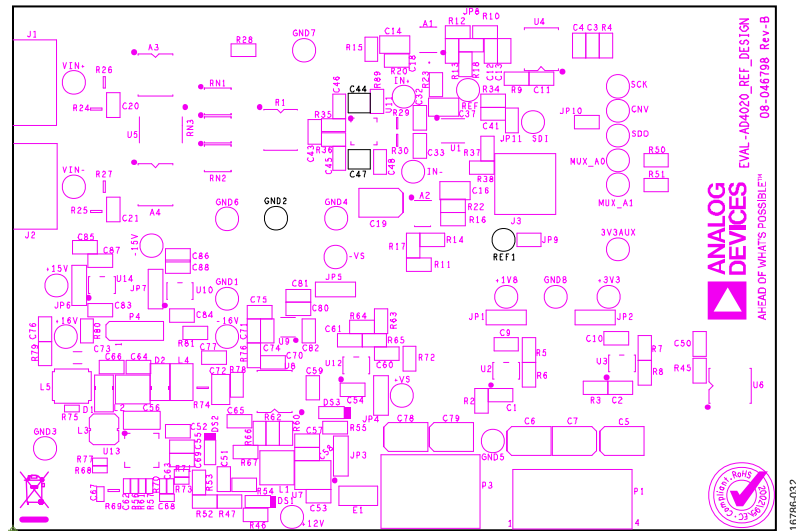


Figure 28. EV-AD4020-REF-DGNZ Reference Design Board Silkscreen

**ESD Caution**

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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