ESP32-PICO-D4

Datasheet

Version 1.7

Espressif Systems

About This Document

This document provides an introduction to the specifications of the ESP32-PICO-D4 module.

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1. Overview

The ESP32-PICO-D4 is a System-in-Package (SiP) module that is based on ESP32, providing complete Wi-Fi and Bluetooth® functionalities. The module has a size as small as (7.000±0.100) mm × (7.000±0.100) mm × (0.940±0.100) mm, thus requiring minimal PCB area. The module integrates a 4-MB SPI flash.

At the core of this module is the ESP32 chip*, which is a single 2.4 GHz Wi-Fi and Bluetooth combo chip designed with TSMC's 40 nm ultra-low power technology. ESP32-PICO-D4 integrates all peripheral components seamlessly, including a crystal oscillator, flash, filter capacitors and RF matching links in one single package. Given that no other peripheral components are involved, module welding and testing is not required either. As such, ESP32-PICO-D4 reduces the complexity of supply chain and improves control efficiency.

With its ultra-small size, robust performance and low-energy consumption, ESP32-PICO-D4 is well suited for any space-limited or battery-operated applications, such as wearable electronics, medical equipment, sensors and other IoT products.

Note:

* For details on ESP32, please refer to the document *ESP32 Datasheet*.

Table 1 provides the specifications of the ESP32-PICO-D4 module.

Table 1: ESP32-PICO-D4 Specifications

Categories	Items	Specifications
Certification	Bluetooth certification	BQB
Wi-Fi	Protocols	802.11 b/g/n (802.11n up to 150 Mbps)
		A-MPDU and A-MSDU aggregation and 0.4 μs guard interval support
	Frequency range	2.4 ~ 2.5 GHz
Bluetooth	Protocols	Bluetooth V4.2 BR/EDR and Bluetooth LE specification
	Radio	NZIF receiver with –97 dBm sensitivity
		Class-1, class-2 and class-3 transmitter
		AFH
	Audio	CVSD and SBC
Hardware	Module interfaces	ADC, DAC, touch sensor, SD/SDIO/MMC Host Controller, SPI, SDIO/SPI Slave Controller, EMAC, motor PWM, LED PWM, UART, I^2C, I^2S, infrared remote controller, GPIO, pulse counter
	On-chip sensor	Hall sensor
	Integrated crystal	40 MHz crystal
	Integrated SPI flash	4 MB
	Operating voltage/Power supply	3.0 V ~ 3.6 V
	Operating current	Average: 80 mA
	Minimum current delivered by power supply	500 mA

Categories	Items	Specifications
	Operating temperature range	–40 °C ~ 85 °C
	Package size	(7.000±0.100) mm×(7.000±0.100) mm×(0.940±0.100) mm
	Moisture sensitivity level (MSL)	Level 3

2. Pin Definitions

2.1 Pin Layout

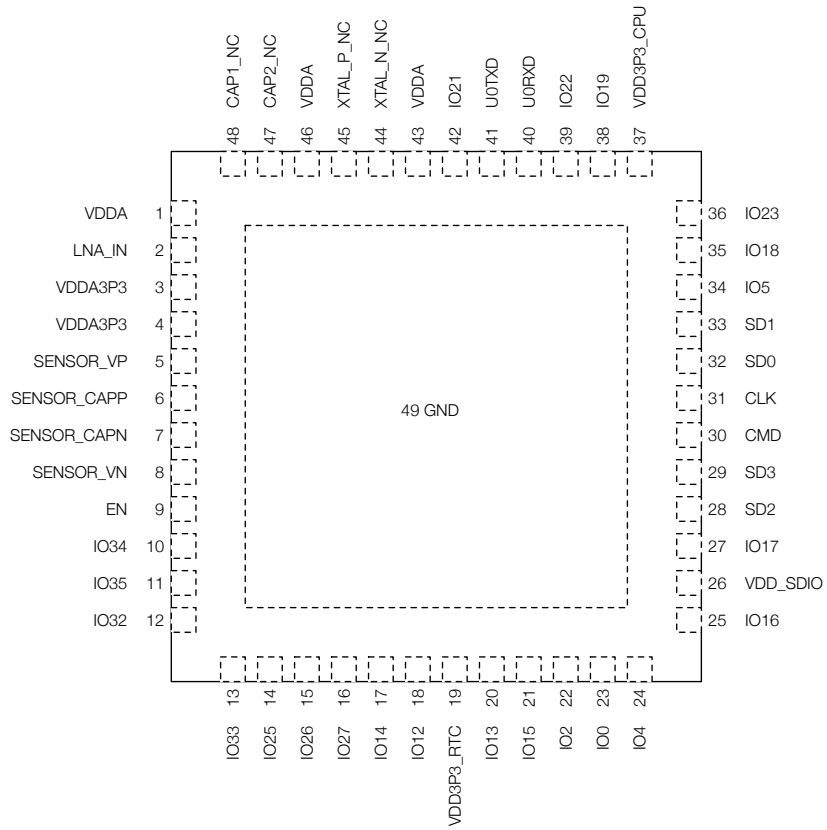


Figure 1: ESP32-PICO-D4 Pin Layout (Top View)

2.2 Pin Description

The ESP32-PICO-D4 module has 48 pins. See pin definitions in Table 2.

Table 2: Pin Description

Name	No.	Type	Function
VDDA	1	P	Analog power supply (2.3 V ~ 3.6 V)
LNA_IN	2	I/O	RF input and output
VDDA3P3	3	P	Analog power supply (2.3 V ~ 3.6 V)
VDDA3P3	4	P	Analog power supply (2.3 V ~ 3.6 V)
SENSOR_VP	5	I	GPIO36, ADC1_CH0, RTC_GPIO0
SENSOR_CAPP	6	I	GPIO37, ADC1_CH1, RTC_GPIO1
SENSOR_CAPN	7	I	GPIO38, ADC1_CH2, RTC_GPIO2
SENSOR_VN	8	I	GPIO39, ADC1_CH3, RTC_GPIO3

Name	No.	Type	Function
EN	9	I	High: On; enables the module Low: Off; the module powers off Note: Do not leave this pin floating.
IO34	10	I	ADC1_CH6, RTC_GPIO4
IO35	11	I	ADC1_CH7, RTC_GPIO5
IO32	12	I/O	32K_XP (32.768 kHz crystal oscillator input), ADC1_CH4, TOUCH9, RTC_GPIO9
IO33	13	I/O	32K_XN (32.768 kHz crystal oscillator output), ADC1_CH5, TOUCH8, RTC_GPIO8
IO25	14	I/O	GPIO25, DAC_1, ADC2_CH8, RTC_GPIO6, EMAC_RXD0
IO26	15	I/O	GPIO26, DAC_2, ADC2_CH9, RTC_GPIO7, EMAC_RXD1
IO27	16	I/O	GPIO27, ADC2_CH7, TOUCH7, RTC_GPIO17, EMAC_RX_DV
IO14	17	I/O	ADC2_CH6, TOUCH6, RTC_GPIO16, MTMS, HSPICLK, HS2_CLK, SD_CLK, EMAC_TXD2
IO12	18	I/O	ADC2_CH5, TOUCH5, RTC_GPIO15, MTDI, HSPIQ, HS2_DATA2, SD_DATA2, EMAC_TXD3
VDD3P3_RTC	19	P	Input power supply for RTC IO (3.0 V ~ 3.6 V)
IO13	20	I/O	ADC2_CH4, TOUCH4, RTC_GPIO14, MTCK, HSPID, HS2_DATA3, SD_DATA3, EMAC_RX_ER
IO15	21	I/O	ADC2_CH3, TOUCH3, RTC_GPIO13, MTDO, HSPICS0, HS2_CMD, SD_CMD, EMAC_RXD3
IO2	22	I/O	ADC2_CH2, TOUCH2, RTC_GPIO12, HSPIWP, HS2_DATA0, SD_DATA0
IO0	23	I/O	ADC2_CH1, TOUCH1, RTC_GPIO11, CLK_OUT1, EMAC_TX_CLK
IO4	24	I/O	ADC2_CH0, TOUCH0, RTC_GPIO10, HSPIHD, HS2_DATA1, SD_DATA1, EMAC_TX_ER
IO16	25	I/O	GPIO16, HS1_DATA4, U2RXD, EMAC_CLK_OUT
VDD_SDIO	26	P	Output power supply. See note 1 under the table.
IO17	27	I/O	GPIO17, HS1_DATA5, U2TXD, EMAC_CLK_OUT_180
SD2	28	I/O	GPIO9, SD_DATA2, SPIHD, HS1_DATA2, U1RXD
SD3	29	I/O	GPIO10, SD_DATA3, SPIWP, HS1_DATA3, U1TXD
CMD	30	I/O	GPIO11, SD_CMD, SPICS0, HS1_CMD, U1RTS
CLK	31	I/O	GPIO6, SD_CLK, SPICLK, HS1_CLK, U1CTS
SD0	32	I/O	GPIO7, SD_DATA0, SPIQ, HS1_DATA0, U2RTS
SD1	33	I/O	GPIO8, SD_DATA1, SPID, HS1_DATA1, U2CTS
IO5	34	I/O	GPIO5, VSPICS0, HS1_DATA6, EMAC_RX_CLK
IO18	35	I/O	GPIO18, VSPICLK, HS1_DATA7
IO23	36	I/O	GPIO23, VSPID, HS1_STROBE
VDD3P3_CPU	37	P	Input power supply for CPU IO (1.8 V ~ 3.6 V)
IO19	38	I/O	GPIO19, VSPIQ, U0CTS, EMAC_TXD0
IO22	39	I/O	GPIO22, VSPIWP, U0RTS, EMAC_TXD1
U0RXD	40	I/O	GPIO3, U0RXD, CLK_OUT2

Name	No.	Type	Function
U0TXD	41	I/O	GPIO1, U0TXD, CLK_OUT3, EMAC_RXD2
IO21	42	I/O	GPIO21, VSPIHD, EMAC_TX_EN
VDDA	43	P	Analog power supply (2.3 V ~ 3.6 V)
XTAL_N_NC	44	-	NC
XTAL_P_NC	45	-	NC
VDDA	46	P	Analog power supply (2.3 V ~ 3.6 V)
CAP2_NC	47	-	NC
CAP1_NC	48	-	NC

Notice:

1. Note that the embedded flash is connected to VDD_SDIO which is driven directly by VDD3P3_RTC through a 6 Ω resistor. Due to this resistor, there is some voltage drop on this pin from VDD3P3_RTC.
2. Pins IO16, IO17, CMD, CLK, SD0 and SD1 are used for connecting the embedded flash, and are not recommended for other uses. For details, please see Section 6 Schematics.
3. For connecting external PSRAM, SD3 (GPIO10) is recommended for PSRAM_CS. For details, please see Section 7 Peripheral Schematics.

2.3 Strapping Pins

ESP32 has five strapping pins, which can be seen in Chapter 6 Schematics:

- MTDI
- GPIO0
- GPIO2
- MTDO
- GPIO5

Software can read the values of these five bits from register "GPIO_STRAPPING".

During the chip's system reset release (power-on-reset, RTC watchdog reset and brownout reset), the latches of the strapping pins sample the voltage level as strapping bits of "0" or "1", and hold these bits until the chip is powered down or shut down. The strapping bits configure the device's boot mode, the operating voltage of VDD_SDIO and other initial system settings.

Each strapping pin is connected to its internal pull-up/pull-down during the chip reset. Consequently, if a strapping pin is unconnected or the connected external circuit is high-impedance, the internal weak pull-up/pull-down will determine the default input level of the strapping pins.

To change the strapping bit values, users can apply the external pull-down/pull-up resistances, or use the host MCU's GPIOs to control the voltage level of these pins when powering on ESP32.

After reset release, the strapping pins work as normal-function pins.

Refer to Table 3 for a detailed boot-mode configuration by strapping pins.

Table 3: Strapping Pins

Voltage of Internal LDO (VDD_SDIO)					
Pin	Default	3.3 V		1.8 V	
MTDI	Pull-down	0		1	
Booting Mode					
Pin	Default	SPI Boot		Download Boot	
GPIO0	Pull-up	1		0	
GPIO2	Pull-down	Don't-care		0	
Enabling/Disabling Debugging Log Print over U0TXD During Booting					
Pin	Default	U0TXD Active		U0TXD Silent	
MTDO	Pull-up	1		0	
Timing of SDIO Slave					
Pin	Default	Falling-edge Sampling Falling-edge Output	Falling-edge Sampling Rising-edge Output	Rising-edge Sampling Falling-edge Output	Rising-edge Sampling Rising-edge Output
MTDO	Pull-up	0	0	1	1
GPIO5	Pull-up	0	1	0	1

Note:

- Firmware can configure register bits to change the settings of "Voltage of Internal LDO (VDD_SDIO)" and "Timing of SDIO Slave", after booting.
- The operating voltage of ESP32-PICO-D4's integrated external SPI flash is 3.3 V. Therefore, the strapping pin MTDI should hold bit "0" during the module power-on reset.

3. Functional Descriptions

This chapter describes the modules integrated in ESP32-PICO-D4, and their functions.

3.1 CPU and Internal Memory

ESP32 contains two low-power Xtensa® 32-bit LX6 microprocessors. The internal memory includes:

- 448 KB of ROM for booting and core functions.
- 520 KB of on-chip SRAM for data and instructions.
- 8 KB of SRAM in RTC, which is called RTC FAST Memory and can be used for data storage; it is accessed by the main CPU during RTC Boot from the Deep-sleep mode.
- 8 KB of SRAM in RTC, which is called RTC SLOW Memory and can be accessed by the co-processor during the Deep-sleep mode.
- 1 Kbit of eFuse: 256 bits are used for the system (MAC address and chip configuration) and the remaining 768 bits are reserved for customer applications, including flash-encryption and chip-ID.

3.2 External Flash and SRAM

ESP32 supports multiple external QSPI flash and SRAM chips. More details can be found in Chapter SPI in the *ESP32 Technical Reference Manual*. ESP32 also supports hardware encryption/decryption based on AES to protect developers' programs and data in flash.

ESP32 can access the external QSPI flash and SRAM through high-speed caches.

- The external flash can be mapped into CPU instruction memory space and read-only memory space simultaneously.
  - When external flash is mapped into CPU instruction memory space, up to 11 MB + 248 KB can be mapped at a time. Note that if more than 3 MB + 248 KB are mapped, cache performance will be reduced due to speculative reads by the CPU.
  - When external flash is mapped into read-only data memory space, up to 4 MB can be mapped at a time. 8-bit, 16-bit and 32-bit reads are supported.
- External SRAM can be mapped into CPU data memory space. Up to 4 MB can be mapped at a time. 8-bit, 16-bit and 32-bit reads and writes are supported.

The ESP32-PICO-D4 module integrates 4 MB of external SPI flash.

3.3 Crystal Oscillators

ESP32-PICO-D4 integrates a 40 MHz crystal oscillator.

3.4 RTC and Power Consumption

With the use of advanced power-management technologies, ESP32 can switch between different power modes.

For details on ESP32's power consumption in different power modes, please refer to section "RTC and Low-Power Management" in *ESP32 Datasheet*.

4. Peripherals and Sensors

Please refer to Section Peripherals and Sensors in *ESP32 Datasheet*.

Note:

- Pins IO16, IO17, CMD, CLK, SD0 and SD1 are used for connecting the embedded flash, and are not recommended for other uses. For details, please see Section 6 Schematics.
- For connecting external PSRAM, SD3 (GPIO10) is recommended for PSRAM_CS. For details, please see Section 7 Peripheral Schematics.

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Stresses beyond the absolute maximum ratings listed in the table below may cause permanent damage to the device. These are stress ratings only, and do not refer to the functional operation of the device that should follow the recommended operating conditions.

Table 4: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
VDD33	Power supply voltage	–0.3	3.6	V
I_{output} [1]	Cumulative IO output current	-	1,100	mA
T_{store}	Storage temperature	–40	150	°C

1. The module worked properly after a 24-hour test in ambient temperature at 25 °C, and the IOs in three domains (VDD3P3_RTC, VDD3P3_CPU, VDD_SDIO) output high logic level to ground. Please note that pins occupied by flash and/or PSRAM in the VDD_SDIO power domain were excluded from the test.
2. Please see Appendix IO_MUX of *ESP32 Datasheet* for IO's power domain.

5.2 Recommended Operating Conditions

Table 5: Recommended Operating Conditions

Symbol	Parameter	Min	Typical	Max	Unit
VDD33	Power supply voltage	3.0	3.3	3.6	V
I_{VDD}	Current delivered by external power supply	0.5	-	-	A
T	Operating temperature	–40	-	85	°C

5.3 DC Characteristics (3.3 V, 25 °C)

Table 6: DC Characteristics (3.3 V, 25 °C)

Symbol	Parameter		Min	Typ	Max	Unit
C_{IN}	Pin capacitance		-	2	-	pF
V_{IH}	High-level input voltage		0.75×VDD[1]	-	VDD[1]+0.3	V
V_{IL}	Low-level input voltage		–0.3	-	0.25×VDD[1]	V
I_{IH}	High-level input current		-	-	50	nA
I_{IL}	Low-level input current		-	-	50	nA
V_{OH}	High-level output voltage		0.8×VDD[1]	-	-	V
V_{OL}	Low-level output voltage		-	-	0.1×VDD[1]	V
I_{OH}	High-level source current (VDD[1] = 3.3 V, V_{OH} >= 2.64 V, output drive strength set to the maximum)	VDD3P3_CPU power domain [1, 2]	-	40	-	mA
		VDD3P3_RTC power domain [1, 2]	-	40	-	mA
		VDD_SDIO power domain [1, 3]	-	20	-	mA

Symbol	Parameter	Min	Typ	Max	Unit
I_{OL}	Low-level sink current (VDD[1] = 3.3 V, V_{OL} = 0.495 V, output drive strength set to the maximum)	-	28	-	mA
R_{PU}	Resistance of internal pull-up resistor	-	45	-	kΩ
R_{PD}	Resistance of internal pull-down resistor	-	45	-	kΩ
V_{IL_nRST}	Low-level input voltage of CHIP_PU to power off the chip	-	-	0.6	V

Notes:

1. Please see Appendix IO_MUX of *ESP32 Datasheet* for IO's power domain. VDD is the I/O voltage for a particular power domain of pins.
2. For VDD3P3_CPU and VDD3P3_RTC power domain, per-pin current sourced in the same domain is gradually reduced from around 40 mA to around 29 mA, V_{OH}>=2.64 V, as the number of current-source pins increases.
3. Pins occupied by flash and/or PSRAM in the VDD_SDIO power domain were excluded from the test.

5.4 Wi-Fi Radio

Table 7: Wi-Fi Radio Characteristics

Description	Min	Typical	Max	Unit
Operating frequency range ^{note1}	2412	-	2484	MHz
Output impedance ^{note2}	-	50	-	Ω
TX power ^{note3}				
Output power of PA for 72.2 Mbps	13	14	15	dBm
Output power of PA for 11b mode	19.5	20	20.5	dBm
Sensitivity				
DSSS, 1 Mbps	-	–98	-	dBm
CCK, 11 Mbps	-	–91	-	dBm
OFDM, 6 Mbps	-	–93	-	dBm
OFDM, 54 Mbps	-	–75	-	dBm
HT20, MCS0	-	–93	-	dBm
HT20, MCS7	-	–73	-	dBm
HT40, MCS0	-	–90	-	dBm
HT40, MCS7	-	–70	-	dBm
MCS32	-	–89	-	dBm
Adjacent channel rejection				
OFDM, 6 Mbps	-	37	-	dB
OFDM, 54 Mbps	-	21	-	dB
HT20, MCS0	-	37	-	dB
HT20, MCS7	-	20	-	dB

1. Device should operate in the frequency range allocated by regional regulatory authorities. Target operating frequency range is configurable by software.
2. For the modules that use IPEX antennas, the output impedance is 50 Ω. For other modules without IPEX antennas, users do not need to concern about the output impedance.
3. Target TX power is configurable based on device or certification requirements.

5.5 Bluetooth LE Radio

5.5.1 Receiver

Table 8: Receiver Characteristics – BLE

Parameter	Conditions	Min	Typ	Max	Unit
Sensitivity @30.8% PER	-	-	–97	-	dBm
Maximum received signal @30.8% PER	-	0	-	-	dBm
Co-channel C/I	-	-	+10	-	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	-	–5	-	dB
	F = F0 – 1 MHz	-	–5	-	dB
	F = F0 + 2 MHz	-	–25	-	dB
	F = F0 – 2 MHz	-	–35	-	dB
	F = F0 + 3 MHz	-	–25	-	dB
	F = F0 – 3 MHz	-	–45	-	dB
Out-of-band blocking performance	30 MHz ~ 2000 MHz	–10	-	-	dBm
	2000 MHz ~ 2400 MHz	–27	-	-	dBm
	2500 MHz ~ 3000 MHz	–27	-	-	dBm
	3000 MHz ~ 12.5 GHz	–10	-	-	dBm
Intermodulation	-	–36	-	-	dBm

5.5.2 Transmitter

Table 9: Transmitter Characteristics – BLE

Parameter	Conditions	Min	Typ	Max	Unit
RF transmit power	-	-	0	-	dBm
Gain control step	-	-	3	-	dBm
RF power control range	-	–12	-	+9	dBm
Adjacent channel transmit power	F = F0 ± 2 MHz	-	–52	-	dBm
	F = F0 ± 3 MHz	-	–58	-	dBm
	F = F0 ± > 3 MHz	-	–60	-	dBm
$\Delta f1_{avg}$	-	-	-	265	kHz
$\Delta f2_{max}$	-	247	-	-	kHz
$\Delta f2_{avg}/\Delta f1_{avg}$	-	-	–0.92	-	-
ICFT	-	-	–10	-	kHz
Drift rate	-	-	0.7	-	kHz/50 μs
Drift	-	-	2	-	kHz

5.6 Reflow Profile

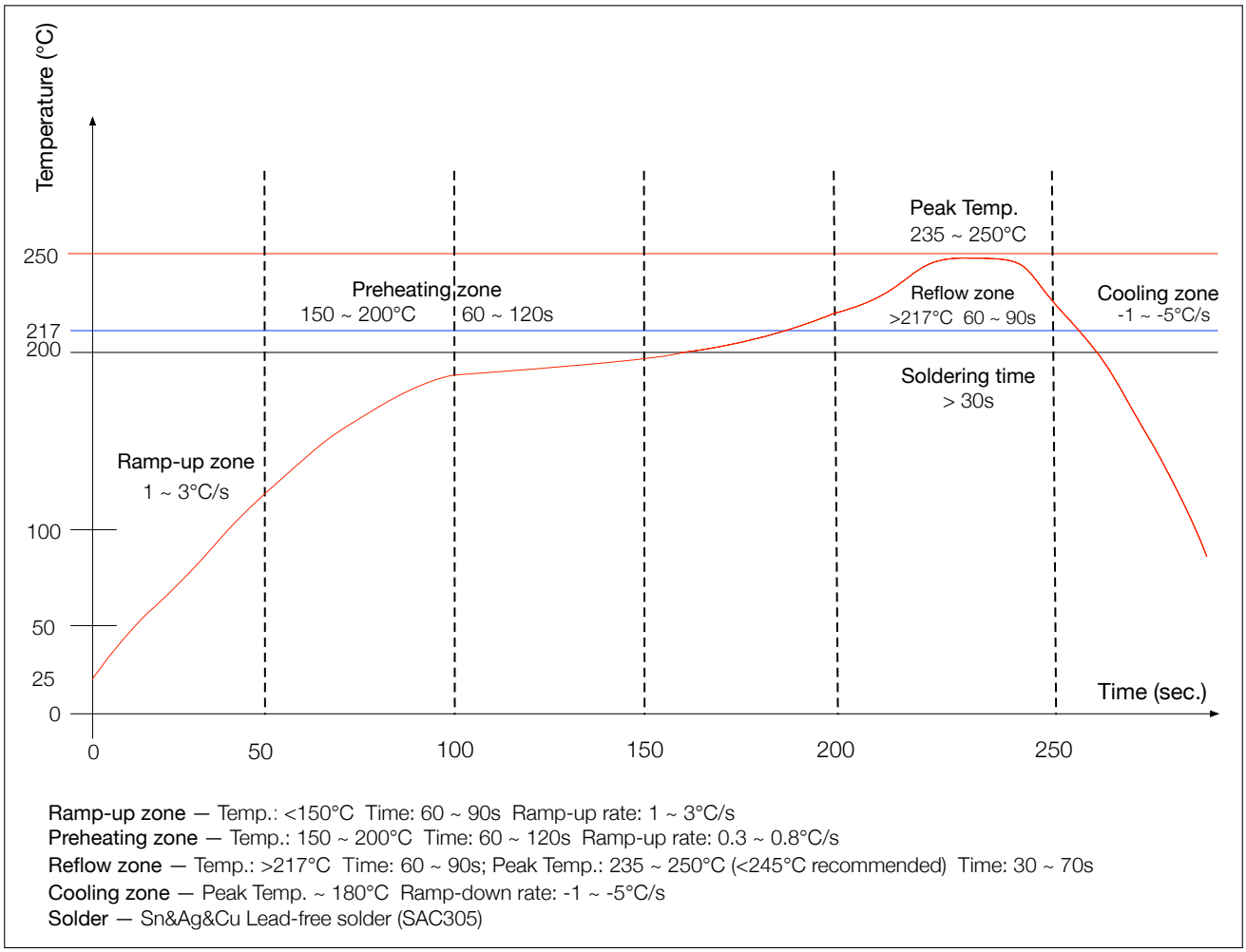


Figure 2: Reflow Profile

Note:

Solder the module in a single reflow. If the PCBA requires multiple reflows, place the module on the PCB during the final reflow.

6. Schematics

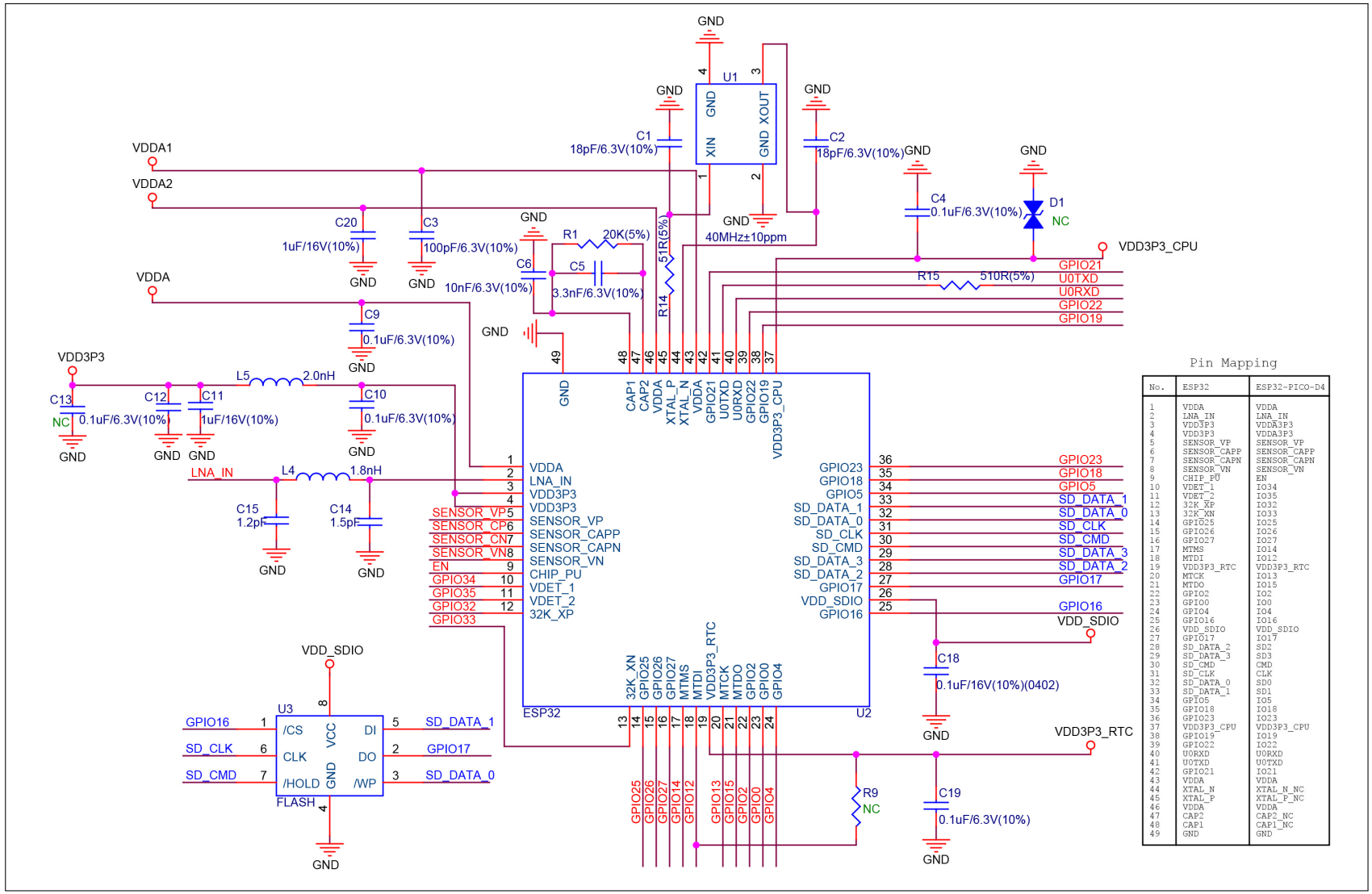
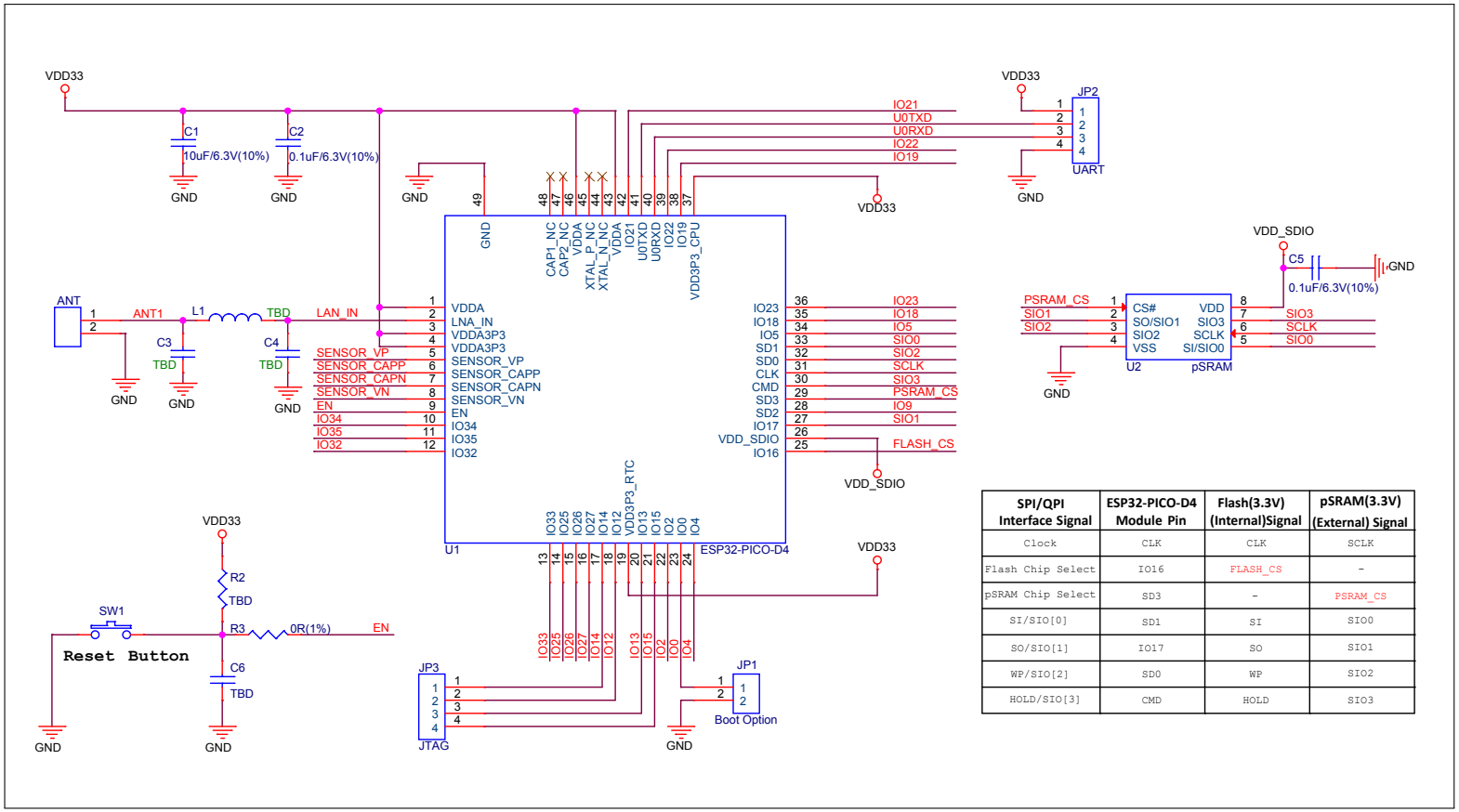


Figure 3: ESP32-PICO-D4 Module Schematics

7. Peripheral Schematics



SPI/QPI Interface Signal	ESP32-PICO-D4 Module Pin	Flash(3.3V) (Internal)Signal	pSRAM(3.3V) (External) Signal
Clock	CLK	CLK	SCLK
Flash Chip Select	IO16	FLASH_CS	-
pSRAM Chip Select	SD3	-	PSRAM_CS
SI/SIO[0]	SD1	SI	SIO0
SO/SIO[1]	IO17	SO	SIO1
WP/SIO[2]	SD0	WP	SIO2
HOLD/SIO[3]	CMD	HOLD	SIO3

Figure 4: ESP32-PICO-D4 Module Peripheral Schematics

Note:

To ensure the power supply to the ESP32 chip during power-up, it is advised to add an RC delay circuit at the EN pin. The recommended setting for the RC delay circuit is usually R = 10 kΩ and C = 0.1 μF. However, specific parameters should be adjusted based on the power-up timing of the module and the power-up and reset sequence timing of the chip. For ESP32's power-up and reset sequence timing diagram, please refer to Section *Power Scheme* in *ESP32 Datasheet*.

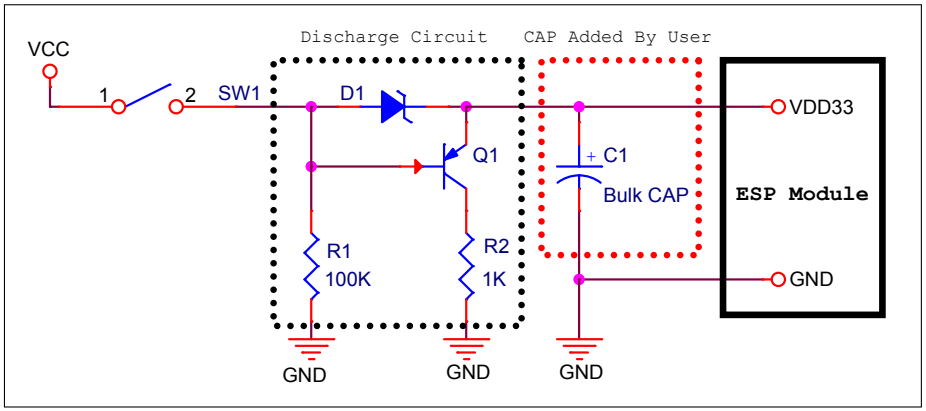


Figure 5: Discharge Circuit for VDD33 Rail

Note:

The discharge circuit can be applied in scenarios where ESP32 is powered on and off repeatedly by switching the power rails, and there is a large capacitor on the VDD33 rail. For details, please refer to Section *Power Scheme* in *ESP32 Datasheet*.

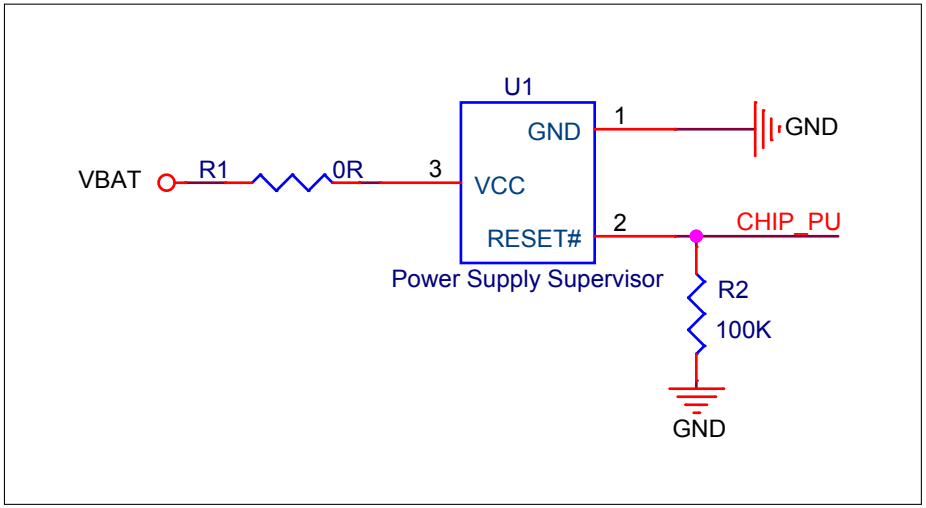
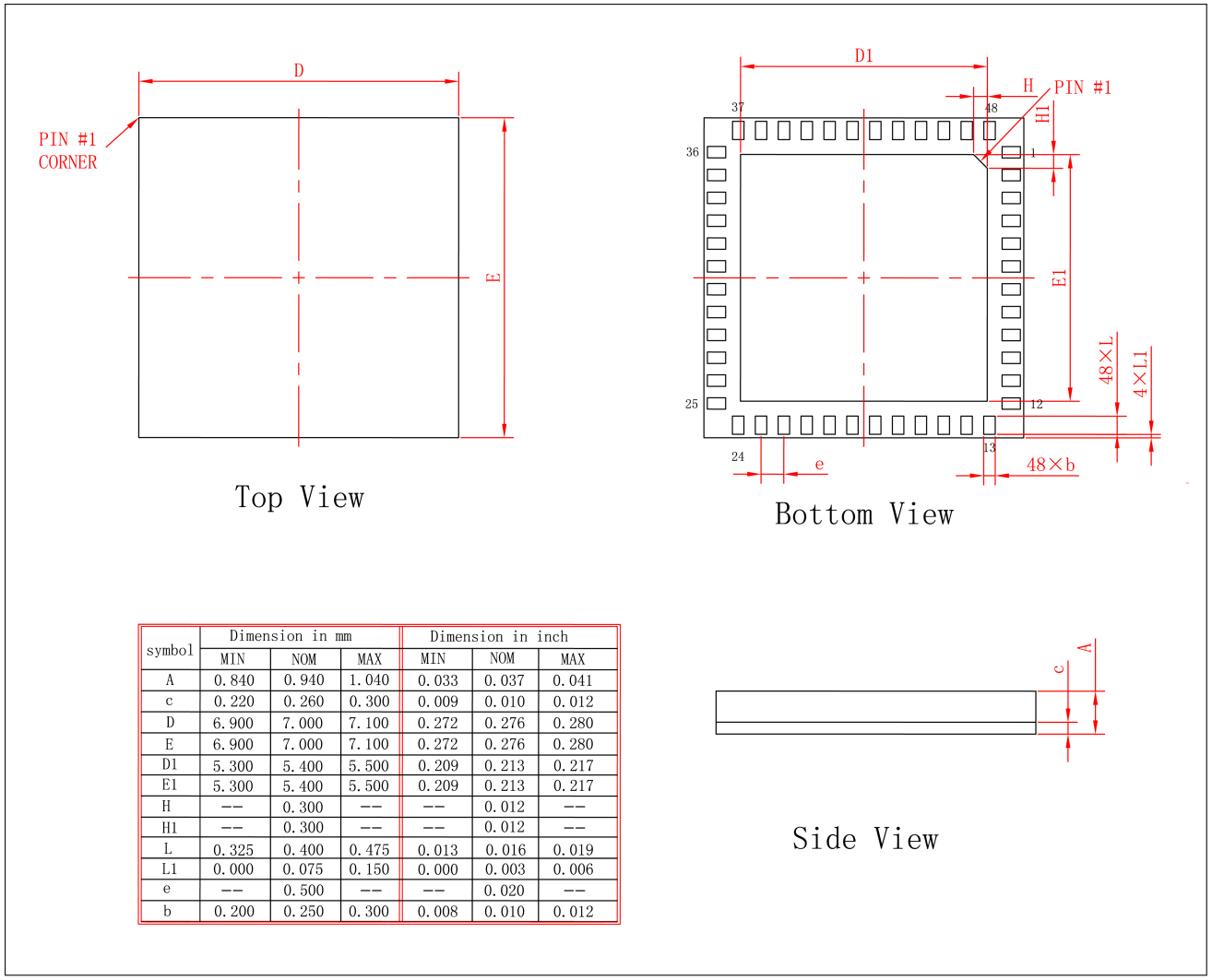


Figure 6: Reset Circuit

Note:

When battery is used as the power supply for ESP32 series of chips and modules, a supply voltage supervisor is recommended to avoid boot failure due to low voltage. Users are recommended to pull CHIP_PU low if the power supply for ESP32 is below 2.3 V.

8. Package Information



symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.840	0.940	1.040	0.033	0.037	0.041
c	0.220	0.260	0.300	0.009	0.010	0.012
D	6.900	7.000	7.100	0.272	0.276	0.280
E	6.900	7.000	7.100	0.272	0.276	0.280
D1	5.300	5.400	5.500	0.209	0.213	0.217
E1	5.300	5.400	5.500	0.209	0.213	0.217
H	--	0.300	--	--	0.012	--
H1	--	0.300	--	--	0.012	--
L	0.325	0.400	0.475	0.013	0.016	0.019
L1	0.000	0.075	0.150	0.000	0.003	0.006
e	--	0.500	--	--	0.020	--
b	0.200	0.250	0.300	0.008	0.010	0.012

Figure 7: ESP32-PICO-D4 Package

9. Learning Resources

9.1 Must-Read Documents

The following link provides documents related to ESP32.

- *ESP32 Datasheet*
  This document provides an introduction to the specifications of the ESP32 hardware, including overview, pin definitions, functional description, peripheral interface, electrical characteristics, etc.
- *ESP-IDF Programming Guide*
  It hosts extensive documentation for ESP-IDF ranging from hardware guides to API reference.
- *ESP32 Technical Reference Manual*
  The manual provides detailed information on how to use the ESP32 memory and peripherals.
- ESP32 Hardware Resources
  The zip files include the schematics, PCB layout, Gerber and BOM list of ESP32 modules and development boards.
- *ESP32 Hardware Design Guidelines*
  The guidelines outline recommended design practices when developing standalone or add-on systems based on the ESP32 series of products, including the ESP32 chip, the ESP32 modules and development boards.
- *ESP32 AT Instruction Set and Examples*
  This document introduces the ESP32 AT commands, explains how to use them, and provides examples of several common AT commands.
- *Espressif Products Ordering Information*

9.2 Must-Have Resources

Here are the ESP32-related must-have resources.

- ESP32 BBS
  This is an Engineer-to-Engineer (E2E) Community for ESP32 where you can post questions, share knowledge, explore ideas, and help solve problems with fellow engineers.
- ESP32 GitHub
  ESP32 development projects are freely distributed under Espressif's MIT license on GitHub. It is established to help developers get started with ESP32 and foster innovation and the growth of general knowledge about the hardware and software surrounding ESP32 devices.
- ESP32 Tools
  This is a webpage where users can download ESP32 Flash Download Tools and the zip file "ESP32 Certification and Test".
- ESP-IDF
  This webpage links users to the official IoT development framework for ESP32.

- ESP32 Resources
  This webpage provides the links to all available ESP32 documents, SDK and tools.

Revision History

Date	Version	Release notes
2019.12	V1.7	• Changed the voltage range of pin VDD3P3_RTC to be consistent with the supply voltage range. • Added a note about pin VDD_SDIO under Table 2.2. • Added a note under Figure 2: *Reflow Profile*. • Added documentation feedback link.
2019.09	V1.6	• Changed the supply voltage range from 2.7 V ~ 3.6 V to 3.0 V ~ 3.6 V; • Added Bluetooth certification and Moisture sensitivity level (MSL) 3 in Table 1 *ESP32-PICO-D4 Specifications*; • Added notes about "Operating frequency range" and "TX power" under Table 7 *Wi-Fi Radio Characteristics*; • Updated Section 7 *Peripheral Schematics* and added a note about RC delay circuit under it.
2019.01	V1.5	Updated the note under Table 2 and that in Section 4; Updated the ESP32-PICO-D4 Module Peripheral Schematics in Chapter 7 by adding the connection between the module and external PSRAM; Changed the RF power control range in Table 9 from –12 ~ +12 to –12 ~ +9 dBm.
2018.10	V1.4	Removed software-specific information from Table 1: ESP32-PICO-D4 Specifications; Added "Cumulative IO output current" entry to Table 4: Absolute Maximum Ratings; Added more parameters to Table 6: DC Characteristics.
2018.06	V1.3	• Changed the voltage range of VDD3P3_RTC from 1.8-3.6V to 2.3-3.6V in Table 2: Pin Description; • Changed the voltage range of VDD_SDIO from "1.8V or the same voltage as VDD3P3_RTC" to "the same voltage as VDD3P3_RTC" in Table 2: Pin Description; • Deleted the content about temperature sensor and LNA pre-amplifier; • Updated Chapter 3: Functional Description; • Updated the note in Chapter 4: Peripherals and Sensors; • Deleted the note on pad49 and added two other notes in Chapter 7: Peripheral Schematics; Changes to electrical characteristics: • Updated Table 4: Absolute Maximum Ratings; • Added Table 5: Recommended Operating Conditions; • Added Table 6: DC Characteristics; • Updated the values of "Gain control step", "Adjacent channel transmit power" in Table 9: Transmitter Characteristics - BLE.
2018.03	V1.2	Updated the pin description of VDD_SDIO in Section 2.2; Updated the ESP32-PICO-D4 Pin Layout in Section 2.1; Updated the ESP32-PICO-D4 Module Schematics in Chapter 6; Updated the ESP32-PICO-D4 Module Peripheral Schematics in Chapter 7.
2017.09	V1.1	Operating voltage/power supply range updated to 2.7 ~ 3.6V;

Date	Version	Release notes
		Added a note in Chapter 7.
2017.08	V1.0	First release.