ESDS312, ESDS314 Data-Line Surge and ESD Protection Diode Array

1 Features

- IEC 61000-4-2 Level 4 ESD Protection
  - ±30-kV Contact Discharge
  - ±30-kV Air Gap Discharge
- IEC 61000-4-4 EFT Protection
  - 80 A (5/50 ns)
- IEC 61000-4-5 Surge Protection
  - 25 A (8/20 μs)
  - Low Surge Clamping Voltage 6.5 V at 25 A Ipp
- IO Capacitance:
  - 4.5 pF (Typical)
- DC Breakdown Voltage: 5.5 V (Minimum)
- Ultra Low Leakage Current: 5 nA (Typical)
- Supports High Speed Interfaces up to 5 Gbps
- Industrial Temperature Range: –40°C to +125°C
- Easy Flow-Through Routing Package (ESDS312)

2 Applications

- End Equipment
  - Ethernet Switches
  - Access Points
  - Gateways
  - Printers
  - DVR and NVR
- Interfaces
  - Ethernet 10/100/1000 Mbps
  - USB 2.0
  - GPIO

3 Description

The ESDS314, ESDS312 devices are unidirectional TVS ESD protection diode array for Ethernet, USB and general purpose data line surge protection up to 25 A (8/20 μs) . The ESDS314, ESDS312 devices are rated to dissipate ESD strikes at the maximum level specified in the IEC 61000-4-2 international standard (Level 4).

The devices features a 4.5-pF IO capacitance per channel making it ideal for protecting high-speed interfaces such as Ethernet 10/100/1000, USB 2.0 and GPIO. The low dynamic resistance and low clamping voltage ensure system level protection against transient events.

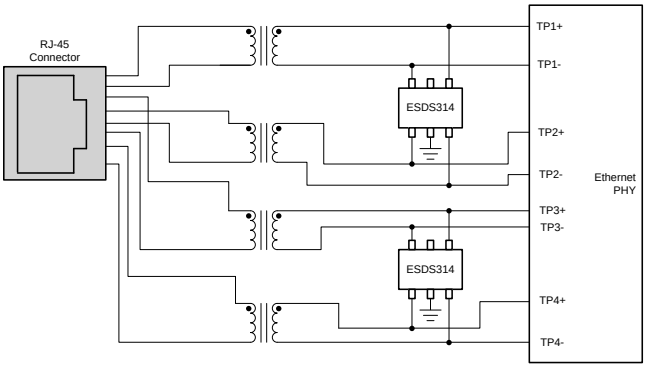
The ESDS314, ESDS312 devices are offered in the industry standard 5-Pin SOT23 packages.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ESDS314	SOT23 (5)	2.9 mm x 1.6 mm x 1.25 mm
ESDS312	SOT23 (5); 2 NC pins	2.9 mm x 1.6 mm x 1.25 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Revision A (July 2018) to Revision B **Page**

- Changed from Advanced Information to Production Data ... 1

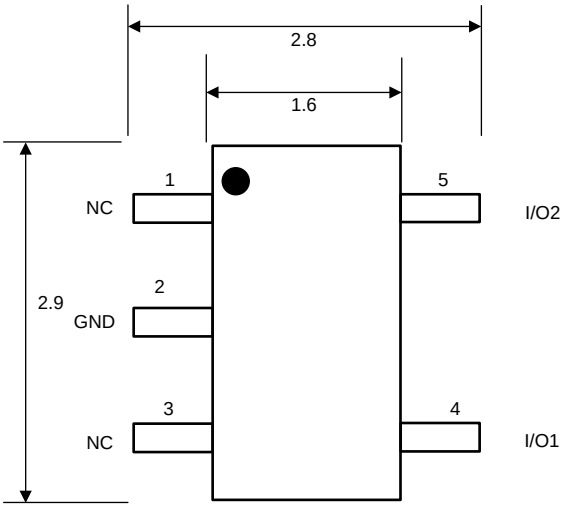
Changes from Original (May 2018) to Revision A **Page**

- Changed from Product Preview to Advance Information ... 1

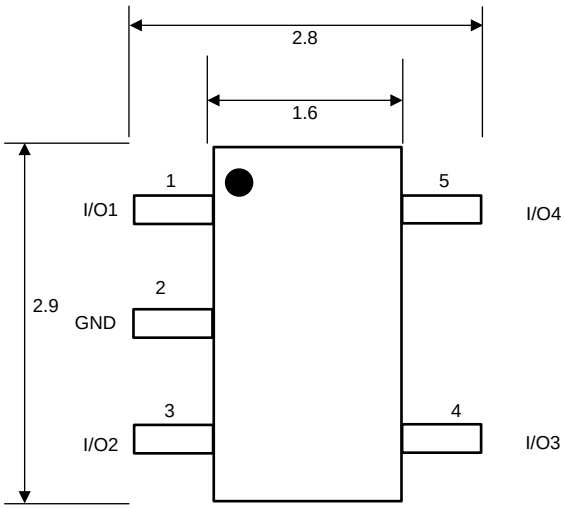
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5 Pin Configuration and Functions

ESDS312 DBV Package
5-Pin SOT23
Top View



ESDS314 DBV Package
5-Pin SOT23
Top View



Pin Functions for ESDS312

PIN		TYPE	DESCRIPTION
NAME	NO.		
I/O1	4	I/O	Surge/ESD protected channels. Connect to the lines being protected.
I/O2	5		
GND	2	GND	Ground. Connect to ground.
NC	1	NC	Not connected; Used for optional straight-through routing. Can be left floating or grounded
NC	3		

Pin Functions for ESDS314

PIN		TYPE	DESCRIPTION
Name	No.		
I/O1	1	I/O	Surge/ESD protected channels. Connect to the lines being protected.
I/O2	3		
I/O3	4		
I/O4	5		
GND	2	GND	Ground. Connect to ground

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
IEC 61000-4-4 Electrical Fast Transient	Peak Power at 25 °C		80	A
IEC 61000-4-5 Surge (t_p 8/20 µs	Peak Power at 25 °C		170	W
	Peak Current at 25 °C		25	A
T_A	Operating free-air temperature	–40	125	°C
T_{stg}	Storage temperature	–65	155	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings -JEDEC Specifications

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, allpins(1)	±2500	V
		Charged device model (CDM), per JEDEC specificationJESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. [Following sentence optional; see the wiki.] Manufacturing with less than 500-V HBM is possible with the necessary precautions. [Following sentence optional; see the wiki.] Pins listed as ±WWW V and/or ±XXX V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. [Following sentence optional; see the wiki.] Manufacturing with less than 250-V CDM is possible with the necessary precautions. [Following sentence optional; see the wiki.] Pins listed as ±YYY V and/or ±ZZZ V may actually have higher performance.

6.3 ESD Ratings - IEC Specifications

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, all pins	±30000	V
		IEC 61000-4-2 Air Discharge, all pins	±30000	

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	0		3.6	V
T_A	Operating Free Air Temperature	–40		125	°C

6.5 Thermal Information

THERMAL METRIC (1)		ESDS312 DBV (SOT-23) 5 PINS	ESDS314 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	163.9	127.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	113.4	78.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	76.9	43.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	59.8	24.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	76.8	43.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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6.6 Electrical Characteristics

At TA = 25°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{IO} < 500 nA, across operating temperature range			3.6	V
$I_{LEAKAGE}$	Leakage current at 3.6 V	V_{IO} = 3.6 V, Any IO pin to GND		5	50	nA
V_{BRF}	Breakdown voltage, IO to GND (1)	I_{IO} = 1 mA	4.5		7.5	V
V_{FWD}	Forward Voltage, GND to IO	I_{IO} = 1 mA		0.8		V
V_{HOLD}	Holding Voltage, IO to GND (2)	I_{IO} = 1 mA		5		V
V_{CLAMP}	Surge Clamping voltage, t_p = 8/20 µs	I_{PP} = 1 A, Any IO pin to GND		5		V
V_{CLAMP}		I_{PP} = 12 A, Any IO pin to GND		5.6		V
V_{CLAMP}		I_{PP} = 25 A, Any IO pin to GND		6.5		V
V_{CLAMP}		I_{PP} = 1 A, GND to any IO pin		1		V
V_{CLAMP}		I_{PP} = 12 A, GND to any IO pin		2.1		V
V_{CLAMP}		I_{PP} = 25 A, GND to any IO pin		3.6		V
V_{CLAMP}	TLP Clamping Voltage, t_p = 100 ns	I_{PP} = 16 A, Any IO pin to GND		5.5		V
V_{CLAMP}		I_{PP} = 16 A, GND to any IO pin		2.2		V
C_{LINE}	Line capacitance, Any IO to GND	V_{IO} = 0 V, V_{p-p} = 30 mV, f = 1 MHz		4.5	5.5	pF
ΔC_{LINE}	Variation of line capacitance	C_{LINE1} - $C_{LINE2,}$ V_{IO} = 0 V, Vp-p = 30 mV, f = 1 MHz		0.05	0.1	pF
C_{CROSS}	Line-to-line capacitance	V_{IO} = 0V, V_{rms} = 30 mV, f = 1 MHz		2.25	2.75	pF

(1) VBRF and VBRR are defined as the voltage obtained at 1 mA when sweeping the voltage up, before the device latches into the snapback state
(2) VHOLD is defined as the voltage when 1 mA is applied, after the device has successfully latched into the snapback state.

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6.7 Typical Characteristics

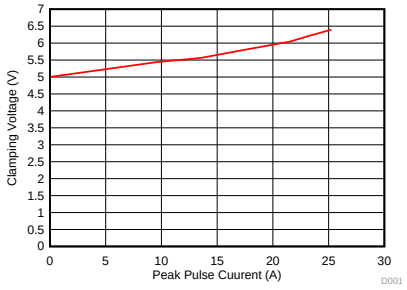


Figure 1. Clamping Voltage vs. Peak Pulse Current (t_p= 8/20 µs), Any IO Pin to GND

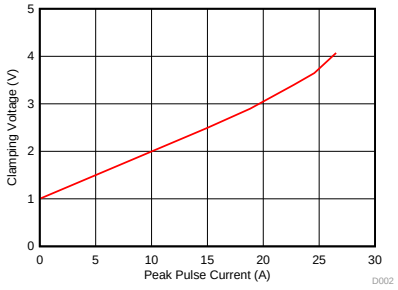


Figure 2. Clamping Voltage vs. Peak Pulse Current (t_p= 8/20 µs), GND to Any IO Pin

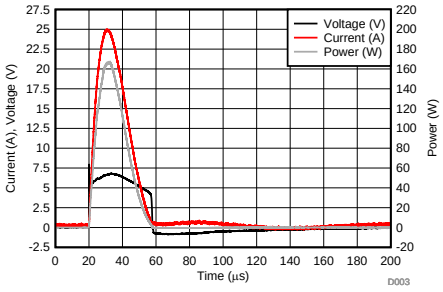


Figure 3. Surge Current, Clamping Voltage and Power Curve (t_p = 8/20 µs), Any IO Pin to GND

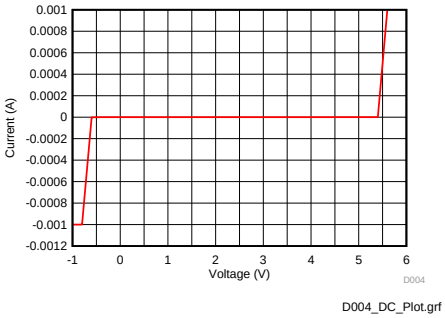


Figure 4. DC I-V Curve

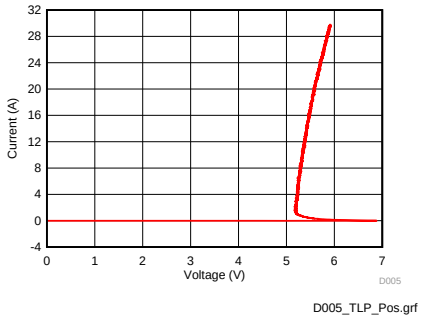


Figure 5. TLP I-V Curve, IO to GND, t_p = 100 ns

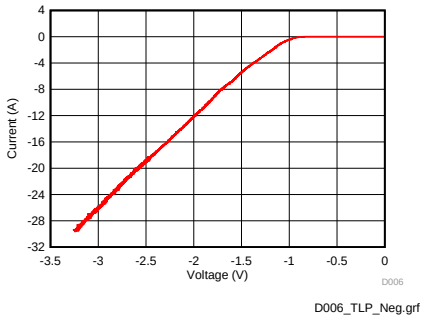


Figure 6. TLP I-V Curve, IO to GND Negative, t_p=100 ns

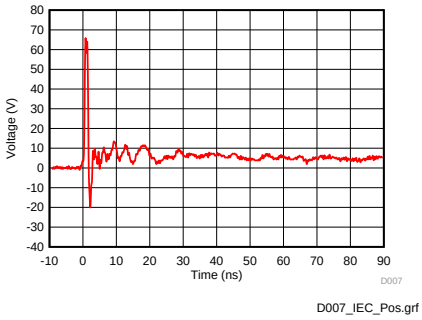


Figure 7. +8 kV IEC 61000-4-2 Clamping Voltage Waveform

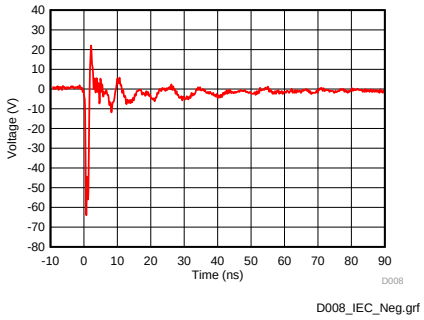


Figure 8. -8 kV IEC 61000-4-2 Clamping Voltage Waveform

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Typical Characteristics (continued)

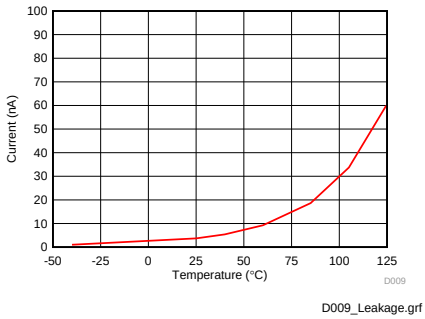


Figure 9. DC Leakage vs. Ambient Temperature, Bias Voltage = 3.6 V

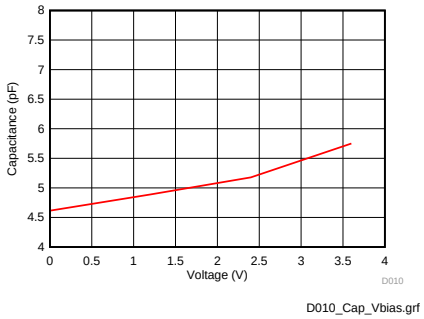


Figure 10. Capacitance vs. Bias Voltage at 25°C

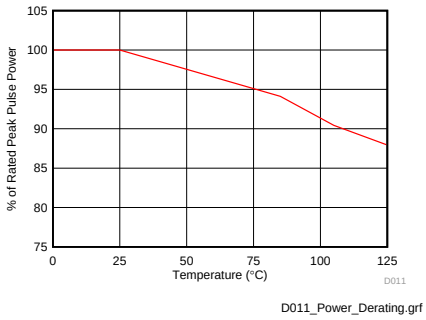


Figure 11. Surge Power Derating with Respect To Ambient Temperature

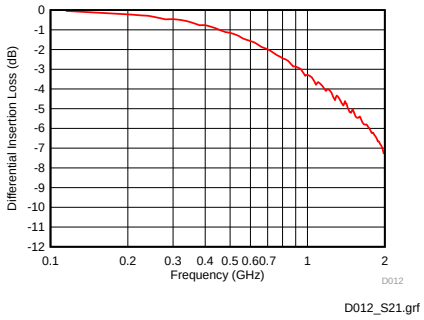


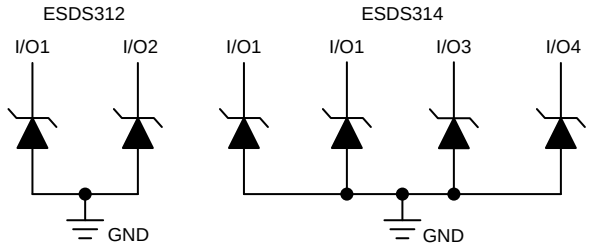
Figure 12. Differential Insertion Loss

7 Detailed Description

7.1 Overview

The ESDS314, ESDS312 devices are unidirectional ESD Protection Diode with a low capacitance. These devices can dissipate high surge currents upto 25 A (8/20 µs) and ESD strikes above the maximum level specified by the IEC 61000-4-2 International Standard. The low capacitance makes this device ideal for protecting high-speed signal interfaces such as Ethernet 10/100/1000 Mbps and general purpose high speed data lines.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 IEC 61000-4-4 EFT Protection

The I/O pins of ESDS314 and ESDS312 can withstand surge events (IEC 61000-4-5, 8/20 µs waveform) up to 25 A and 170 W. These devices also provide ESD protection up to ±30-kV contact and ±30-kV air gap per IEC 61000-4-2 standard. The I/O pins can withstand an electrical fast transient burst of up to 80 A (IEC 61000-4-4 5/50 ns waveform, 4 kV with 50-Ω impedance). The capacitance between each I/O pin to ground is 4.5 pF (typical) and 5.5 pF (maximum). This device supports data rates up to 1 Gbps.

The reverse DC breakdown voltage of each I/O pin is a minimum of 4.5 V. This ensures that sensitive equipment is protected from surges above the reverse standoff voltage of 3.6 V. The I/O pins feature an ultra-low leakage current of 100 nA (maximum) with a bias of 3.6 V. This device features an industrial operating range of –40°C to +125°C.

7.4 Device Functional Modes

The ESDS314, ESDS312 devices are a passive integrated circuit that triggers when voltages are above V_{BRF} or below 0.7 V. During ESD events, voltages as high as ±30 kV (air) can be directed to ground via the internal diode network. When the voltages on the protected line fall below the trigger levels of ESDS314, ESDS312 (usually within a few nano-seconds) the devices reverts to passive.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The ESDS314, ESDS312 devices are diode type TVS which is used to provide a path to ground for dissipating surge and ESD events on high-speed signal lines between a human interface connector and a system. As the current from surge or ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a safe level for the protected IC.

8.2 Typical Application

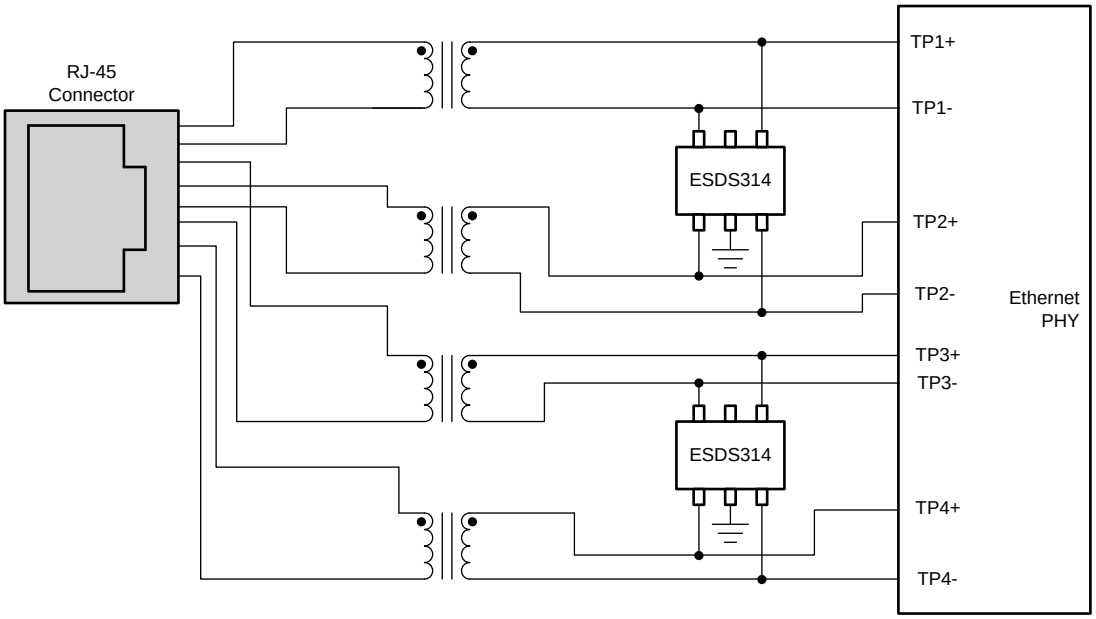


Figure 13. ESDS314 Protecting the Ethernet 1Gbps Interface

8.2.1 Design Requirements

A typical operation for the ESDS314 would be protecting a high speed dataline similar to one shown in Figure 13. In this example, the ESDS314 is protecting an Ethernet PHY's data lines that has a nominal operating voltage of 3.6 V. Many of the Ethernet interfaces that connect to long cables require protection against ±1 kV surge test through a 42-Ω coupling resistor and a 0.5 µF capacitor, equaling roughly 24 A of surge current. Without any input protection, if a surge event is caused by lightning, coupling, ringing, or any other fault condition, this input voltage will rise to hundreds of volts for multiple microseconds, harming the device.

For Ethernet 1000Base-T (1Gbps), application design parameters listed in Table 1 are known.

Table 1. Design Parameters

DESIGN PARAMETER	VALUE
Signal range on differential data line pairs	0 to 3.6 V
Operating frequency	125 MHz

8.2.2 Detailed Design Procedure

8.2.2.1 Signal Range

The ESDS314 has 4 identical surge protection channels with each channel supporting a signal range of 0 to 3.6 V. The device will work well with any Ethernet PHY that drives the single ended voltage on the data line up to a 3.6 V.

8.2.2.2 Operating Frequency

The ESDS314 has a capacitance of 4.5 pF (typical) and can support the 125 MHz operation of Ethernet 1000Base-T application

8.2.3 Application Curves

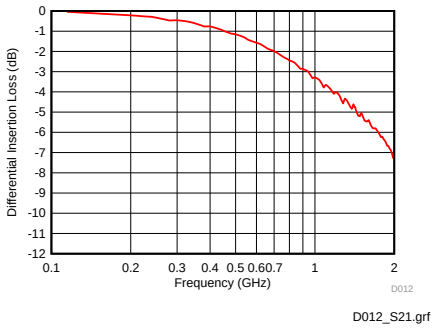


Figure 14. Differential Insertion Loss vs. Frequency

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9 Power Supply Recommendations

The ESDS314, ESDS312 devices are passive ESD devices and there is no need to power it. Take care not to violate the recommended I/O specification (0 V to 3.6 V) to ensure the device functions properly.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Example

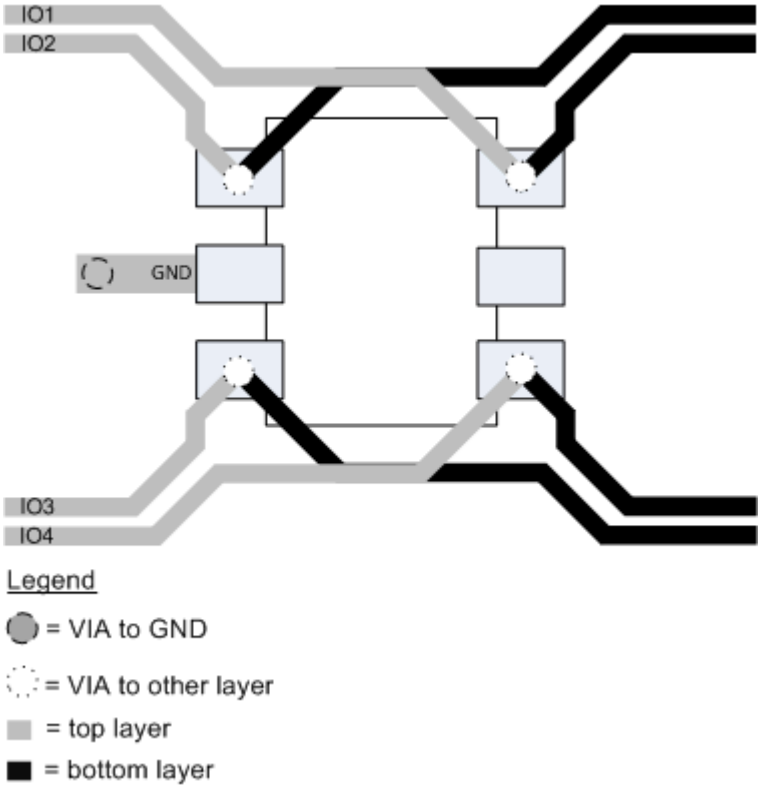


Figure 15. Layout Example for 4-channel Device

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.

11.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ESDS312DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	1R4B	Samples
ESDS314DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	1R2B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

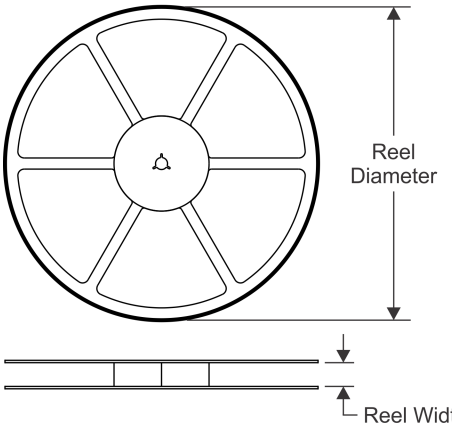
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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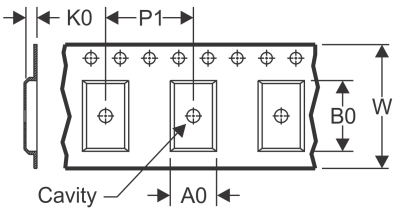
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

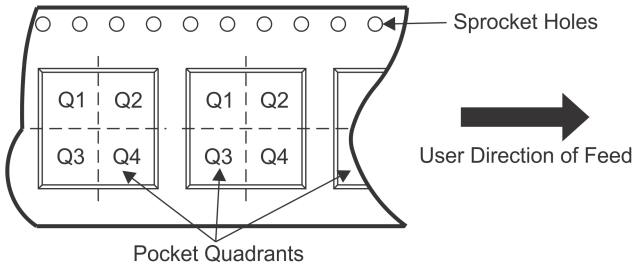


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

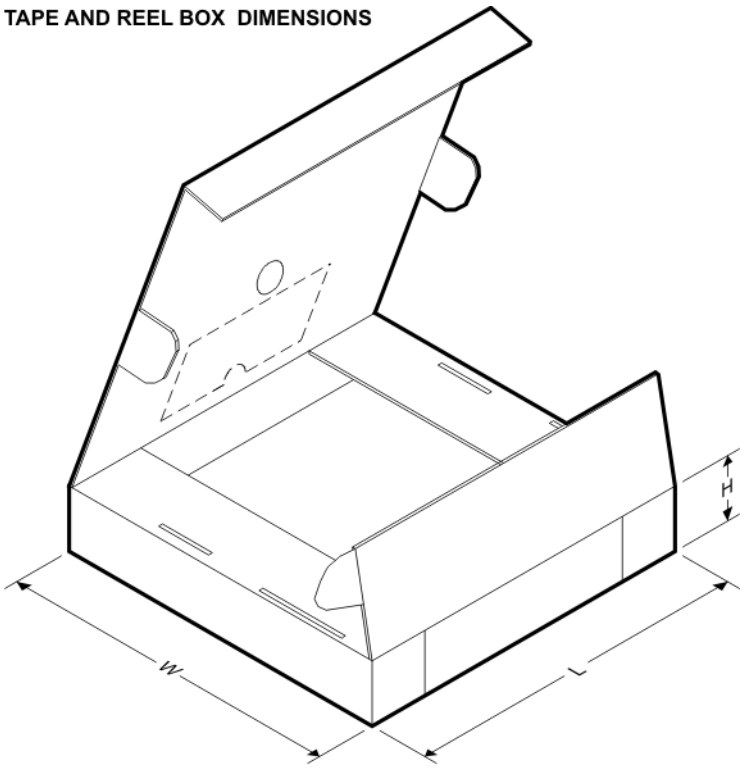
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESDS312DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
ESDS314DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

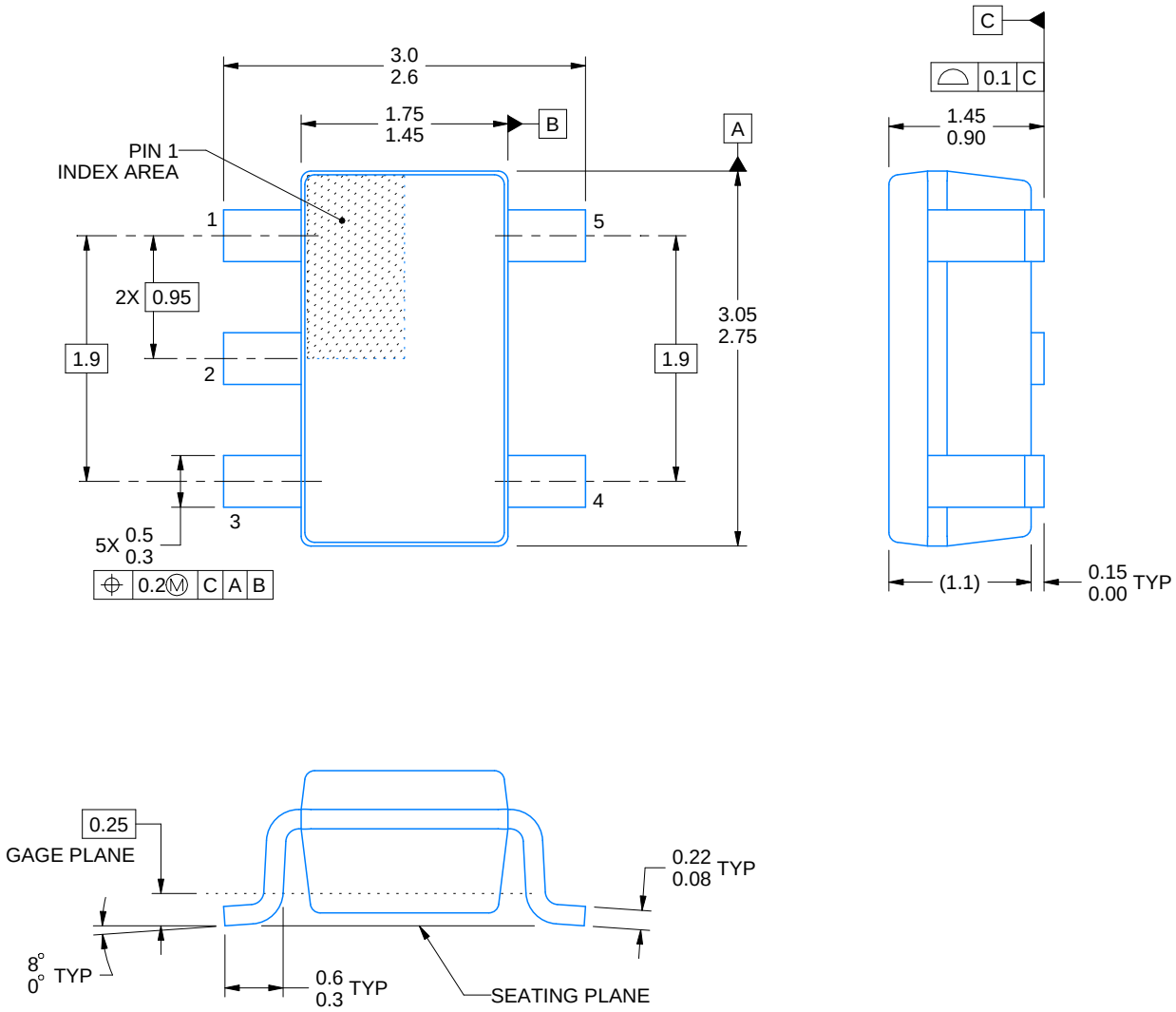
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESDS312DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
ESDS314DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

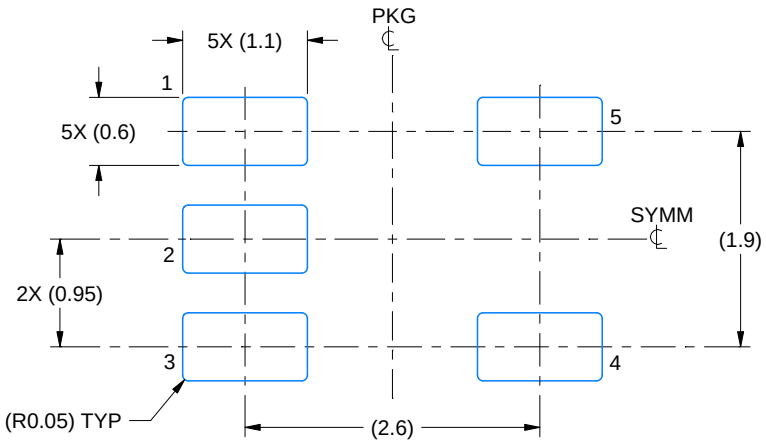
SMALL OUTLINE TRANSISTOR



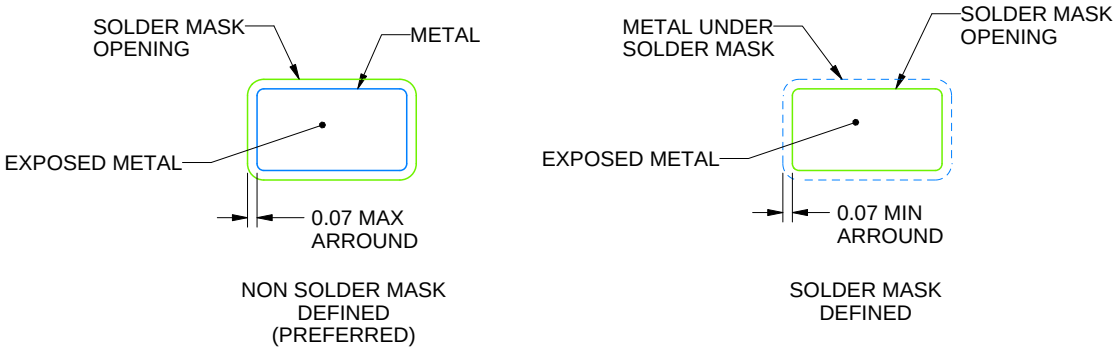
4214839/E 09/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

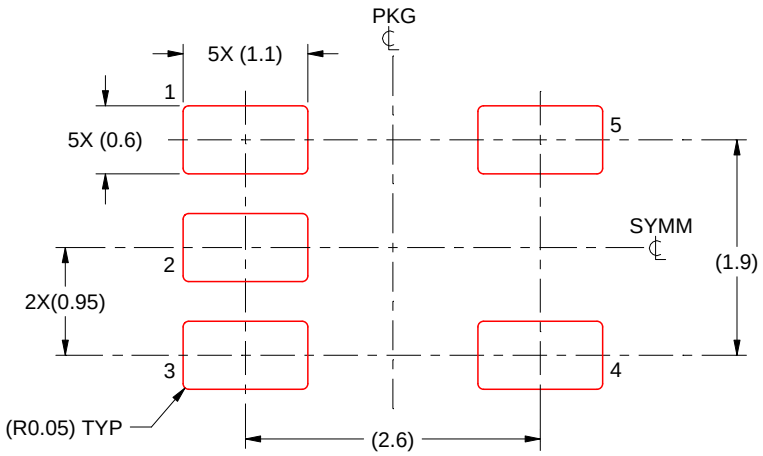


SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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