ESDAxxSCx

Quad Transil™ array for ESD protection

Features

- 4 unidirectional Transil Functions
- Low leakage current: I_R max. < 20 µA at V_{RM}
- 400 W peak pulse power (8/20 µs)

Benefits

- High ESD protection level: up to 25 kV
- High integration
- Suitable for high density boards

Complies with the following standards:

- IEC 61000-4-2 level 4:
  - 15 kV (air discharge)
  - 8 kV (contact discharge)
- MIL STD 883E- Method 3015-7: class3B
  - human body model

Applications

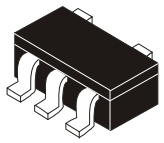
Where transient overvoltage protection in ESD sensitive equipment is required, such as :

- Computers
- Printers
- Communication systems
- Cellular phone handsets and accessories
- Other telephone set
- Set top boxes

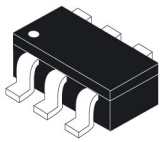
Description

The ESDAxxSC5 and ESDAxxSC6 are monolithic voltage suppressors designed to protect components which are connected to data and transmission lines against ESD.

They clamp the voltage just above the logic level supply for positive transients, and to a diode drop below ground for negative transient.



SOT23-5L (SC-59)
ESDAxxSC5



SOT23-6L (SC-59)
ESDAxxSC6

Figure 1. ESDAxxSC5 functional diagram

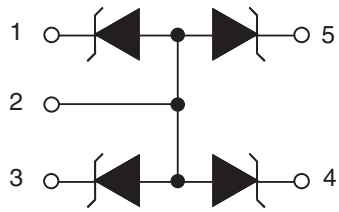
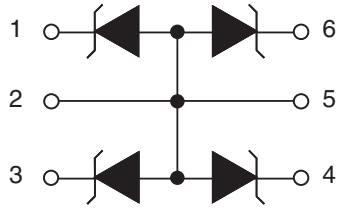


Figure 2. ESDAxxSC6 functional diagram



TM: Transil is a trademark of STMicroelectronics.

1 Characteristics

Table 1. Absolute ratings (T_{amb} = 25 °C)

Symbol	Parameter		Value	Unit
V_{PP}	ESD discharge	MIL STD 883E - Method 3015-7 IEC61000-4-2 air discharge IEC61000-4-2 contact discharge	25	kV
P_{PP}	Peak pulse power (8/20µs)	ESDA5V3SCx ESDA6V1SCx	500 400	W
		ESDA14V2SCx ESDA17SC6 ESDA19SC6 ESDA25SC6	300	W
T_j	Junction temperature		150	°C
T_{stg}	Storage temperature range		-55 to +150	°C
T_L	Maximum lead temperature for soldering during 10 s at 5mm for case		260	°C
T_{op}	Operating temperature range		-40 to +125	°C

Table 2. Electrical characteristics - definitions (T_{amb} = 25 °C)

Symbol	Parameter
V_{RM}	Stand-off voltage
V_{BR}	Breakdown voltage
V_{CL}	Clamping voltage
I_{RM}	Leakage current @ V_{RM}
I_{PP}	Peak pulse current
αT	Voltage temperature coefficient
C	Capacitance
R_d	Dynamic resistance
V_F	Forward voltage dropt

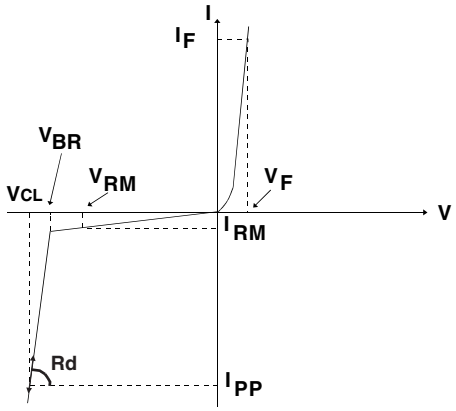


Table 3. Electrical characteristics - values (T_{amb} = 25 °C)

Order codes	V_{BR} @ I_R			I_{RM} @ V_{RM}		Rd	αT	C	V_F@ I_F	
	min.	max.		max.		typ.(1)	max.(2)	typ. 0 V bias	max.	
	V	V	mA	µA	V	mΩ	10^{-4}/C	pF	V	mA
ESDA5V3SC5 ESDA5V3SC6	5.3	5.9	1	2	3	230	5	280	1.25	200
ESDA6V1SC5 ESDA6V1SC6	6.1	7.2	1	20	5.25	350	6	190	1.25	200
ESDA14V2SC5 ESDA14V2SC6	14.2	15.8	1	5	12	650	10	100	1.25	200
ESDA17SC6 ESDA19SC6	17 19	19 21	1 1	0.075 0.1	14 15	700 800	10 8.5	85 80	1.2 1.2	10 10
ESDA25SC6	25	30	1	1	24	1000	10	60	1.2	10

1. Square pulse, I_{pp} = 15 A, t_p=2.5 µs.
2. Δ VBR = αT* (T_{amb} -25 °C) * V_{BR} (25 °C)

Figure 3. Peak power dissipation versus initial junction temperature

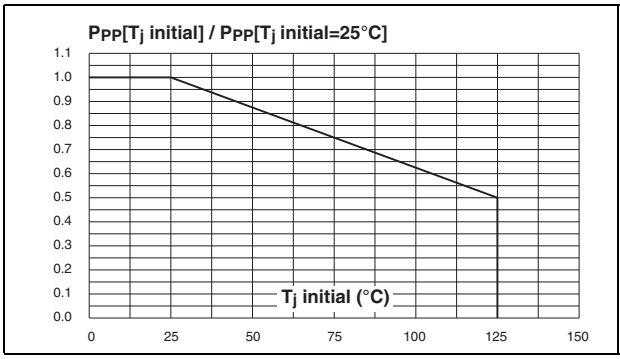


Figure 4. Peak pulse power versus exponential pulse duration (Tj initial = 25 °C)

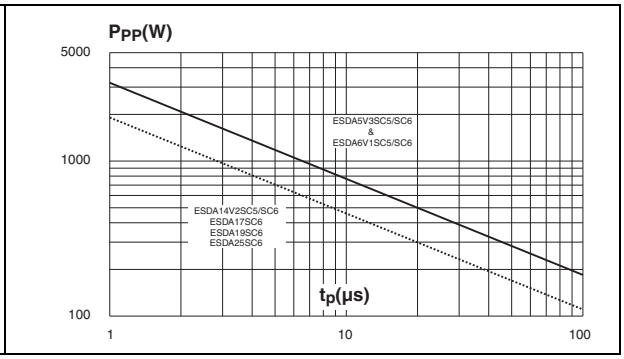


Figure 5. Clamping voltage versus peak pulse current (Tj initial = 25 °C). Rectangular waveform tp = 2.5 µs

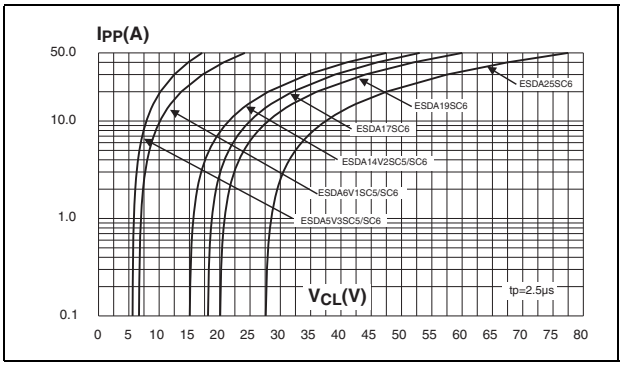


Figure 6. Capacitance versus reverse applied voltage (typical values)

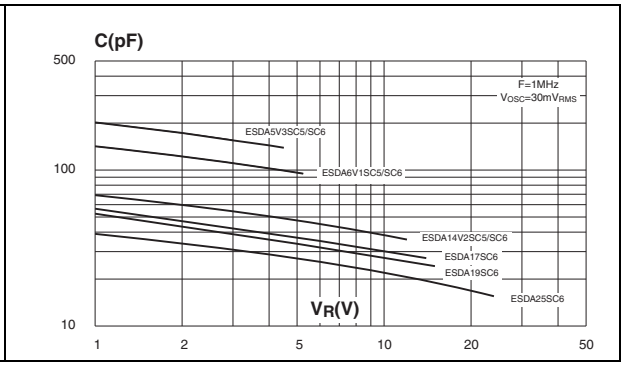


Figure 7. Relative variation of leakage current versus junction temperature (typical values)

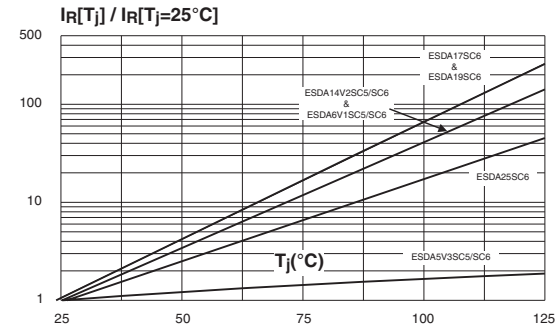
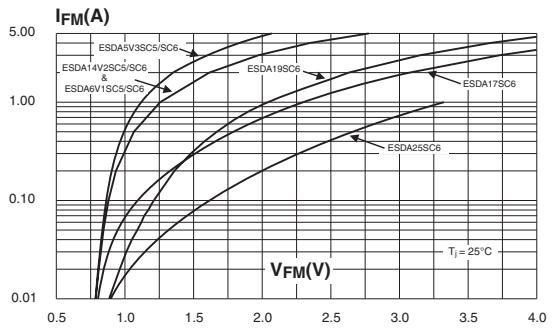


Figure 8. Peak forward voltage drop versus peak forward current (typical values)



2 Application information

2.1 Calculation of the clamping voltage use of the dynamic resistance

The ESDA family has been designed to clamp fast spikes like ESD. Generally the PCB designers need to calculate easily the clamping voltage V_{CL}. This is why we give the dynamic resistance in addition to the classical parameters. The voltage across the protection cell can be calculated with the following formula:

$$V_{CL} = V_{BR} + R_d I_{PP}$$

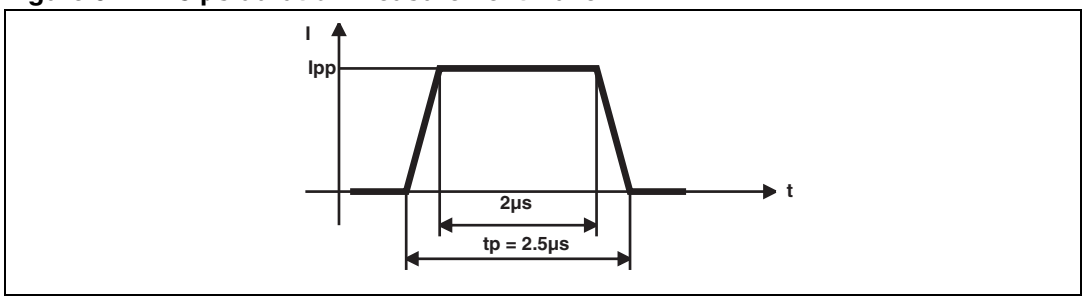
Where I_{PP} is the peak current through the ESDA cell.

As the value of the dynamic resistance remains stable for a surge duration lower than 20 µs, the 2.5 µs rectangular surge is well adapted. In addition both rise and fall times are optimized to avoid any parasitic phenomenon during the measurement of R_d.

2.2 Dynamic resistance measurement

The short duration of the ESD has led us to prefer a more adapted test wave, as below defined, to the classical 8/20µs and 10/1000 µs surges.

Figure 9. 2.5 µs duration measurement wave



2.3 ESD protection with ESDAxxSCx

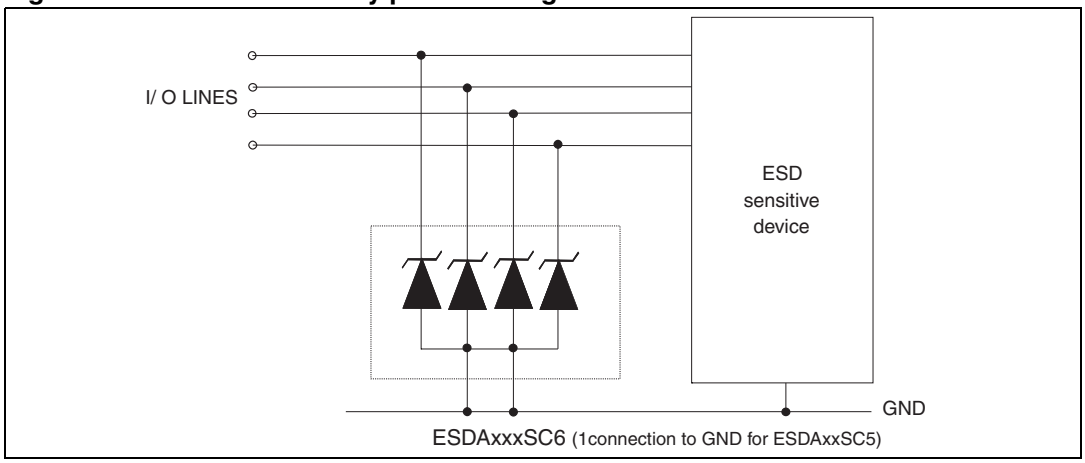
Electrostatic discharge (ESD) is a major cause of failure in electronic systems.

Transient Voltage Suppressors (TVS) are an ideal choice for ESD protection. They are capable of clamping the incoming transient overvoltage to a low enough level such that damage to the protected semiconductor is prevented.

Surface mount TVS arrays offer the best choice for minimal lead inductance.

They serve as parallel protection elements, connected between the signal line and ground. As the transient rises above the operating voltage of the device, the TVS array becomes a low impedance path diverting the transient current to ground.

Figure 10. ESDAxxSCx array protection against ESD



The ESDAxxSCx array is the ideal board level protection of ESD sensitive semiconductor components.

The tiny SOT23-5L and SOT23-6L packages allow design flexibility in the high density boards where the space saving is at a premium. This enables to shorten the routing and contributes to hardening against ESD.

2.4 Advice for optimizing circuit board layout

Circuit board layout is a critical design step in the suppression of ESD induced transients. The following guidelines are recommended:

- The ESDAxxSC5/6 should be placed as close as possible to the input terminals or connectors.
- The path length between the ESD suppressor and the protected line should be minimized
- All conductive loops, including power and ground loops should be minimized
- The ESD transient return path to ground should be kept as short as possible
- Ground planes should be used whenever possible

3 Technical information

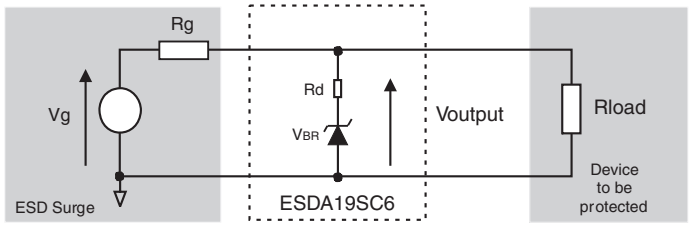
3.1 ESD protection

The ESDA19SC6 is particularly optimized to perform ESD protection. ESD protection is achieved by clamping the unwanted overvoltage. The clamping voltage is given by the following formula :

$$V_{CL} = V_{BR} + R_d \cdot I_{PP}$$

As shown in *Figure 11.*, the ESD strikes are clamped by the transient voltage suppressor.

Figure 11. ESD clamping behavior (example)



To have a good approximation of the remaining voltages at both VI/O side, we provide the typical dynamical resistance value Rd. By taking into account the following hypothesis :

$$R_g > R_d \text{ and } R_{load} > R_d$$

we have:

$$V_{output} = V_{BR} + R_d \times \frac{V_g}{R_g}$$

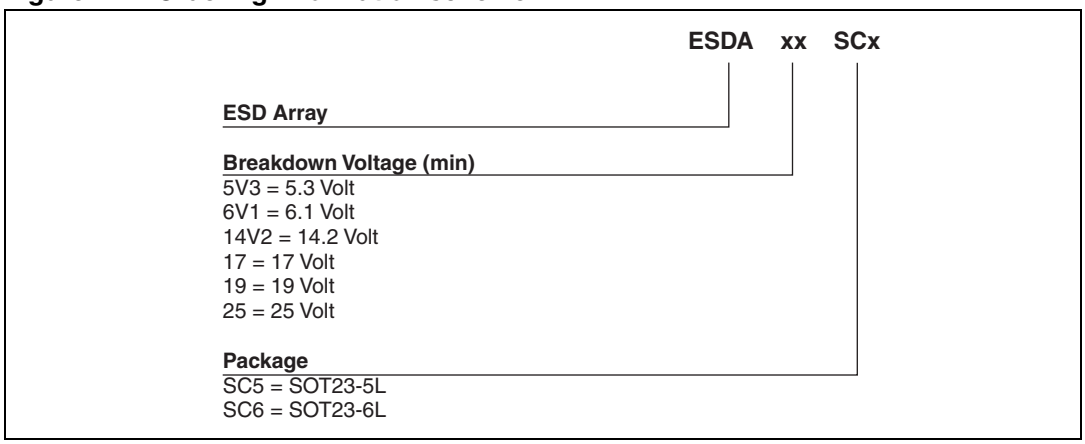
The results of the calculation done for V_g = 8 kV, R_g = 330 Ω (IEC61000-4-2 standard), V_{BR} = 19 V (typ.) and R_d = 0.80 Ω (typ.) give:

$$V_{ouput} = 38.4 \text{ V}$$

This confirms the very low remaining voltage across the device to be protected. It is also important to note that in this approximation the parasitic inductance effect was not taken into account. This could be a few tenths of volts during a few nanoseconds at the output side.

4 Ordering information

Figure 12. Ordering information scheme



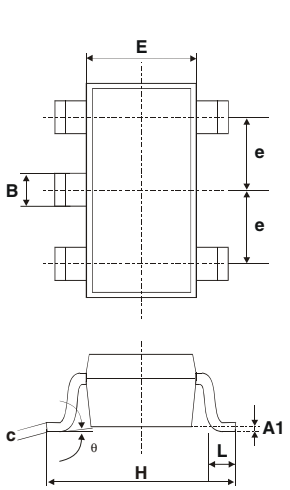
5 Package information

- Epoxy meets UL94, V0 standard

In order to meet environmental requirements, ST (also) offers these devices in ECOPACK® packages. ECOPACK® packages are Lead-free. The category of second level Interconnect is marked on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Table 4. SOT23-5L dimensions



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90		1.45	0.035		0.057
A1	0		0.10	0		0.004
A2	0.90		1.30	0.035		0.051
b	0.35		0.50	0.014		0.020
c	0.09		0.20	0.004		0.008
D	2.80		3.05	0.11		0.118
E	1.50		1.75	0.059		0.069
e		0.95			0.037	
H	2.60		3.00	0.102		0.118
L	0.10		0.60	0.004		0.024
M	0°		10°	0°		10°

Figure 13. SOT23-5L footprint (dimensions in mm)

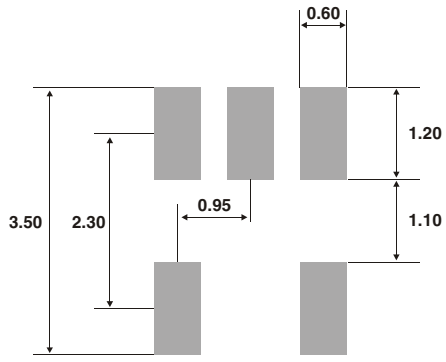
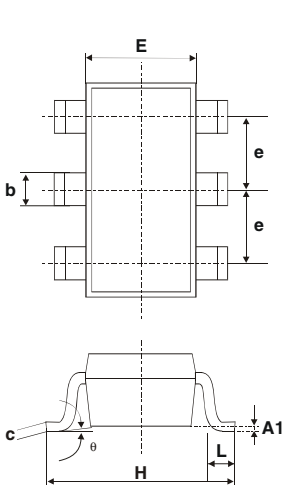
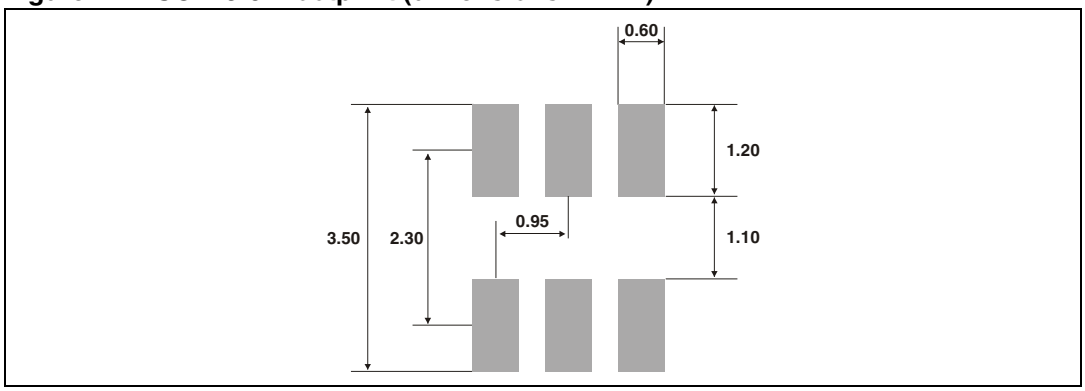


Table 5. SOT23-6L dimensions



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90		1.45	0.035		0.057
A1	0		0.10	0		0.004
A2	0.90		1.30	0.035		0.051
b	0.35		0.50	0.014		0.020
c	0.09		0.20	0.004		0.008
D	2.80		3.05	0.11		0.118
E	1.50		1.75	0.059		0.069
e		0.95			0.037	
H	2.60		3.00	0.102		0.118
L	0.10		0.60	0.004		0.024
θ	0°		10°	0°		10°

Figure 14. SOT23-6L footprint (dimensions in mm)



6 Ordering information

Table 6. Ordering information

Order codes	Marking	Package	Weight	Base qty	Delivery mode
ESDA5V3SC5	EC53	SOT23-5L	16.7 mg	3000	Tape and reel
ESDA6V1SC5	EC61				
ESDA14V2SC5	EC15				
ESDA5V3SC6	ES53	SOT23-6L			
ESDA6V1SC6	ES61				
ESDA14V2SC6	ES15				
ESDA17SC6	ES17				
ESDA19SC6	ES19				
ESDA25SC6	ES25				

7 Revision history

Table 7. Document revision history

Date	Revision	Description of changes
Nov-2003	7F	Previous issue.
4-Nov-2004	8	SOT23-6L package dimensions change for reference “D” from 3.0 millimeters (0.118 inches) to 3.05 millimeters (0.120 inches).
22-Nov-2007	9	Reformatted to current standard. Units for I_{RM} MAX in *Table 3* corrected to µA. *Ordering information scheme* expanded to cover all devices. Package information for SOT23-5L updated.

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