# Excalibur Device Overview

May 2002, ver. 2.0 Data Sheet

## Features...

- Combination of a world-class RISC processor system with industry-leading programmable logic on a single device
- Industry-standard ARM922T™ 32-bit RISC processor core operating at up to 200 MHz
  - ARMv4T instruction set with Thumb® extensions
  - Memory management unit (MMU) included for real-time operating system (RTOS) support
  - Harvard cache architecture with 64-way set associative separate 8-Kbyte instruction and 8-Kbyte data caches
- APEX™ 20KE-like programmable logic architecture ranging from 100,000 to 1,000,000 gates (see Table 1 on page 3)
- Advanced bus architecture based on advanced microcontroller bus architecture (AMBA™) high-performance bus (AHB)
- Embedded programmable on-chip peripherals
  - ETM9 embedded trace module to assist software debugging
  - Flexible interrupt controller
  - Universal asynchronous receiver/transmitter (UART)
  - General-purpose timer
  - Watchdog timer
- Advanced memory support
  - Internal single-port SRAM up to 256 Kbytes
  - Internal dual-port SRAM up to 128 Kbytes
  - Internal SDRAM controller
    - Single data-rate (SDR) and double data-rate (DDR) support
    - Up to 512 Mbytes
    - Data rates to 133 (266) MHz
  - Expansion bus interface (EBI)
    - Compatible with industry-standard flash memory, SRAMs, and peripheral devices
    - Four devices, each up to 32 Mbytes
- PLD configuration/reconfiguration possible via the embedded processor software
- Fully configurable memory map
- Extensive embedded system debug facilities
  - SignalTap™ embedded logic analyzer
  - ARM® JTAG processor debug support
  - Real-time data/instruction processor trace
  - Background debug monitoring via the IEEE Std. 1149.1 (JTAG) interface

- Multiple and separate clock domains controlled by software-programmable phased-lock loops (PLLs) for embedded processor, SDRAM, and PLD
  - ClockBoost™ circuitry provides clock multiplication for the embedded stripe and the PLD
  - ClockLock™ circuitry reduces clock delay and skew in the PLD
- Advanced packaging options (see Tables 2 and 3 on page 3)
- 1.8-V supply voltage, but many I/O standards supported:
  - SSTL-3
  - LVTTL
  - GTL+
  - LVDS
- SOPC Builder system development tool
  - Intuitive graphical user interface (GUI) simplifies system definition and customization
  - Wizard interface facilitates function customization for each component
  - Automatically-generated logic integrates processors, memories, peripherals, IP cores, on-chip buses and bus arbiters
  - VHDL or Verilog HDL code created for system connection
  - Software develoment environment generated to match the target hardware
- Extended Quartus™ II development environment for Excalibur™ support
  - Integrated hardware and software development environment
  - MegaWizard® Plug-In interface configures the embedded processor, PLD, bus connections, and peripherals
  - C/C++ compiler, source-level debugger, and RTOS support



This document provides updated information about Excalibur devices and should be used together with the *APEX 20K Programmable Logic Device Family Data Sheet*.

| Table 1. Excalibur Device Overview | | | |
|---|---|---|---|
| **Feature** | **EPXA1** | **EPXA4** | **EPXA10** |
| Processor | ARM922T | ARM922T | ARM922T |
| Maximum operating frequency | 200 MHz | 200 MHz | 200 MHz |
| Single-port SRAM | 32 Kbytes | 128 Kbytes | 256 Kbytes |
| Dual-port SRAM | 16 Kbytes | 64 Kbytes | 128 Kbytes |
| Typical gates | 100,000 | 400,000 | 1,000,000 |
| Logic elements (LEs) | 4,160 | 16,640 | 38,400 |
| Embedded system blocks (ESBs) | 26 | 104 | 160 |
| Maximum system gates | 263,000 | 1,052,000 | 1,772,000 |
| Maximum user I/Os *(1)* | 246 | 488 | 711 |
| UART, timer, watchdog timer | Yes | Yes | Yes |
| JTAG debug module | Yes | Yes | Yes |
| Embedded trace module | – | Yes | Yes |
| General purpose I/O Port | 4 bits | 8 bits | - |
| Low-power PLL | Yes | - | - |

*Note:*
(1) Maximum available user I/Os = shared stripe I/O + PLD I/O

| Table 2. Excalibur Device FineLine™ BGA Package Sizes | | | |
|---|---|---|---|
| **Feature** | **FineLine BGA** | | |
| | **484 Pin** | **672 Pin** | **1,020 Pin** |
| Pitch (mm) | 1.00 | 1.00 | 1.00 |
| Area ($mm^2$) | 529 | 729 | 1,089 |
| Length × Width (mm × mm) | 23 × 23 | 27 × 27 | 33 × 33 |

| Table 3. Excalibur Device FineLine BGA Package Options & User I/O Counts *Note (1)* | | | |
|---|---|---|---|
| **Device** | **FineLine BGA** | | |
| | **484 Pin** | **672 Pin** | **1,020 Pin** |
| EPXA1 | 186 | 246 | |
| EPXA4 | | 426 | 488 |
| EPXA10 | | | 711 |

*Note to Tables 2 and 3:*
(1) I/O counts include dedicated input and clock pins.

## General Description

Devices belonging to the Excalibur family combine an unparalleled degree of integration and programmability. They offer an outstanding embedded system development platform, providing a cost-efficient access to leading-edge embedded processors and PLD performance.

The Excalibur family offers a variety of PLD densities and memory sizes to fit a wide range of applications and requirements. The high-performance embedded architecture is ideal for compute-intensive as well as high data-bandwidth applications.

Figure 1 shows the structure of the Excalibur devices. The embedded stripe contains the processor core, peripherals, and memory subsystem. The amounts of single- and dual-port memory vary as listed in Table 1 on page 3.

Figure 2 on page 5 shows the system architecture of the embedded stripe and the interfaces to the PLD portion of the devices. This architecture promotes maximum integration with minimal system cost and allows the embedded stripe and PLD to be independently optimized for maximum performance.

***Figure 1. Excalibur Architecture***

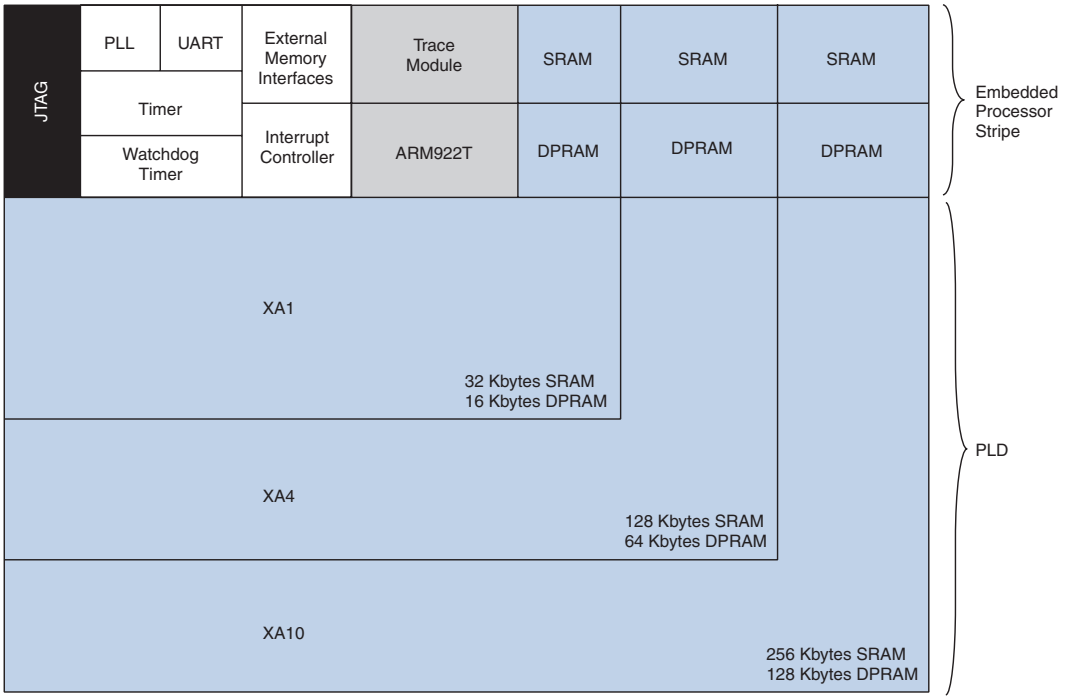
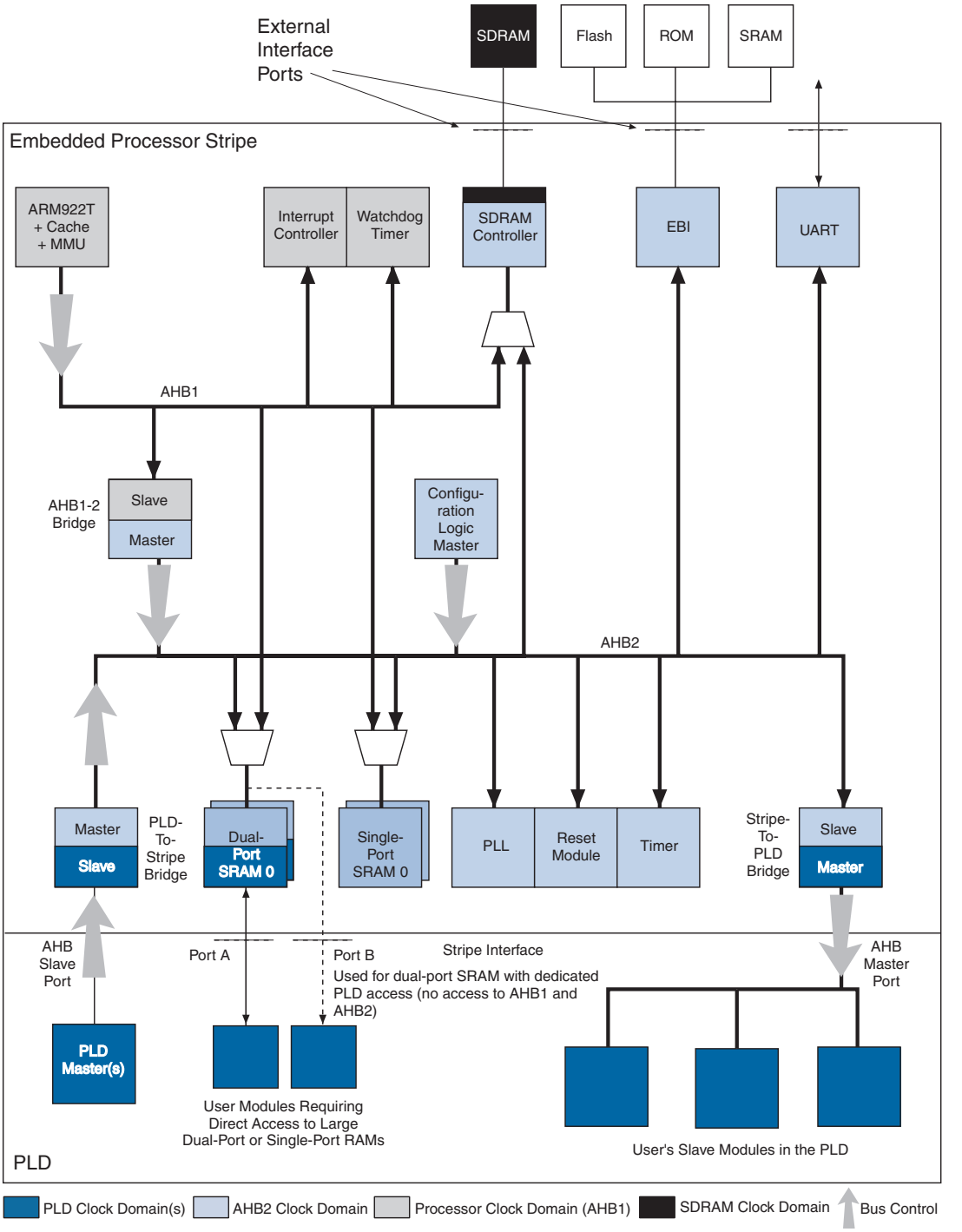


*Figure 2. Excalibur System Architecture*



Two AMBA-compliant AHBs ensure that the embedded processor activity is unaffected by peripheral and memory operation. Three bidirectional AHB-to-AHB bridges enable embedded peripherals and PLD-implemented peripherals to exchange data with the embedded processor or with other peripherals.

The Excalibur family is supported by the following development tools:

- SOPC Builder from Altera®
- Quartus II from Altera
- ADS, GNUPro and other third-party tools

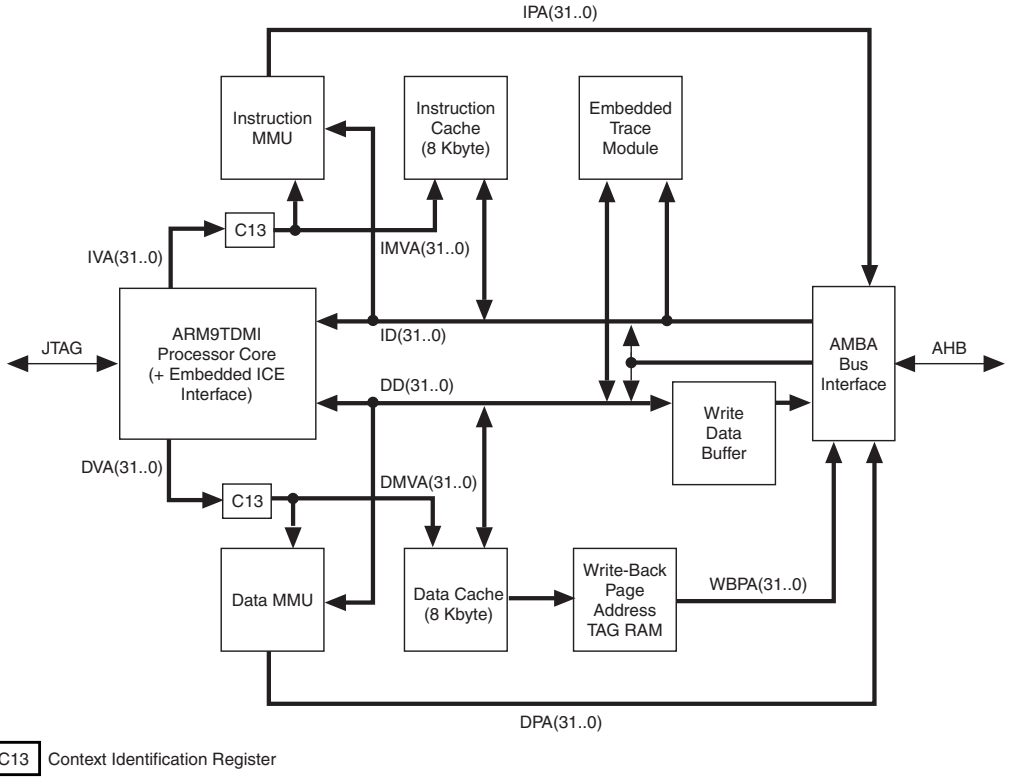
# Functional Description

The Excalibur system architecture (embedded processor bus structure, on-chip memory, and peripherals) combines the performance advantages of ASIC integration with the flexibility and time-to-market advantages of PLDs.

## The Embedded Processor

The ARM922T is a member of the ARM9 family of processor cores. Its Harvard architecture, implemented using a five-stage pipeline, allows single clock-cycle instruction operation through simultaneous fetch, decode, execute, memory, and write stages. Figure 3 on page 7 shows the Excalibur embedded processor, the ARM922T.

*Figure 3. ARM922T Embedded Processor Internal Organization*




Independent of PLD configuration, the embedded processor can undertake the following activities:

- Boot from external memory
- Execute embedded software
- Communicate with the external world
- Run a real-time operating system
- Run interactive embedded software debugging sessions
- Configure/reconfigure the PLD
- Detect errors and restart/reboot/reconfigure the entire system as necessary

The PLD can be configured to implement various extensions:

- Additional soft-core peripherals such as a UART, Ethernet MAC, CAN controllers, PCI, or any other IP core
- Peripherals that are bus masters, sharing the embedded stripe on-chip and off-chip memories as well as other PLD peripheral
- Peripherals that are slaves, controlled by the embedded processor

- Peripherals that exchange data using the on-chip dual-port RAM
- High speed data paths under embedded processor control
- Multi-processor systems, using multiple Nios embedded processor solutions
- Additional embedded processor interrupt sources and controls

PLD designers can take full advantage of the extensive range of Altera intellectual property (IP) Megacore® functions to implement complex system-on-a-programmable-chip (SOPC) designs in minimal time but with maximum customization.

The bidirectional bridges and dual-port memory interfaces between the embedded stripe and the PLD are synchronous to the clock domain that drives them; however, the embedded processor domain and the PLD domains are asynchronous. The clock domain for each side of the interfaces can be optimized for performance. The bidirectional bridges handle the resynchronization across the domains and are capable of supporting 32-bit data accesses to the entire 4-Gbyte address range (32-bit address bus).

The SDRAM memory controller PLL allows users to tune the frequency of the system clock to the speed of the external memory implemented in their systems.

## Internal Memory

The embedded stripe contains both single-port and dual-port SRAM. There are two blocks of single-port SRAM; both are accessible to the AHB masters via an arbitrated interface within memory. Each block is independently arbitrated, allowing one block to be accessed by one bus master while the other block is accessed by the other bus master.

Up to 256 Kbytes of single-port SRAM are available, as two blocks of 2 × 128 Kbytes. Each single-port SRAM block is byte-addressable. The size of the SRAM blocks depends on the device, as shown in Table 1. Byte, half-word and word accesses are allowed and are enabled by the slave interface. The behavior of byte and half-word reads is controlled by the system endianness.

In addition, there are either one or two blocks of dual-port SRAM in the embedded stripe, depending on the device type. The outputs of the dual-port memories can be registered. One of the ports gives dedicated access to the PLD; the other port can be configured for access by AHB masters or by the PLD. The width of the data port to the PLD is configurable as ×8, ×16, or ×32 bits. For the larger devices, the dual-port SRAM blocks can be combined to form a ×64-bit data-width interface. This allows the designer to build deeper and wider memories and multiplex the data outputs within the stripe.

## External Memory Controllers

The Excalibur family provides two embedded memory controllers that can be accessed by any of the bus masters: one for external SDRAM, and a second for external flash memory or SRAM.

The SDRAM memory controller supports the following commonly-available memory standards, without the addition of any logic:

- Single-data rate (SDR) 133-MHz data rates
- Double-data rate (DDR) 266-MHz data rates

An embedded stripe PLL supplies the appropriate timing to the SDRAM memory controller subsystem. Users can program the frequency to match the chosen memory components.

The EBI supports the interface to system ROM, allowing external flash memory access and reprogramming. In addition, static RAM and simple peripherals can be connected to this interface externally.

## Embedded Peripherals

A single 16-Kbyte memory region in the embedded stripe contains configuration and control registers, plus status and control registers for the embedded peripherals. The region contains the following modules:

- Configuration Registers
- Embedded Stripe PLLs
- UART
- Timer
- Watchdog timer
- General Purpose I/O Port
- Interrupt controller

# Software Development Tools

In a co-development environment where both the hardware and software components constitute an integral part of the embedded processor PLD design process, Altera provides seamless support with SOPC Builder and Quartus II; ADS, GNUPro and third-party development tools are also available.

See the Altera web site, http://www.altera.com, for details of the software development tools.

Excalibur devices are compatible with any available tools for the ARM922T from ARM or third parties.

## SOPC Builder

SOPC Builder allows embedded system designers to create system-on-a-programmable-chip (SOPC) designs in a fraction of the time traditionally required for embedded system-on-chip (SOC) design. It provides an intuitive GUI that simplifies the definition and customization of a user's system. Designers select and parameterize IP blocks from a drop-down list of communication, digital signal processing (DSP), microprocessor, and bus interface cores. Then SOPC Builder automatically generates all of the logic necessary to integrate them and also uses the specified system information to create appropriate VHDL or Verilog HDL code to connect the system components together, resulting in an HDL description of the entire system.

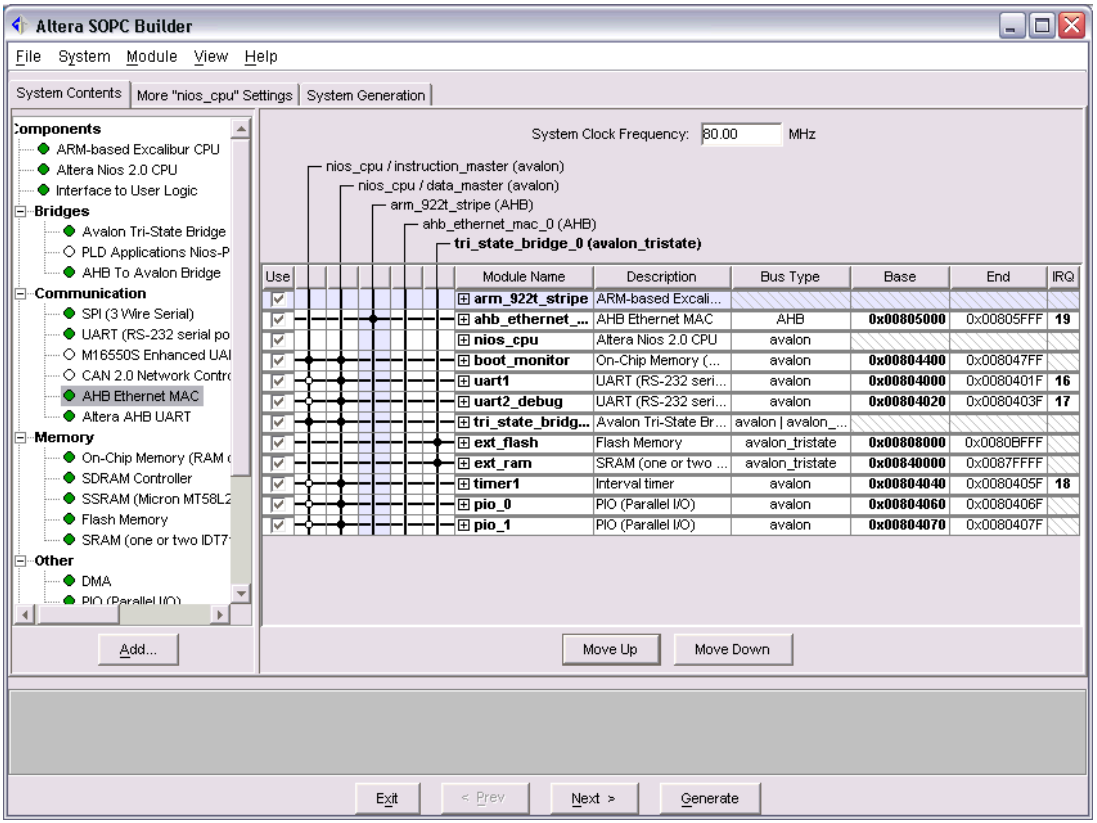
SOPC Builder automatically generates a software development environment that matches the target hardware, saving days or weeks of software design time, and jump-starts software development with components such as the following:

- Header files that define memory maps, interrupt priorities and data structures corresponding to each hardware peripheral
- Routines to access hardware peripherals in the system
- OS/RTOS kernels with appropriate hardware drivers

SOPC Builder automatically generates a simulation model of the system, a test bench for the system, and a full environment for immediate system simulation.

Figure 4 on page 11 shows an example of an SOPC Builder screen.

*Figure 4. Sample SOPC Builder Screen*

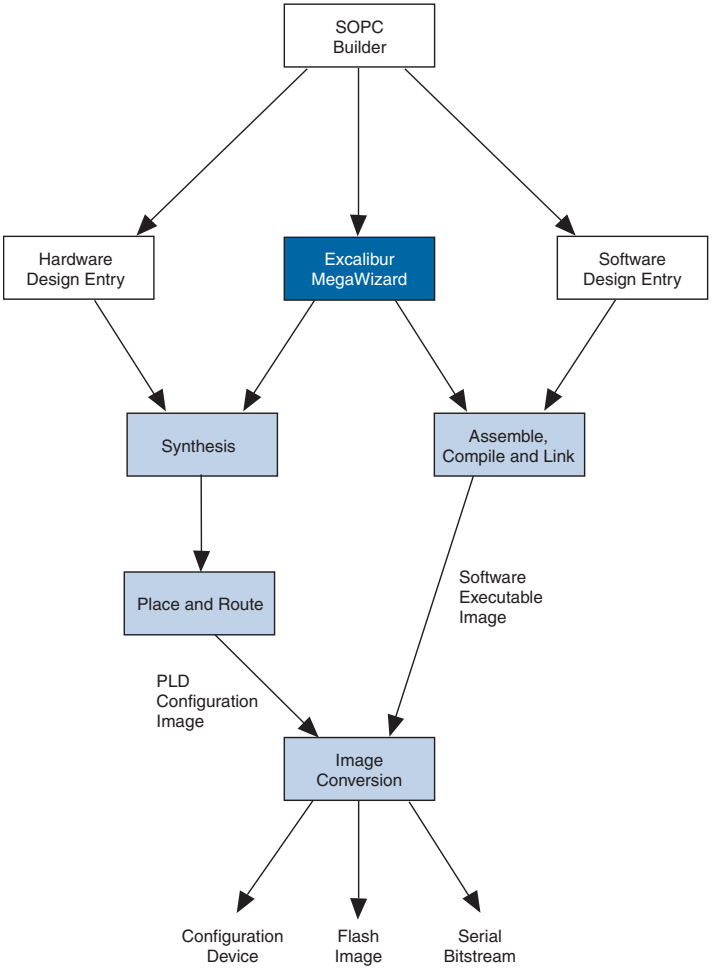



## Quartus II

The Quartus II development system can be used for both PLD logic design and the integration of embedded software. The Quartus II software provides an integrated package for complete hardware logic design, including HDL and schematic design entry, compilation and logic synthesis, full simulation and timing analysis, and programming file generation, as well as hardware logic debug using SignalTap logic analyzer.

With the Quartus II SoftMode™ co-design capability, embedded software development, debugger support, and unified programming file generation can be easily combined from a single integrated design environment (IDE). The Quartus II tools are pre-configured to support embedded software development tools such as the ARM Developer Suite or Red Hat GNUPro Tools for ARM922T processors. The Quartus II software operates on Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations. The Quartus II software provides NativeLink® integration to third-party, industry-standard PC and UNIX workstation-based electronic design automation (EDA) tools. Figure 5 shows the Quartus II development tool flow.

***Figure 5. Quartus II Development Tool Flow***



Altera supplies a variety of embedded software functions to support flash memory programming and PLD configuration.

## Configuration

Excalibur devices are configured at system power-up with data stored in a configuration device or flash memory. The same memory can store application software for the embedded processor. The user can reconfigure the device in-circuit by using the on-chip processor, using configuration data stored anywhere in its memory system. The user can make real-time changes during system operation, which enables innovative reconfigurable computing applications.

### Simulation Model

Initial simulation models of the ARM922T are compatible with the following simulators:

- Quartus II simulator
- Cadence NC-Verilog and NC-VHDL simulators
- ModelSim simulator
- Synopsys VCS simulator

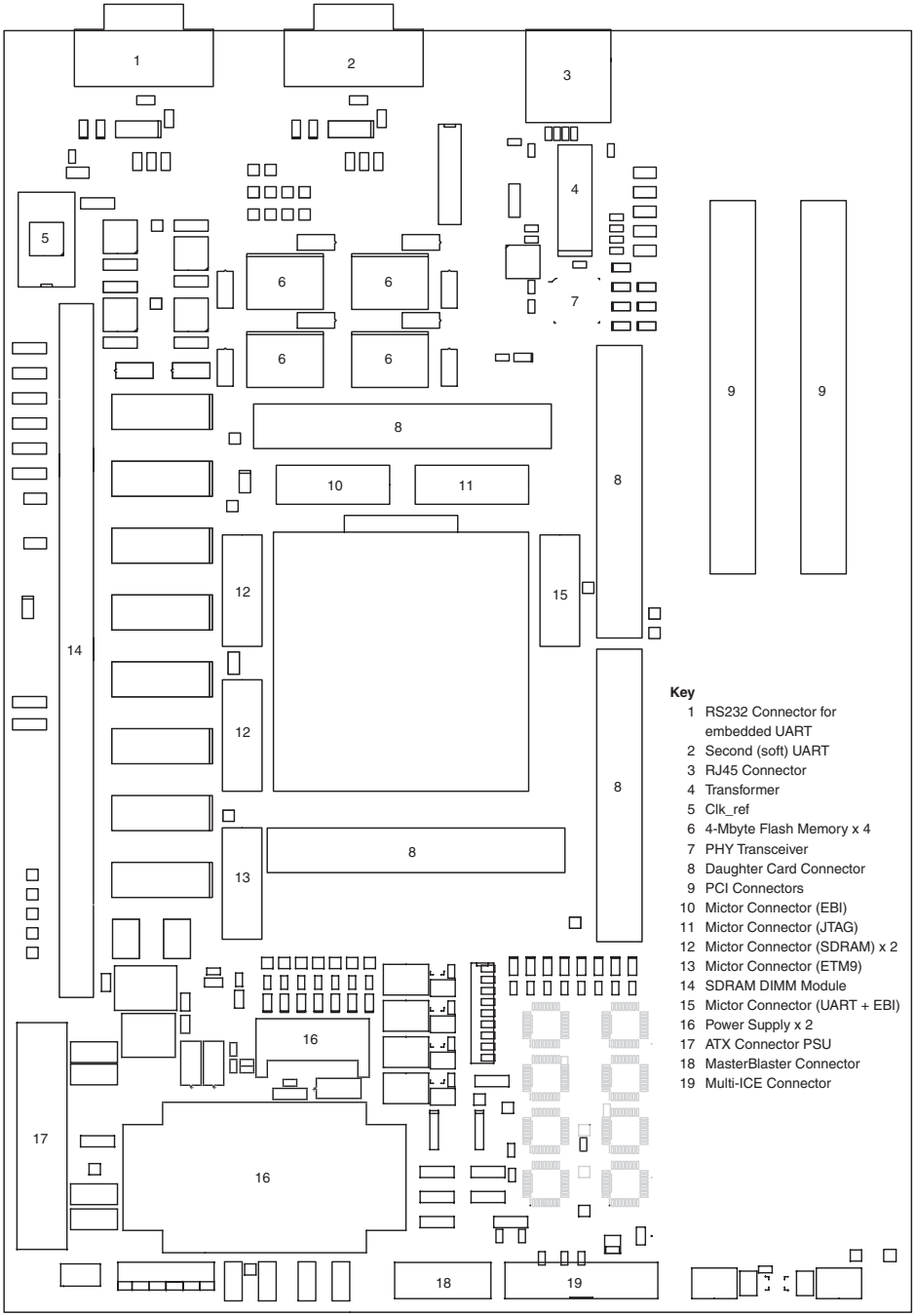
### Trace

A trace port provided on the ETM9 is compatible with the external trace analysis tools. This feature allows real-time visibility of embedded processor execution, and is tightly integrated with the source-level debugging tools.

### Excalibur Development Kit

Altera offers separately an Excalibur development kit, which includes a development board compatible with the EPXA10 device. Figure 6 on page 14 illustrates the Altera Excalibur development board, showing the provision for board expansion.

*Figure 6. Excalibur Development Board*

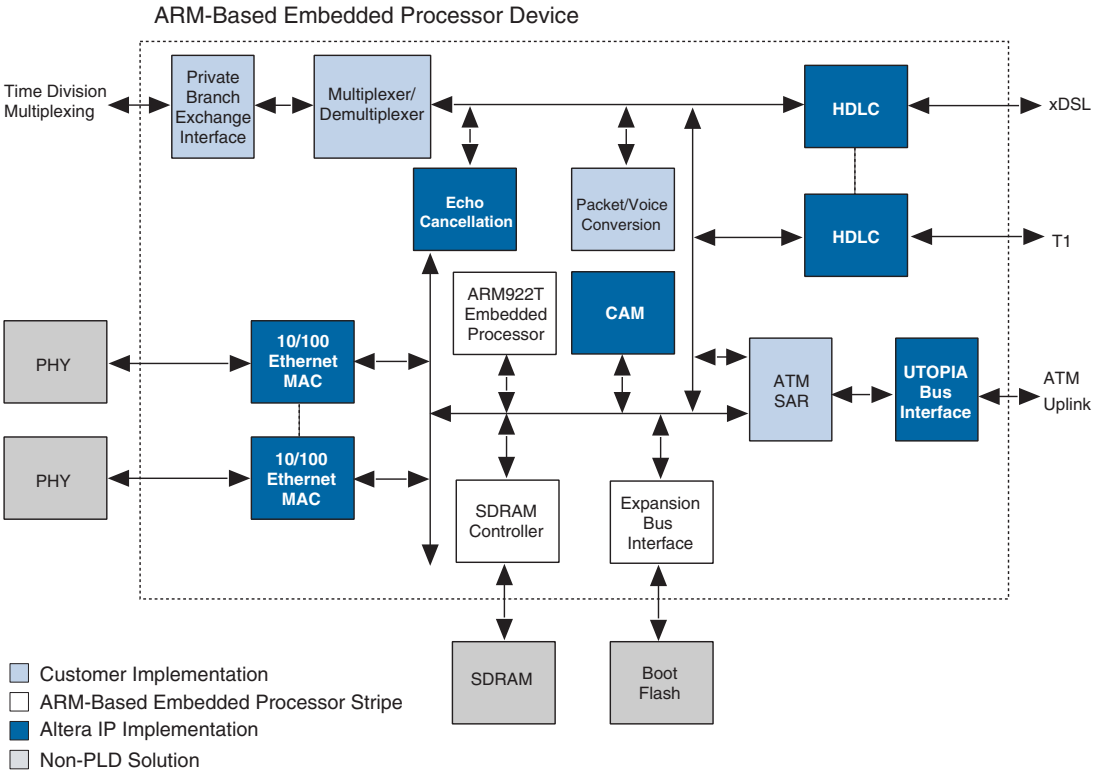


The EPXA10 development kit provides a powerful platform for designing embedded processor PLD solutions. The kit features the EPXA10 device, a member of the Excalibur family with an ARM922T-based processor subsystem tightly coupled to the PLD fabric. The EPXA10 development kit delivers flexible debug and trace facilities to support the system under development, connection cables and a full complement of software solutions including SOPC Builder to generate the system, utilities and resource material, third-party demo and evaluation software and documentation. The development kit is the ideal development platform for complete SOPC designs based on Excalibur devices for both ASIC prototyping and low-to-moderate volume production runs.

## Typical Application

Figure 7 on page 15 shows how the Excalibur device and other elements can be integrated in an application. In this example, the Excalibur device is configured for a voice-over packet gateway application. The elements of the embedded processor stripe, PLD modules, and off-chip peripherals are clearly identified.

***Figure 7. Excalibur Device in a Voice-Over Packet Gateway Application***



# Revision History

This document provides updated information as described below.

## Version 2.0

This version provides updated information, including:

- Device features and package sizes
- Functional description
- Software development tools
- Excalibur development boards

## Version 1.2

This version provides updated information, including:

- Operating speed and other device features
- Updated system architecture (Figure 2)
- Minor textual changes

## Version 1.1

This version provides updated information, including:

- Revised maximum amount of external SDRAM supported
- Minor formatting and textual changes

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