Fully integrated standalone light barrier driver & receiver

General Description

The epc111/112 is a general purpose, fully integrated self-contained CMOS circuit family to be used in light-barrier applications.

The chip contains a controller which drives an LED, typically an IR-LED. The LED is used in a pulsed mode to increase the signal-to-noise ratio even when there is very strong sunlight biasing the photo diode.

It contains also a high sensitive photo diode amplifier and a signal conditioning circuitry to cancel unwanted environmental light including strong sunlight and pulsed light sources. The receiver is built around a synchronous demodulator circuitry. Two output signals with different threshold levels are implemented in order to trigger the light barrier output or to indicate light reserve.

The chip also includes a power supply circuitry to establish all internally required voltages from one source only.

It can be used as a standalone device forming the whole core of an industrial light barrier.

Features

- Fully integrated light barrier chip
- Needs just a photo diode and a LED with a LED driver
- Various types are available, i.e. high sensitivity or high speed
- Integrated clock generator
- CSP10 package with very small footprint
  or standard QFN16 package available

Applications

- Light barriers ranging from millimeters to tens of meters
- Smoke detectors
- Liquid detectors

Functional Block Diagram

for 10-Pin Chip Scale Package (for 16-pin QFN Package)

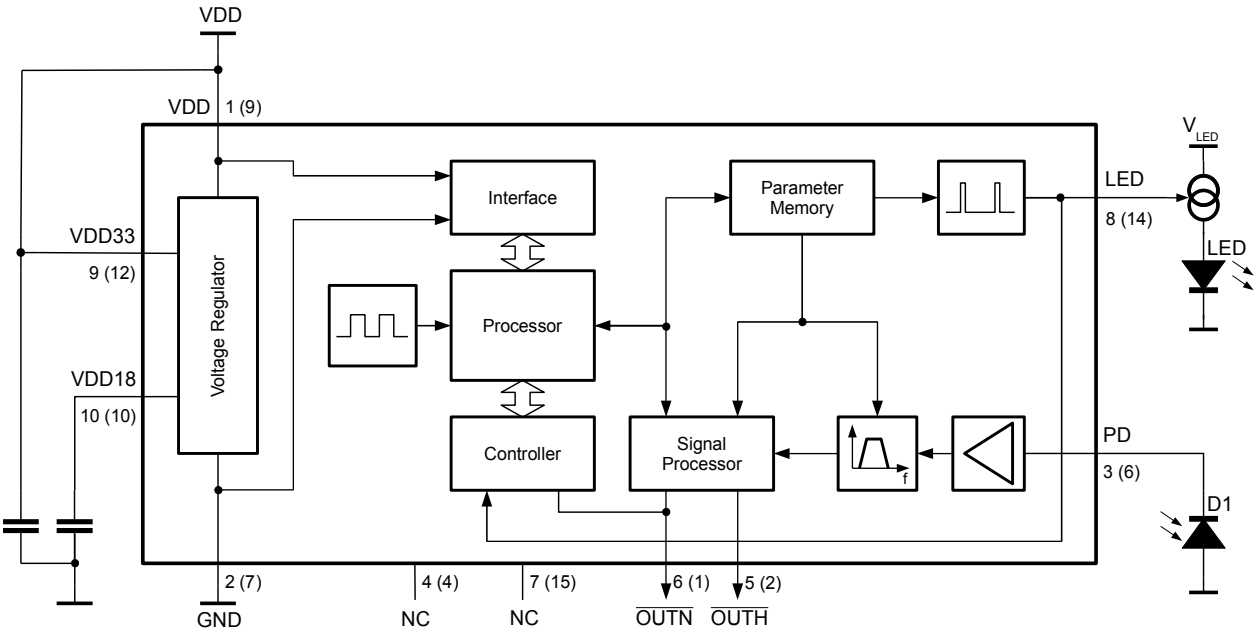


Figure 1: Block Diagram

Type	Response Time	Sensitivity	Typical Application
epc111	Medium	Medium (High)	Long range light barrier
epc112	Fast	Medium	High speed detection rate

Table 1: Characteristics of available types

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Absolute Maximum Ratings (Notes 1, 2)

Power Supply Voltage at pin VDD	-0.3V to +5.5V
Voltage to any pin except VDD	-0.3V to VDD +0.3 V
Output current at any pin except LED	-6mA to +6mA
Power Consumption with maximum load	125 mW
Lead Temperature solder, 4 sec. (T_L)	+260°C

Recommended Operating Conditions

	Min.	Max.	Units
Supply voltage at VDD (=VDD33)	3.0	3.6	V
Supply voltage at VDD33 (=VDD)	3.0	3.6	V
Operating Temperature (T_O)	-40°	+85°	C
Relative Humidity (non-condensing)	+5	+95	%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended operating conditions indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specific - ations and test conditions, see Electrical Characteristics.

Note 2: This device is a highly sensitive CMOS ac current amplifier with an ESD rating of JEDEC HBM class 0 (<250V). Handling and assembly of this device should only be done at ESD protected workstations.

Electrical Characteristics

3.0V < V_{DD} < 3.6V, -40°C < T_A < +85°C, unless otherwise specified

General Data

Symbol	Parameter	Conditions/Comments		Values			Units
				Min.	Typ.	Max.	
V_N	Power supply voltage	at VDD and VDD33		3.0	3.3	3.6	
V_{PUP}	Power-up Threshold Voltage	Voltage at VDD33 when the device starts up		2.4		3	V
V_{PP}	Ripple on supply voltage, peak to peak	Type	Input pulse $I_{PD\ NST}$				
		epc111	60nA			250	mV
		epc112	108nA			600	mV
I_{DD_OP}	Current consumption	in operation mode I_{PD} = 0 mA, no load				2	mA
V_{NOH}	Output high voltage $\overline{OUTN}$			V_N- 0.5V			V
V_{NOL}	Output low voltage $\overline{OUTN}$	@ 4mA source				0.5	V
V_{HOH}	Output high voltage $\overline{OUTH}$	see Figure 6					
V_{HOL}	Output low voltage $\overline{OUTH}$	@ 3mA source. See Figure 6.				0.5	V
V_{LEDH}	Output high voltage			V_N- 0.5V			V
V_{LEDL}	Output low voltage					0.5	V
I_{LED}	Source current maximum	@ Pin LED		0.7			mA
f_{clk}	Reference clock	of internal oscillator - for information only			1		MHz
df_{clk}	Temperature drift	of the oscillator - for information only			640		ppm/K

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Other Data

Symbol	Parameter	Conditions/Comments	Types	Values			Units
				Min.	Typ.	Max.	
I_{PDN}	Photo Current Sensitivity $\overline{OUTN}$	Pulse height to trigger internal threshold $\overline{OUTN}$. Refer to Functional Description	epc111		60		nA
			epc112		108		
I_{PDH}	Photo Current Sensitivity $\overline{OUTH}$	Pulse height to trigger internal threshold $\overline{OUTH}$. Refer to Functional Description	epc111		96		nA
			epc112		144		
I_{pulse}	Maximum Input Pulse Current	If the input current pulse is above this level, the recovery time t_{REC} becomes t_{relax}. (refer to parameter t_{relax})	epc111			100	µA
			epc112			100	
I_{N_Imin}	Input related noise	@ I_{PDDC} =0				15	nA $_{RMS}$
I_{N_Imax}	Input related noise	@ I_{PDDC} =$I_{PDDCMax}$				20	nA $_{RMS}$
I_{PDDC}	DC Photo Diode Current	generated by ambient light with no effect to the sensitivity		0.0		2	mA
C_{PD}	Photodiode Capacitance	Refer to section Application Information, Photodiode Capacitance				50	pF
t_{Pulse}	LED Pulse Length		epc111		2		µs
			epc112		1		
t_{Cycle}	LED Cycle Time		epc111		100		µs
			epc112		10		
t_{relax}	Recovery time	after a strong current pulse (I_{pulse} = 100µA)	epc111			50	µs
			epc112			50	
t_R	Response Time	Minimum time from light beam detection to status change of the output $\overline{OUTN}$ or $\overline{OUTH}$. $t_{R_MAX} = (n_V + 1) * t_{Cycle}$	epc111		800	900	µs
			epc112		30	40	
t_F	Release Time (fall time)	Minimum time from beam interruption to status change of the output $\overline{OUTN}$ or $\overline{OUTH}$. $t_{F_MAX} = (n_M + 1) * t_{Cycle}$	epc111		800	900	µs
			epc112		20	30	
n_V	Valid pulse counts	Number of valid (non-missing) pulses to trigger the output. Refer to Functional Description	epc111		8		
			epc112		3		
n_M	Missing pulse counts	Number of missing pulses to release the output. Refer to Functional Description	epc111		8		
			epc112		2		

Other Parameters

(typical values, T_{amb} = 25°C, V_{DD} = 3.3V)

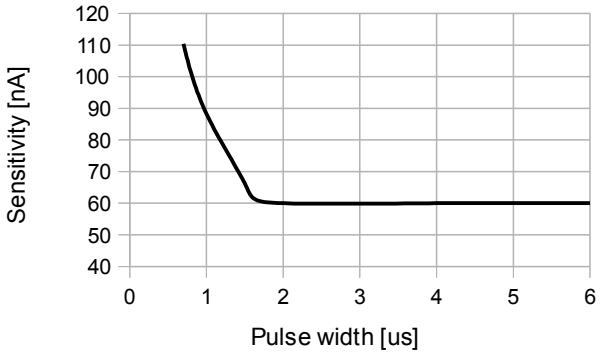
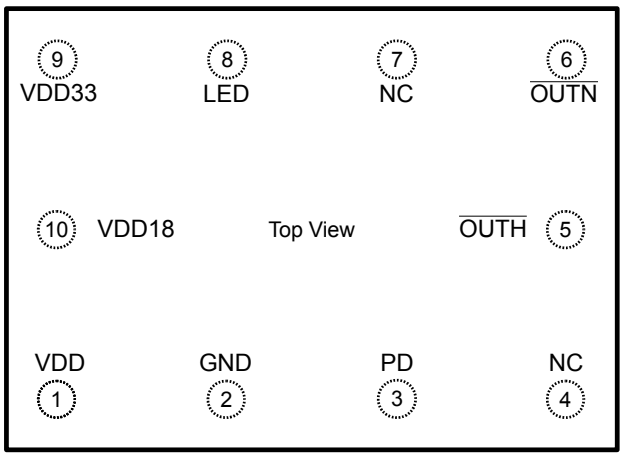


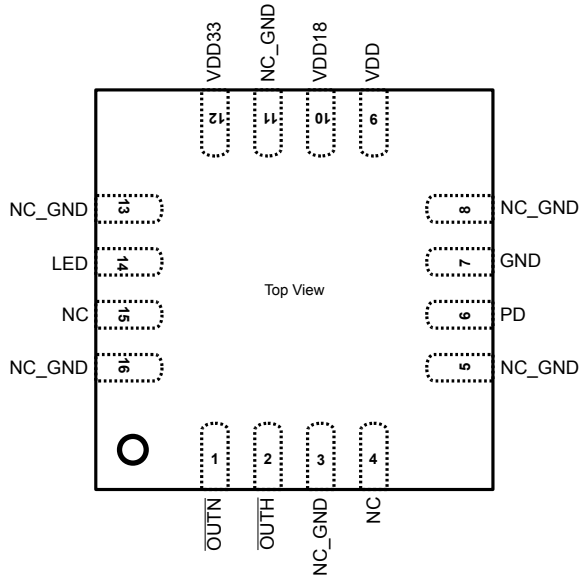
Figure 2: Input Sensitivity vs. LED pulse width

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Connection Diagrams



10-Pin Chip Scale Package (CSP)



16-Pin QFN Package

10-Pin CSP	16-Pin QFN	Pin Name	Type	Description
1	9	VDD	Power Supply	Positive power supply. To be connect to VDD33.
2	7	GND	Power Supply	Negative power supply pin.
3	6	PD	Analog Input	Photo diode input.
4	4	NC		Do not connect this pin. Internally terminated.
5	2	$\overline{\text{OUTH}}$	Digital Out Load depending	Light reserve detected - see Figure 6. Threshold level around 50% above the threshold of the filtered signal level. Open drain output
6	1	$\overline{\text{OUTN}}$	Digital Output	Light pulses detected by the photo diode - see Functional Description Amplified and filtered signal Open drain output
7	15	NC		Do not connect this pin. Internally terminated.
8	14	LED	Digital Out	Output to LED driver
9	12	VDD33	Power Supply	Positive power supply. To be connected to VDD.
10	10	VDD18	Decoupling	Pin for external filter/decoupling of the internal 1.8V supply: 4.7nF ceramic type Not for supply of external circuits
n/a	3, 5, 8, 11, 13, 16	NC_GND		Not connected. Connect this pins to GND (Guarding).

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Functional Description

Evaluation of single light pulse

For each single light pulse, received and detected by the LED, the threshold levels are processed according to the following principle to propagate the output signals OUTN and OUTH resp. $OUTN_{INT}$ and $OUTH_{INT}$. As far the received light pulse signal exceeds the corresponding threshold level, the pulse will be recognized as a valid pulse and the detection circuit sets the appropriate output signal OUTN $_{INT}$ or $OUTH_{INT}$.

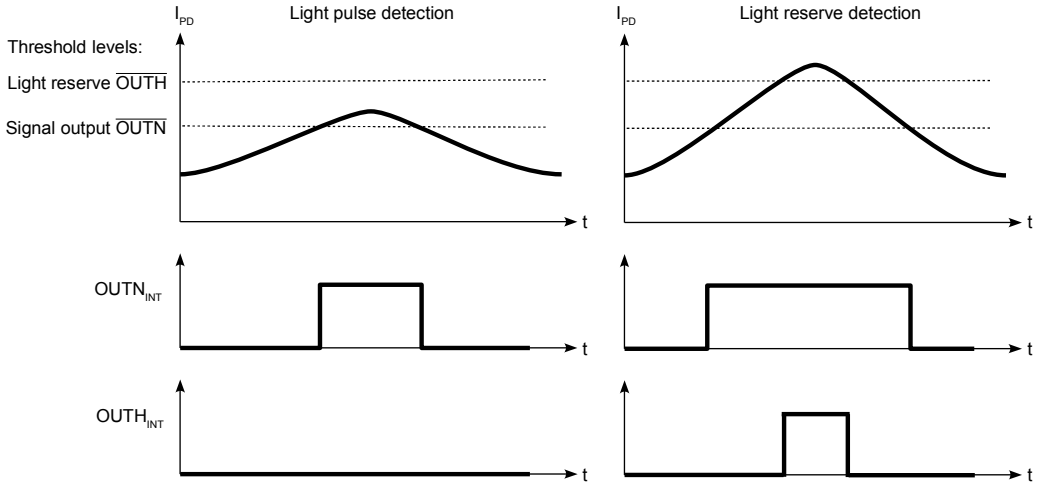


Figure 3: Pulse evaluation

Pulse Modulated Operation (e.g. $OUTN_{int}$ to $\overline{OUTN}$)

The epc111/112 chip operates the LED and the receiver path on a pulse modulated concept. Thus, the LED is operated with short pulses whereas the receiver channel does synchronous demodulation of the received light pulses by reading the current pulses of the photodiode. This concept allows a very high sensitivity, high speed operation, and a high suppression of input ambient or foreign light (DC currents) generated by sunlight or other DC light sources like light bulbs.

In order to eliminate interference caused by modulated light, e.g. a flashing light or by other light barriers, the input signal from the photodiode is amplified, filtered, and processed by an integrated signal processor. If the photodiode signal meets the required frequency, pattern and amplitude, the output(s) are triggered. The following timing diagram shows the basic concept.

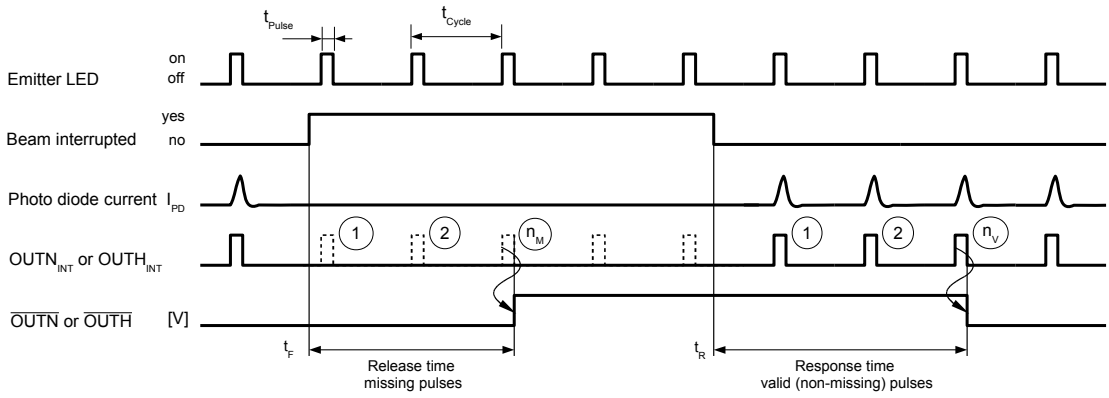


Figure 4: Pulse modulation concept

It is in fact a digital filter which counts missing and non-missing pulses to change the ou tput state of $\overline{OUTN}$ or $\overline{OUTH}$.

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Working principle of the digital filter e.g. for the signal $OUTN_{int}$ to OUTN Filter:

The aim of this programmable filter is to suppress single pulses, so they cannot trigger the output and generate a false signal.

This filter is based on a counter, which is counting up (increment) the valid pulses and counting down (decrement) the missing pulses in a weighted manner. There are separate weighting factors for valid pulses (parameter n_V) and missing pulses (parameter n_M). If the counter reaches the upper limit (maximum count, response time), the signal $\overline{OUTN}$ is set to LOW. Similar in the opposite direction, if the counter reaches zero, the lower limit (minimum count, release time), the signal $\overline{OUTN}$ is put to HIGH. With the parameters n_V and n_M the filter has the advantage of individual selectable gradients of the slopes. Counter will never exceed maximum nor minimum limit. In between it acts as an integrator of both parameters.

IF Pulse then

- IF Pulse = valid then
  Counter = Counter + (n_V * 1024)
  IF counter > 2^{15} (maximum limit) then Counter = maximum limit
  IF counter = maximum limit then $\overline{OUTN}$ = 0
- IF Pulse = missing then
  Counter = Counter – (2^{n_M})
  IF counter < 0 (minimum limit) then Counter = minimum limit
  IF counter = minimum limit then $\overline{OUTN}$ = 1

ELSE wait for Pulse

Lets assume that the photodiode does not receive light pulses for a long time: This means the light beam is interrupted. Then $\overline{OUTN}$ is at high level. If the light beam is not interrupted anymore, the photodiode receives light pulses which are strong enough to trigger the $OUTN_{INT}$ threshold and the internal pulse evaluation unit (designated in Figure 3 with 'Pulse evaluation') starts to count the received pulses. If the number of received pulses reach the set level n_V, the output $\overline{OUTN}$ turns to low level. Thus, single pulses cannot trigger the output and generate a false signal.

The same procedure is used when a beam changes from not interrupted to interrupted. The internal pulse evaluation unit counts the missing pulses. If the number of missing pulses reaches the level n_M, $\overline{OUTN}$ is turned to high level.

The same principle applies to the counter and signal of $\overline{OUTH}$.

The counter limit values are different, depending on the device:

Type	No. of Pulses n_M	No. of missing Pulses n_V
epc111	8	8
epc112	3	2

Table 2: Filter coefficients

Light Pulse Detection Output $\overline{OUTN}$

The epc111/112 contains two digital outputs to indicate that a valid signal of light pulses are received by the photodiode. The first output $\overline{OUTN}$ is triggered, when the lower threshold is reached by the input signal (see Figure 3). This output is used usually to drive the output of the light barrier. This is a fully CMOS compatible digital output.

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Light Reserve Output OUTH

However, if the incoming signal is just at the trigger threshold of OUTN, an unstable situation can occur. Thus, a second output OUTH is integrated with a higher trigger threshold to indicate that a certain 'light reserve' is reached (see Figure 3). This output is usually used to drive a visible LED to indicate to the operator a stable detection function of the light barrier. To have not too short pulses OUTH, this signal is stimulated by signal OUTH Filter and synchronously reset by OUTN.

The trigger threshold of OUTH is set approx. 50% above the trigger threshold of OUTN.

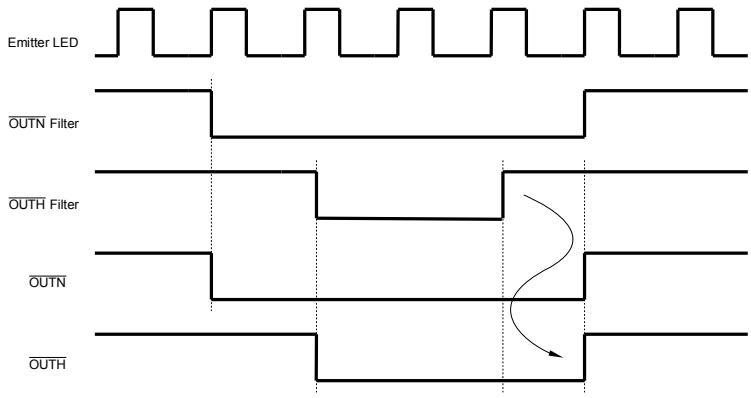


Figure 5: synchronization OUTH with OUTN

This output is not CMOS compatible. Its voltage is depending of the load according to Figure 6. To have still digital compatible signals a level conversion is necessary.

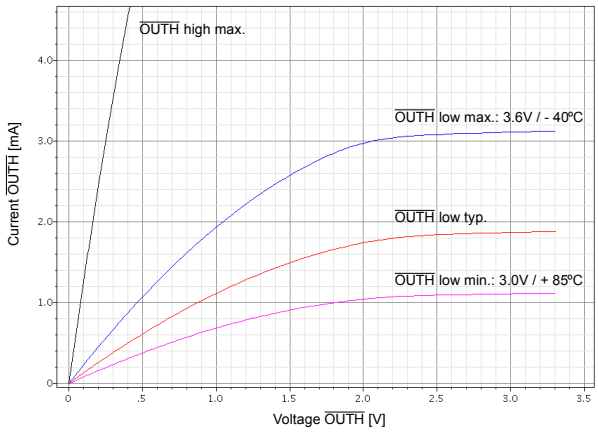


Figure 6: Output voltage versus output current of output OUTH

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Below you find some examples for such circuits for converting $\overline{\text{OUTH}}$ levels to full CMOS compatible digital output.

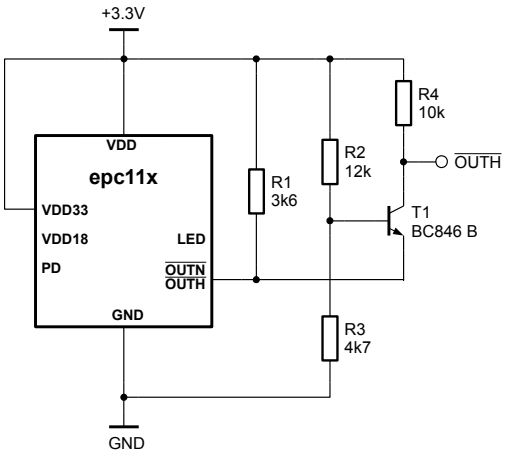


Figure 7: Non-inverting, low power level shifter (additional current ca.0.6mA)

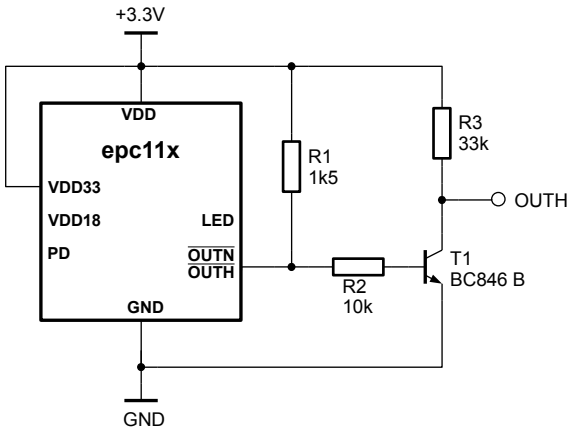


Figure 8: Simple inverting level shifter (additional current ca.1.6mA or 2.6mA)

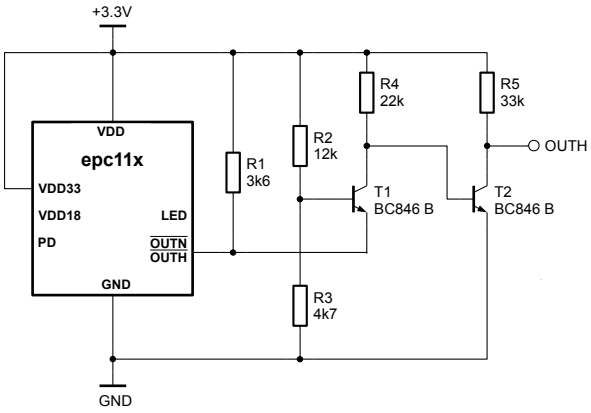


Figure 9: Inverting, low power level shifter (additional current ca.0.8 ... 1.0mA)

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Applications

Long range light barrier application

Figure 10 shows the epc111 as an example in a long range light barrier application with minimal part count. The LED flashes according to the description of the previous chapter. Light of the LED is passing either direct, reflected from a reflecting object or a retro reflector to the photo diode PD. If the received light fulfills the criteria according to the description in the previous chapter, the output signals $\overline{\text{OUTN}}$ and $\overline{\text{OUTH}}$ are set.

The epc111 device is designed to operate at 3.3V power supply (VDD and VDD33).

LED Driver:
The output LED of the epc111 to drive the LED driver circuit is a current source capable to drive typically 1mA. For a high performance long range light barrier (>8m), an LED peak current of up to 1.5A is needed. To generate such a high LED current, an external driver circuit is necessary. The circuitry in Figure 10 is a simple implementation of such a driver circuit. The darlington circuit with T2 and T3 and R2 and R3 does the job. In order to avoid interference on the supply voltage, the supply is isolated (filtered) with R1 and C1. The high peak LED pulse current is delivered by the capacitor C1, which itself is charged by R1. Make sure, that there is no coupling of the high LED current to the ground of the epc111 or to the cathode of the photo diode. This driver circuit operates with a VDD_{LED} in a range of 10 to 30 VDC.

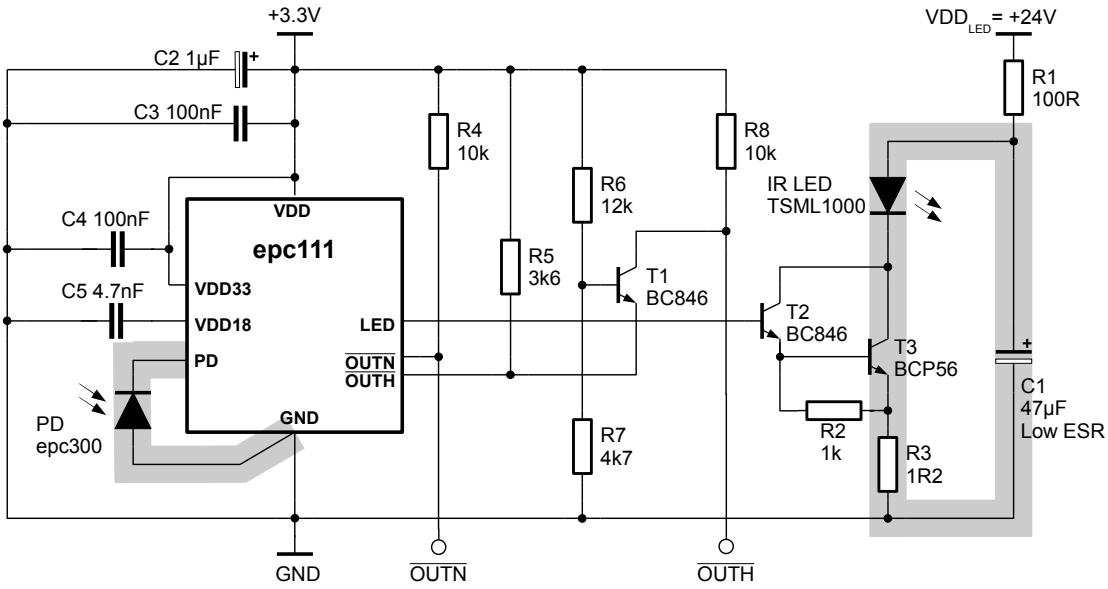


Figure 10: Long range light barrier application with minimal part count

Notice:
The schematic is for illustrating the basic circuit idea only. For the real built up the designer has to take all other additional influence factors in consideration too e.g. design rules, power rating, heat dissipation, ...

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High speed detection rate design

Figure 11 shows the epc 112 as an example in a high speed detection rate light barrier application with minimal part count. This design is optimized for a fast reading of light beam interruptions. Whereas the working principle is similar to the above example. This driver circuit operates with a VDD_{LED} in a range of 6 to 20 VDC.

The epc112 device is designed to operate at 3.3V power supply (VDD and VDD33).

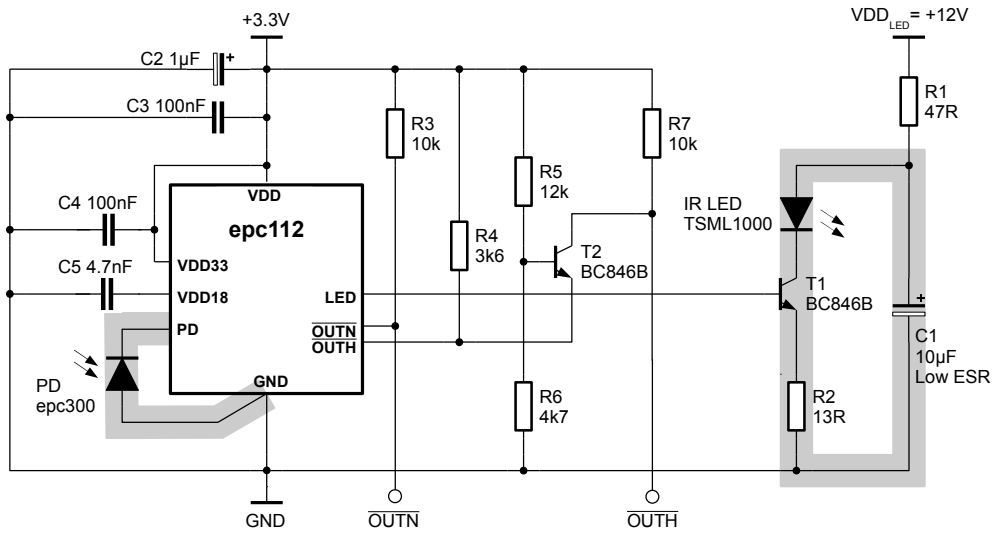


Figure 11: High speed detection rate light barrier application with minimal part count

Notice:
The schematic is for illustrating the basic circuit idea only. For the real built up the designer has to take all other additional influence factors in consideration too eg. design rules, power rating, heat dissipation, ...

Design Precautions: EMC shielding

The sensitivity at pin PD is very high in order to achieve a long operation range of light barriers even without lenses in front of the IR LED and/or the photo diode. Thus, the pin PD is very sensitive to EMI. Special care should be taken to keep the PCB track at pin PD as short as possible (a few mm only!). This track should be kept away from the IR LED signal tracks and from other sources which may induce unwanted signals. It is strongly recommended to cover the chip, the photodiode and all passive components around the chip with a metal shield. A recommended part is shown in Figure 12. The pins at the bottom are to solder the shield to the PCB with electrical connection to GND. The hole in the front is the opening window for the photo diode. The backside of the PCB below the sensitive area (PD, epc111 or epc112) shall be a polygon connected to GND to shield the circuit from the backside as well.

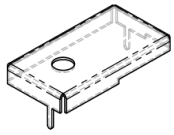


Figure 12: Recommended EMC shield

Ambient Light

Photodiode DC current can be generated by ambient light, e.g. sunlight. DC current at pin PD does not generate a DC output signal. However, if I_{PDDC} is above the stated maximal value, the input is saturated. This blocks the detection of AC current pulses.

Photodiode Capacitance

If the photo diode capacity is above the specified value, a lower detection sensitivity and a possible higher sensitivity spread results.

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Layout Information (all measures in mm,)

CSP-10 Package

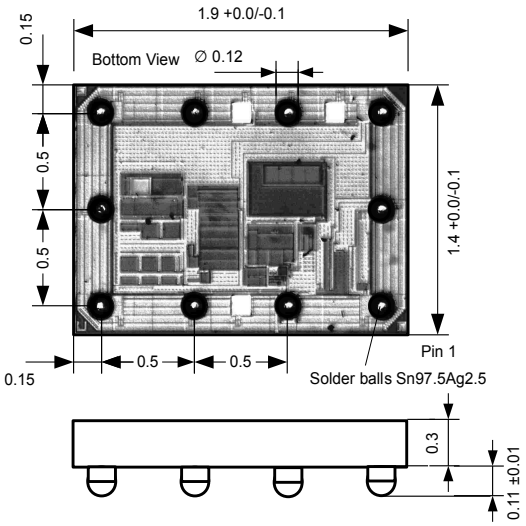


Figure 13: CSP10: Mechanical dimensions

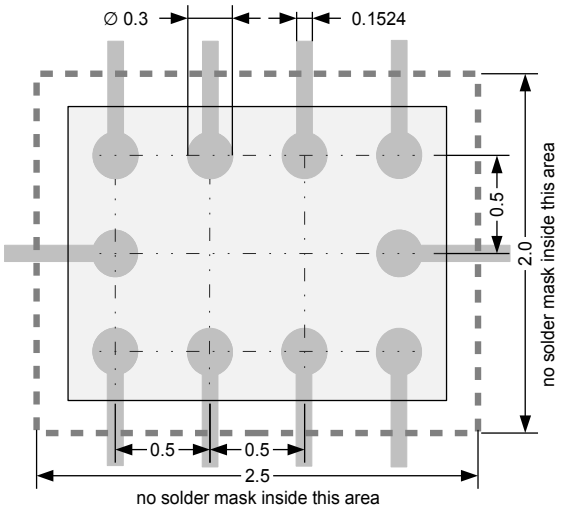


Figure 14: CSP10: Layout recommendation

Recommendations for reliable soldering of solder balls:

- Use a pad layout similar to the one shown in Figure 14. Notice that all tracks should go underneath the solder mask area.
- Do not connect any pins direct pin to pin inside of the opening of the solder mask.
- In case of the conductors are with a Au-Ni surface finish the preferred landing pad design for the solder balls will be covering the round landing pad with a gold surface finish as a solderable area only.

QFN-16 Package

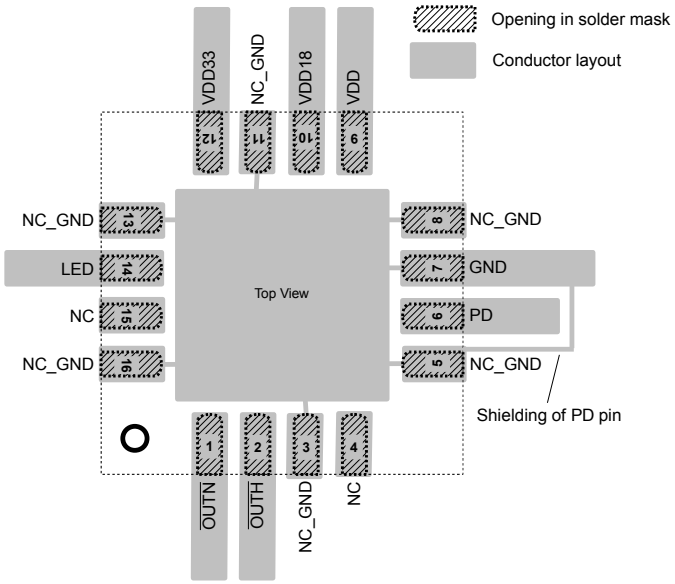


Figure 15: QFN-16: Layout recommendation

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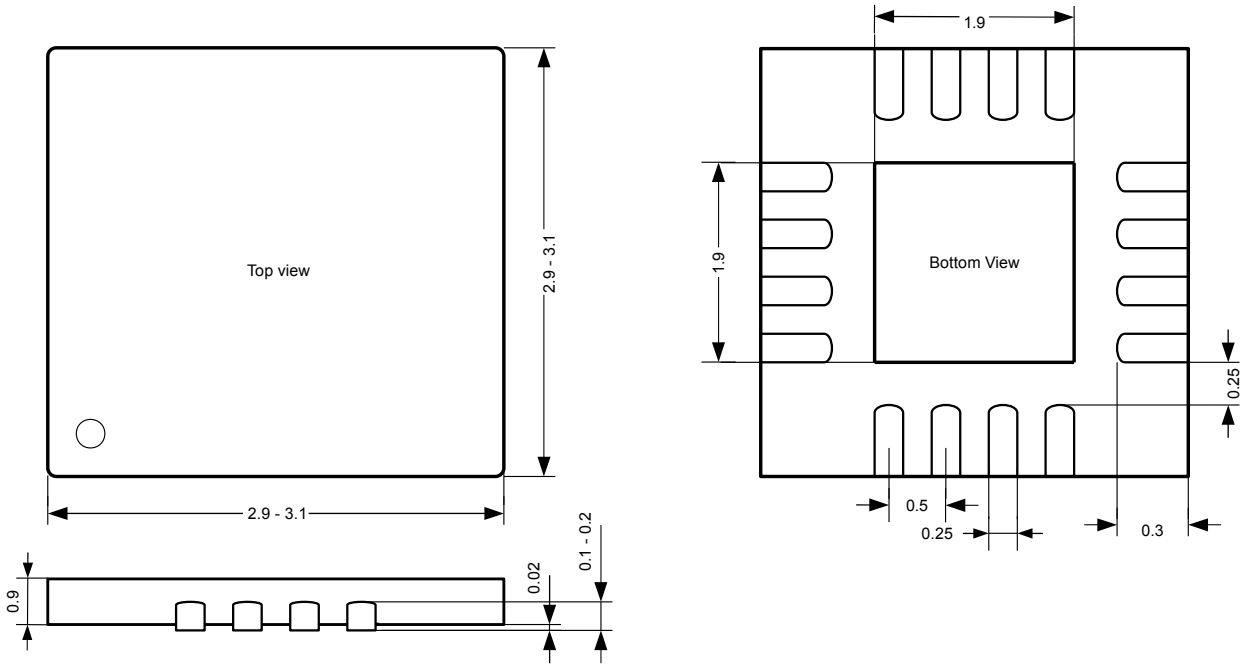


Figure 16: QFN-16: Mechanical dimensions

Reflow Solder Profile

For infrared or conventional soldering the solder profile has to follow the recommendations of IPC/JEDEC J-STD-020C (min. revision C) for Pb-free assembly for both types of packages. The peak soldering t emperature (T_L) should not exceed +260°C for a maximum of 4 sec.

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Packaging Information (all measures in mm)

Tape & Reel Information

The devices are mounted on embossed tape for automatic placement systems. The tape is wound on 178 mm (7 inch) or 330 mm (13 inch) reels and individually packaged for shipment. General tape-and-reel specification data are available in a separate data sheet and indicate the tape sizes for various package types. Further tape-and-reel specifications can be found in the Electronic Industries Association (EIA) standard 481-1, 481-2, 481-3.

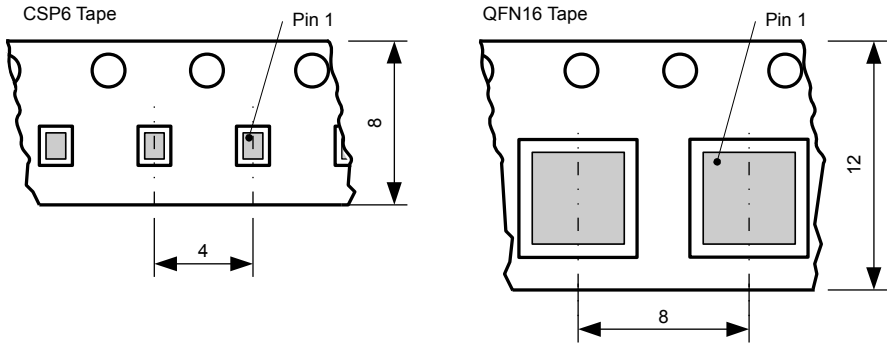


Figure 17: CSP10 and QFN16 Tape Dimension. Parts are placed with solder pads on bottom side

ESPROS Photonics AG does not guarantee that there are no empty cavities. Thus, the pick-and-place machine should check the presence of a chip during picking.

Ordering Information

Type	Response Time	Sensitivity	Package	RoHS compliance	Packaging Method
epc111-CSP10	Medium	High	CSP10	Yes	Reel
epc111-QFN16	Medium	High	QFN16	Yes	Reel
epc112-CSP10	Fast	Medium	CSP10	Yes	Reel
epc112-QFN16	Fast	Medium	QFN16	Yes	Reel

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