

8 Pin DIP Dual Fast Logic TTL Compatible Active Delay Lines EPA509-XX & EPA509-XX-LF

Add "-LF" after part number for Lead-Free

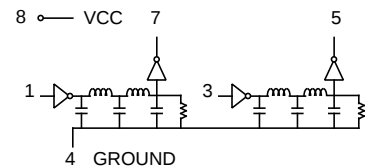
PCA Part Number	Delay Time *	PCA Part Number	Delay Time *	PCA Part Number	Delay Time *
EPA509-5(-LF)	5 ± 1	EPA509-18(-LF)	18	EPA509-55(-LF)	55
EPA509-6(-LF)	6 ± 1	EPA509-19(-LF)	19	EPA509-60(-LF)	60
EPA509-7(-LF)	7 ± 1	EPA509-20(-LF)	20	EPA509-65(-LF)	65
EPA509-8(-LF)	8 ± 1	EPA509-21(-LF)	21	EPA509-70(-LF)	70
EPA509-9(-LF)	9 ± 1	EPA509-22(-LF)	22	EPA509-75(-LF)	75
EPA509-10(-LF)	10 ± 1.5	EPA509-23(-LF)	23	EPA509-80(-LF)	80
EPA509-11(-LF)	11 ± 1.5	EPA509-24(-LF)	24	EPA509-85(-LF)	85
EPA509-12(-LF)	12 ± 1.5	EPA509-25(-LF)	25	EPA509-90(-LF)	90
EPA509-13(-LF)	13 ± 1.5	EPA509-30(-LF)	30	EPA509-95(-LF)	95
EPA509-14(-LF)	14 ± 1.5	EPA509-35(-LF)	35	EPA509-100(-LF)	100
EPA509-15(-LF)	15	EPA509-40(-LF)	40	EPA509-150(-LF)	150
EPA509-16(-LF)	16	EPA509-45(-LF)	45	EPA509-200(-LF)	200
EPA509-17(-LF)	17	EPA509-50(-LF)	50	EPA509-250(-LF)	250

Delay Times referenced from input to leading edges at 25°C, 5.0V, with no load.

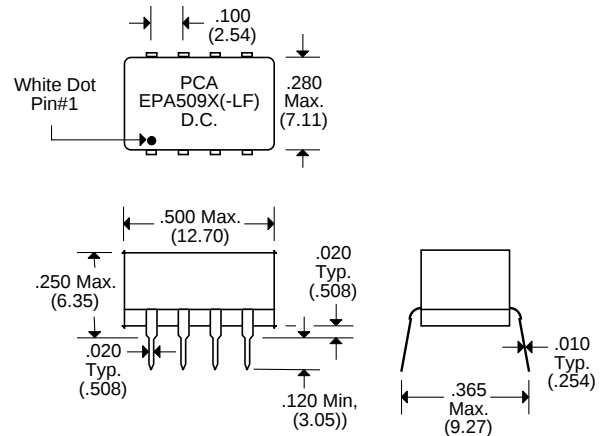
* Unless otherwise specified, delay tolerance is ± 2 nS or ± 5%, whichever is greater.

DC Electrical Characteristics		Test Conditions	Min.	Max.	Unit
V _{OH}	High-Level Output Voltage	V _{CC} = min. V _{IL} = max. I _{OH} = max	2.7		V
V _{OL}	Low-Level Output Voltage	V _{CC} = min. V _{IH} = min. I _{OL} = max		0.5	V
V _{IK}	Input Clamp Voltage	V _{CC} = min. I _I = I _{IK}		-1.2	V
I _{IH}	High-Level Input Current	V _{CC} = max. V _{IN} = 2.7V		50	µA
		V _{CC} = max. V _{IN} = 5.25V		1.0	mA
I _{IL}	Low-Level Input Current	V _{CC} = max. V _{IN} = 0.5V		-2	mA
I _{OS}	Short Circuit Output Current	V _{CC} = max. V _{OUT} = 0.	-40	-100	mA
		(One output at a time)			
I _{CCH}	High-Level Supply Current	V _{CC} = max. V _{IN} = OPEN		90	mA
I _{CCL}	Low-Level Supply Current	V _{CC} = max. V _{IN} = 0		90	mA
T _{RO}	Output Rise Time	T _d ≤ 500 nS (0.75 to 2.4 Volts)		4	nS
N _H	Fanout High-Level Output	V _{CC} = max. V _{OH} = 2.7V		20 TTL Load	
N _L	Fanout Low-Level Output	V _{CC} = max. V _{OL} = 0.5V		10 TTL Load	

Schematic



Package



Recommended Operating Conditions		Min.	Max.	Unit
V _{CC}	Supply Voltage	4.75	5.25	V
V _{IH}	High-Level Input Voltage	2.0		V
V _{IL}	Low-Level Input Voltage		0.8	V
I _{IK}	Input Clamp Current		-18	mA
I _{OH}	High-Level Output Current		-1.0	mA
I _{OL}	Low-Level Output Current		20	mA
PW*	Pulse Width of Total Delay	40		%
d*	Duty Cycle		40	%
T _A	Operating Free-Air Temperature	0	+70	°C

*These two values are inter-dependent.

Input Pulse Test Conditions @ 25° C		Unit	
E _{IN}	Pulse Input Voltage	3.2	Volts
PW	Pulse Width % of Total Delay	110	%
T _{RI}	Pulse Rise Time (0.75 - 2.4 Volts)	2.0	nS
P _{RR}	Pulse Repetition Rate	1.0	MHz
V _{CC}	Supply Voltage	5.0	Volts

Notes :	EPA509-XX	EPA509-XX-LF
1. Lead Finish	SnPb	Hot Tin Dip (Sn)
2. Peak Solder Rating (Wave Solder Process)	260°C 10 (+2/-0) seconds	260°C 10 (+2/-0) seconds
4. Weight	TBD grams	TBD grams
5. Packaging Information (Tube)	TBD pieces/tube	TBD pieces/tube

Unless Otherwise Specified Dimensions are in Inches /mm ± .010 / .25