EP2015C/EP2015AC
Fast Quad PNP Array

Features

- Four independent fast PNP's
- 350 MHz f_t
- Tight V_{BE} matching—1 mV
- Tight H_{fe} matching—5%
- One chip construction with dielectric isolation
- Excellent thermal tracking
- High H_{fe}—150 minimum
- 40V minimum BV_{ceo}
- Each transistor similar to 2N3906
- Pin compatible with TPQ3906 and MPQ3906

Applications

- Current sources
- Current mirrors
- Log amplifiers
- Multipliers

Ordering Information

Part No.	Temp. Range	Package	Outline #
EP2015CN	0°C to +75°C	P-DIP	MDP0031
EP2015ACN	0°C to +75°C	P-DIP	MDP0031
EP2015CM	0°C to +75°C	20-Lead SOL	MDP0027

General Description

The EP2015 family are quad monolithic vertical PNP transistor arrays which offer excellent parametric matching and high speed performance. The 350 MHz f_t provides A.C. performance similar to 2N3906 class devices. Manufactured on Elantec's Complementary Bipolar process, these transistors are electrically isolated from each other by a layer of oxide. The resulting low collector to substrate capacitance allows very high speed performance with minimal crosstalk. In addition, complete D.C. isolation is achieved. Substrate biasing is not required for normal operation, however for optimum high speed performance the substrate should be grounded. One-chip construction insures excellent parameter matching and tracking over temperature.

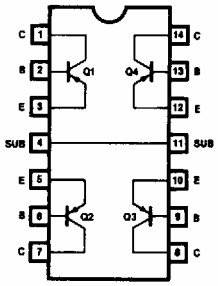
The low cost EP2015C is specified at 25°C. The EP2015AC is more tightly specified and guaranteed over the commercial temperature range of 0°C to +75°C. The EP2015C and EP2015AC are available in 14-pin plastic dual-in-line packages.

For information on a complementary NPN transistor array, see Elantec's EN2016 family data sheet.

Elantec facilities comply with MIL-I-45208A and other applicable quality specifications. For information on Elantec's processing, request our brochure, QRA1: *Elantec's Processing—Monolithic Products.*

Connection Diagrams

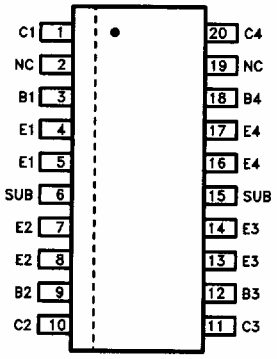
DIP Package



2015-1

Top View

20-Lead SOL



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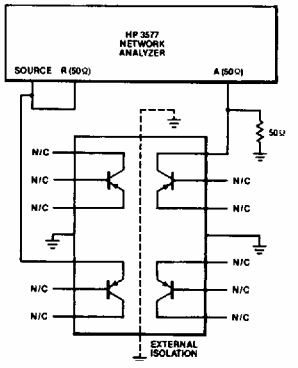
Isolation Characteristics Test Circuit



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EP2015C/EP2015AC
Fast Quad PNP Array

Absolute Maximum Ratings

P_D	Power Dissipation	
	Each Transistor	500 mW (T_A = 25°C)
	Total Package	1.25W (T_A = 25°C)
T_A	Operating Temperature Range	−0°C to +75°C
T_J	Maximum Junction Temperature	150°C

T_{ST}	Storage Temperature	−65°C to +150°C
	Lead Temperature	
	SOL Package	
	Vapor Phase (60 seconds)	215°C
	Infrared (15 seconds)	220°C
	(Soldering, <10 seconds)	300°C
V_{CB}	Max	40V
V_{EB}	Max	5V
V_{CE}	Max	40V
I_C	Max	50 mA
I_B	Max	10 mA

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Electrical Characteristics

Parameter	Description	Test Conditions	EP2015C Min	EP2015C Typ	EP2015C Max	EP2015C Test Level	Units
ΔV_{BE}	(Note 1)	V_{CE} = 4V, I_C = 1 mA, T_A = 25°C			5	I	mV
		$T_{MIN} < T_A < T_{MAX}$					mV
ΔH_{fe1}	(Notes 1, 2)	V_{CE} = 1V, I_C = 0.1 mA, T_A = 25°C			10	I	%
		$T_{MIN} < T_A < T_{MAX}$					%
ΔH_{fe2}	(Notes 1, 2)	V_{CE} = 1V, I_C = 1 mA, T_A = 25°C			10	I	%
		$T_{MIN} < T_A < T_{MAX}$					%
ΔH_{fe3}	(Notes 1, 2)	V_{CE} = 1V, I_C = 10 mA, T_A = 25°C			10	I	%
		$T_{MIN} < T_A < T_{MAX}$					%
H_{fe1}	(Note 3)	V_{CE} = 1V, I_C = 0.1 mA, T_A = 25°C	75			I	
		$T_{MIN} < T_A < T_{MAX}$					
H_{fe2}	(Note 3)	V_{CE} = 1V, I_C = 1.0 mA, T_A = 25°C	75			I	
		$T_{MIN} < T_A < T_{MAX}$					

Electrical Characteristics — Contd.

Parameter	Description	Test Conditions	EP2015 Min	EP2015 Typ	EP2015 Max	EP2015 Test Level	Units
H_{fe3}	(Note 3)	V_{CE} = 1V, I_C = 10 mA T_A = 25°C	75			I	
		$T_{MIN} < T_A < T_{MAX}$					
V_{BEsat}	(Note 3)	I_C = 10 mA, I_B = 1 mA T_A = 25°C			0.90	I	V
		$T_{MIN} < T_A < T_{MAX}$					V
V_{CEsat}	(Note 3)	I_C = 10 mA, I_B = 1 mA T_A = 25°C			0.20	I	V
		$T_{MIN} < T_A < T_{MAX}$					V
BV_{ceo}	(Note 3)	I_C = 1 mA, I_B = 0 mA T_A = 25°C	40			I	V
		$T_{MIN} < T_A < T_{MAX}$					V
BV_{cbo}	(Note 3)	I_C = 10 μA, I_E = 0 mA T_A = 25°C	40			I	V
		$T_{MIN} < T_A < T_{MAX}$					V
BV_{ebo}	(Note 3)	I_B = 10 μA, I_C = 0 mA T_A = 25°C	5			I	V
		$T_{MIN} < T_A < T_{MAX}$					V
I_{cbo}	(Note 3)	V_{CB} = 30V, I_E = 0 mA T_A = 25°C			50	I	nA
		$T_{MIN} < T_A < T_{MAX}$					nA
I_{ebo}	(Note 3)	V_{CE} = 4V, I_C = 0 mA T_A = 25°C			50	I	nA
		$T_{MIN} < T_A < T_{MAX}$					nA
f_t	(Note 3)	V_{CE} = 20V, I_C = 10 mA T_A = 25°C		350		V	MHz
r_{BE}	(Notes 3, 4)	10 μA, < I_C < 2 mA T_A = 25°C		1		V	Ω

Parameter	Description	Test Conditions	EP2015AC Min	EP2015AC Typ	EP2015AC Max	EP2015AC Test Level	Units
ΔV_{BE}	(Note 1)	V_{CE} = 4V, I_C = 1 mA T_A = 25°C			1	I	mV
		$T_{MIN} < T_A < T_{MAX}$			2	III	mV
ΔH_{fe1}	(Notes 1, 2)	V_{CE} = 1V, I_C = 0.1 mA T_A = 25°C			5	I	%
		$T_{MIN} < T_A < T_{MAX}$			10	III	%
ΔH_{fe2}	(Notes 1, 2)	V_{CE} = 1V, I_C = 1 mA T_A = 25°C			5	I	%
		$T_{MIN} < T_A < T_{MAX}$			10	III	%
ΔH_{fe3}	(Notes 1, 2)	V_{CE} = 1V, I_C = 10 mA T_A = 25°C			5	I	%
		$T_{MIN} < T_A < T_{MAX}$			10	III	%

EP2015C/EP2015AC
Fast Quad PNP Array

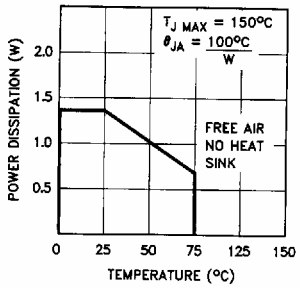
Electrical Characteristics — Contd.

Parameter	Description	Test Conditions	EP2015A				Units
			Min	Typ	Max	Test Level	
H_{fe1}	(Note 3)	V_{CE} = 1V, I_C = 0.1 mA T_A = 25°C	150			I	
		$T_{MIN} < T_A < T_{MAX}$	60			III	
H_{fe2}	(Note 3)	V_{CE} = 1V, I_C = 1.0 mA T_A = 25°C	150			I	
		$T_{MIN} < T_A < T_{MAX}$	60			III	
H_{fe3}	(Note 3)	V_{CE} = 1V, I_C = 10 mA T_A = 25°C	100			I	
		$T_{MIN} < T_A < T_{MAX}$	40			III	
V_{BEsat}	(Note 3)	I_C = 10 mA, I_B = 1 mA T_A = 25°C			0.90	I	V
		$T_{MIN} < T_A < T_{MAX}$			1.10	III	V
V_{CEsat}	(Note 3)	I_C = 10 mA, I_B = 1 mA T_A = 25°C			0.20	I	V
		$T_{MIN} < T_A < T_{MAX}$			0.30	III	V
BV_{ceo}	(Note 3)	I_C = 1 mA, I_B = 0 mA T_A = 25°C	40			I	V
		$T_{MIN} < T_A < T_{MAX}$	40			I	V
BV_{cbo}	(Note 3)	I_C = 10 μA, I_E = 0 mA T_A = 25°C	40			I	V
		$T_{MIN} < T_A < T_{MAX}$	40			III	V
BV_{ebo}	(Note 3)	I_B = 10 μA, I_C = 0 mA T_A = 25°C	5			I	V
		$T_{MIN} < T_A < T_{MAX}$	5			III	V
I_{cbo}	(Note 3)	V_{CB} = 30V, I_E = 0 mA T_A = 25°C			50	II	nA
		$T_{MIN} < T_A < T_{MAX}$			50	III	nA
I_{ebo}	(Note 3)	V_{CE} = 4V, I_C = 0 mA T_A = 25°C			50	I	nA
		$T_{MIN} < T_A < T_{MAX}$			50	III	nA
f_t	(Note 3)	V_{CE} = 20V, I_C = 10 mA T_A = 25°C		350		V	MHz
r_{BE}	(Notes 3, 4)	10 μA < I_C < 2 mA T_A = 25°C		1		V	Ω

Note 1: ΔV_{BE} and ΔH_{fe} are measured between each of six possible pairs of transistors.
Note 2: ΔH_{fe} is calculated based on the difference divided by the larger of the two readings.
Note 3: Applies to all four transistors.
Note 4: Estimated from log conformity.

Typical Performance Curves

20-Lead SOL
Maximum Power Dissipation
vs Ambient Temperature



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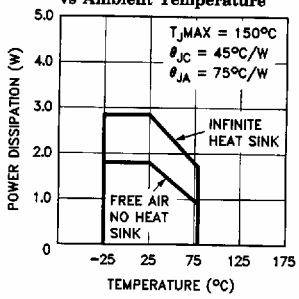
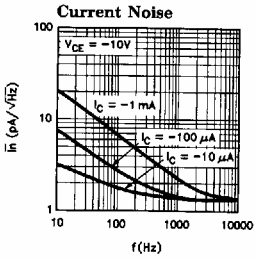
14-Lead Plastic DIP
Maximum Power Dissipation
vs Ambient Temperature

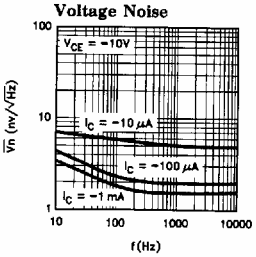


2015-12

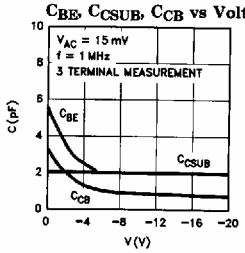
Current Noise



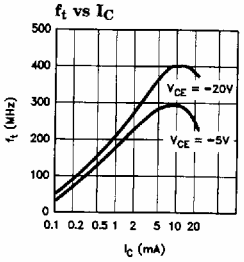
Voltage Noise



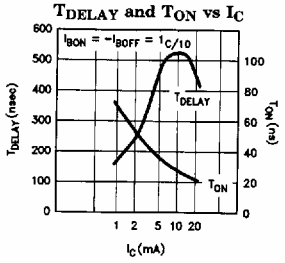
C_{BE}, C_{CSUB}, C_{CB} vs Voltage



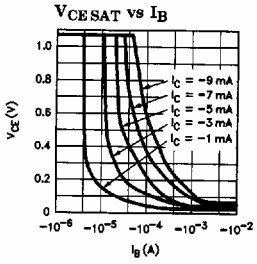
f_t vs I_C



T_{DELAY} and T_{ON} vs I_C



$V_{CE\,SAT}$ vs I_B



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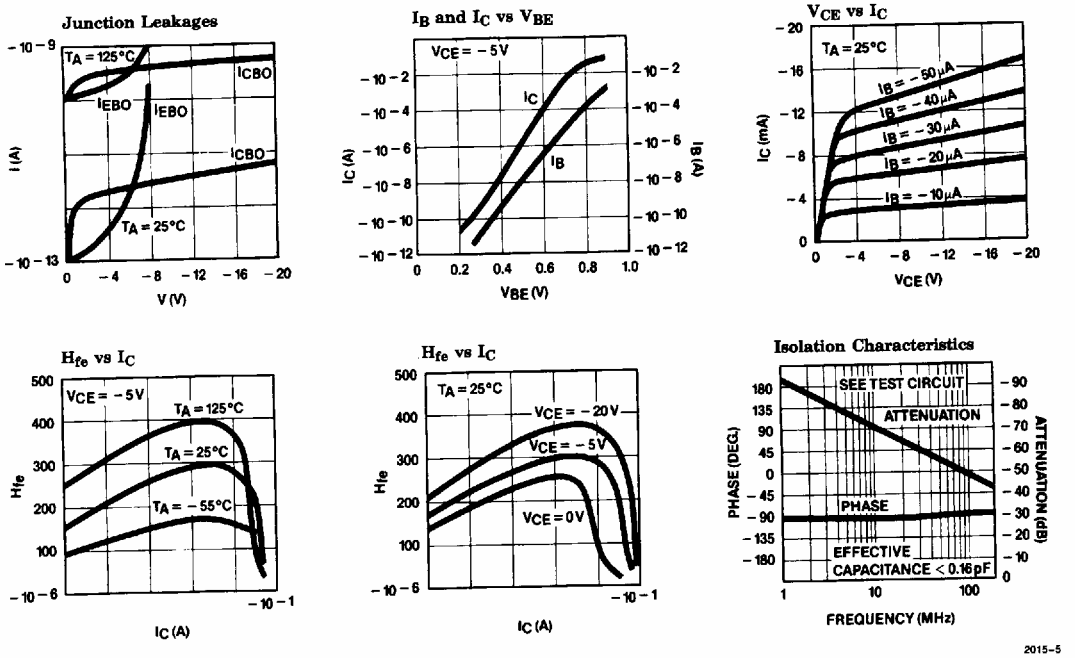
EP2015C/EP2015AC
Fast Quad PNP Array

Typical Performance Curves — Contd.



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EP2015 PSPICE® Model

IS = 8E − 15 BF = 300 VA = 47 IK = 0.03
XTB = 1.3 BR = 4.5 TF = 0.3N TR = 280N
RB = 230 RC = 170 ISE = 1E − 15 NE = 1.24
CCS = 2P MS = 0 CJC = 3.7P PC = 0.5 MC = 0.45
CJE = 5.4P PE = 0.6 ME = 0.33 PTF = 15

Note that for the above model the maximum "soft" saturation collector RC is used. For "hard" saturation modeling set RC ≈ 9.

PSPICE® is a registered trademark of MicroSim Corporation.

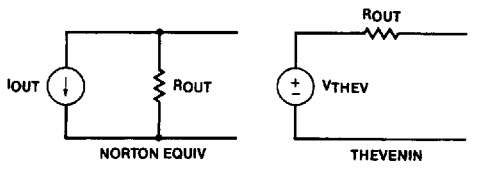
Matched NPN transistors have allowed system designers to make NPN current sinks. Now for the first time Elantec's fast matched PNP transistors are available. These make excellent, fast, matched current sources. The advantages of using current sources as active loads, instead of pullup resistors include:

- Faster, linear pull up (Not exponential)
- High output resistance (This increases voltage gain in many applications)

Current Sources and Current Mirrors

Current sinks and current mirrors have long been a tool available to the designer of monolithic ICs.

The Norton and Thevenin equivalent circuits of a current source are:



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$$\text{And } V_{THEV} = I_{OUT} \times R_{OUT}$$

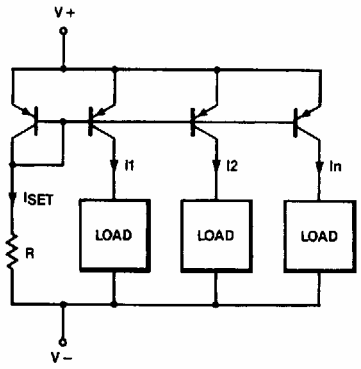
Four examples of current mirrors are shown, along with some of the advantages and limitations of each topology. For a more thorough discussion see "Analysis and Design of Analog Integrated Circuits" by Grey & Meyer (Wiley 1984), pages 233–247.

All current sources are only as good as the transistors that make them. If the transistors' V_{BE} match is 5 mV the output current would have a 20% error.

All current sources shown can be improved by putting a resistor in series with the topmost emitters. A 250 mV drop across these resistors reduces a 5 mV V_{BE} mismatch to a 2% current error. This has the added benefit of increasing output resistance. Elantec can guarantee a 1 mV V_{BE} match so resistors may not be necessary.

Basic Current Source

The Basic Current Mirror is simple and works well at low currents. Its limitations are low output resistance and it is not as fast as the Wilson.



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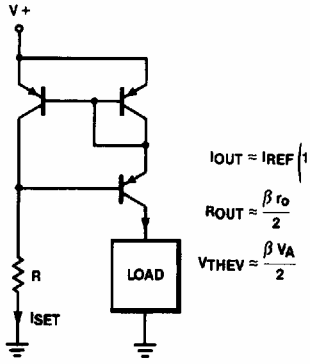
$$I_{SET} \approx \frac{((V+) - (V-)) - V_{BE}}{R}$$

$$I1 = I2 = In = \frac{\beta I1}{\beta + n + 1}$$

$$R_{OUT} = \frac{V_A}{I_{OUT}} = \frac{\text{EARLY VOLTAGE}}{I_{OUT}} = r_o$$

PNP Wilson Current Mirror

The Wilson is the best Current Mirror for high frequency applications, and it has plenty of output resistance.



$$I_{OUT} \approx I_{REF}\left(1 - \frac{2}{\beta^2 + 2\beta + 2}\right)$$

$$R_{OUT} \approx \frac{\beta r_o}{2}$$

$$V_{THEV} \approx \frac{\beta V_A}{2}$$

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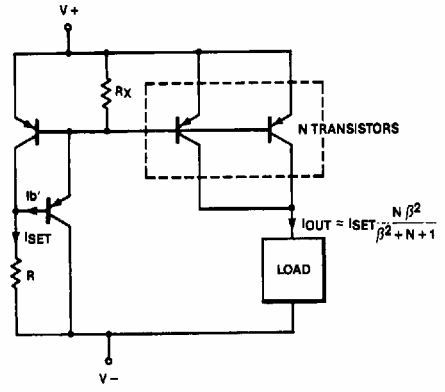
Fast Quad PNP Array

Precision Current Source

The Precision Current Source has excellent current match since the error reduction is proportional to β^2. It is slow to turn off since it has no base turn off current. The turn off speed can be increased by using R_X, at the expense of reduced accuracy.



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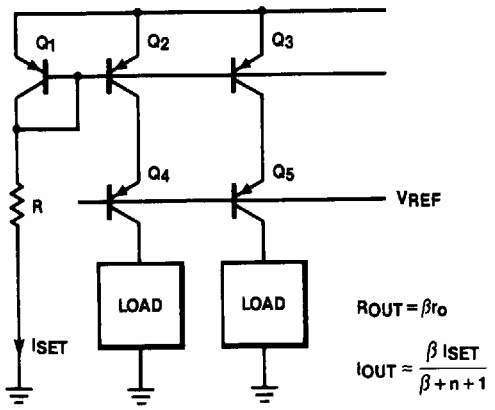
$$I_{SET} \approx \frac{((V+) - (V-)) - 2(V_{BE})}{R}$$

$$I_{OUT} \approx I_{SET} \frac{N\beta^2}{\beta^2 + N + 1}$$

$$R_{OUT} = \frac{V_A}{I_{OUT}}$$

Cascode Current Source

The Cascode Current Source is a basic current mirror with a common base transistor in the collector. This makes V_{CE} relatively constant for the mirror transistors and greatly increases the output resistance. This has good high frequency characteristics. Note that Q4 and Q5 can be in a package separate from Q1, Q2 and Q3.



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EP2015 Macromodel

```
* Connections:      q1c
*                   |   q1b
*                   |   |   q1e
*                   |   |   |   q2c
*                   |   |   |   |   q2b
*                   |   |   |   |   |   q2e
*                   |   |   |   |   |   |   q3c
*                   |   |   |   |   |   |   |   q3b
*                   |   |   |   |   |   |   |   |   q3e
*                   |   |   |   |   |   |   |   |   |   q4c
*                   |   |   |   |   |   |   |   |   |   |   q4b
*                   |   |   |   |   |   |   |   |   |   |   |   q4e
*                   |   |   |   |   |   |   |   |   |   |   |   |
.subckt em2015      1   2   3   7   6   5   8   9   10  14  13  12
* Models
.model ep2015 pnp (is=8e-15 bf=300 va=47 ikf=30mA xtb=1.3 br=4.5 tf=0.3nS
+tr=280nS rb=230 rc=170 ise=1e-15 ne=1.24 ccs=2pF cjc=3.7pF pc=0.5
+mc=0.45 cje=5.4pF pe=0.6 me=0.33 ptf=15)
* Transistors
q1 1 2 3 ep2015
q2 7 6 5 ep2015
q3 8 9 10 ep2015
q4 14 13 12 ep2015
.ends
```