
**ENC424J600/624J600 Silicon Errata
and Data Sheet Clarification**

The ENC424J600/624J600 devices that you have received conform functionally to the current Device Data Sheet (DS39935B), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the combined Device/Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (A2).

Data Sheet clarifications and corrections start on page 5, following the discussion of silicon issues.

The silicon revision level can be retrieved by querying the read-only EIDLEDL register (when using one of the 8-bit interfaces) or the lower byte of the EIDLED register (when using a 16-bit interface). Please refer to the Device Data Sheet for detailed information on accessing these registers.

The values for the various ENC424J600/624J600 silicon revisions are shown in Table 1.

TABLE 1: COMBINED DEVICE/REVISION ID

Part Number	Value of EIDLEDL or EIDLED<7:0>
	A2
ENC424J600	21h
ENC624J600	

ENC424J600/624J600

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions ⁽¹⁾
				A2
PHY	Receive	1.	Rare packet loss following collisions, 10Base-T Half-Duplex mode	X
PHY	Transmit	2.	Deviations from MAU Eye Pattern in 10Base-T mode	X
PHY	Transmit	3.	Rise time/fall time asymmetry in MLT3 signal	X
Memory	SFR	4.	CRYPTEN bit cannot be changed by BFC/BFS/BFCU/BFSU opcodes or EIRSET/EIRCLR registers.	X
AES	—	5.	AES module produces incorrect results.	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (A2).

1. Module: PHY (Receive)

On rare occasions, in 10Base-T Half-Duplex mode, a collision will cause the immediately following packet to be received incorrectly. This causes the packet to be dropped. This condition may occur on an average of one to four times per 10,000 collisions.

Full-Duplex mode and 100Base-TX modes are unaffected by this issue. Typical modern networks are deployed using Ethernet switching technology and will not experience any collisions or packet loss due to this issue. In the uncommon case that an affected network infrastructure is used, upper layer communications protocols, such as TCP, will normally perform automatic retransmission to ensure that no application data is lost.

Work around

None.

Affected Silicon Revisions

A2								
X								

2. Module: PHY (Transmit)

When transmitting random data in 10Base-T mode, the PHY transmit waveform slightly violates the MAU eye diagram keep-out zones specified in the IEEE 802.3™ Std. 2005, Section 14.3.1.2.1. Specifically, the waveform amplitude is slightly too high for '0' to '1' and '1' to '0' bit transitions when tested against the twisted-pair model, as shown in Figure 1.

This issue applies only to 10 Mbps speed and is unlikely to cause compatibility problems in real networks. When terminated with a 100Ω resistor without the twisted-pair model, the transmit waveform stays within the amplitude limits of +2.2V to +2.8V and -2.2V to -2.8V required by the standard.

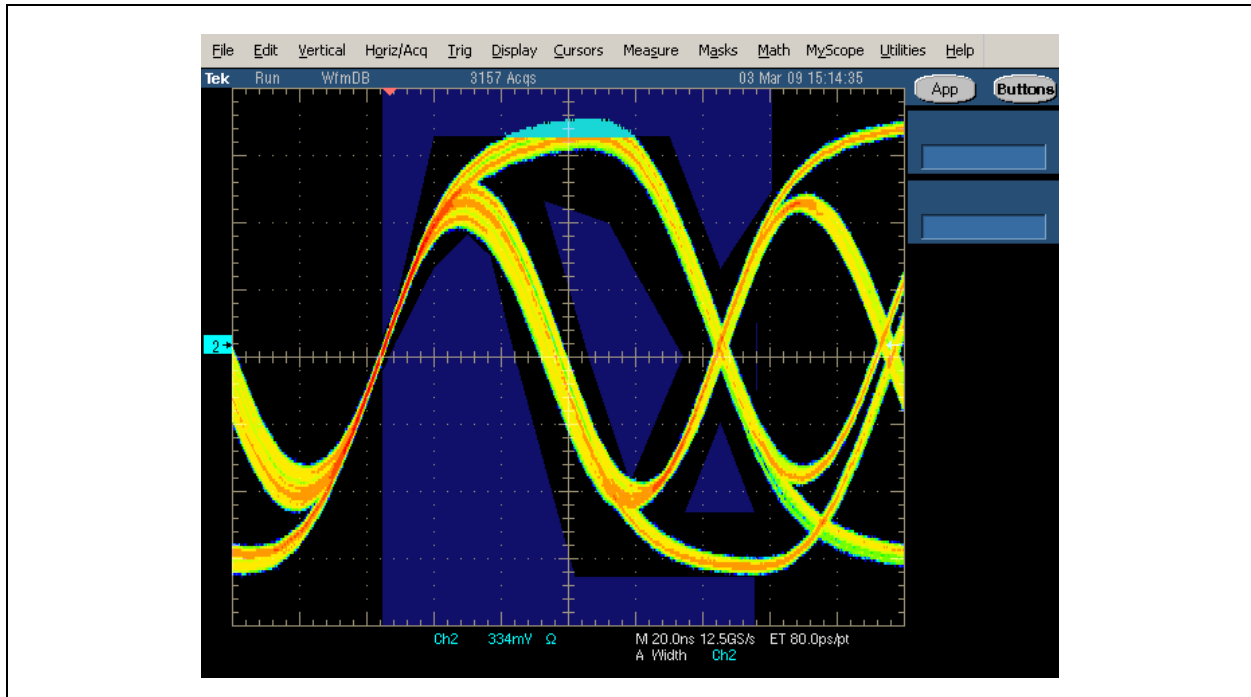
Work around

None.

Affected Silicon Revisions

A2								
X								

FIGURE 1: 10Base-T MAU EYE DIAGRAM



3. Module: PHY (Transmit)

For 100Base-TX operation, the IEEE 802.3 specification requires the rise and fall times of the MLT3 signal to match within 0.5 ns, measured over 10 different intervals. The actual rise/fall time symmetry measurements may occasionally be slightly above this level.

This issue has no substantial impact on the quality of the transmitted signal and will not impact applications operating in real networks.

Work around

None.

Affected Silicon Revisions

A2							
X							

4. Module: Memory (SFR)

The CRYPTEN bit (EIR<15>) cannot be changed using the Bit Field Set (BFS), Bit Field Clear (BFC), Bit Field Set Unbanked (BFSU) or Bit Field Clear Unbanked (BFCU) SPI opcodes. Similarly, when the PSP interface is being used, CRYPTEN cannot be changed by writing to the EIRSET or EIRCLR registers.

Work around

Set or clear the CRYPTEN bit using the Write Control Register (WCR) or Write Control Register Unbanked (WCRU) SPI opcodes, or a direct PSP write to the EIR register.

If the application is not constrained by power consumption, it is possible to set the CRYPTEN bit at device initialization and leave it set.

If the application must change CRYPTEN at run time, care must be taken to ensure that no required interrupt flag bits in EIR are corrupted in the process. For example, if the Link Change Interrupt Flag, LINKIF (EIR<11>), is used by the software, writing to EIR will cause potential loss of information. This can be avoided by sampling the interrupt source (PHYLNK bit in ESTAT) before and after changing CRYPTEN. If the PHYLNK bit has changed, the LINKIF bit can be manually set through a safe BFS operation or write to EIRSET. Any intermediate spurious interrupts on the INT pin can be suppressed by appropriately controlling the EIE interrupt enable bits.

Ideally, if using the SPI interface or using a PSP interface with byte write capability, write only to EIRH and avoid writing to EIRL.

Affected Silicon Revisions

A2							
X							

5. Module: AES

At room temperature, the AES module may compute valid results. However, across voltage, temperature, and ordinary part-to-part device variation, the AES engine will compute incorrect results or fail to finish computations.

Work around

Use a software implementation of AES. For applications based on Microchip PIC® microcontrollers or dsPIC® digital signal controllers, consider using the libraries documented in the Microchip Application Notes AN953, "Data Encryption Routines for the PIC18" or AN1044, "Data Encryption Routines for PIC24 and dsPIC® Devices". The source code for these libraries is available on the Data Encryption Libraries CD, Microchip part number SW300052.

Affected Silicon Revisions

A2							
X							

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS39935**B**):

Note: Corrections are shown in bold . Where possible, the original bold text formatting has been removed for clarity.

No issues.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (6/2009)

Initial release of this document; issued for revision A2.
Includes silicon issues 1 (PHY – Receive), 2-3 (PHY –
Transmit), 4 (Memory – SFR) and 5 (AES).

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

Trademarks

The Microchip name and logo, the Microchip logo, dsPIC, KEELOQ, KEELOQ logo, MPLAB, PIC, PICmicro, PICSTART, rfPIC and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

FilterLab, Hampshire, HI-TECH C, Linear Active Thermistor, MXDEV, MXLAB, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Application Maestro, CodeGuard, dsPICDEM, dsPICDEM.net, dsPICworks, dsSPEAK, ECAN, ECONOMONITOR, FanSense, HI-TIDE, In-Circuit Serial Programming, ICSP, ICEPIC, Mindi, MiWi, MPASM, MPLAB Certified logo, MPLIB, MPLINK, mTouch, nanoWatt XLP, Omniscent Code Generation, PICC, PICC-18, PICkit, PICDEM, PICDEM.net, PICTail, PIC³² logo, REAL ICE, rfLAB, Select Mode, Total Endurance, TSHARC, WiperLock and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2009, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

 Printed on recycled paper.

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
== ISO/TS 16949:2002 ==

Microchip received ISO/TS-16949:2002 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.



WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office

2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
<http://support.microchip.com>
Web Address:
www.microchip.com

Atlanta

Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Boston

Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago

Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Cleveland

Independence, OH
Tel: 216-447-0464
Fax: 216-447-0643

Dallas

Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit

Farmington Hills, MI
Tel: 248-538-2250
Fax: 248-538-2260

Kokomo

Kokomo, IN
Tel: 765-864-8360
Fax: 765-864-8387

Los Angeles

Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

Santa Clara

Santa Clara, CA
Tel: 408-961-6444
Fax: 408-961-6445

Toronto

Mississauga, Ontario,
Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office

Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon
Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

Australia - Sydney

Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing

Tel: 86-10-8528-2100
Fax: 86-10-8528-2104

China - Chengdu

Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Hong Kong SAR

Tel: 852-2401-1200
Fax: 852-2401-3431

China - Nanjing

Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao

Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai

Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang

Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen

Tel: 86-755-8203-2660
Fax: 86-755-8203-1760

China - Wuhan

Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xiamen

Tel: 86-592-2388138
Fax: 86-592-2388130

China - Xian

Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

China - Zhuhai

Tel: 86-756-3210040
Fax: 86-756-3210049

ASIA/PACIFIC

India - Bangalore

Tel: 91-80-3090-4444
Fax: 91-80-3090-4080

India - New Delhi

Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune

Tel: 91-20-2566-1512
Fax: 91-20-2566-1513

Japan - Yokohama

Tel: 81-45-471- 6166
Fax: 81-45-471-6122

Korea - Daegu

Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul

Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur

Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang

Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila

Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore

Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu

Tel: 886-3-6578-300
Fax: 886-3-6578-370

Taiwan - Kaohsiung

Tel: 886-7-536-4818
Fax: 886-7-536-4803

Taiwan - Taipei

Tel: 886-2-2500-6610
Fax: 886-2-2508-0102

Thailand - Bangkok

Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels

Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen

Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris

Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Munich

Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan

Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands - Drunen

Tel: 31-416-690399
Fax: 31-416-690340

Spain - Madrid

Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

UK - Wokingham

Tel: 44-118-921-5869
Fax: 44-118-921-5820