EMIF10-LCD01F2

IPAD™

10 line EMI filter and ESD protection

Main product characteristics:

Where EMI filtering in ESD sensitive equipment is required :

- LCD for Mobile phones
- Computers and printers
- Communication systems
- MCU Boards

Description

The EMIF10-LCD01F2 is a 10 line highly integrated device designed to suppress EMI/RFI noise in all systems subjected to electromagnetic interferences. The EMIF10 Flip-Chip packaging means the package size is equal to the die size.

This filter includes ESD protection circuitry, which prevents damage to the application when it is subjected to ESD surges up to 15 kV.

Benefits

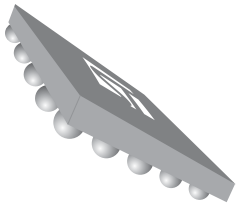
- EMI symmetrical (I/O) low-pass filter
- High efficiency in EMI filtering
- Very low PCB space consuming: < 6 mm^2
- Lead free package
- Very thin package: 0.69 mm
- High efficiency in ESD suppression on input pins (IEC 61000-4-2 level 4)
- High reliability offered by monolithic integration
- High reducing of parasitic elements through integration and wafer level packaging.

Complies with following standards:

IEC 61000-4-2

level 4 input pins	15 kV	(air discharge)
	8 kV	(contact discharge)

MIL STD 883G - Method 3015-7 Class 3



Flip-Chip
(25 bumps)

Order code

Part Number	Marking
EMIF10-LCD01F2	FL

Figure 1. Pin Configuration (bump side)

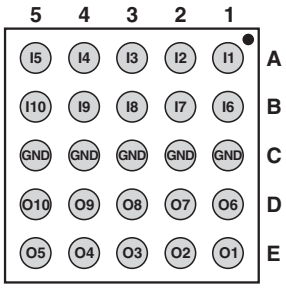
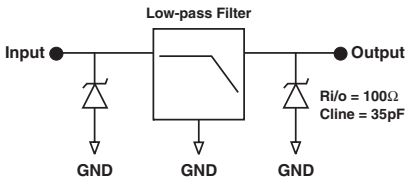


Figure 2. Basic Cell Configuration



TM: IPAD is a trademark of STMicroelectronics.

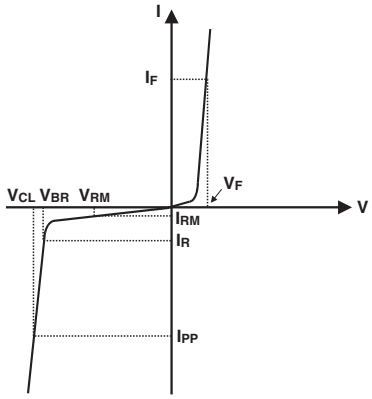
1 Characteristics

Table 1. Absolute Maximum Ratings (T_{amb} = 25° C)

Symbol	Parameter	Value	Unit
T_j	Junction temperature	125	° C
T_{op}	Operating temperature range	-40 to + 85	° C
T_{stg}	Storage temperature range	-55 to +150	° C

Table 2. Electrical Characteristics (T_{amb} = 25° C)

Symbol	Parameter
V_{BR}	Breakdown voltage
I_{RM}	Leakage current @ V_{RM}
V_{RM}	Stand-off voltage
V_{CL}	Clamping voltage
R_d	Dynamic resistance
I_{PP}	Peak pulse current
$R_{I/O}$	Series resistance between Input and Output
C_{line}	Input capacitance per line



Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	I_R = 1 mA	6	8	10	V
I_{RM}	V_{RM} = 3 V			500	nA
$R_{I/O}$		90	100	110	Ω
C_{line}	@ 0 V bias		28	35	pF
Rt / Ft	Induced rise and fall time 10-90% at 26 MHz frequency signal V = 1.9 V (Rt / Ft input 1 ns, 50Ω impedance generator)		8(1)		ns

1. guaranteed by design

Figure 3. S21(dB) attenuation measurement

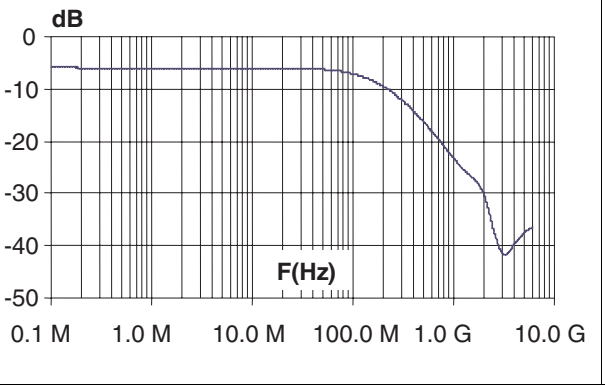


Figure 4. Analog cross talk measurement

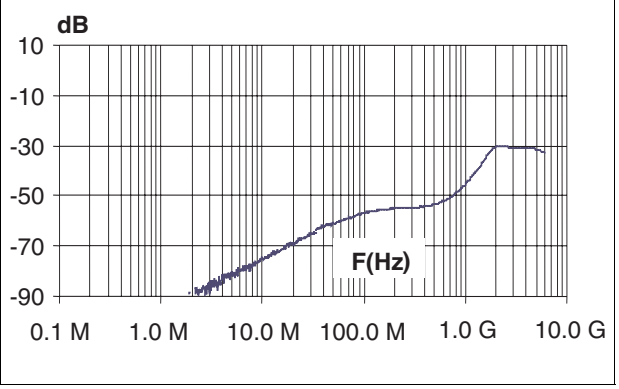


Figure 5. ESD response to IEC 61000-4-2 (+15 kV air discharge) on one input and on one output

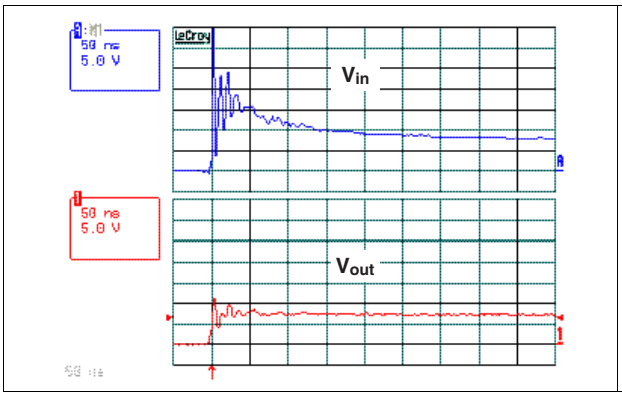


Figure 6. ESD response to IEC 61000-4-2 (-15 kV air discharge) on one input and on one output

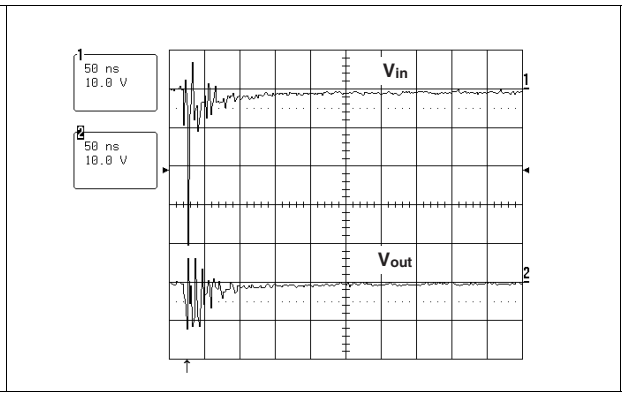


Figure 7. Line capacitance versus applied voltage

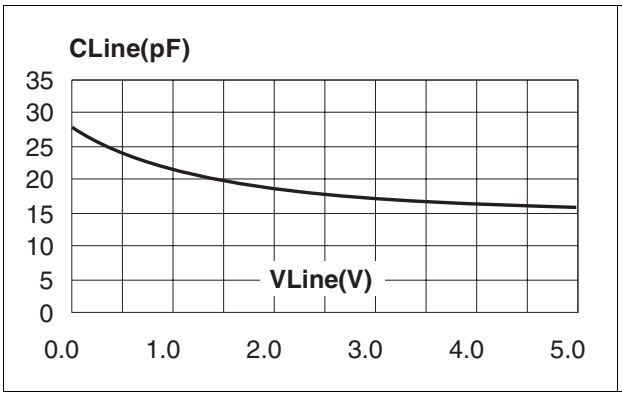


Figure 8. Rise time 10-90% measurements with 1.9 V signal at 26 MHz frequency (50 Ω generator)

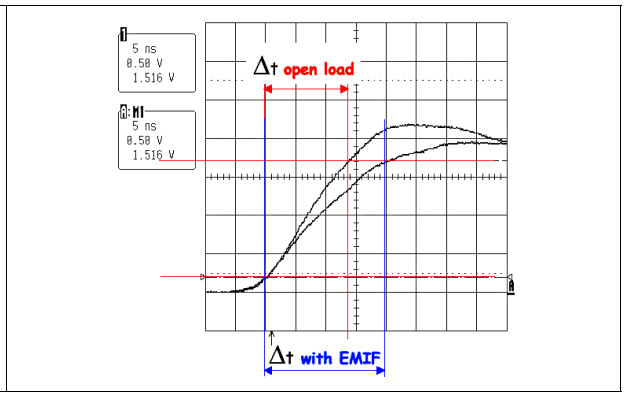


Figure 9. Fall time 10-90% measurements with 1.9 V signal at 26 MHz frequency (50 Ω generator)

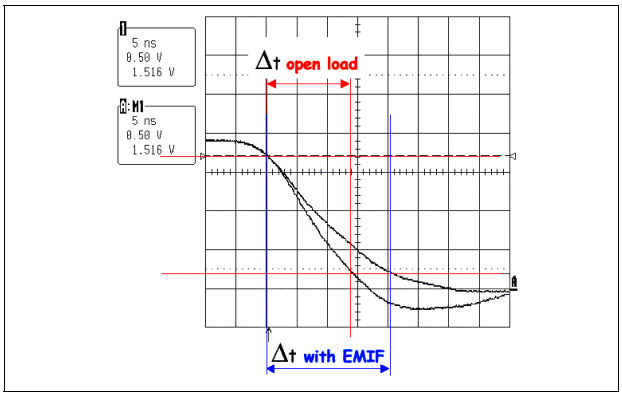


Figure 10. Aplac model

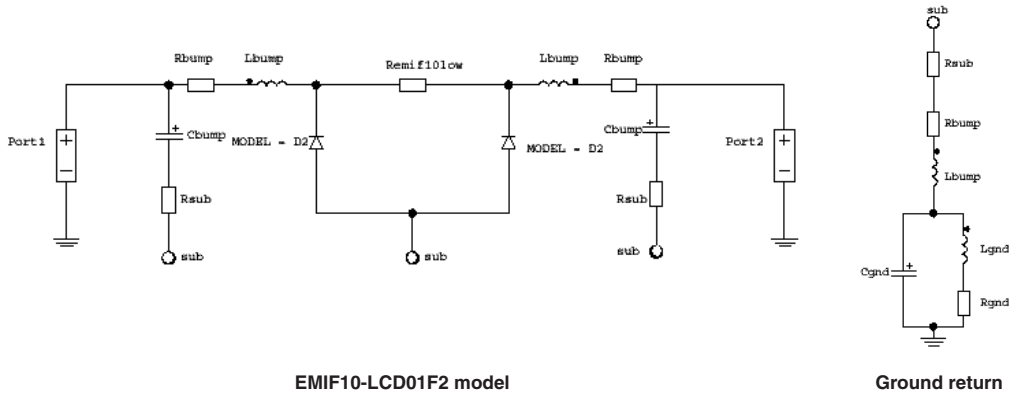


Figure 11. Aplac parametersl

ZRZ structure
aplacvar Remif10low 100
aplacvar Cemif10flow 17.5pF
Bumps
aplacvar Lbump 50pH
aplacvar Rbump 20m
aplacvar Cbump 1.5pF
Bulk
aplacvar Rsub 100m
Gnd connections
aplacvar Rgnd 100m
aplacvar Lgnd 200pH
aplacvar Cgnd 0.15pF

BV = 7
CJO = Cemif10low
IBV = 1u
IKF = 1000
IS = 10f
ISR = 100p
N = 1
M = 0.3333
RS = 0.015
VJ = 0.6
TT = 50n

2 Ordering information scheme

EMIF yy - xxx zz Fx

EMI Filter

Number of lines

Information
x = resistance value (Ohms)
z = capacitance value / 10(pF)
or
3 letters = application
2 digits = version

Package
F = Flip-Chip
x = 1: 500µm, Bump = 315µm
= 2: Leadfree Pitch = 500µm, Bump = 315µm
= 3: Leadfree Pitch = 400µm, Bump = 250µm

3 Package information

Figure 12. Flip-Chip Dimensions

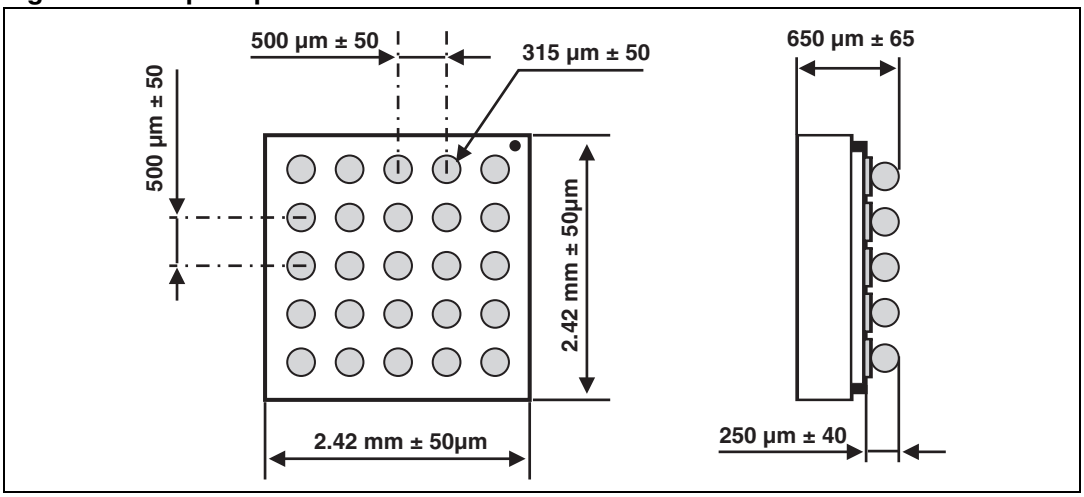


Figure 13. Marking

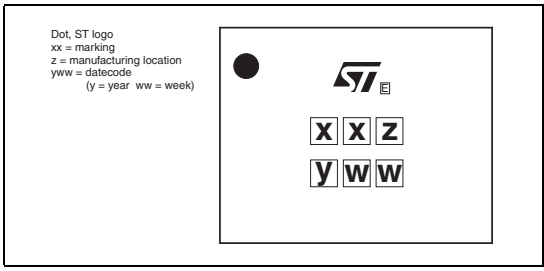


Figure 14. Footprint recommendation

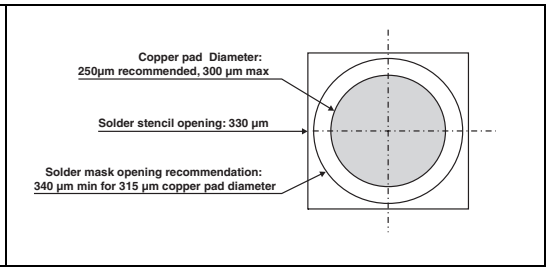
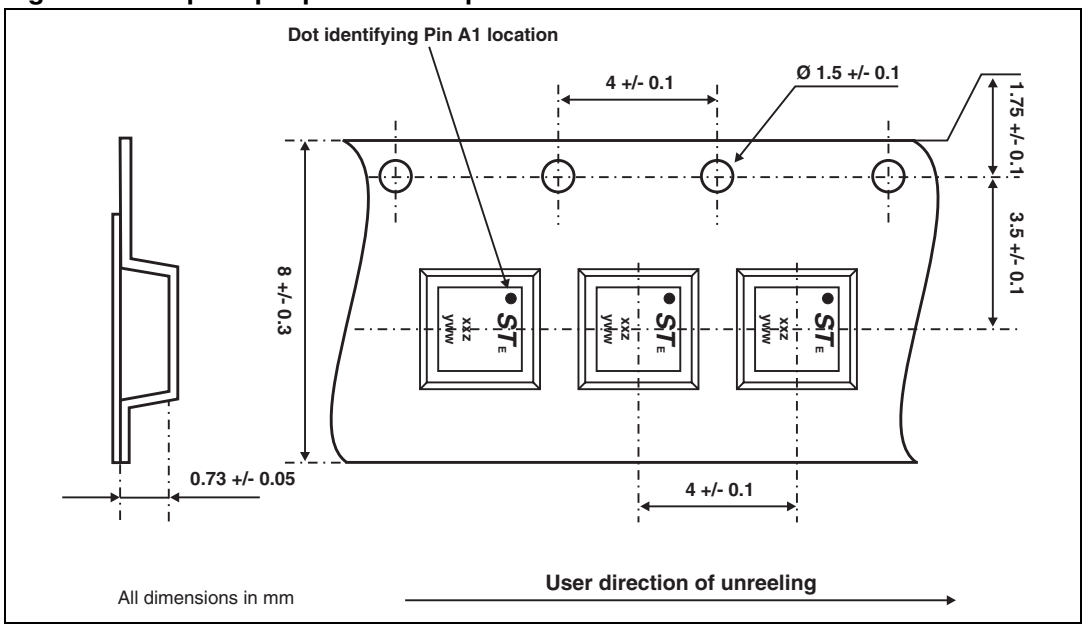


Figure 15. Flip-Chip tape and reel specification



In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Note: More packing information is available in the application notes:

AN1235: "Flip-Chip: Package description and recommendations for use"

AN1751: "EMI Filters: Recommendations and measurements"

4 Ordering information

Ordering code	Marking	Package	Weight	Base qty	Delivery mode
EMIF10-LCD01F2	FL	Flip-Chip	9.3 mg	5000	Tape and reel (7")

5 Revision history

Date	Revision	Changes
14-Feb-2005	1	Initial release.
17-Mar-2005	2	Capacitance C_{line} specification changed from 47 pF (typ) to 28 pF (typ) and 35 pF (max).
30-Jan-2007	3	Reformatted to current standards. Reduced die size and updated Figures 3 and 4.

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