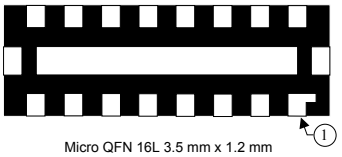
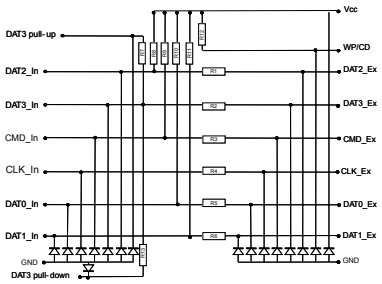
EMIF06-MSD02N16

Datasheet

6-line IPAD EMI filter and ESD protection in micro QFN package



Micro QFN 16L 3.5 mm x 1.2 mm
(bottom view)



Features

- High design flexibility
- Lead free package
- Very low PCB space consuming: 3.5 mm x 1.2 mm
- Very thin package: 0.55 mm max.
- High efficiency in ESD suppression
- Complies with following standards:
  - IEC 61000-4-2 level 4 externals pins
- High reliability offered by monolithic integration
- High reduction of parasitic elements through integration and µQFN packaging

Applications

Where EMI filtering in ESD sensitive equipment is required:

- Mobile telephones
- Navigation systems
- Digital still cameras
- Portable devices

Description

The EMIF06-MSD02N16 is a 6-line, highly integrated device designed to suppress EMI/RFI noise in all systems exposed to electromagnetic interference.

This filter includes an ESD protection circuitry, which prevents damage to the application when subjected to ESD surges.

Product status
EMIF06-MSD02N16

Product label
LONGEVITY 10 YEARS COMMITMENT

1 Characteristics

Figure 1. Pin configuration

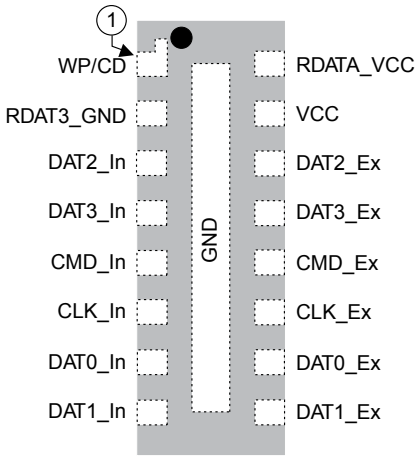


Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter	Value	Unit
V_{PP}	ESD IEC 61000-4-2 Contact discharge on DATx_In, CMD_In and CLK_In pins On all other pins: Contact discharge Air discharge	 2 8 12	kV
T_j	Maximum junction temperature	125	°C
T_{op}	Operating temperature range	- 30 to + 85	°C
T_{stg}	Storage temperature range	- 55 to + 150	°C

Figure 2. Electrical characteristics (definitions)

Symbol	Parameter
V_{BR}	Breakdown voltage
I_{RM}	Leakage current at VRM
V_{RM}	Stand-off voltage
V_{CL}	Clamping voltage
R_d	Dynamic resistance
I_{PP}	Peak pulse current
$R_{I/O}$	Series resistance between Input and Output
C_{line}	Input capacitance per line

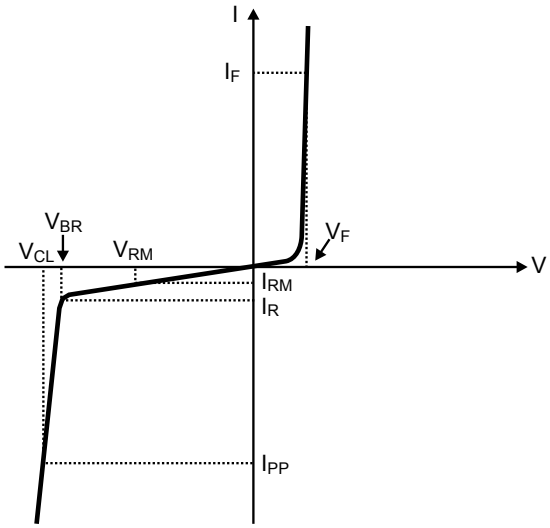


Table 2. Electrical characteristics (T_{amb} = 25 °C)

Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	I_R = 1 mA	5		8	V
I_{RM}	V_{RM} = 3 V per line			200	nA
R1, R2, R3, R4, R5, R6	Series resistors - tolerance ±20%	36	45	54	Ω
R7, R8, R9, R10, R11, R12	Pull-up resistors	80	90	100	kΩ
R13	Pull-down resistor - tolerance ±20%	375	470	565	kΩ
C_{line}	V_{LINE} = 0 V dc, V_{OSC} = 30 mV, F = 1 MHz			20	pF

1.1 Characteristics (curves)

Figure 3. S21 attenuation measurement

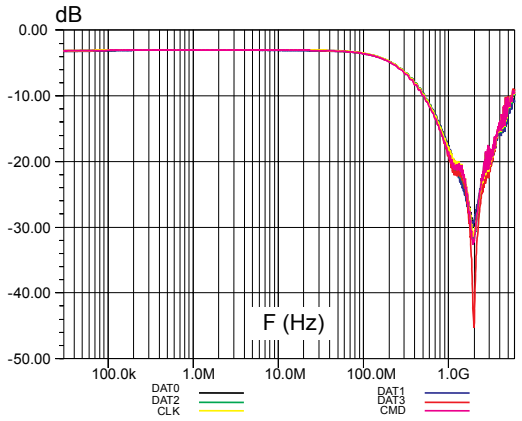


Figure 4. Analog cross talk measurements

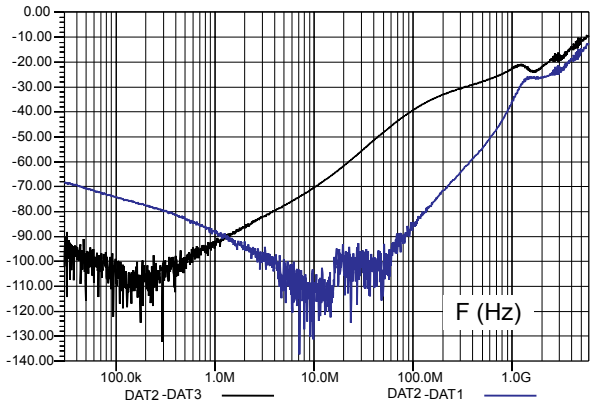


Figure 5. ESD response to IEC 61000-4-2 (+12 kV air discharge) on one input (V_{in}) and on one output (V_{out})

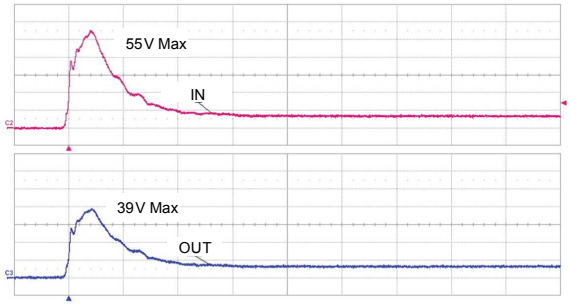


Figure 6. ESD response to IEC 61000-4-2 (- 12 kV air discharge) on one input (V_{in}) and on one output (V_{out})

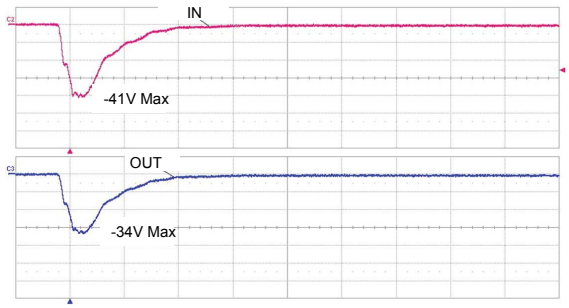
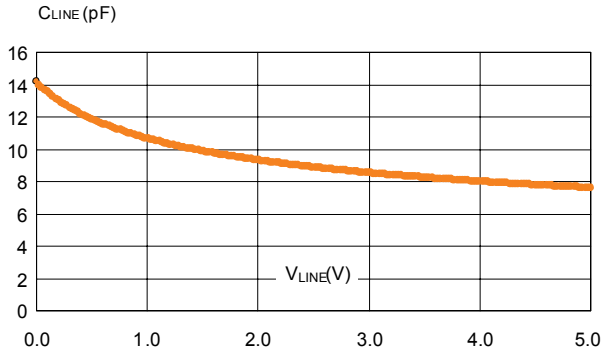


Figure 7. Line capacitance versus reverse voltage applied on DATx and CMD line



2 Application information

The EMIF06-mSD02N16 is a dedicated interface device for micro SD card/T-Flash card in mobile phones. The device provides:

- ESD protection
- EMI filterering
- Pull-up resistors
- Card detection circuit

2.1 ESD protection

Each pin is connected to a TVS diode able to withstand 12 kV on all pins except on DATx_In, CMD_In and CLK_In.

2.2 EMI filtering

DATx, CMD and CLK lines are immunized against EMI radiations thanks to pi-filters. To avoid any degradation of the signal integrity at high frequency, the total line capacitance stays lower than 20 pF making the device compatible with a clock frequency up to 52 MHz.

2.3 Pull-up resistors

As recommended by the SD Specifications (Part 1 Physical Layer Version 2.00), all the data lines DATx and the CMD line must be pulled-up with resistors of 10 to 100 kΩ to avoid bus floating not only in SD 4-bit mode but also in SD 1-bit and SPI mode.

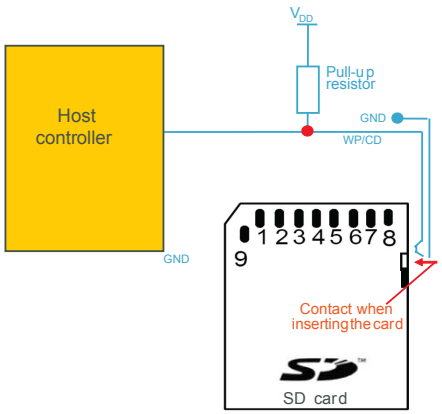
For the EMIF06-MSD02N16 device the pull-up resistor value has been fixed at 90 kΩ. This value makes the EMIF06-MSD02N16 compatible with most of the level shifters that may be used in the circuit including auto direction-sensing translators known to exhibit a weak current output.

2.4 Card detection circuit

The EMIF06-mSD02N16 provides the flexibility to use either mechanical card detection with a dedicated pin connected to the memory card slot or the electrical card detection using the internal pull resistor of DAT3 of the micro SD card/T-Flash card.

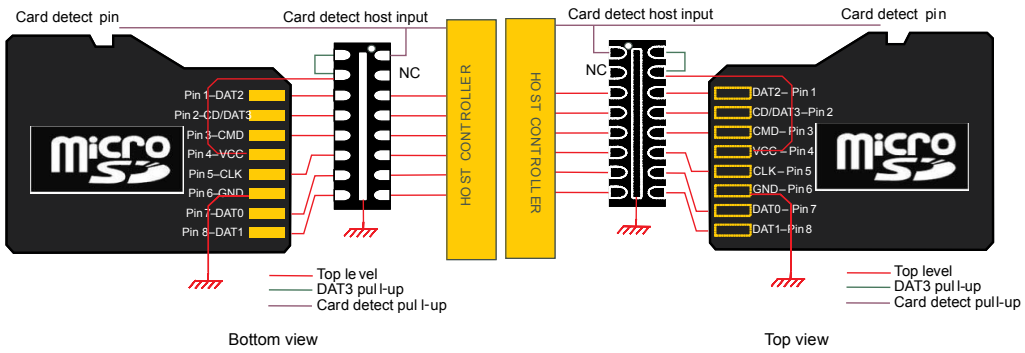
In case of mechanical card detection, the user must add a pull-up on the circuit connected to the CD (Card Detect) of the micro-SD/T-Flash slot as shown in Figure 8.

Figure 8. Mechanical card detection



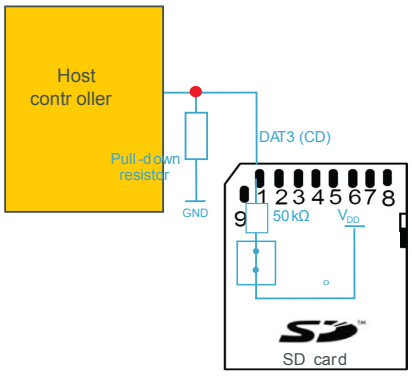
A pull-up of 90 kΩ is embedded into the EMIF06-MSD02N16. The routing corresponding to the mechanical card detection configuration is shown in Figure 9.

Figure 9. Circuit routing for mechanical card detection



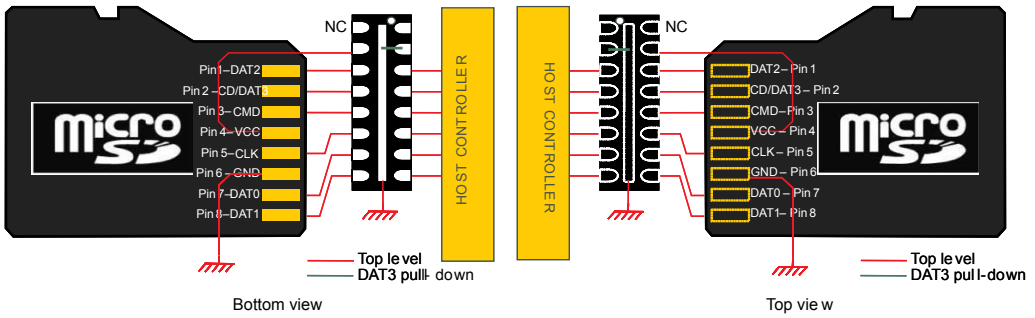
In case of electrical card detection, the user must add a pull-down on the circuit connected to the CD/DAT3 pin of the micro-SD/T-Flash pin as shown in Figure 10.

Figure 10. Electrical card detection



A pull-down of 470k is embedded into the EMIF06-mSD02N16. The routing corresponding to the electrical card detection configuration is shown in Figure 11.

Figure 11. Circuit routing for electrical card detection



3 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

3.1 Micro QFN 3.5x1.2-16L package information

- Epoxy meets UL94, V0

Figure 12. Micro QFN 3.5x1.2-16L package outline

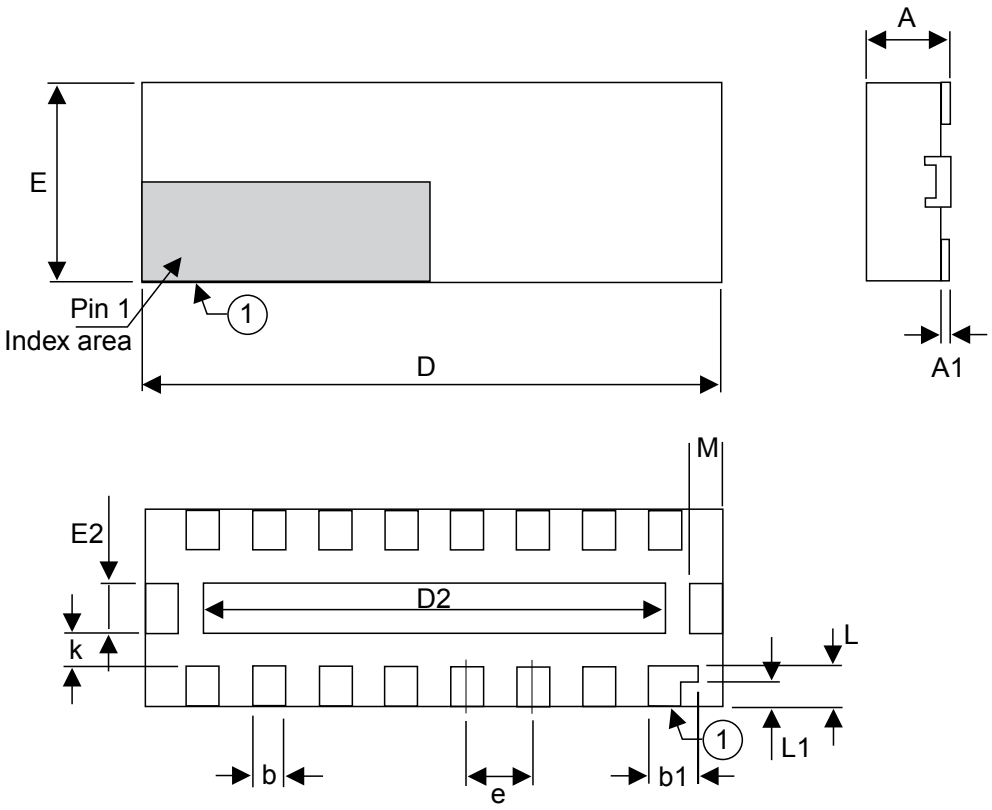


Table 3. **Micro QFN 3.5x1.2-16L package mechanical data**

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.45	0.50	0.55	0.018	0.020	0.022
A1	0.00		0.05	0.000		0.002
b	0.15	0.20	0.25	0.006	0.008	0.010
b1	0.25	0.30	0.35	0.010	0.012	0.014
D	3.45	3.50	3.55	0.136	0.138	0.140
D2	2.70	2.80	2.90	0.106	0.110	0.114
E	1.15	1.20	1.25	0.045	0.047	0.049
E2	0.20	0.30	0.40	0.008	0.012	0.016
e		0.40			0.016	
k		0.20			0.008	
L	0.20	0.25	0.30	0.008	0.010	0.012
L1		0.15			0.006	
M		0.20			0.008	

Figure 13. **Micro QFN 3.5x1.2-16L footprint (dimensions in mm)**

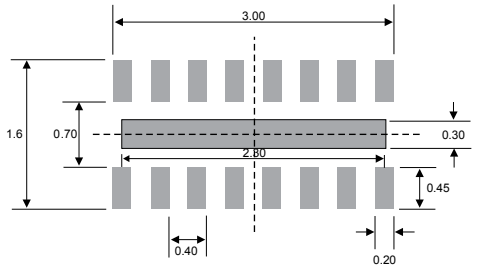


Figure 14. **Marking**

Dot : Pin 1 Identification
N6 = Marking

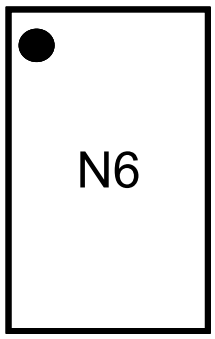
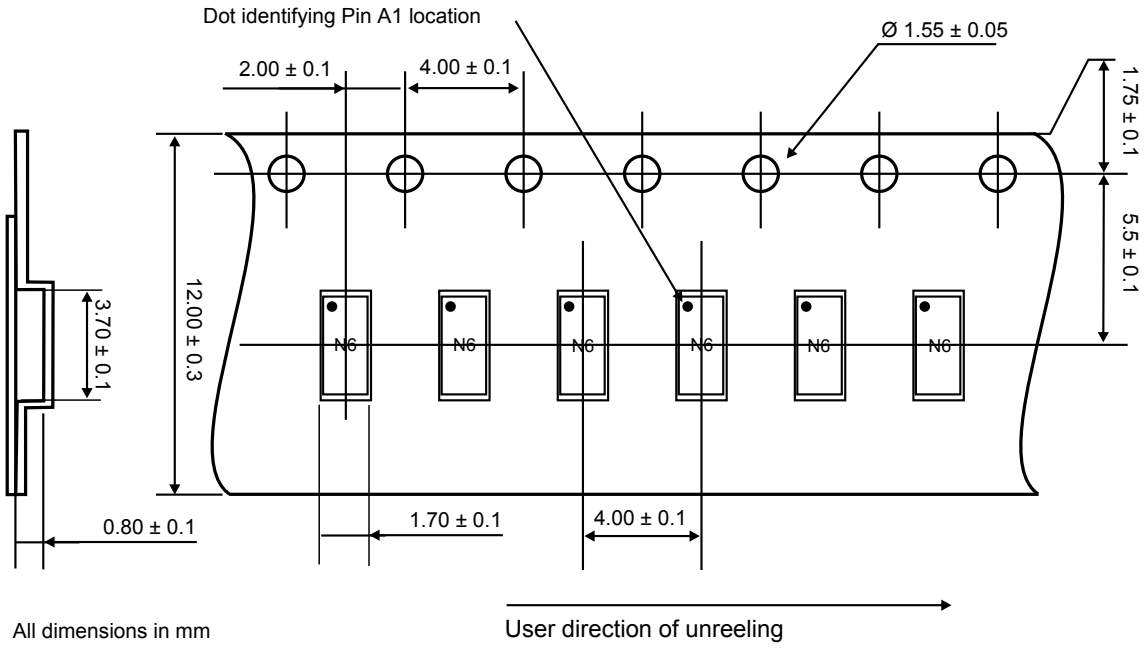


Figure 15. Tape and reel outline



Product marking may be rotated by 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

4 Recommendation on PCB assembly

4.1 Stencil opening design

1. General recommendation on stencil opening design
   a. Stencil opening dimensions: L (Length), W (Width), T (Thickness).
2. General design rule
   a. Stencil thickness (T) = 75 ~ 125 µm
   b. Aspect ratio = $\frac{W}{T} \geq 1.5$
   c. Aspect area = $\frac{L \times W}{2T(L+W)} \geq 0.66$
3. Reference design
   a. Stencil opening thickness: 100 µm
   b. Stencil opening for central exposed pad: Opening to footprint ratio is 50%.
   c. Stencil opening for leads: Opening to footprint ratio is 90%

Figure 16. Stencil opening dimensions

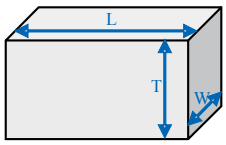
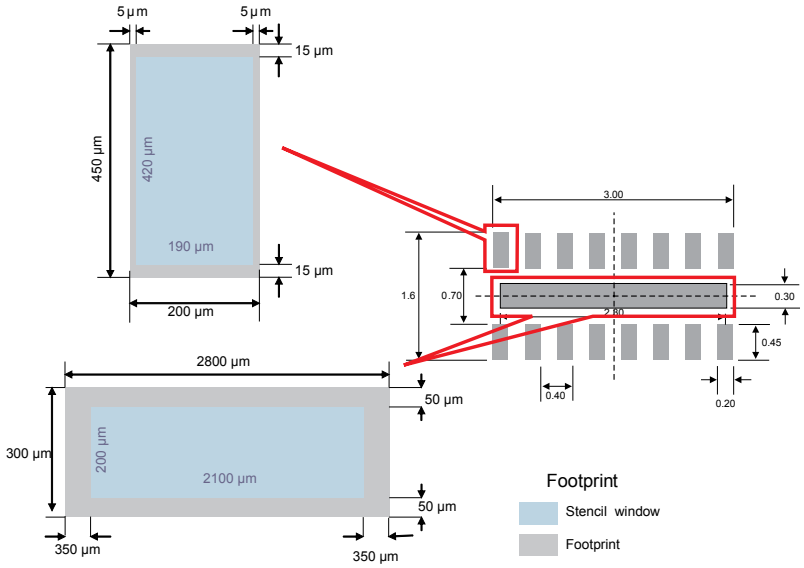


Figure 17. Recommended stencil window position



4.2 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Solder paste with fine particles: powder particle size is 20-45 µm.

4.3 Placement

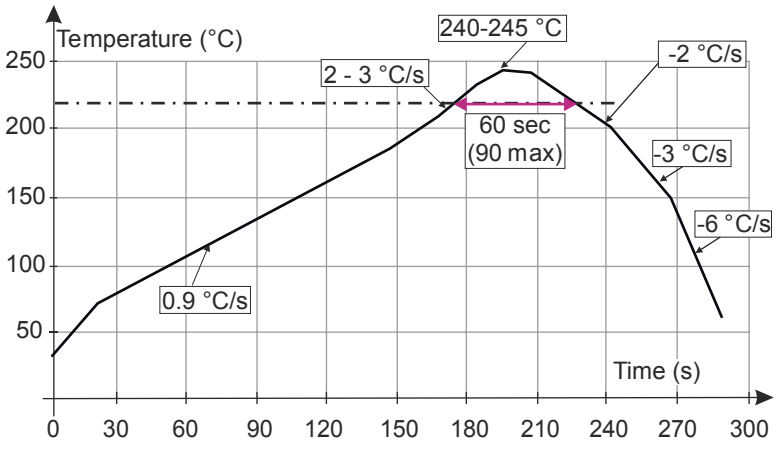
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of ±0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

4.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. A symmetrical layout is recommended, to avoid any tilt phenomena caused by asymmetrical solder paste due to solder flow away.

4.5 Reflow profile

Figure 18. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement. Maximum soldering profile corresponds to the latest IPC/JEDEC J-STD-020.

5 Ordering information

Figure 19. **Ordering information scheme**

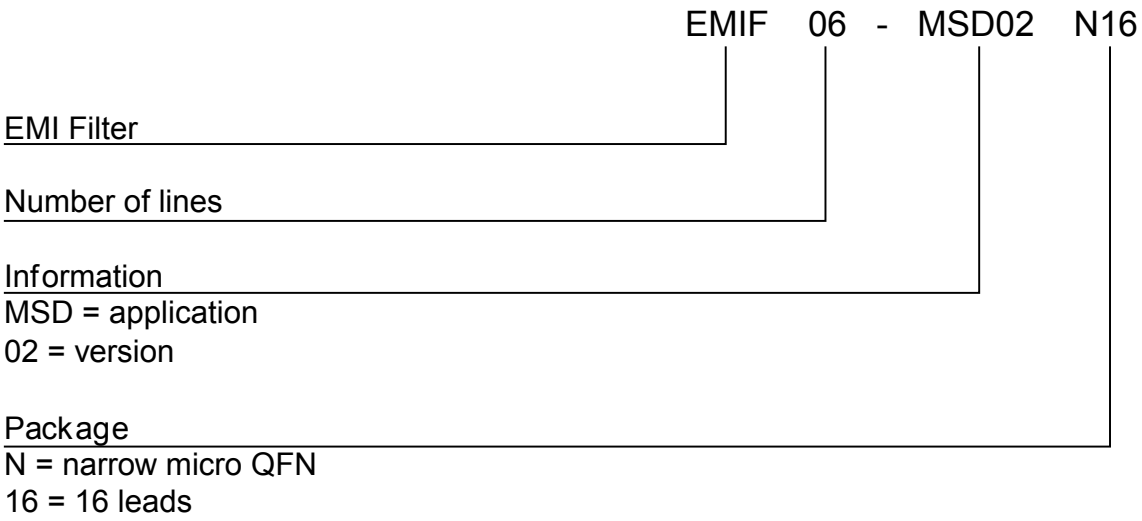


Table 4. **Ordering information**

Part number	Marking	Package	Weight	Base qty.	Delivery mode
EMIF06-MSDN16	N16(1)	Micro QFN	6.17 mg	3000	Tape and reel (7”)

1. *The marking can be rotated by 90° to differentiate assembly location*

Revision history

Table 5. **Document revision history**

Date	Version	Changes
21-Nov-2008	1	Initial release.
06-Sep-2019	2	Updated Table 3. Minor text changed.
11-May-2020	3	Updated product links and product label.

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