EMIF04-10006F2

4 LINES EMI FILTER AND ESD PROTECTION

IPAD™

MAIN PRODUCT CHARACTERISTICS

Where EMI filtering in ESD sensitive equipment is required:

- Mobile phones and communication systems
- Computers, printers and MCU Boards

DESCRIPTION

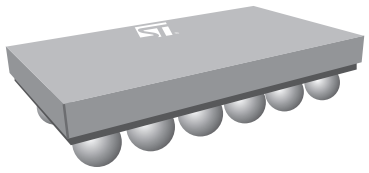
The EMIF04-10006F2 is a highly integrated devices designed to suppress EMI/RFI noise in all systems subjected to electromagnetic interferences. The EMIF04 flip-chip packaging means the package size is equal to the die size.
This filter includes an ESD protection circuitry which prevents the device from destruction when subjected to ESD surges up 15kV. This device includes four EMIF filters and 4 separated ESD diodes.

BENEFITS

- EMI symmetrical (I/O) low-pass filter
- High efficiency in EMI filtering
- Lead free package
- Very low PCB space consuming: 2.92mm x 1.29mm
- Very thin package: 0.65 mm
- High efficiency in ESD suppression (IEC61000-4-2 level 4)
- High reliability offered by monolithic integration
- High reducing of parasitic elements through integration and wafer level packaging.

COMPLIES WITH THE FOLLOWING STANDARDS:

IEC 61000-4-2 level 4:
15kV (air discharge)
8kV (contact discharge)
MIL STD 883E - Method 3015-6 Class 3: 30kV

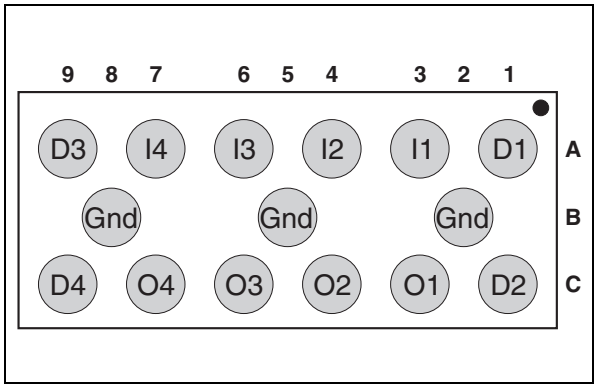


Flip-Chip
(15 Bumps)

Table 1: Order Code

Part Number	Marking
EMIF04-10006F2	FS

Figure 1: Pin Configuration (ball side)



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Figure 2: Basic Cell Configuration

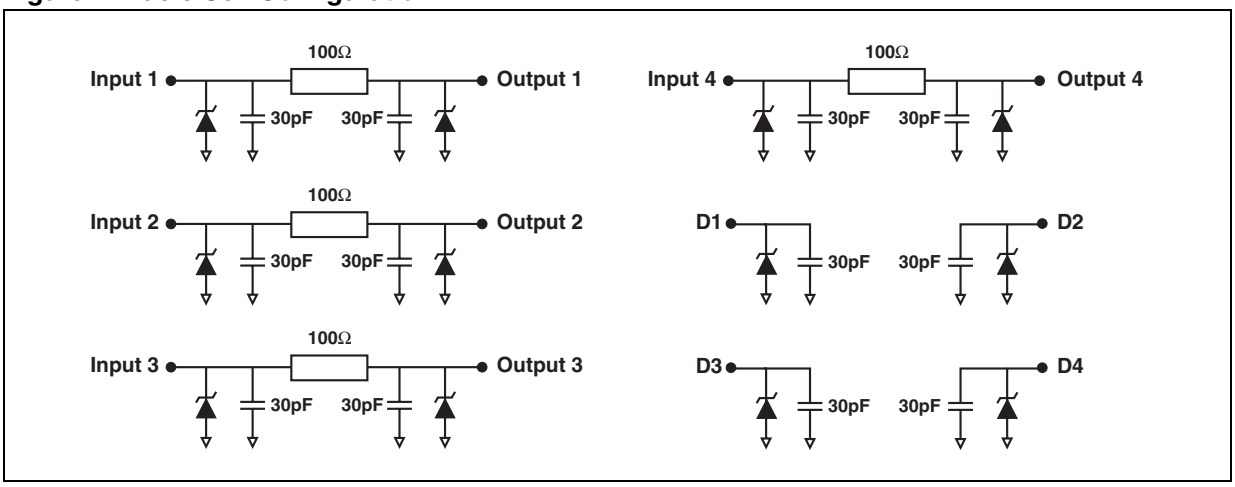
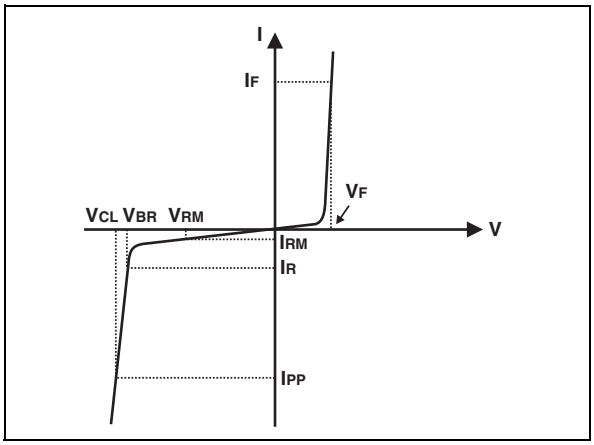


Table 2: Absolute Ratings (limiting values)

Symbol	Parameter and test conditions	Value	Unit
P_R	DC power per resistance	0.1	W
P_T	Total DC power per package	0.6	W
T_j	Maximum junction temperature	125	°C
T_{op}	Operating temperature range	- 40 to + 85	°C
T_{stg}	Storage temperature range	125	°C

Table 3: Electrical Characteristics (T_{amb} = 25 °C)

Symbol	Parameter
V_{BR}	Breakdown voltage
I_{RM}	Leakage current @ V_{RM}
V_{RM}	Stand-off voltage
V_{CL}	Clamping voltage
R_d	Dynamic impedance
I_{PP}	Peak pulse current
$R_{I/O}$	Series resistance between Input and output
C_{line}	Capacitance per line



Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	I_R = 1 mA	5.5	7	9	V
I_{RM}	V_{RM} = 3.3 V per line			500	nA
$R_{I/O}$	I = 10 mA	80	100	120	Ω
C_{line}	V_R = 2.5 V, F = 1 MHz, 30 mV (on filter cells)	50	60	70	pF

Figure 3: S21 (dB) attenuation measurements and Aplac simulation

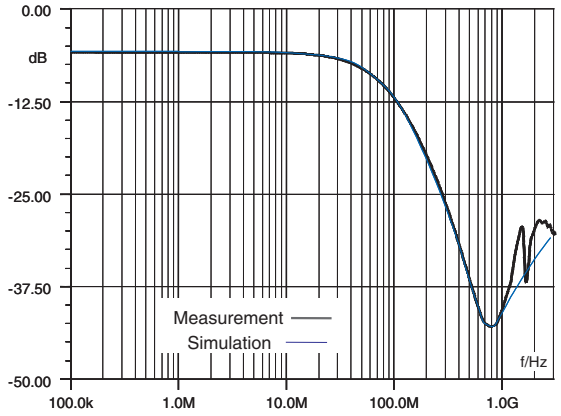


Figure 4: Analog crosstalk measurements

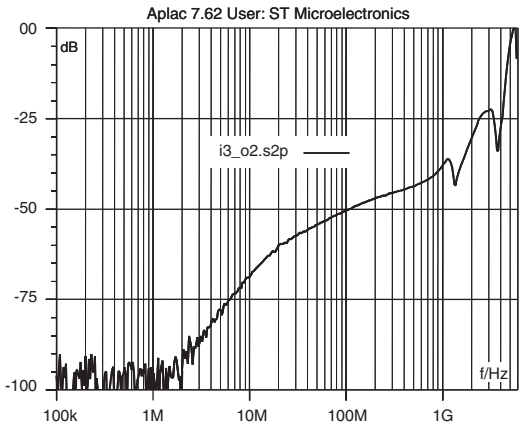


Figure 5: Digital crosstalk measurements

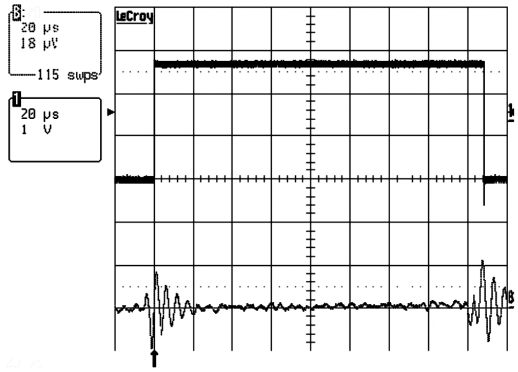


Figure 6: ESD response to IEC61000-4-2 (+15kV air discharge) on one imput V(in) and one output V(out)

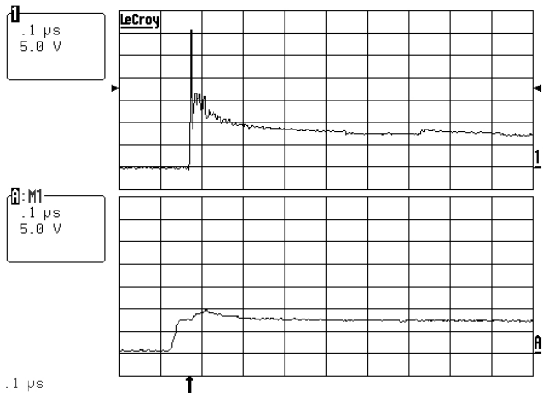


Figure 7: ESD response to IEC61000-4-2 (–15kV air discharge) on one imput V(in) and one output V(out)

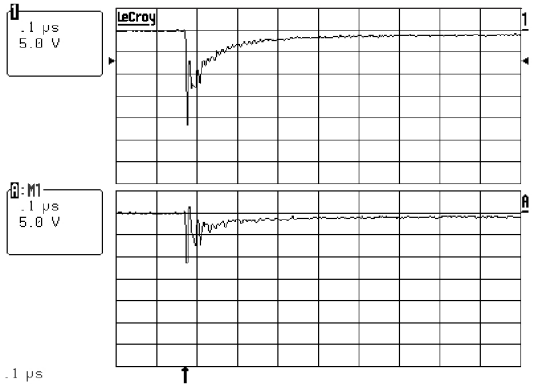


Figure 8: Line capacitance versus applied voltage for filter

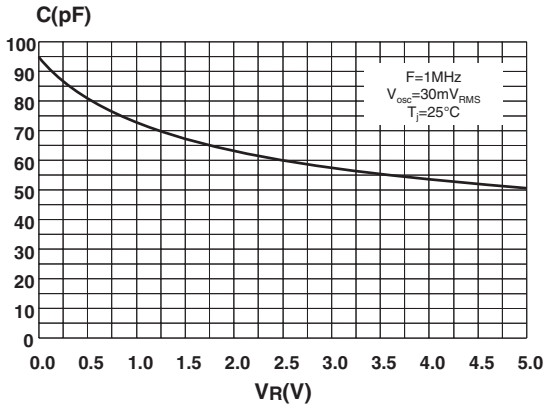


Figure 9: Aplac model

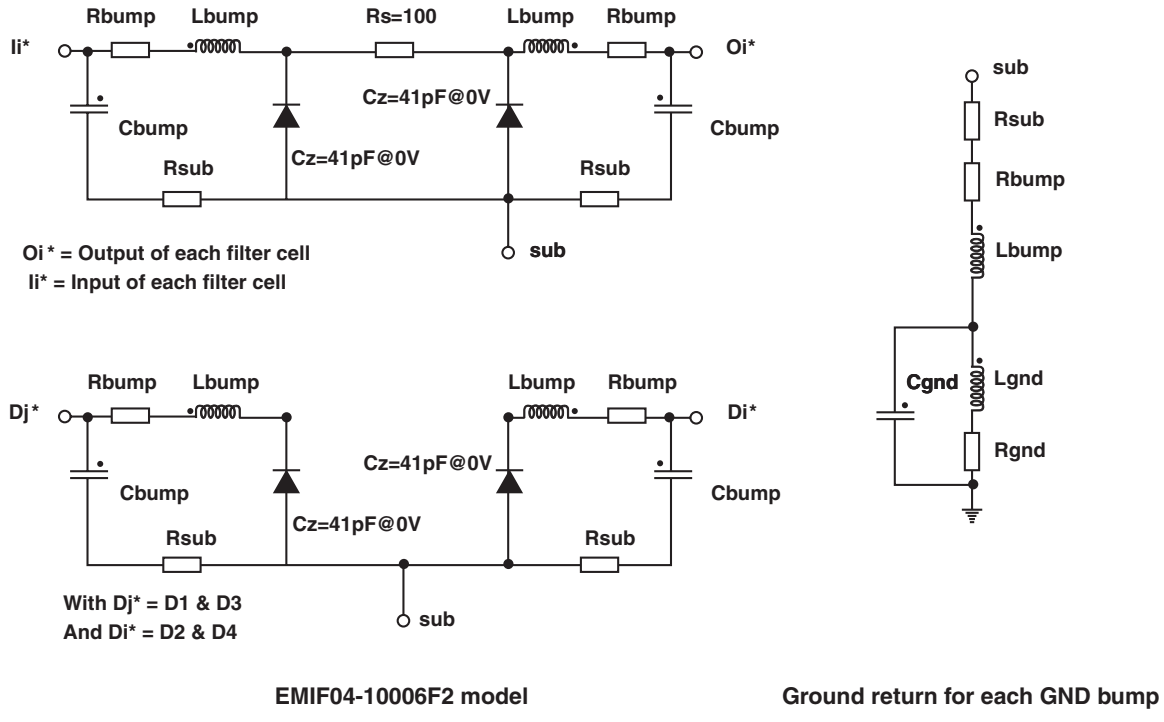


Figure 10: Aplac parameters

aplacvar RS	100Ω
aplacvar Cz	41 pF
aplacvar Lbump	50 pH
aplacvar Rbump	20 m
aplacvar Cbump	1.2 pF
aplacvar Rsub	100 m
aplacvar Rgnd	100 m
aplacvar Lgnd	100 pH
aplacvar Cgnd	0.15 pF

Figure 11: Order code

EMIF yy - xxx zz Fx

EMI Filter

Number of lines

Information
x = resistance value (Ohms)
z = capacitance value / 10(pF)
or
3 letters = application
2 digits = version

Package
F = Flip-Chip
x = 1: 500µm, Bump = 315µm
= 2: Leadfree Pitch = 500µm, Bump = 315µm

Figure 12: FLIP-CHIP Package Mechanical Data

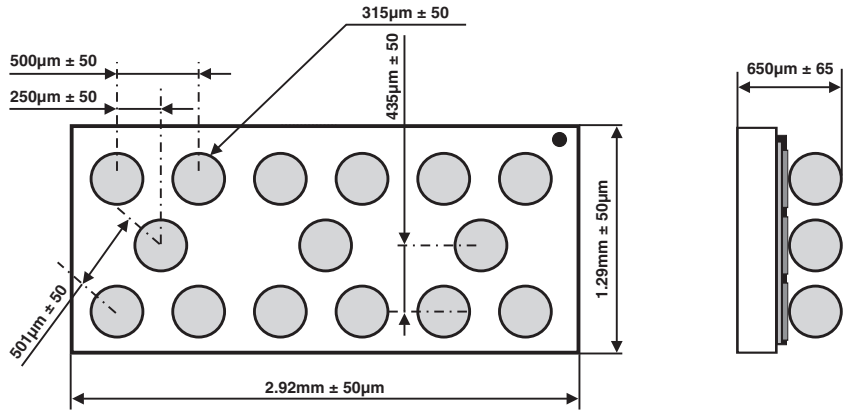


Figure 13: Foot print recommendations

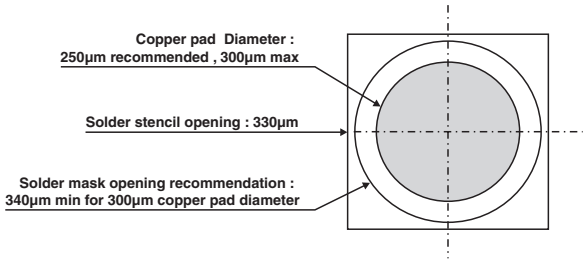


Figure 14: Marking

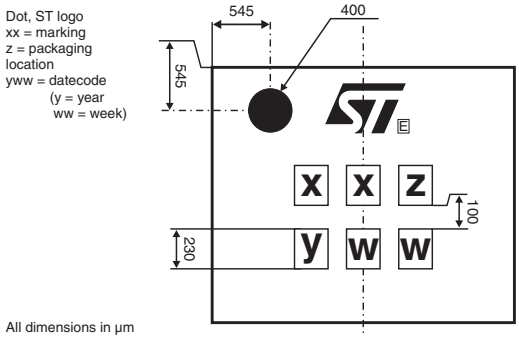


Figure 15: FLIP-CHIP Tape and Reel Specification

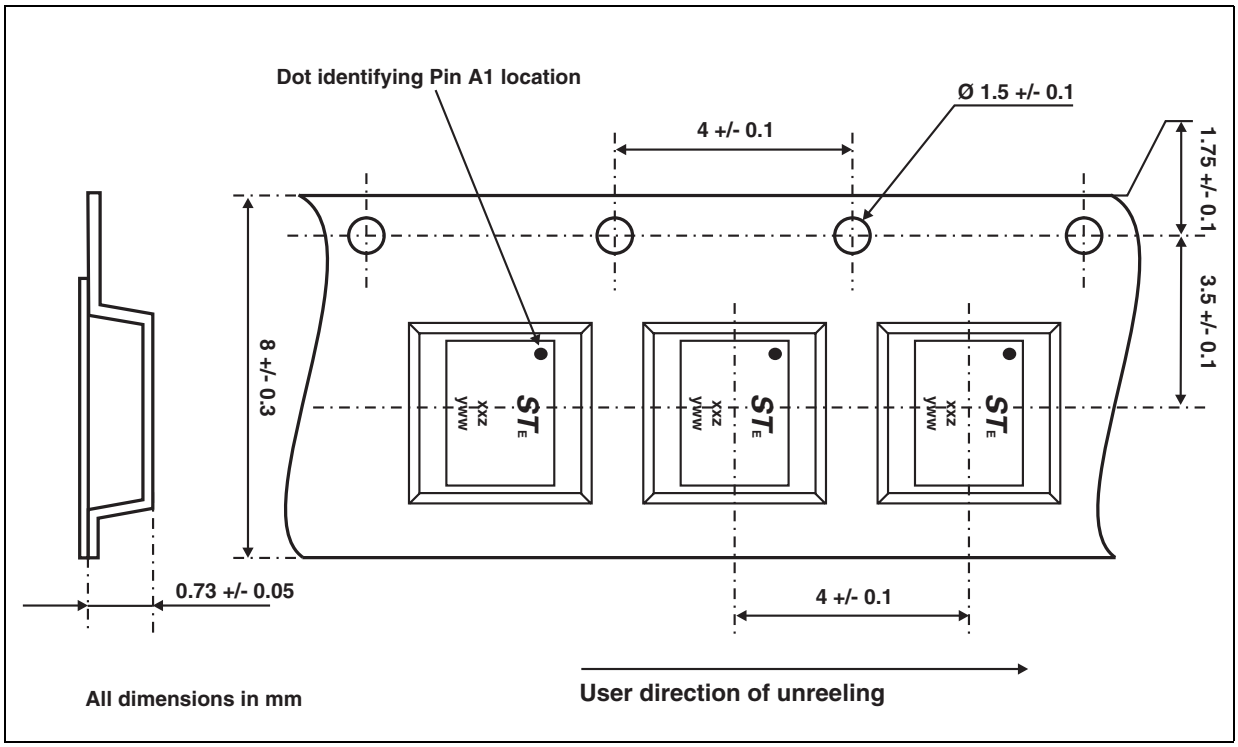


Table 4: Ordering Information

Ordering code	Marking	Package	Weight	Base qty	Delivery mode
EMIF04-10006F2	FS	Flip-Chip	5.4 mg	5000	Tape & reel 7”

Note: More packing informations are available in the application note
AN1235: “Flip-Chip: Package description and recommendations for use”
AN1751: "EMI Filters: Recommendations and measurements"

Table 5: Revision History

Date	Revision	Description of Changes
08-Sep-2004	1	First issue

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