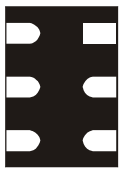
EMIF02-SPK01M6

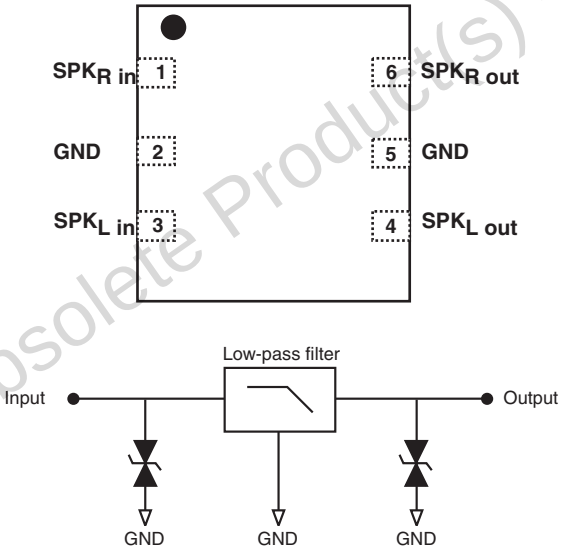
2-line IPAD™, EMI filter and ESD protection for speaker

Datasheet - production data



Micro QFN 6 leads
1.45 mm x 1.00 mm
(bottom view)

Figure 1. Pin configuration (top view) and basic cell configuration



Features

- EMI symmetrical (I/O) low-pass filter
- High efficiency in EMI filtering
- Very low PCB space consumption: 1.0 mm x 1.45 mm
- Pitch 0.5 mm
- Very thin package: 0.6 mm max
- High efficiency in ESD suppression
- High reliability offered by monolithic integration
- High reduction of parasitic elements through integration and wafer level packaging
- Lead-free package

Complies with following standards

- IEC 61000-4-2 level 4, input pins
  - 15 kV (air discharge)
  - 8 kV (contact discharge)
- IEC 61000-4-2 level 1, output pins
  - 2 kV (air discharge)
  - 2 kV (contact discharge)
- MILSTD883 Class 3B

Application

- Mobile telephones

Description

The EMIF02-SPK01M6 is a 2-line, highly integrated device designed to suppress EMI/RFI noise in all systems exposed to electromagnetic interference. This filter includes ESD protection circuitry, which prevents damage to the application when subjected to ESD surges up to 15 kV.

TM: IPAD is a trademark of STMicroelectronics

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This is information on a product in full production. www.st.com

1 Characteristics

Table 1. Absolute ratings (limiting values at T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Value	Unit
V_{PP}	ESD discharge IEC 61000-4-2 air discharge on input pins Air discharge Contact discharge ESD discharge IEC 61000-4-2 contact discharge on output pins Air discharge Contact discharge MILSTD883 Class 3B	 15 8 2 2 8	kV
T_j	Junction temperature	125	°C
T_{op}	Operating temperature range	-30 to +85	°C
T_{stg}	Storage temperature range	-55 to +150	°C

Figure 2. Electrical characteristics (definitions)

Symbol		Parameter
V_{BR}	=	Breakdown voltage
V_{CL}	=	Clamping voltage
I_{RM}	=	Leakage current @ V_{RM}
V_{RM}	=	Stand-off voltage
I_{PP}	=	Peak pulse current
I_R	=	Breakdown current

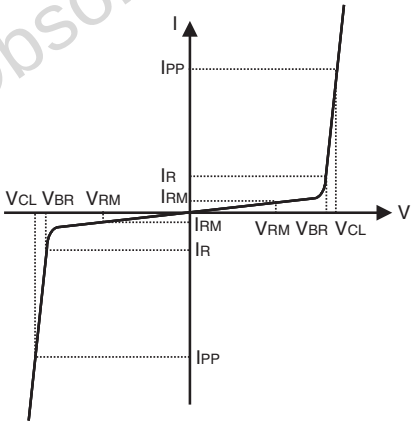

Table 2. Electrical characterisitcs (T_{amb} = 25 °C)

Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	I_R = 1 mA	6	8		V
I_{RM}	V_{RM} = 3 V per line			500	nA
$R_{I/O}$	Tolerance ± 20%		10		Ω
C_{line}	V_R= 0, F = 1 MHz, V_{OSC} = 30 mV, ±30%		220		pF

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Figure 3. Attenuation measurement

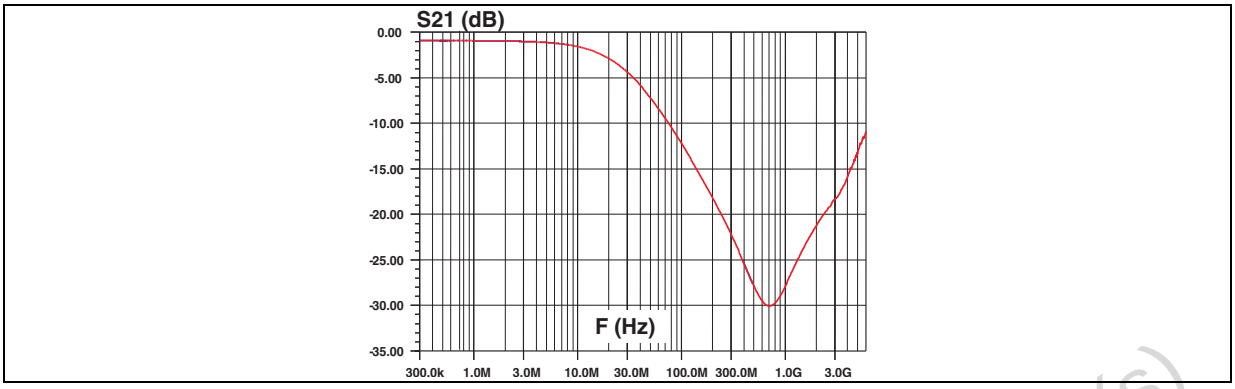


Figure 4. ESD response to IEC 61000-4-2 +15 kV air discharge on SPK R line

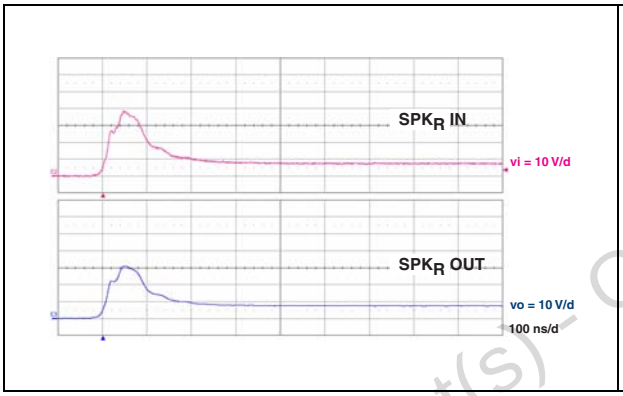


Figure 5. ESD response to IEC 61000-4-2 +15 kV air discharge on SPK L line

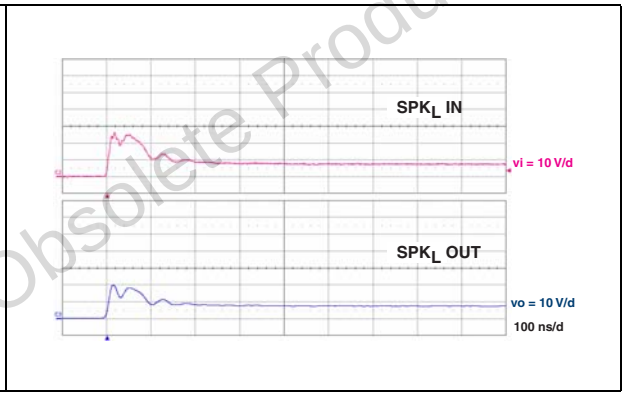


Figure 6. ESD response to IEC 61000-4-2 - 15 kV air discharge on SPK R line

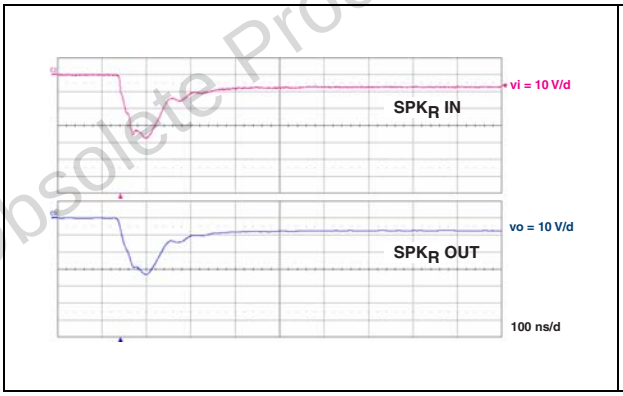
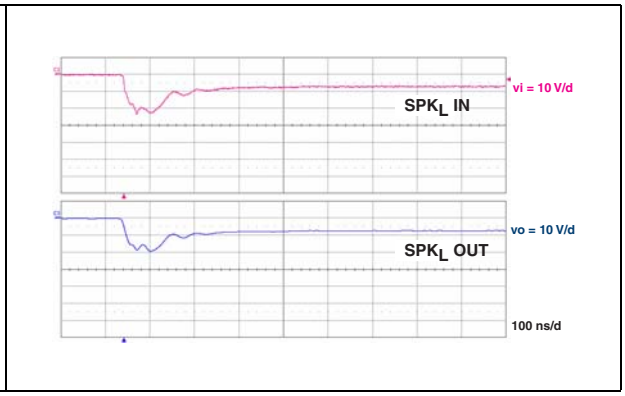


Figure 7. ESD response to IEC 61000-4-2 - 15 kV air discharge on SPK Lline



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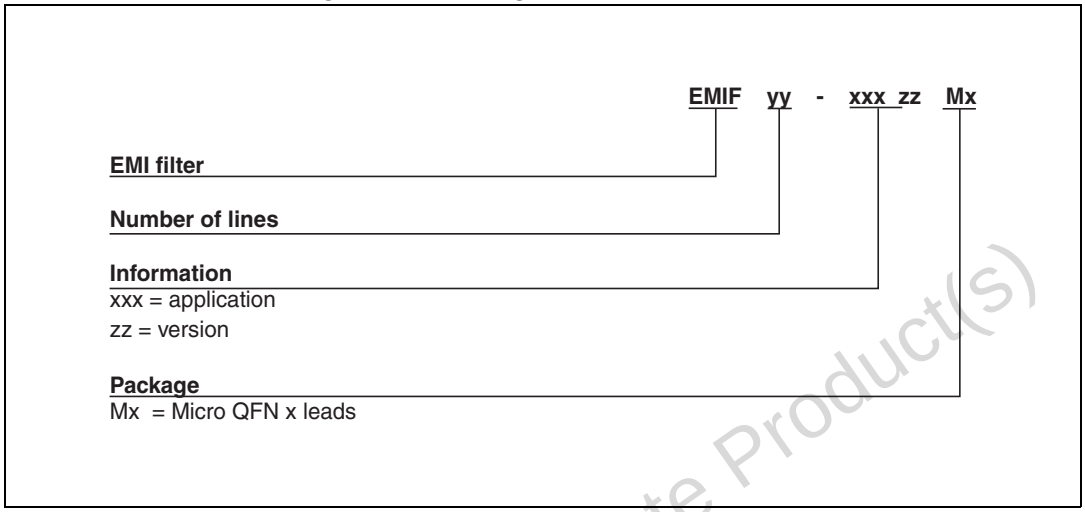
2 Ordering information scheme

Figure 8. Ordering information scheme



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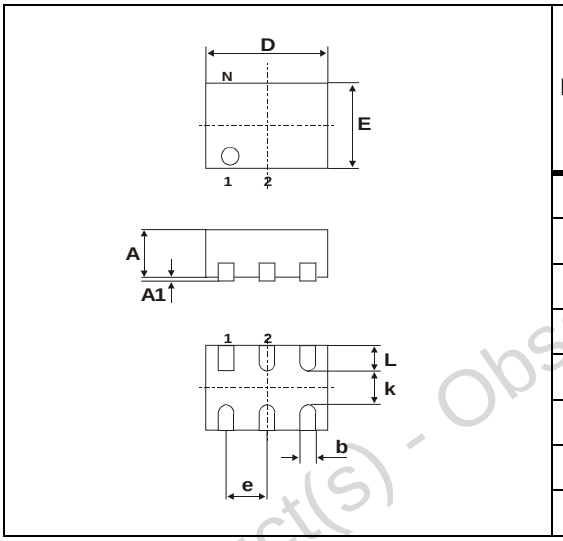
3 Package information

- Epoxy meets UL94, V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 3. Micro QFN 1.45 x 1.00 6L dimensions



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.18	0.25	0.30	0.007	0.010	0.012
D		1.45			0.057	
E		1.00			0.039	
e		0.50			0.020	
K	0.20			0.008		
L	0.30	0.35	0.40	0.012	0.014	0.016

Figure 9. Footprint in mm [inches]

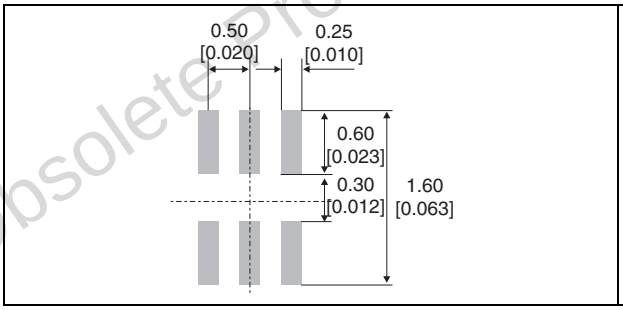


Figure 10. Marking

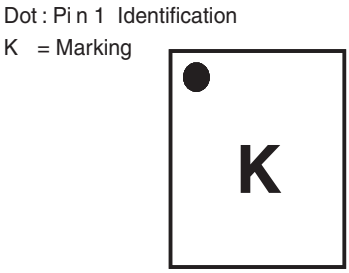


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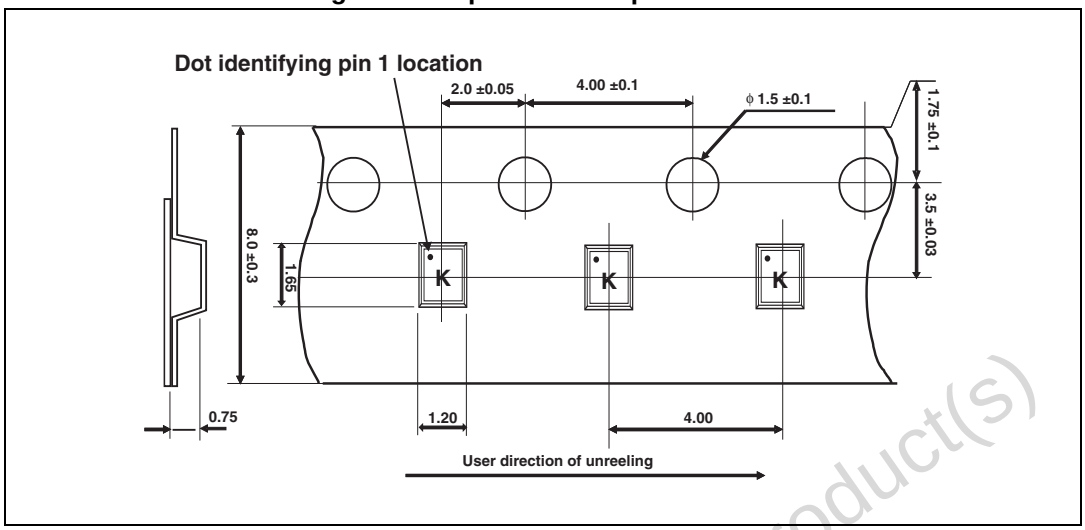
Figure 11. Tape and reel specification



Note: Product marking may be rotated by 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

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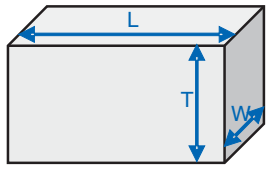
4 Recommendation on PCB assembly

4.1 Stencil opening design

1. General recommendation on stencil opening design
   a) Stencil Opening Dimensions: L (Length), W (Width), T (Thickness).

Figure 12. Stencil opening dimensions



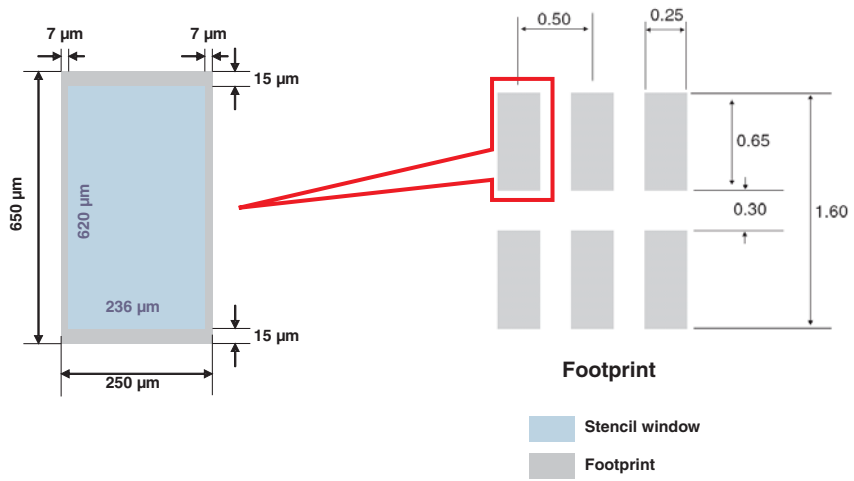
   b) General Design Rule
   Stencil thickness (T) = 75 ~ 125 µm

$$\text{Aspect Ratio} = \frac{W}{T} \geq 1.5$$

$$\text{Aspect Area} = \frac{L \times W}{2T(L+W)} \geq 0.66$$

2. Reference design
   a) Stencil opening thickness: 100 µm
   b) Stencil opening for leads: Opening to footprint ratio is 90%.

Figure 13. Recommended stencil window position



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4.2 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed
4. Solder paste with fine particles: powder particle size is 20-45 µm.

4.3 Placement

1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

4.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

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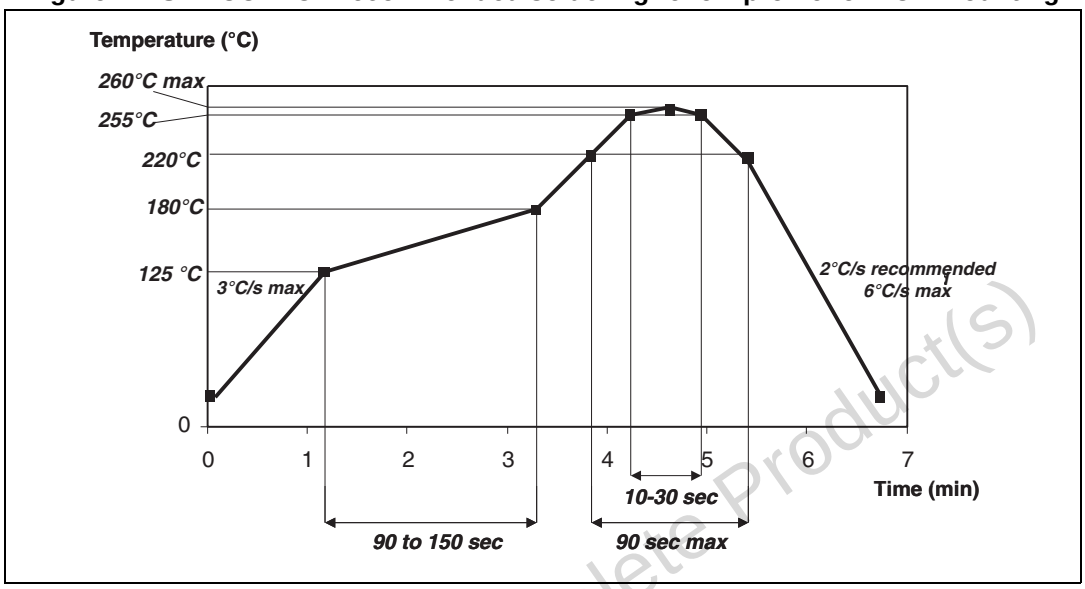
4.5 Reflow profile

Figure 14. ST ECOPACK recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

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5 Ordering information

Table 4. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
EMIF02-SPK01M6	K(1)	Micro QFN	2.2 mg	3000	Tape and reel (7”)

1. The marking can be rotated by 90° to diferentiate assembly location

6 Revision history

Table 5. Document revision history

Date	Revision	Changes
11-Sep-2009	1	Initial release
21-Sep-2009	2	Updated *Figure 2*.
14-Mar-2014	3	Minor text changes

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