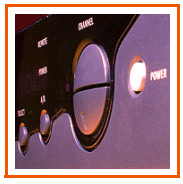
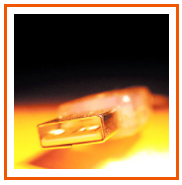
EMC6D103

Fan Control Device with High Frequency PWM Support and Hardware Monitoring Features

PRODUCT FEATURES

Datasheet

- 3.3 Volt Operation (5 Volt Tolerant Input Buffers)
- SMBus 2.0 Compliant Interface (Fixed, not Discoverable) with Three Slave Address Options
- Fan Control
  - PWM (Pulse width Modulation) Outputs (3)
  - Fan Tachometer Inputs (4)
  - Programmable automatic fan control based on temperature
  - Backwards compatible with fans requiring lower frequency PWM drive
  - High frequency fan support for 4 wire fans
  - One fan can be controlled from as many as 3 temperature zones
  - Fan ramp rate control for acoustic noise reduction
- Power Savings Modes
  - Two monitoring modes: continuous or cycling (for power savings)
  - Two low power modes when monitoring if off: Sleep and Shutdown
- Temperature Monitor
  - Monitoring of Two Remote Thermal Diodes (+/- 3 deg C accuracy)
  - Internal Ambient Temperature Measurement
  - Limit Comparison of all Monitored Values
  - Interrupt Pin for out-of-limit Temperature Indication
- Voltage Monitor
  - Monitor Power supplies (+2.5V, +5V, +12V, Vccp, and VCC)
  - Limit Comparison of all Monitored Values
  - Interrupt Pin for out-of-limit Voltage Indication
- 5 VID (Voltage Identification) Inputs
- XOR Tree Test Mode
- 24-Pin SSOP Package; green, lead-free package also available.

ORDER NUMBER(S):

EMC6D103-CK FOR 24 PIN SSOP PACKAGE

EMC6D103-CK-TR FOR 24 PIN SSOP PACKAGE (TAPE AND REEL)

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Evaluation Board is available.

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0.1 Reference Documents

- System Management Bus (SMBus) Specification, Version 2.0, dated August 3, 2000
- I^2C Bus Specification, version 2.0, Philips Semiconductors, Dec. 1998

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Chapter 1 General Description

The EMC6D103 is an environmental monitoring device with automatic fan control capability. This ACPI compliant device provides hardware monitoring for up to five voltages and three thermal zones, measures the speed of up to four fans, and controls the speed of multiple DC fans using Pulse Width Modulator (PWM) outputs. High frequency and low frequency PWMs are supported.

The EMC6D103 hardware monitor provides analog inputs for monitoring external voltages of +2.5V, +5V, +12V and Vccp. This device has the capability to monitor its own internal VCC power supply, which may be connected to either main power (VCC) or the suspend power well (VTR). In addition to monitoring the processor voltage, VID inputs are available to identify the voltage specification. External components are not required for voltage scaling or similar treatment.

The EMC6D103 hardware monitor includes support for monitoring three thermal zones: two external and one internal. The external temperatures are measured via thermal diode inputs capable of monitoring remote devices. In addition, they are equipped with an ambient temperature sensor for measuring the internal temperature.

Pulse Width Modulators (PWM) control the speed of the fans by varying the output duty cycle of the PWM. Each PWM can be associated with any or all of the thermal zones monitored. As the temperature of the associated zone varies, the PWM duty cycle is adjusted accordingly. The Ramp Rate Control feature controls the rate of change of the PWM output, thereby reducing system noise created by changing the fan speed. The speed of each fan is monitored by a Fan Tachometer input. The measured values are compared to values stored in Limit Registers to detect if a fan has stalled or seized.

Fan speed may be under host software control or automatic. In host control mode, the host software continuously monitors temperature and fan speed registers, makes decisions as to desired fan speed and sets the PWM's to drive the required fan speed. This device offers an interrupt output signal (INT#), which may be used to interrupt the host on out-of-limit temperature or voltage condition enabling an ACPI response as opposed to the host software continuously monitoring status. In auto "zone" mode, the logic continuously monitors the temperature and fan speeds and adjusts speeds without intervention from the host CPU. Fan speed is adjusted according to an algorithm using the temperature measured in the selected zone, the high and low limits set by the user, and the current fan speed.

The EMC6D103 supports two Monitoring modes: Continuous Mode and Cycle Mode. In the continuous monitoring mode, the sampling and conversion process is performed continuously for each voltage and temperature reading after monitoring is enabled. The time for each voltage and temperature reading varies depending on the measurement option. In cycle monitoring mode, the part completes all sampling and conversions, then waits approximately one second to repeat the process. It repeats the sampling and conversion process typically every 1.2 seconds (1.4 sec max - default averaging enabled). The sampling and conversion of each voltage and temperature reading is performed once every monitoring cycle. (This is a power saving mode.)

The EMC6D103 can be placed in one of two low-power modes: Sleep mode or Shutdown mode. These modes do not reset any of the registers of the device. In Sleep mode bias currents are on and the internal oscillator is on, but the the A/D converter and monitoring cycle are turned off. Serial bus communication is still possible with any register in the Hardware Monitor Block while in this low-power mode. In Shutdown mode the bias currents are off, the internal oscillator is off, and the the A/D converter and monitoring cycle are turned off. Serial communication is only possible with a select register.

Chapter 2 Pinout

This Environmental Monitoring and Control device (EMC) is offered in a 24 pin SSOP mechanical package.

2.1 EMC6D103 Pinout

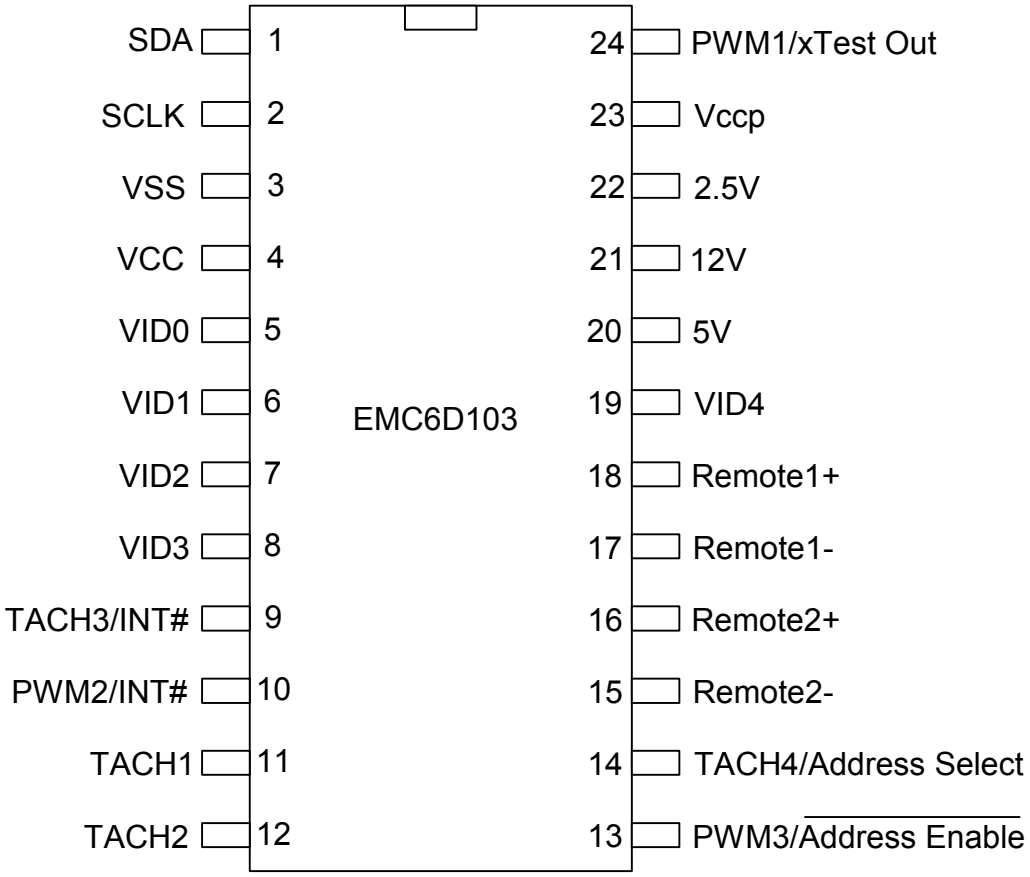


Figure 2.1 EMC6D103 24 Pin SSOP Pinout

Chapter 3 Pin Description

3.1 Pin Functions

Table 3.1 Pin Description

PIN #	NAME	FUNCTION	BUFFER TYPE	BUFFER REQUIREMENT PER FUNCTION (Note 3.1)	POWER WELL	NOTES
HARDWARE MONITORING BLOCK (24)						
1	SDA	System Management Bus bi-directional Data. Open Drain output.	I_MOD3	I_MOD3	VCC	
2	SCLK	System Management Bus Clock.	I_M	I_M	VCC	
5	VID0	Voltage ID 0 Input	I_M	I_M	VCC	
6	VID1	Voltage ID 1 Input	I_M	I_M	VCC	
7	VID2	Voltage ID 2 Input	I_M	I_M	VCC	
8	VID3	Voltage ID 3 Input	I_M	I_M	VCC	
19	VID4	Voltage ID 4 Input	I_M	I_M	VCC	
17	Remote1-	This is the negative Analog input (current sink) from the remote thermal diode. This serves as the negative input into the A/D. Digital Input.	I_{AN}	I_{AN}	VCC	
18	Remote1+	This is the positive input (current source) from the remote thermal diode. This serves as the positive input into the A/D.	I_{AN}	I_{AN}	VCC	
15	Remote2-	This is the negative Analog input (current sink) from the remote thermal diode. This serves as the negative input into the A/D. Digital Input.	I_{AN}	I_{AN}	VCC	
16	Remote2+	This is the positive input (current source) from the remote thermal diode. This serves as the positive input into the A/D.	I_{AN}	I_{AN}	VCC	
20	+5V_IN	Analog input for +5V	I_{AN}	I_{AN}	VCC	Note 3.2
22	+2.5V_IN	Analog input for +2.5V	I_{AN}	I_{AN}	VCC	Note 3.2
23	Vccp	Analog input for +Vccp (processor voltage: 0 to 3.0V).	I_{AN}	I_{AN}	VCC	Note 3.2
21	12V_IN	Analog input for +12V	I_{AN}	I_{AN}	VCC	Note 3.2

Table 3.1 Pin Description (continued)

PIN #	NAME	FUNCTION	BUFFER TYPE	BUFFER REQUIREMENT PER FUNCTION (Note 3.1)	POWER WELL	NOTES
HARDWARE MONITORING BLOCK (24)						
11	TACH1	Input for monitoring a fan tachometer input.	I_M	I_M	VCC	
12	TACH2	Input for monitoring a fan tachometer input.	I_M	I_M	VCC	
9	TACH3 /INT#	Input for monitoring a fan tachometer input. /Interrupt output to indicate a thermal and/or voltage event.	I_MOD3	I_M /OD3	VCC	
14	TACH4 /Address Select	Input for monitoring a fan tachometer input. If in Address Select Mode, determines the SMBus address of the device.	I_M	I_M	VCC	
24	PWM1 /xTest Out	PWM Output 1 controlling speed of fan. When in XOR tree test mode, functions as XOR Tree output.	O8	OD8/O8	VCC	
10	PWM2 /INT#	PWM Output 2 controlling speed of fan. /Interrupt output to indicate a thermal and/or voltage event.	OD8	OD8/OD8	VCC	
13	PWM3 /Address Enable#	PWM Output 3 controlling speed of fan. If pulled to ground at power on, enables Address Select Mode (Address Select pin controls SMBus address of the device).	IOD8	OD8/I	VCC	
4	VCC	Positive Power Supply. Nominal 3.3V. VCC is monitored by the Hardware Monitoring Block. (Can be powered by +3.3V Standby power if monitoring in low power states is required.)				
3	VSS	Analog Ground.				

Note: The “#” as the suffix of a signal name indicates an “Active Low” signal.

Note 3.1 Buffer types per function on multiplexed pins are separated by a slash “/”. Buffer types in parenthesis represent multiple buffer types for a single pin function.

Note 3.2 This analog input is backdrive protected.

3.2 Buffer Type Description

Note: The buffer type values are specified at VCC=3.3V

Table 3.2 Buffer Type Descriptions

BUFFER TYPE	DESCRIPTION
I_M	Digital Input
I_{AN}	Analog Input, Hardware Monitoring Block.
I_MOD3	Input/Output (Open Drain), 3mA sink.
O8	Output, 8mA sink, 4mA source.
OD8	Output (Open Drain), 8mA sink.
IO8	Input/Output, 8mA sink, 4mA source.

3.3 3.3V Operation, 5V Tolerance

The EMC6D103 is intended to operate with a nominal 3.3V power supply. The analog voltage pins are connected to voltage sources at their respective nominal levels. All digital signal pins are 3V switching, but are tolerant to 5V.

Chapter 4 Operational Description

4.1 Maximum Guaranteed Ratings

Operating Temperature Range . . . . . 0°C to +70°C

Storage Temperature Range . . . . . -55° to +150°C

Lead Temperature Range . . . . . Refer to JEDEC Spec. J-STD-020

Maximum V_{cc} 5.0V

Positive Voltage on any pin (except for analog inputs), with respect to Ground 5.5V

Negative Voltage on any pin (except for analog inputs), with respect to Ground. . . . . -0.3V

Positive Voltage on voltage analog inputs:

- Vccp_in 4.5V
- 2.5V_in 5.0V
- +5V_in. 8.0V
- 12V_in. 17V

Note: Stresses above those listed could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied. When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

4.2 Ratings for Operation

TA = 0°C - 70°C, VCC=+3.3V±10%

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
Temperature-to-Digital Converter Characteristics						
Internal Temperature Accuracy		-3 -2	±0.25	+3 +2	°C °C	0°C <= T_A <= 70°C 40°C <= T_A <= 70°C
External Diode Sensor Accuracy		-5 -3	±0.25	+5 +3	°C °C	-40°C <= T_S <= 125°C 40°C <= T_S <= 100°C

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
Analog-to-Digital Converter Characteristics						
Total Unadjusted Error	TUE			±2	%	Note 4.1
Differential Non-Linearity	DNL		±1		LSB	
Power Supply Sensitivity	PSS		±1		%/V	
Total Monitoring Cycle Time (Cycle Mode, Default Averaging)	$t_{C(Cycle)}$		1.22	1.4	sec	Note 4.2
Conversion Time (Continuous Mode, Default Averaging)	$t_{C(Cts)}$	203	223	248	msec	Note 4.3
Input Resistance			140	200	kΩ	
ADC Resolution						10 bits Note 4.6
Input Buffer (VID0-VID4,TACH1-TACH4)						
Low Input Level	V_{ILI}			0.8	V	
High Input Level	V_{IHI}	2.0		Vcc+0.3	V	
IOD Type Buffer (SCL, SDA, PWM1, PWM2, PWM3/ADDRESS ENABLE, INT#						
Low Input Level	V_{ILI}			0.8	V	
High Input Level	V_{IHI}	2.0		Vcc+0.3	V	
Hysteresis	V_{HYS}		500		mV	
Low Output Level	V_{OL}			0.4	V	I_{OL} = +4.0 mA (Note 4.5)
Leakage Current (ALL - Digital)						(Note 4.4)
Input High Current	$ILEAK_{IH}$			10	µA	$V_{IN} = V_{CC}$
Input Low Current	$ILEAK_{IL}$			-10	µA	V_{IN} = 0V
Digital Input Capacitance	C_{IN}			10	pF	
V_{CC} Supply Current						All outputs open, all inputs transitioning from/to 0V to/from 3.3V.
Active Mode	I_{CC}			3	mA	
Sleep Mode	I_{CC}			500	µA	
Shutdown Mode	I_{CC}			3	µA	

Notes:

- Voltages are measured from the local ground potential, unless otherwise specified.
- Typical values are at TA=25°C and represent most likely parametric norm.

- Timing specifications are tested at the TTL logic levels, VIL=0.4V for a falling edge and VIH=2.4V for a rising edge. TRI-STATE output voltage is forced to 1.4V.

Note 4.1 TUE (Total Unadjusted Error) includes Offset, Gain and Linearity errors of the ADC.

Note 4.2 Total Monitoring Cycle Time for cycle mode includes a one second delay plus all temperature conversions and all analog input voltage conversions.

Note 4.3 See Table 6.2, “Conversion Cycle Timing,” on page 24 for conversion cycle timing for all averaging options. Only the nominal default case is shown in this section.

Note 4.4 All leakage currents are measured with all pins in high impedance.

Note 4.5 The low output level for PWM pins is actually +8.0mA.

Note 4.6 The h/w monitor analog block implements a 10-bit ADC. The output of this ADC goes to an averager block, which can be configured to accumulate the averaged value of the analog inputs. The amount of averaging is programmable. The output of the averaging block produces a 12-bit temperature or voltage reading value. The 8 MSbits go to the reading register and the 4 LSbits to the A/D LSb register.

Chapter 5 SMBus Interface

The host processor communicates with the Fan Monitoring device through a series of read/write registers via the SMBus interface. SMBus is a serial communication protocol between a computer host and its peripheral devices.

5.1 Slave Address

The default Slave Address is 0101110b. If this address is desired, the designer should not ground the Address Enable# pin and should not apply a strapping resistor to the Address Select pin.

If multiple devices are implemented in a system or another SMBus device requires address 0101110b, TACH4 and PWM3 must be disabled. In this case, addressing is implemented as follows:

The board designer will apply a 10KΩ pull-down resistor to ground on the Address Enable# pin. Upon power up, the EMC6D103 device will be placed into Address Enable mode and assign itself an SMBus address according to the Address Select input. The device will latch the address during the first valid SMBus transaction in which the first five bits of the targeted address match those of the EMC6D103 address. This feature eliminates the possibility of a glitch on the SMBus interfering with address selection.

Table 5.1 SMBus Slave Address Options

ADDRESS ENABLE#	ADDRESS SELECT	BOARD IMPLEMENTATION	SMBUS ADDRESS [7:1]
1	X	Address Enable# pulled to VCC through resistor **Note:** Resistor value will be dependent on PWM circuit implemented.	0101 110b (default)
0	0	Address Enable# pulled to ground through 10kΩ resistor Address Select Pulled to ground through a 10kΩ resistor	0101 100b
0	1	Address Enable# pulled to ground through 10kΩ resistor Address Select pulled to VCC through a 10kΩ resistor	0101 101b

In this way, there can be up to three EMC6D103 devices on the SMBus at any time. Multiple EMC6D103 devices can be used to monitor additional processors and temperature zones.

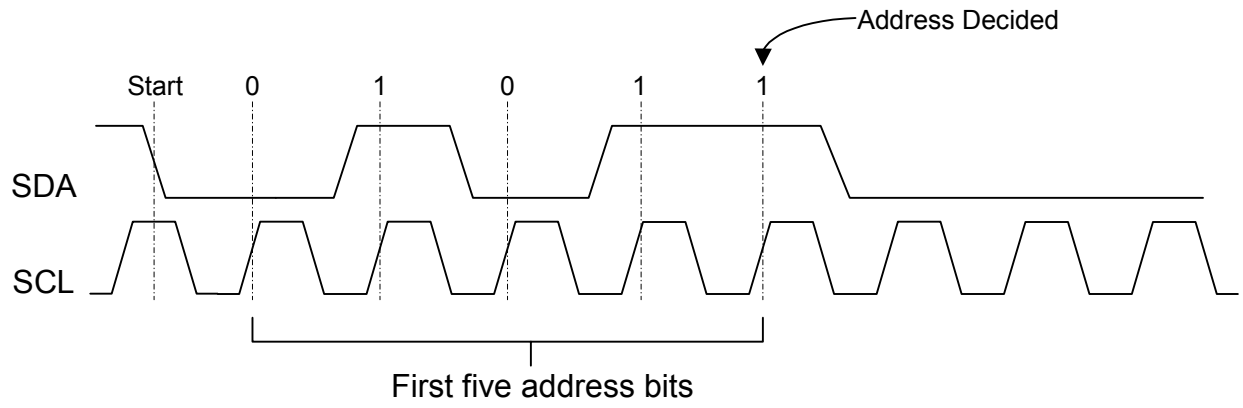


Figure 5.1 Address Selection on EMC6D103

5.2 Slave Bus Interface

The EMC6D103 device SMBus implementation is a subset of the SMBus interface to the host. The device is a *slave-only* SMBus device. The implementation in the device is a subset of SMBus since it only supports Write Byte and Read Byte protocols.

The Write Byte and Read Byte protocols are valid SMBus protocols for the device. This part responds to other protocols as described in the Invalid Protocol Section. Reference the System Management Bus Specification, Rev 2.0.

The SMBus interface is used to read and write the registers in the device. The register set is shown in Chapter 8, "Register Set," on page 49.

5.3 Bus Protocols

Typical Write Byte and Read Byte protocols are shown below. Register accesses are performed using 7-bit slave addressing, an 8-bit register address field, and an 8-bit data field. The shading indicates the Hardware Monitor Block driving data on the SDA line; otherwise, host data is on the SDA line.

The slave address is the unique SMBus Interface Address for the Hardware Monitor Block that identifies it on SMBus. The register address field is the internal address of the register to be accessed. The register data field is the data that the host is attempting to write to the register or the contents of the register that the host is attempting to read.

Note: Data bytes are transferred MSB first.

Byte Protocols

A write byte transfer will always consist of the SMBus Interface Address byte, followed by the Internal Address Register byte, then the data byte.

The normal read protocol consists of a write to the Hardware Monitor Block with the SMBus Interface Address byte, followed by the Internal Address Register byte. Then restart the Serial Communication with a Read consisting of the SMBus Interface Address byte, followed by the data byte read from the Hardware Monitor Block. This can be accomplished by using the Read Byte protocol.

Write Byte

The Write Byte protocol is used to write data to the registers. The data will only be written if the protocol shown in Table 5.2 is performed correctly. Only one byte is transferred at time for a Write Byte protocol.

Table 5.2 SMBus Write Byte Protocol

FIELD	START	SLAVE ADDR	WR	ACK	REG. ADDR	ACK	REG. DATA	ACK	STOP
Bits	1	7	1	1	8	1	8	1	1

Read Byte

The Read Byte protocol is used to read data from the registers. The data will only be read if the protocol shown in Table 5.3 is performed correctly. Only one byte is transferred at time for a Read Byte protocol.

Table 5.3 SMBus Read Byte Protocol

FIELD:	START	SLAVE ADDR	WR	ACK	REG. ADDR	ACK	START	SLAVE ADDR	RD	ACK	REG. DATA	NACK	STOP
Bits:	1	7	1	1	8	1	1	7	1	1	8	1	1

5.4 Invalid Protocol Response Behavior

Registers that are accessed with an invalid protocol will not be updated. A register will only be updated following a valid protocol. The only valid protocols are the Write Byte and Read Byte protocols, which are described above.

The EMC6D103 device responds to three SMBus slave addresses:

1. The SMBus slave address that supports the valid protocols defined in the previous sections is determined by the level on the Address Select and Address Enable pins as shown in Section 5.1, "Slave Address," on page 18.
2. SMBus Alert Response (0001 100). The SMBus will only respond to the SMBus Alert Response Address if the SMBus Alert Response interrupt was generated to request a response from the Host. The SMBus Alert Response is defined in Section 5.10, "SMBus Alert Response Address," on page 21.

Attempting to communicate with the Hardware Monitor Block over SMBus with an invalid slave address, or invalid protocol will result in no response, and the SMBus Slave Interface will return to the idle state.

The only valid registers that are accessible by the SMBus slave address are the registers defined in the Registers Section. See Section 5.4.1, "Undefined Registers" for response to undefined registers.

5.4.1 Undefined Registers

Reads to undefined registers return 00h. Writes to undefined registers have no effect and return no error.

5.5 General Call Address Response

The EMC6D103 will not respond to a general call address of 0000_000.

5.6 Slave Device Time-Out

The EMC6D103 supports the slave device timeout as per the SMBus Specification, v2.0.

According to SMBus specification, v2.0 devices in a transfer can abort the transfer in progress and release the bus when any single clock low interval exceeds 25ms ($T_{TIMEOUT, MIN}$). Devices that have detected this condition must reset their communication and be able to receive a new START condition no later than 35ms ($T_{TIMEOUT, MAX}$).

Note: Some simple devices do not contain a clock low drive circuit; this simple kind of device typically may reset its communications port after a start or stop condition

5.7 Stretching the SCLK Signal

The EMC6D103 supports stretching of the SCLK by other devices on the SMBus. The Hardware Monitor Block does not stretch the SCLK.

5.8 SMBus Timing

The SMBus Slave Interface complies with the SMBus AC Timing Specification. See the SMBus timing diagram shown in the section titled Section 9.2, "SMBus Interface," on page 84.

5.9 Bus Reset Sequence

The SMBus Slave Interface will reset and return to the idle state upon a START field followed immediately by a STOP field.

5.10 SMBus Alert Response Address

The EMC6D103 device responds to the SMBus Alert Response Address, 0001 100, if the INTEN bit (register 7Ch bit 2) is set and one or more status events bits are high. The interrupt signal (INT#), which can be enabled on either the PWM2 or TACH3 pins, can be used as the SMBALERT#. See the section describing the Interrupt Status Registers on page 26 and the section describing the Interrupt Pin on page 28 for more details on interrupts.

The device can signal the host that it wants to talk by pulling the SMBALERT# low, if a status bit is set in one of the interrupt status registers and properly enabled onto the INT# pin. The host processes the interrupt and simultaneously accesses all SMBALERT# devices through a modified Receive Byte operation with the Alert Response Address (ARA).

The EMC6D103 device, which pulled SMBALERT# low, will acknowledge the Alert Response Address and respond with its device address. The 7-bit device address provided by the EMC6D103 device is placed in the 7 most significant bits of the byte. The eighth bit can be a zero or one.

Table 5.4 Modified SMBus Receive Byte Protocol Response to ARA

FIELD:	START	ALERT RESPONSE ADDRESS	RD	ACK	EMC6D103 SLAVE ADDRESS	NACK	STOP
Bits:	1	7	1	1	8	1	1

After acknowledging the slave address, the EMC6D103 device will disengage the SMBALERT# pull-down by clearing the INT enable bit. If the condition that caused the interrupt remains, the Fan Control device will reassert the SMBALERT# on the next monitoring cycle, provided the INT enable bit has been set back to ‘1’ by software.

Note: The INT# signal is an alternate function on the PWM2 and TACH3 pins. The EMC6D103 device will respond to the SMBus Alert Response address even if the INT# signal is not selected as the alternate function on one of these pins as long as the following conditions exist: the INTEN

bit (register 7Ch bit 2) is set, an individual status bit is set in one of the interrupt status registers, and the corresponding group enable bit is set. Each interrupt event must be enabled into the interrupt status registers, and the status bits must be enabled onto the INT# signal via the group enable bits for each type of event (i.e., temperature, voltage and fan). See the section titled Interrupt Status Registers on page 26.

Chapter 6 Hardware Monitoring

The following sub-sections describe the EMC6D103 Hardware Monitoring features.

6.1 Input Monitoring

The EMC6D103 device's monitoring function is started by writing a '1' to the START bit in the **Ready/Lock/Start** Register (0x40). Measured values from the analog inputs and temperature sensors are stored in Reading Registers. The values in the reading registers can be accessed via the SMBus interface. These values are compared to the programmed limits in the Limit Register. The out-of-limit and diode fault conditions are stored in the Interrupt Status Registers.

6.2 Resetting the EMC6D103

6.2.1 Power-On Reset

All the registers in the Hardware Monitor Block, except the reading registers, reset to a default value when power is applied to the block. The default state of the register is shown in the table in the Register Summary subsection. The default state of Reading Registers are not shown because these registers have indeterminate power on values.

Note: Usually the first action after power up is to write limits into the Limit Registers.

6.2.2 Soft Reset (Initialization)

Setting bit 7 of the CONF register performs a soft reset. This bit is self-clearing. Soft Reset performs reset on all the registers except the Reading Registers.

6.3 Monitoring Modes

The Hardware Monitor Block supports two Monitoring modes: Continuous Mode and Cycle Mode. These modes are selected using bit 1 of the Special Function Register (7Ch). The following subsections contain a description of these monitoring modes.

The hardware monitor conversion clock is 45KHz ± 10%. Temperature conversions take 96 clocks, each (2.133ms nom.); voltage conversions take 68 clocks, each (1.511ms nom). The time to complete a conversion cycle depends upon the number of inputs in the conversion sequence to be measured (see Table 6.3, "ADC Conversion Sequence," on page 25) and the amount of averaging per input, which is selected using the AVG[2:0] bits in the Special Function register (see Register 7Ch: Special Function Register on page 73).

For each mode, there are four options for the number of measurements that are averaged for each temperature and voltage reading. These options are selected using bits[7:5] of the Special Function register (7Ch). These bits are defined as follows:

Bits [7:5] AVG[2:0]

The AVG[2:0] bits determine the amount of averaging for each of the measurements that are performed by the hardware monitor before the reading registers are updated (Table 6.1). The AVG[2:0] bits are priority encoded where the most significant bit has highest priority. For example, when the AVG2 bit is asserted, 32 averages will be performed for each measurement before the reading registers are updated regardless of the state of the AVG[1:0] bits.

Table 6.1 AVG[2:0] Bit Decoder

SFTR[7:5]			MEASUREMENTS PER READING			
AVG2	AVG1	AVG0	REMOTE DIODE 1	REMOTE DIODE 2	INTERNAL DIODE	ALL VOLTAGE READINGS (+2.5V, +5V, +12V, VCCP, AND VCC)
0	0	0	128	128	8	8
0	0	1	16	16	1	1
0	1	X	16	16	16	16
1	X	X	32	32	32	32

Note: The default for the AVG[2:0] bits is '010'b.

To calculate conversion cycle timing for a given averaging mode:

- Compute total number of temperature conversions (TEMP_CONV)
- Compute total number of voltage conversions (VOLT_CONV)
- Calculate Time to complete all conversions is:

Total Conversion Time = (TEMP_CONV)*96/(45kHz +/-10%)+ (VOLT_CONV)*68/(45kHz +/-10%)

Example: To calculate the nominal conversion time FOR AVG[2:0] = 001b.

Total Conversion Time = (TEMP_CONV)*96/(45kHz)+ (VOLT_CONV)*68/(45kHz)

Total Conversion Time = (16+16+1)*96/(45kHz)+ (5*1)*68/(45kHz)

Total Conversion Time = (33)*2.133ms+ (5)*1.511ms = ~78ms

Table 6.2 illustrates the min., nom., and max. conversion cycle timing for each of the four averaging modes.

Table 6.2 Conversion Cycle Timing

AVG[2:0]	TOTAL TEMPERATURE CONVERSIONS	TOTAL VOLTAGE CONVERSIONS	CONVERSION CYCLE TIME (MSEC)		
			MIN.	NOM.	MAX.
000	(2x128)+(1x8)=264	5x8=40	567	624	693
001	(2x16)+(1x1)=33	5x1=5	71	78	87
01X (default)	3x16=48	5x16=80	203	223	248
1XX	3x32=96	5x32=160	406	447	496

Note 6.1 The hardware monitor conversion clock is 45KHz ± 10%.

Note 6.2 Temperature conversions take 96 clocks, each (2.133ms nom.); Voltage conversions take 68 clocks, each (1.511ms nom).

6.3.1 Continuous Monitoring Mode

In the continuous monitoring mode, the sampling and conversion process is performed continuously for each voltage and temperature reading after the Start bit is set high. The time for each voltage and temperature reading is shown above for each measurement option.

The continuous monitoring function is started by doing a write to the Ready/Lock/Start Register, setting the Start bit (Bit 0) high. The part then performs a “round robin” sampling of the inputs, in the order shown below (see Table 6.3). Sampling of all values occurs in a nominal 223 ms (default - see Table 6.2, “Conversion Cycle Timing,” on page 24).

Table 6.3 ADC Conversion Sequence

SAMPLING ORDER	REGISTER
1	Remote Diode Temp Reading 1
2	Ambient Temperature reading
3	VCC reading
4	+12V reading
5	+5V reading
6	+2.5V reading
7	Vccp (processor) reading
8	Remote Diode Temp Reading 2

When the continuous monitoring function is started, it cycles through each measurement in sequence, and it continuously loops through the sequence approximately once every 223 ms (default - see Table 6.2, “Conversion Cycle Timing,” on page 24). Each measured value is compared to values stored in the Limit registers. When the measured value violates the programmed limit the Hardware Monitor Block will set a corresponding status bit in the Interrupt Status Registers.

If auto fan option is selected, the hardware will adjust the operation of the fans accordingly. See Auto Fan Control Operating Mode on page 35.

The results of the sampling and conversions can be found in the Reading Registers and are available at any time.

6.3.2 Cycle Monitoring Mode

In cycle monitoring mode, the part completes all sampling and conversions, then waits approximately one second to repeat the process. It repeats the sampling and conversion process typically every 1.2 seconds (1.4 sec max - default averaging enabled). The sampling and conversion of each voltage and temperature reading is performed once every monitoring cycle. This is a power saving mode.

The cycle monitoring function is started by doing a write to the Ready/Lock/Start Register, setting the Start bit (Bit 0) high. The part then performs a “round robin” sampling of the inputs, in the order shown above.

When the cycle monitoring function is started, it cycles through each measurement in sequence, and it produces a converted voltage and temperature reading for each input. The state machine waits approximately one second before repeating this process. Each measured value is compared to values stored in the Limit registers. When the measured value violates (or is equal to) the programmed limit the Hardware Monitor Block will set a corresponding status bit in the Interrupt Status Registers.

If auto fan option is selected, the hardware will adjust the operation of the fans accordingly. See the section titled Auto Fan Control Operating Mode on page 35.

The results of each sampling and conversion can be found in the Reading Registers and are available at any time, however, they are only updated once per conversion cycle.

6.4 Interrupt Status Registers

The Hardware Monitor Block contains two interrupt status registers: Register 41h: Interrupt Status Register 1 on page 60 and on page 61. These registers are used to reflect the state of all temperature, voltage and fan violation of limit error conditions and diode fault conditions that the Hardware Monitor Block monitors.

When an error occurs during the conversion cycle, its corresponding bit is set in its respective interrupt status register. The bit remains set until the register is read by software, at which time the bit will be cleared to '0' if the associated error event no longer violates the limit conditions or if the diode fault condition no longer exists. Reading the register will not cause a bit to be cleared if the source of the status bit remains active.

These registers are read only – a write to these registers have no effect. These registers default to 0x00 on VCC POR and Initialization.

See the description of the Interrupt Status registers in Chapter 8, "Register Set," on page 49.

Each interrupt status bit has a corresponding bit located in an interrupt enable register, which may be used to enable/disable the individual event from setting the status bit. See the following figure for the status and enable bits used to control the interrupt bits and INT# pin.

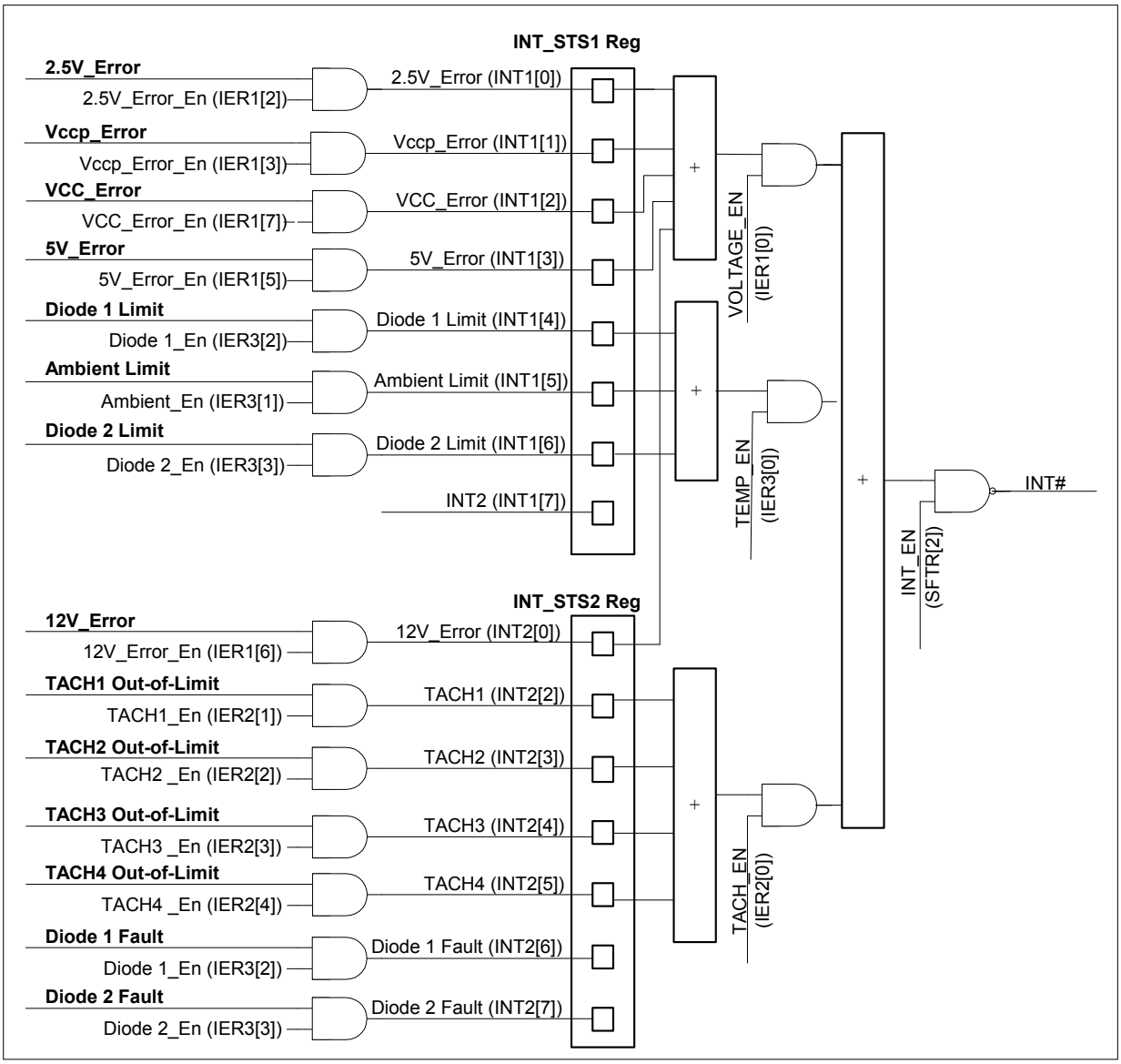


Figure 6.1 Interrupt Control

Note: The diode fault bits are not mapped directly to the INT# pin. A diode fault condition forces the diode reading register to a value of 80h, which will generate a Diode Error condition. See section Diode Fault on page 27.

6.4.1 Diode Fault

The EMC6D103 Chip automatically sets the associated diode fault bit to 1 when any of the following conditions occur on the Remote Diode pins:

- The positive and negative terminal are an open circuit.
- Positive terminal is connected to VCC
- Positive terminal is connected to ground
- Negative terminal is connected to VCC
- Negative terminal is connected to ground

The occurrence of a fault will cause 80h to be loaded into the associated reading register, except for the case when the negative terminal is connected to ground. A temperature reading of 80h will cause the corresponding diode error bit to be set. This will cause the INT# pin to become active if the individual, group (TEMP), and global enable (INTEN) bits are set.

Notes:

- The individual remote diode enable bits and the TEMP bit are located in on page 75. The INTEN bit is located in bit[2] of Register 7Ch: Special Function Register on page 73.
- When 80h is loaded into the Remote Diode Reading Register the PWM output(s) controlled by the zone associated with that diode input will be forced to full on. See Thermal Zones on page 32.

If the diode is disabled, the fault bit in the interrupt status register will not be set. In this case, the occurrence of a fault will cause 00h to be loaded into the associated reading register. The limits must be programmed accordingly to prevent unwanted fan speed changes based on this temperature reading. If the diode is disabled and a fault condition does not exist on the diode pins, then the associated reading register will contain a “valid” reading.

6.5 Interrupt Pin

The INT# function is used as an interrupt output for out-of-limit temperature, voltage events, and/or fan errors.

- The INT# signal can be enabled onto the PWM2 or the TACH3 pins.

  To configure the PWM2/INT# pin for the interrupt function, set bit[1] P2INT of the CONF register (7Fh) to ‘1’

  To configure the TACH3/INT# pin for the interrupt function, set bit[0] T3INT of the CONF register (7Fh) to ‘1’
- To enable the interrupt pin to go active, set bit 2 of the Special Function Register (7Ch) to ‘1’.

To enable temperature event, voltage events and/or fan events onto the INT# pin:

- To enable out-of-limit temperature events set bit[0] of the Interrupt Enable 3 (TEMP) register (82h) to ‘1’.
- To enable out-of-limit voltage events set bit[0] of the Interrupt Enable 1(VOLT) register (7Eh) to ‘1’
- To enable Fan tachometer error events set bit[0] of the Interrupt Enable 2(Fan Tachs) register (80h) to ‘1’.

See Figure 6.1 on page 27. The following description assumes that the interrupt enable bits for all events are set to enable the interrupt status bits to be set.

If the internal or remote temperature reading violates the low or high temperature limits, INT# will be forced active low (if all the corresponding enable bits are set: individual enable bits (D1_EN, D2_EN, and/or AMB_EN), group enable bit (TEMP_EN) and the global enable bit (INTEN)). This pin will remain low while the Internal Temp Error bit or one or both of the Remote Temp Error bits in Interrupt Status 1 Register is set and the enable bit is set.

The INT# pin will not become active low as a result of the remote diode fault bits becoming set. However, the occurrence of a fault will cause 80h to be loaded into the associated reading register, which will cause the corresponding diode error bit to be set. This will cause the INT# pin to become active if enabled.

The INT# pin can be enabled to indicate out-of-limit voltages. Bit[0] of the Interrupt Enable 1(VOLT) register (7Eh) is used to enable this option. When this bit is set, if one or more of the voltage readings violates the low or high limits, INT# will be forced active low (if all the corresponding enable bits are set: individual enable bits (VCC_Error_En, 12V_Error_En, 5V_Error_En, 33V_Error_En, VCCP_Error_En, 25V_Error_En, 18V_Error_En, and/or 15V_Error_En), group enable (VOLT_EN), and global enable (INT_EN)). This pin will remain low while the associated voltage error bit in the Interrupt Status Register 1 or Interrupt Status Register 2 is set.

The INT# pin can be enabled to indicate fan errors. Bit[0] of the Interrupt Enable 2(Fan Tachs) register (80h) is used to enable this option. This pin will remain low while the associated fan error bit in the Interrupt Status Register 2 is set.

The INT# pin will remain low while any bit is set in any of the Interrupt Status Registers. Reading the interrupt status registers will cause the logic to attempt to clear the status bits; however, the status bits will not clear if the interrupt stimulus is still active. The interrupt enable bit (Special Function Register bit[2]) should be cleared by software before reading the interrupt status registers to insure that the INT# pin will be re-asserted while an interrupt event is active, when the INT_EN bit is written to '1' again.

The INT# pin can also be deasserted by issuing an Alert Response Address Call. See the description in the section titled SMBus Alert Response Address on page 21.

The INT# pin may only become active while the monitor block is operational.

6.6 Low Power Modes

The Hardware Monitor Block can be placed in a low-power mode by writing a '0' to Bit[0] of the Ready/Lock/Start Register (0x40). The low power mode that is entered is either sleep mode or shutdown mode as selected using Bit[0] of the Special Function Register (7Ch). These modes do not reset any of the registers of the Hardware Monitor Block. In both of these modes, the PWM pins are at 100% duty cycle.

Table 6.4 Low Power Mode Control Bits

START	LPMD	DESCRIPTION
0	0	Sleep Mode
0	1	Shutdown Mode
1	x	Monitoring

Notes:

- START and LPMD bits cannot be modified when the LOCK bit is set.
- START bit is located in the Ready/Lock/Start register (40h). LPMD bit is located in the Special Function Register (7Ch)

6.6.1 Sleep Mode

This is a low power mode in which bias currents are on and the internal oscillator is on, but the the A/D converter and monitoring cycle are turned off. Serial bus communication is still possible with any register in the Hardware Monitor Block while in this low-power mode.

6.6.2 Shutdown Mode

This is a low power mode in which bias currents are off, the internal oscillator is off, and the the A/D converter and monitoring cycle are turned off. Serial communication is only possible with Bits[2:0] of the Special Function Register at 7Ch and Bits [7:0] of the Configuration Register at 7Fh, which become write-only registers in this mode.

6.7 Analog Voltage Measurement

The Hardware Monitor Block contains inputs for directly monitoring the power supplies (+12 V, +5 V, +2.5V, +Vccp, and VCC). These inputs are scaled internally to an internal reference source, converted via an 8 bit successive approximation register ADC or a Delta-Sigma ADC (Analog-to-Digital Converter), and scaled such that the correct value refers to 3/4 scale or 192 decimal (except the Vccp input). This removes the need for external resistor dividers and allows for a more accurate means of measurement since the voltages are referenced to a known value. Since any of these inputs can be above VCC or below Ground, they are not diode protected to the power rails. The measured values

are stored in the Reading registers and compared with the Limit registers. The status bits in the Interrupt Status Register 1 and 2 are set if the measured values violate the programmed limits.

The Vccp voltage input measures the processor voltage, which will lie in the range of 0V to 3.0V.

Table 6.5, "Min/Max ADC Conversion Table" shows the values of the analog inputs that correspond to the min and max output codes of the A/D converter. For a complete list of the ADC conversions see Appendix A, "ADC Voltage Conversion," on page 86.

Table 6.5 Min/Max ADC Conversion Table

INPUT VOLTAGE	+12VIN	+5VIN	VCC/3.3VIN	+2.5VIN	+1.8VIN	+1.5VIN	+VCCP
Min Value (Corresponds to A/D output 00000000)	<0.062	<0.026	<0.017	<0.013	<0.009	<0.008	<0.012
Max Value (Corresponds to A/D output 11111111)	>15.938	>6.640	>4.383	>3.320	>2.391	>1.992	>2.988

6.8 Voltage ID

VID0-VID4 digital inputs are used to store processor Voltage ID codes (for processor operating voltage) in the VID0-4 register (43h). These VIDs can be read out by the management system using the SMBus interface.

6.9 Temperature Measurement

Temperatures are measured internally by bandgap temperature sensor and externally using two sets of diode sensor pins (for measuring two external temperatures). See subsections below.

Note: The temperature sensing circuitry for the two remote diode sensors is calibrated for a 3904 type diode.

6.9.1 Internal Temperature Measurement

Internal temperature can be measured by bandgap temperature sensor. The measurement is converted into digital format by internal ADC. This data is converted in two's complement format since both negative and positive temperature can be measured. This value is stored in Internal Temperature Reading register (26h) and compared to the Temperature Limit registers (50h – 51h). If this value violates the programmed limits in the Internal High Temperature Limit register (51h) or the Internal Low Temperature Limit register (50h) the corresponding status bit in Interrupt Status Register 1 is set.

If auto fan option is selected, the hardware will adjust the operation of the fans accordingly. See the section titled Auto Fan Control Operating Mode on page 35.

6.9.2 External Temperature Measurement

The Hardware Monitor Block also provides a way to measure two external temperatures using diode sensor pins (Remote x+ and Remote x-). The value is stored in the register (25h) for Remote1+ and Remote1- pins. The value is stored in the Remote Temperature Reading register (27h) for Remote2+ and Remote2- pins. If these values violate the programmed limits in the associated limit registers, then the corresponding Remote Diode 1 (D1) or Remote Diode 2 (D2) status bits will be set in the Interrupt Status Register 1.

If auto fan option is selected, the hardware will adjust the operation of the fans accordingly. See Auto Fan Control Operating Mode on page 35.

There are Remote Diode (1 or 2) Fault status bits in Interrupt Status Register 2 (42h), which, when one, indicate a short or open-circuit on remote thermal diode inputs (Remote x+ and Remote x-).

Before a remote diode conversion is updated, the status of the remote diode is checked. In the case of a short or open-circuit on the remote thermal diode inputs, the value in the corresponding reading register will be forced to 80h. Note that this will cause the associated remote diode limit exceeded status bit to be set (i.e. Remote Diode x Limit Error bits (D1 and D2) are located in the Interrupt Status 1 Register at register address 41h).

The temperature change is computed by measuring the change in Vbe at two different operating points of the diode to which the Remote x+ and Remote x- pins are connected. But accuracy of the measurement also depends on non-ideality factor of the process the diode is manufactured on.

6.9.3 Temperature Data Format

Temperature data can be read from the three temperature registers:

- Internal Temp Reading register (26h)
- Remote Diode 1 Temp Reading register (25h)
- Remote Diode 2 Temp Reading register (27h)

Table 6.6, "Temperature Data Format" shows several examples of the format of the temperature digital data, represented by an 8-bit, two's complement word with an LSB equal to 1.0 ^{0}C.

Table 6.6 Temperature Data Format

TEMPERATURE	READING (DEC)	READING (HEX)	DIGITAL OUTPUT
-127^{0}C	-127	81h	1000 0001
⋮	⋮	⋮	⋮
-50 ^{0}C	-50	CEh	1100 1110
⋮	⋮	⋮	⋮
-25 ^{0}C	-25	E7h	1110 0111
⋮	⋮	⋮	⋮
-1 ^{0}C	-1	FFh	1111 1111
0 ^{0}C	0	00h	0000 0000
+1 ^{0}C	1	01h	0000 0001
⋮	⋮	⋮	⋮
+25 ^{0}C	25	19h	0001 1001
⋮	⋮	⋮	⋮
+50^{0}C	50	32h	0011 0010
⋮	⋮	⋮	⋮
+127^{0}C	127	7Fh	0111 1111
SENSOR ERROR	128	80h	1000 0000

6.10 Thermal Zones

Each temperature measurement input is assigned to a Thermal Zone to control the PWM outputs in Auto Fan Control mode. These zone assignments are as follows:

- Zone 1 = Remote Diode 1 (Processor)
- Zone 2 = Ambient (Internal) Temperature Sensor
- Zone 3 = Remote Diode 2

Chapter 7 Fan Control

The following sections describe the various fan control and monitoring modes in the part.

7.1 General Description

This Fan Control device is capable of driving multiple DC fans via three PWM outputs and monitoring up to four fans equipped with tachometer outputs in either Manual Fan Control mode or in Auto Fan Control mode. The three fan control outputs (PWMx pins) are controlled by a Pulse Width Modulation (PWM) scheme. The four pins dedicated to monitoring the operation of each fan are the TACH[1:4] pins. Fans equipped with Fan Tachometer outputs may be connected to these pins to monitor the speed of the fan.

7.1.1 Limit and Configuration Registers

At power up, all the registers are reset to their default values and PWM[1:3] are set to “Fan always on Full” mode. Before initiating the monitoring cycle for either manual or auto mode, the values in the limit and configuration registers should be set.

The limit and configuration registers are:

- Registers 54h – 5Bh: TACHx Minimum
- Registers 5Fh – 61h: Zone x Range/FANx Frequency
- Registers 5Ch – 5Eh: PWMx Configuration
- Registers 62h – 63h: PWM x Ramp Rate Control
- Registers 64h – 66h: PWMx Minimum Duty Cycle
- Registers 67h – 69h: Zone x Low Temp LIMIT
- Registers 6Ah – 6Ch: Zone x Temp Absolute Limit – all fans in Auto Mode are set to full
- Register 81h: TACH_PWM Association
- Registers 90h – 93h: Tachx Option Registers
- Registers 94h – 96h: PWMx Option Registers

The limit and configuration registers are defined in Chapter 8, Register Set.

Notes:

- The START bit in Register 40h Ready/Lock/Start Register must be set to ‘1’ to start temperature monitoring functions.
- Setting the PWM Configuration register to Auto Mode will not take effect until after the START bit is set

7.1.2 Device Set-Up

BIOS will follow the steps listed below to configure the fan registers on this device. The registers corresponding to each function are listed. All steps may not be necessary if default values are acceptable. Regardless of all changes made by the BIOS to the limit and parameter registers during configuration, the EMC6D103 will continue to operate based on default values until the Start bit, in the Ready/Lock/Start register, is set. Once the Start bit is set, the EMC6D103 will operate according to the values that were set by BIOS in the limit and parameter registers.

1. Set limits and parameters (not necessarily in this order)

a. [5F-61h] Set PWM frequencies and Auto Fan Control Range.

b. [62-63h] Set Ramp Rate Control and min/off

c. [5C-5Eh] Set the fan spin-up delays.
d. [5C-5Eh] Match each PWM output with a corresponding thermal zone.
e. [67-69h] Set the zone temperature low limits.
f. [6A-6Ch] Set the zone temperature absolute limits.
g. [64-66h] Set the PWM minimum duty cycle.
h. [81h] Associate a Tachometer input to a PWM output Register
i. [90-93h] Select the TACH Mode of operation (Mode 1 or Mode 2)
j. [90-93h] Set the number of edges per tach reading
k. [90-93h] Set the ignore first 3 edges of tach input bit
l. [90-93h] Set the SLOW bit to 0b if tach reading should indicated slow fan event as FFFEh and 1b if stalled fan event as FFFFh.
m. [94-96h] Set the TACH Reading Update rate
n. [94-96h] Set the tach reading guard time (Mode 2 Only)
o. [94-96h] Set the TACH reading logic for Opportunistic Mode (Mode 2 Only)
p. [94-96h] Set the SZEN bit, which determines if the PWM output will ramp to Off or jump to Off.

2. [40h] Set bit 0 (Start) to start monitoring.
3. [40h] Set bit 1 (Lock) to lock the limit and parameter registers (optional)

7.1.3 PWM Fan Speed Control

Note: The following description applies to PWM1, PWM2, and PWM3.

When describing the operation of the PWMs, the terms “Full on” and “100% duty cycle” means that the PWM output will be high for 255 clocks and low for 1 clock (INVERT bit = 0). The exception to this is during fan spin-up when the PWM pin will be forced high for the duration of the spin-up time.

7.1.3.1 Manual Fan Control Operating Mode (Test Mode)

When operating in Manual Fan Control Operating Mode, software controls the speed of the fans by directly programming the PWM duty cycle. The operation of the fans can be monitored based on reading the temperature and tachometer reading registers and/or by polling the interrupt status registers. The EMC6D103 offers the option of generating an interrupt indicated by the INT# signal located on the PWM2 and TACH3 pins.

To control the PWM outputs in manual mode:

- Write ‘111’ to bits[7:5] Zone/Mode, located in Registers 5Ch-5Eh: PWMx Configuration.
- The speed of the fan is controlled by the duty cycle set for that PWM output. The duty cycle must be programmed in Registers 30h-32h: Current PWM Duty

To monitor the fans:

Fans equipped with Tachometer outputs can be monitored via the TACHx input pins. See Section 7.1.4, "Fan Speed Monitoring," on page 42.

If an out-of-limit condition occurs, the corresponding status bit will be set in the Interrupt Status registers. Setting this status bit will generate an interrupt signal on the INT# pin (if enabled). Software must handle the interrupt condition and modify the operation of the device accordingly. Software can evaluate the operation of the Fan Control device through the Temperature and Fan Tachometer Reading registers.

When in manual mode, the current PWM duty cycle registers can be written to adjust the speed of the fans, when the start bit is set. These registers are not writable when the lock bit is set.

Note: The PWMx Current Duty Cycle register is implemented as two separate registers: a read-only and a write-only. When a value is written to this register in manual mode there will be a delay before the programmed value can be read back by software. The hardware updates the read-

only PWMx Current Duty Cycle register on the beginning of a PWM cycle. If Ramp Rate Control is disabled, the delay to read back the programmed value will be from 0 seconds to 1/(PWM frequency) seconds. Typically, the delay will be 1/(2*PWM frequency) seconds.

7.1.3.2 Auto Fan Control Operating Mode

The EMC6D103 implements automatic fan control. In Auto Fan Mode, this device automatically adjusts the PWM duty cycle of the PWM outputs, according to the flow chart on the following page (see Figure 7.1 Automatic Fan Control Flow Diagramon page 36).

PWM outputs are assigned to a thermal zone based on the PWMx Configuration registers (see Section 6.10, "Thermal Zones," on page 32). It is possible to have more than one PWM output assigned to a thermal zone. For example, PWM outputs 2 and 3, connected to two chassis fans, may both be controlled by thermal zone 2. At any time, if the temperature of a zone exceeds its absolute limit, all PWM outputs go to 100% duty cycle to provide maximum cooling to the system (except those fans that are disabled or in manual mode).

It is possible to have a single fan controlled by multiple zones, turning on when either zone requires cooling based on its individual settings.

A VCC POR resets all values to their initial or default states.

If the start bit is one, the Auto Fan Control block will evaluate the temperature in the zones configured for each Fan in a round robin method. The Auto Fan Control block completely evaluates the zones for all three fans in a maximum of 0.25sec.

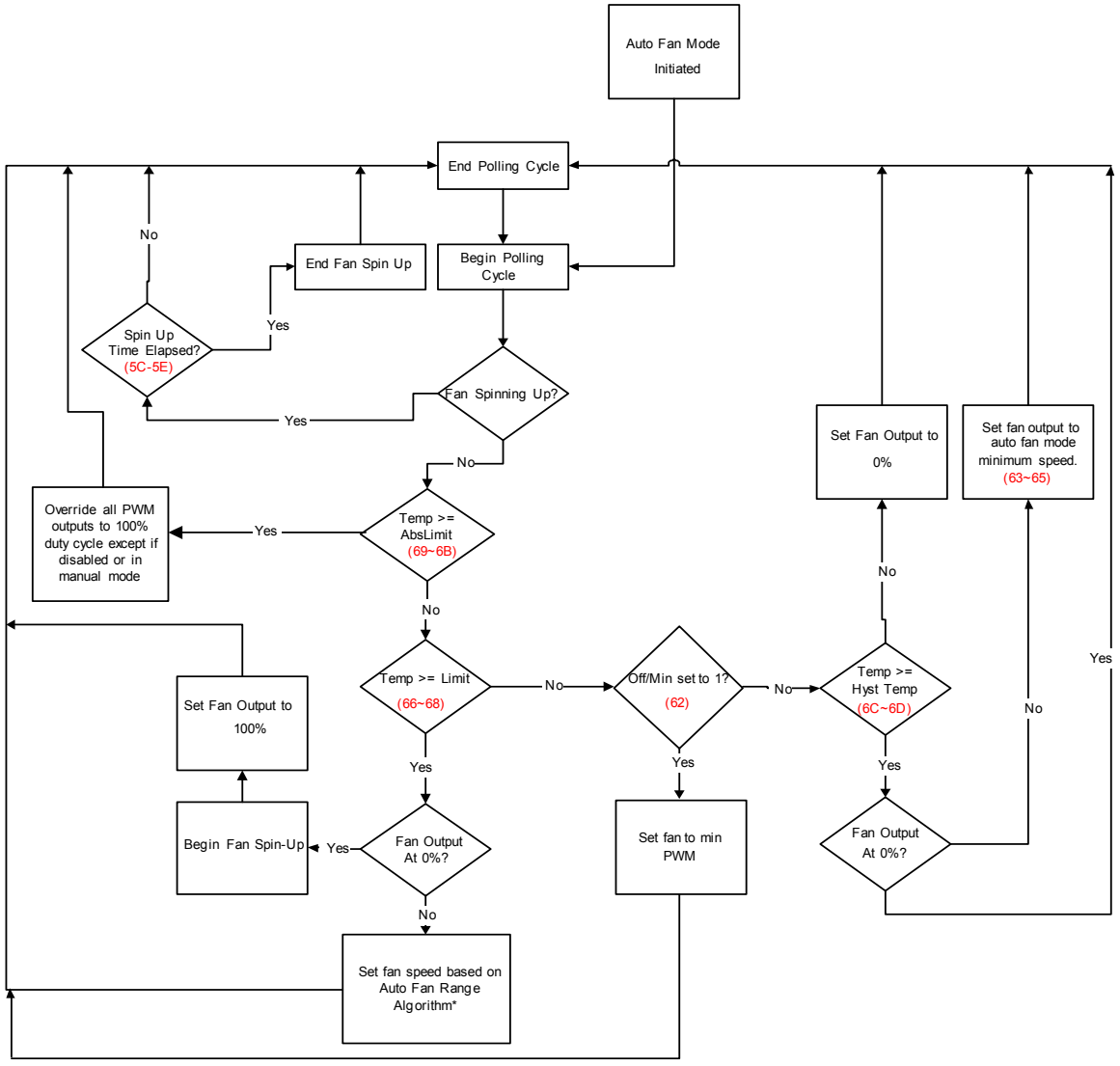


Figure 7.1 Automatic Fan Control Flow Diagram

*See Registers 5C-5Eh: PWM Configuration on page 65 for details.

When in Auto Fan Control Operating Mode the hardware controls the fans directly based on monitoring of temperature and speed.

To control the fans:

Set the minimum temperature that will turn the fans on. This value is programmed in Registers 67h-69h: Zone x Low Temp Limit (Auto Fan Mode Only).

The speed of the fan is controlled by the duty cycle set for that device. The duty cycle for the minimum fan speed must be programmed in Registers 64h-66h: PWMx Minimum Duty Cycle. This value corresponds to the speed of the fan when the temperature reading is equal to the minimum temperature LIMIT setting. As the actual temperature increases and is above the Zone LIMIT temperature and below the Absolute Temperature Limit, the PWM will be determined by a linear function based on the Auto Fan Speed Range bits in Registers 5Fh-61h.

Set the absolute temperature for each zone in Registers 6Ah-6Ch: Zone x Temp Absolute Limit (Auto Fan Mode only). If the actual temperature is equal to or exceeds the absolute temperature in one or more of the associated zones, all Fans operating in auto mode will be set to Full on, regardless of which zone they are operating in (except those that are disabled or configured for Manual Mode).

Note: Fans can be disabled via the PWMx Configuration registers and the absolute temperature safety feature can be disabled by writing 80h into the Zone x Temp Absolute Limit registers.

To set the mode to operate in auto mode, set Bits[7:5] Zone/Mode, located in Registers 5Ch-5Eh: PWM Configuration Bits[7:5]='000' for PWM on Zone 1; Bits[7:5]='001' for PWM on Zone 2; Bits[7:5]='010' for PWM on Zone 3. If the "Hottest" option is chosen (101 or 110), then the PWM output is controlled by the zone that results in the highest PWM duty cycle value.

Notes:

- Software can be alerted of an out-of-limit condition by the INT# pin if a status bit is set and enabled and the interrupt function is enabled on either the PWM2 or TACH3 pins
- Software can monitor the operation of the Fans through the Fan Tachometer Reading registers and by the PWM x Current PWM duty registers. It can also monitor current temperature readings through the Temperature Limit Registers if hardware monitoring is enabled.
- Fan control in auto mode is implemented without any input from external processor.

In auto "Zone" mode, the speed is adjusted automatically as shown in the following figure. Fans are assigned to a zone(s). It is possible to have more than one fan assigned to a thermal zone or to have multiple zones assigned to one fan.

Figure 7.2 on page 38 shows the control for the auto fan algorithm. The part allows a minimum temperature to be set, below which the fan will run at minimum speed . A temperature range is specified over which the part will automatically adjust the fan speed. If the fan is off and the current temperature is below the minimum temperature, then when the temperature exceeds the minimum, the fan will "spin up" by going on full for a programmable amount of time. Following this spin up time, the fan will go to a duty cycle computed by the auto fan algorithm. As the temperature rises, the duty cycle will increase until the fan is running at full-speed when the temperature reaches the minimum plus the range value. The effect of this is a temperature feedback loop, which will cause the temperature to reach equilibrium between the minimum temperature and the minimum temperature plus the range. Provided that the fan has adequate cooling capacity for all environmental and power dissipation conditions, this system will maintain the temperature within acceptable limits, while allowing the fan to run slower (and quieter) when less cooling is required.

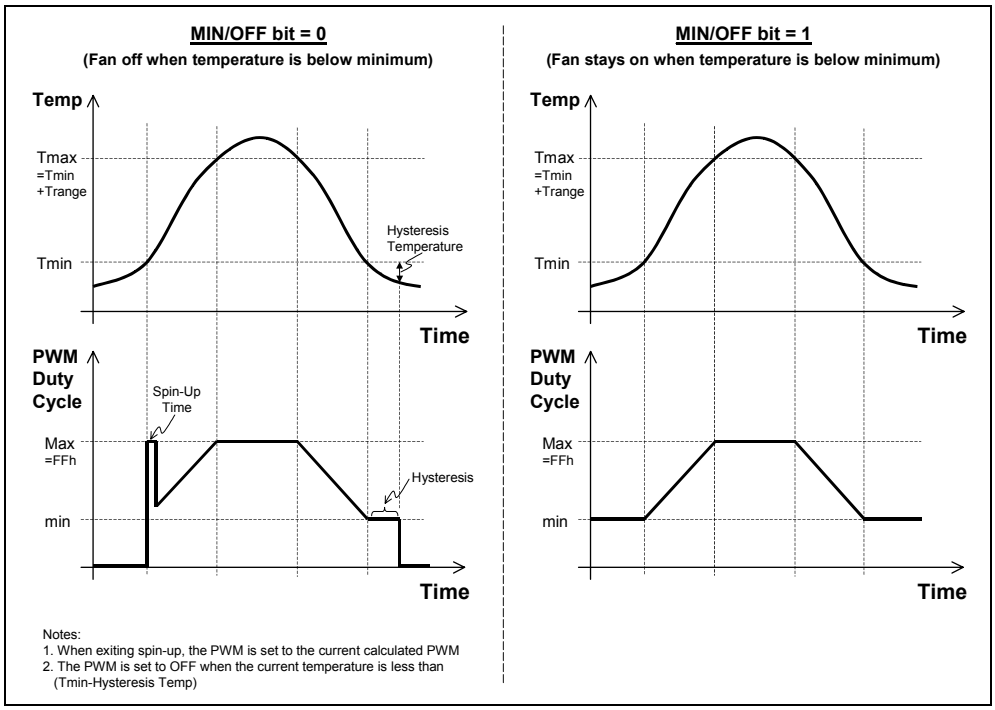


Figure 7.2 Automatic Fan Control

7.1.3.3 Spin Up

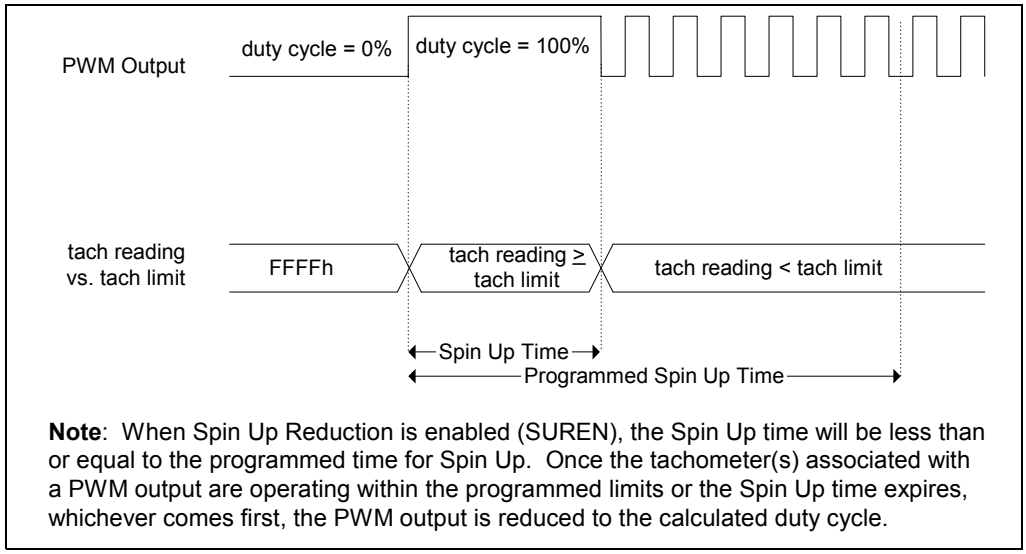
When a fan is being started from a stationary state (PWM duty cycle =00h), the part will cause the fan to “spin up” by going to 100% duty cycle for a programmable amount of time to overcome the inertia of the fan (i.e., to get the fan turning). Following this spin up time, the fan will go to the duty cycle computed by the auto fan algorithm.

During spin-up, the PWM duty cycle is reported as 0%.

To limit the spin-up time and thereby reduce fan noise, the part uses feedback from the tachometers to determine when each fan has started spinning properly. The following tachometer feedback is included into the auto fan algorithm during spin-up.

Auto Fan operation during Spin Up:

The PWM goes to 100% duty cycle until the tachometer reading register is below the minimum limit (see Figure 7.3), or the spin-up time expires, whichever comes first. This causes spin-up to continue until the tachometer enters the valid count range, unless the spin up time expires. If the spin up expires before the tachometer enters the valid range, an interrupt status bit will be set once spin-up expires. Note that more than one tachometer may be associated with a PWM, in which case all tachometers associated with a PWM must be in the valid range for spin-up to end.



Note: When Spin Up Reduction is enabled (SUREN), the Spin Up time will be less than or equal to the programmed time for Spin Up. Once the tachometer(s) associated with a PWM output are operating within the programmed limits or the Spin Up time expires, whichever comes first, the PWM output is reduced to the calculated duty cycle.

Figure 7.3 Spin Up Reduction Enabled

This feature defaults to enabled; it can be disabled by clearing bit 4 of the Configuration register (7Fh). If disabled, the all fans go to 100% duty cycle for the duration of their associated spin up time. Note that the Tachometer x minimum registers must be programmed to a value less than FFFFh in order for the spin up reduction to work properly.

Notes:

- The tachometer reading register always gives the actual reading of the tachometer input.
- No interrupt bits are set during spin-up.

7.1.3.4 Hottest Option

If the “Hottest” option is chosen (101 or 110), then the fan is controlled by the limits and parameters associated with the zone that requires the highest PWM duty cycle value, as calculated by the auto fan algorithm.

7.1.3.5 Ramp Rate Control Logic

The Ramp Rate Control Logic, if enabled, limits the amount of change in the PWM duty cycle over a specified period of time. This period of time is programmable in the Ramp Rate Control registers located at offsets 62h and 63h.

RAMP RATE CONTROL DISABLED: (DEFAULT)

The Auto Fan Control logic determines the duty cycle for a particular temperature. If PWM Ramp Rate Control is disabled, the PWM output will be set to this calculated duty cycle.

RAMP RATE CONTROL ENABLED:

If PWM Ramp Rate Control is enabled, the PWM duty cycle will Ramp up or down to the new duty cycle computed by the auto fan control logic at the programmed Ramp Rate. The PWM Ramp Rate Control logic compares the current duty cycle computed by the auto fan logic with the previous ramp rate duty cycle. If the current duty cycle is greater than the previous ramp rate duty cycle the ramp rate duty cycle is incremented by ‘1’ at the programmed ramp rate until it is greater than or equal to the current calculated duty cycle. If the current duty cycle is less than the previous ramp rate duty cycle, the ramp rate duty cycle is decremented by ‘1’ until it is less than or equal to the current duty

cycle. If the current PWM duty cycle is equal to the calculated duty cycle the PWM output will remain unchanged.

Internally, the PWM Ramp Rate Control Logic will increment/decrement the internal PWM Duty cycle by '1' at a rate determined by the Ramp Rate Control Register (see Register 62h, 63h: PWM Ramp Rate Control on page 69). The actual duty cycle output is changed once per the period of the PWM output, which is determined by the frequency of the PWM output. (See Figure 7.4 Illustration of PWM Ramp Rate Controlon page 41.)

- If the period of the PWM output is less than the step size created by the PWM Ramp Rate, the PWM output will hold the duty cycle constant until the Ramp Rate logic increments/decrements the duty cycle by '1' again. For example, if the PWM frequency is 87.7Hz (1/87.7Hz = 11.4msec) and the PWM Step time is 206msec, the PWM duty cycle will be held constant for a minimum of 18 periods (206/11.4 = 18.07) until the Ramp Logic increments/decrements the actual PWM duty cycle by '1'.
- If the period of the PWM output is greater than the step size created by the PWM Ramp Rate, the ramp rate logic will force the PWM output to increment/decrement the actual duty cycle in increments larger than 1/255. For example, if the PWM frequency is 11Hz (1/11Hz = 90.9msec) and the PWM Step time is 5msec, the PWM duty cycle output will be incremented 18 or 19 out of 255 (i.e., 90.9/5 = 18.18) until it reaches the calculated duty cycle.

Notes:

- The step size may be less if the calculated duty cycle minus the actual duty cycle is less than 18.
- The calculated PWM Duty cycle reacts immediately to a change in the temperature reading value. The temperature reading value may be updated once in 624msec, once in 78msec, once in 223msec (default), or once in 447msec (see Table 6.2, "Conversion Cycle Timing," on page 24). The internal PWM duty cycle generated by the Ramp Rate control logic gradually ramps up/down to the calculated duty cycle at a rate pre-determined by the value programmed in the PWM Ramp Rate Control bits . The PWM output latches the internal duty cycle generated by the Ramp Rate Control Block every 1/(PWM frequency) seconds to determine the actual duty cycle of the PWM output pin.

PWM Output Transition from OFF to ON

When the calculated PWM Duty cycle generated by the auto fan control logic transitions from the 'OFF' state to the 'ON' state (i.e., Current PWM duty cycle>00h), the internal PWM duty cycle in the Ramp Rate Control Logic is initialized to the calculated duty cycle without any ramp time and the PWMx Current Duty Cycle register is set to this value. The PWM output will latch the current duty cycle value in the Ramp Rate Control block to control the PWM output.

PWM Output Transition from ON to OFF

Each PWM output has a control bit to determine if the PWM output will transition immediately to the OFF state (default) or if it will gradually step down to Off at the programmed Ramp Rate. These control bits (SZEN) are located in the PWMx Options registers at offsets 94h-96h.

Table 7.1 PWM Ramp Rate

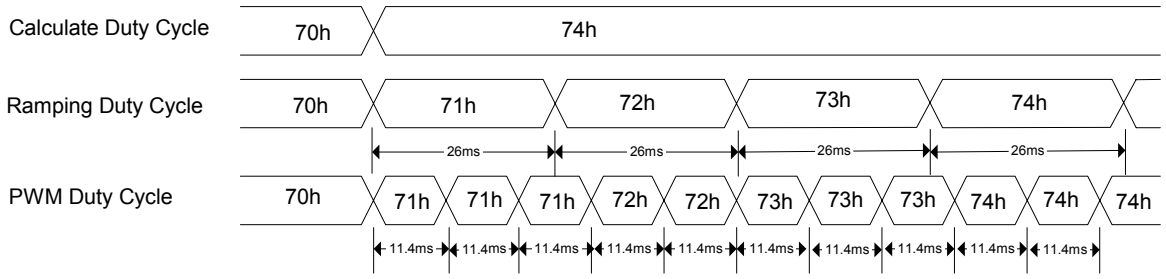
RRX-[2:0]	PWM RAMP TIME (SEC) (TIME FROM 33% DUTY CYCLE TO 100% DUTY CYCLE)	PWM RAMP TIME (SEC) (TIME FROM 0% DUTY CYCLE TO 100% DUTY CYCLE)	TIME PER PWM STEP (PWM STEP SIZE = 1/255)	PWM RAMP RATE (HZ)
000	35	52.53	206 msec	4.85
001	17.6	26.52	104 msec	9.62
010	11.8	17.595	69 msec	14.49

Table 7.1 PWM Ramp Rate (continued)

RRX-[2:0]	PWM RAMP TIME (SEC) (TIME FROM 33% DUTY CYCLE TO 100% DUTY CYCLE)	PWM RAMP TIME (SEC) (TIME FROM 0% DUTY CYCLE TO 100% DUTY CYCLE)	TIME PER PWM STEP (PWM STEP SIZE = 1/255)	PWM RAMP RATE (HZ)
011	7.0	10.455	41 msec	24.39
100	4.4	6.63	26 msec	38.46
101	3.0	4.59	18 msec	55.56
110	1.6	2.55	10 msec	100
111	0.8	1.275	5 msec	200

Example 1: PWM period < Ramp Rate Step Size

PWM frequency = 87.7Hz (11.4msec) & PWM Ramp Rate = 38.46Hz (26msec)



Example 2: PWM period > Ramp Rate Step Size

PWM frequency = 11Hz (90.9msec) & PWM Ramp Rate = 38.46Hz (26msec)

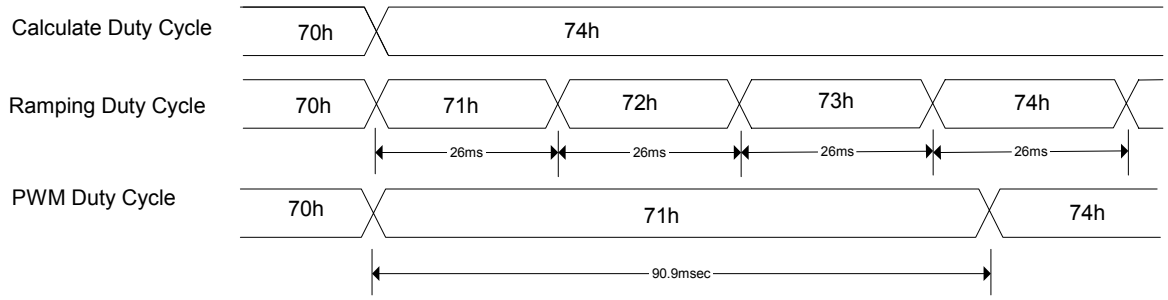


Figure 7.4 Illustration of PWM Ramp Rate Control

Notes:

- The PWM Duty Cycle latches the Ramping Duty Cycle on the rising edge of the PWM output.
- The calculated duty cycle, ramping duty cycle, and the PWM output duty cycle are asynchronous to each other, but are all synchronized to the internal 90kHz clock source.

It should be noted that the actual duty cycle on the pin is created by the PWM Ramp Rate Control block and latched on the rising edge of the PWM output. Therefore, the current PWM duty cycle may lag the PWM Calculated Duty Cycle.

7.1.4 Fan Speed Monitoring

The chip monitors the speed of the fans by utilizing fan tachometer input signals from fans equipped with tachometer outputs. The fan tachometer inputs are monitored by using the Fan Tachometer registers. These signals, as well as the Fan Tachometer registers, are described below.

The tachometers will operate in one of two modes:

- Mode 1: Standard tachometer reading mode. This mode is used when the fan is always powered when the duty cycle is greater than 00h.
- Mode 2: Enhanced tachometer reading mode. This mode is used when the PWM is pulsing the fan.

7.1.4.1 TACH Inputs

The tachometer inputs are implemented as digital input buffers with logic to filter out small glitches on the tach signal.

7.1.4.2 Selecting the Mode of Operation:

The mode is selected through the Mode Select bits located in the Tach Option register. This Mode Select bit is defined as follows:

- 0=Mode 1: Standard tachometer reading mode
- 1=Mode 2 (default): Enhanced tachometer reading mode.

Default Mode of Operation:

- Mode 2
- Slow interrupt disabled (Force FFFEh)
- Tach interrupt enabled via enable bit
- Tach Limit = FFFFh
- Look for 5 tach edges
- Don't ignore first 3 edges after guard time
- Guard Time = 32 clock periods (1 clock period = 1/90kHz).
- Tach readings updated once a second

7.1.4.3 Mode 1 – Always Monitoring

Mode 1 is the simple case. In this mode, the Fan is always powered when it is 'ON' and the fan tachometer output ALWAYS has a valid output. This mode is typically used if a linear DC Voltage control circuit drives the fan. In this mode, the fan tachometer simply counts the number of 90kHz pulses between the programmed number of edges (default = 5 edges). The fan tachometer reading registers are continuously updated.

Notes:

- Some enhanced features added to support Mode 2, are available to Mode 1 also. They are: programmable number of tach edges and force tach reading register to FFFEh to indicate a SLOW fan.
- Five edges or two tach pulses are generated per revolution.

The counter is used to determine the period of the Fan Tachometer input pulse. The counter starts counting on the first edge and continues counting until it detects the last edge or until it reaches FFFFh. If the programmed number of edges is detected on or before the counter reaches FFFFh, the reading

register is updated with that count value. If the counter reaches FFFFh and no edges were detected a stalled fan event has occurred and the Tach Reading register will be set to FFFFh. If one or more edges are detected, but less than the programmed number of edges, a slow fan event has occurred and the Tach Reading register will be set to either FFFEh or FFFFh depending on the state of the Slow Tach bits located in the TACHx Options registers at offsets 90h - 93h. Software can easily compute the RPM value using the tachometer reading value if it knows the number of edges per revolution.

7.1.4.4 Mode 2 – Monitor Tach input When PWM is 'ON'

In this mode, the PWM is used to pulse the Fan motor of a 3-wire fan. 3-wire fans use the same power supply to drive the fan motor and to drive the tachometer output logic. When the PWM is 'ON' the fan generates valid tach pulses. When the PWM is not driving the Fan, the tachometer signal is not generated and the tach signal becomes indeterminate or tristate. Therefore, Mode 2 only makes tachometer measurements when the associated PWM is driving high during an update cycle. As a result, the Fan tachometer measurement is "synchronized" to the PWM output, such that it only looks for tach pulses when the PWM is 'ON'.

Notes:

- High frequency PWM operation is designed for use with four wire fans. Although some three wire fans are capable of operating with high frequency PWM, the tach output is very difficult to read. External circuitry is required for accurate tach reading of a three wire fan that is driven with high frequency PWM.
- Any fan tachometer input may be associated with any PWM output (see Linking Fan Tachometers to PWMs on page 47.)

ASSUMPTIONS (REFER TO FIGURE 7.5, "PWM AND TACHOMETER CONCEPT"):

The Tachometer pulse generates 5 transitions per fan revolution (i.e., two fan tachometer periods per revolution, edges 2→6). One half of a revolution (one tachometer period) is equivalent to three edges (2→4 or 3→5). One quarter of a revolution (one-half tachometer period) is equivalent to two edges. To obtain the fan speed, count the number of 90Khz pulses that occurs between 2 edges i.e., 2→3, between 3 edges i.e., 2→4, or between 5 edges, i.e. 2→6 (the case of 9 edges is not shown). The time from 1-2 occurs through the guard time and is not to be used. For the discussion below, an edge is a high-to-low or low-to-high transition (edges are numbered – refer to Figure 7.5, "PWM and Tachometer Concept").

The Tachometer circuit begins monitoring the tach when the associated PWM output transitions high and the guard time has expired. Each tach circuit will continue monitoring until the programmed number of edges has been detected, whichever comes first.

The Fan Tachometer value may be updated every 300ms, 500ms, or 1000ms.

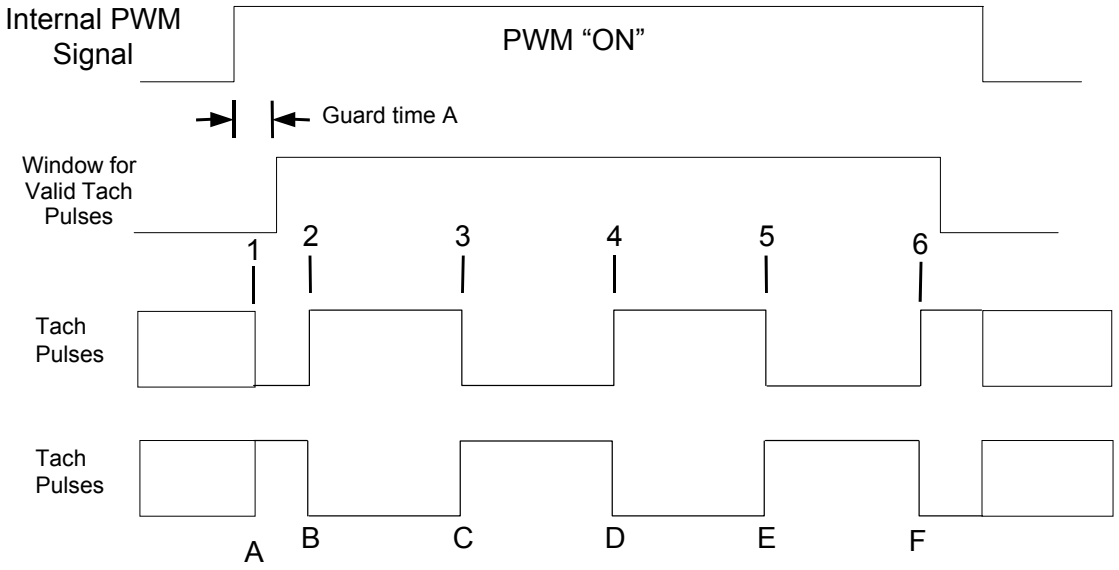


Figure 7.5 PWM and Tachometer Concept

FAN TACHOMETER OPTIONS FOR MODE 2

- 2, 3, 5 or 9 “edges” to calculate the fan speed (Figure 7.5)
- Guard time A is programmable (8-63 clocks) to account for delays in the system (Figure 7.5)
- The PWM frequencies for modes 1 & 2 are: 11.0 Hz, 14.6 Hz, 21.9 Hz, 29.3 Hz, 35.2 Hz, 44.0 Hz, 58.6 Hz, 87.7Hz and 25Khz
- Option to ignore first 3 tachometer edges after guard time
- Option to force tach reading register to FFFEh to indicate a slow fan.

7.1.4.5 Fan Tachometer Reading Registers:

The Tachometer Reading registers are 16 bits, unsigned. When one byte of a 16-bit register is read, the other byte latches the current value until it is read, in order to ensure a valid reading. The order is LSB first, MSB second. The value FFFFh indicates that the fan is not spinning, or the tachometer input is not connected to a valid signal (this could be triggered by a counter overflow). These registers are read only – a write to these registers has no effect.

Notes:

- The Fan Tachometer Reading registers always return an accurate fan tachometer measurement, even when a fan is disabled or non-functional.
- FFFFh indicates that the fan is not spinning, or the tachometer input is not connected to a valid signal (This could be triggered by a counter overflow).
- The Tachometer registers are read only – a write to these registers has no effect.
- Mode 1 should be enabled and the tachometer limit register should be set to FFFFh if a tachometer input is left unconnected.

7.1.4.6 Programming Options for Each Tachometer Input

The features defined in this section are programmable via the TACHx Option registers located at offsets 90h-93h and the PWMx Option registers located at offsets 94h-96h.

TACH READING UPDATE TIME

In Mode 1, the Fan Tachometer Reading registers are continuously updated. In Mode 2, the fan tachometer registers are updated every 300ms, 500msec, or 1000msec. This option is programmed via bits[1:0] in the PWMx Option register. The PWM associated with a particular TACH(s) determines the TACH update time.

PROGRAMMED NUMBER OF TACH EDGES

In modes 1 & 2, the number of edges is programmable for 2, 3, 5 or 9 edges (i.e., ½ tachometer pulse, 1 tachometer pulse, 2 tachometer pulses, 4 tachometer pulses). This option is programmed via bits[2:1] in the TachX Option register.

Note: The “5 edges” case corresponds to two tachometer pulses, or 1 RPM for most fans. Using the other edge options will require software to scale the values in the reading register to correspond to the count for 1 RPM.

GUARD TIME (MODE 2 ONLY)

The guard time is programmable from 8 to 63 clocks (90kHz). This option is programmed via bits[4:3] in the TachX Option register.

IGNORE FIRST 3 TACHOMETER EDGES (MODE 2 ONLY)

Option to ignore first 3 tachometer edges after guard time. This option is programmed for each tachometer via bits[2:0] in the TACHx Option register. Default is do not ignore first 3 tachometer edges after guard time.

7.1.4.7 Summary of Operation for Modes 1 & 2

The following summarizes the detection cases:

- **No edge occurs during the PWM ‘ON’ time:** indicate this condition as a stalled fan
  –The tachometer reading register contains FFFFh.
- **One edge (or less than programmed number of edges) occurs during the PWM ‘ON’ time :** indicate this condition as a slow fan.
  –If the SLOW bit is set to 0, the tachometer reading register will be set to FFFEh to indicate that this is a slow fan instead of a seized fan. Note: This operation also pertains to the case where the tachometer counter reaches FFFFh before the programmed number of edges occurs.
  –If the SLOW bit is set to one, the tachometer reading register will be set to FFFFh. In this case, no distinction is made between a slow or seized fan.

Note: The Slow Interrupt feature (SLOW) is configured in the TACHx Options registers at offsets 90h to 93h.

- **The programmed number of edges occurs:**
  -Mode 1: If the programmed number of edges occurs before the counter reaches FFFFh latch the tachometer count
  -Mode 2: If the programmed number of edges occurs during the PWM ‘ON’ time: latch the tachometer count. (see **Note** below).

Notes:

- Whenever the programmed number of edges is detected, the edge detection ends and the state machine is reset. The tachometer reading register is updated with the tachometer count value at this time. See Note 7.1 below for the one exception to this behavior.

Note 7.1 This max value will be FFFFh if the programmed number of edges is detected when the count reaches FFFFh or if no edges are detected. If the count reaches FFFFh in Mode 1 and some edges were detected, but less than the programmed number of edges, the maximum tach count value is determined by the Slow Interrupt Enable bit located in the TACHx Options registers at offsets 90h to 93h. If slow interrupt detection is set to 0, the count will be forced to FFFEh, else the count will be forced to FFFFh.

7.1.4.8 Examples of Minimum RPMs Supported

The following tables show minimum RPMs that can be supported with the different parameters. The first table uses 3 edges and the second table uses 2 edges.

Table 7.2 Minimum RPM Detectable Using 3 Edges

PWM FREQUENCY	PULSE WIDTH AT DUTY CYCLE (PWM "ON" TIME)			MINIMUM RPM AT DUTY CYCLE (Note 7.3) ($30/T_{TachPulse}$)		
(HZ)	25% (MSEC)	50% (MSEC)	100% (MSEC) (Note 7.2)	25%	50%	100%
87.7	2.85	5.7	11.36	10865	5347	2662
58.6	4.27	8.53	17	7175	3554	1774
44	5.68	11.36	22.64	5366	2662	1330
35.2	7.1	14.2	28.3	4279	2126	1063
29.3	8.53	17.06	34	3554	1768	885
21.9	11.42	22.83	45.48	2648	1319	661
14.6	17.12	34.25	68.23	1761	878	440
11	22.73	45.45	90.55	1325	661	332

Note 7.2 100% duty cycle is 255/256.

Note 7.3 RPM=$60/T_{Revolution}$, $T_{TachPulse}$= $T_{Revolution}/2$. Using 3 edges for detection, $T_{TachPulse}$ = (PWM "ON" Time – Guard Time). Minimum RPM values shown use minimum guard time (88.88usec).

Table 7.3 Minimum RPM Detectable Using 2 Edges

PWM FREQUENCY	PULSE WIDTH AT DUTY CYCLE (PWM "ON" TIME)			MINIMUM RPM AT DUTY CYCLE (Note 7.5) ($30/T_{TachPulse}$)		
(HZ)	25% (MSEC)	50% (MSEC)	100% (MSEC) (Note 7.4)	25%	50%	100%
87.7	2.85	5.7	11.36	5433	2673	1331
58.6	4.27	8.53	17	3588	1777	887
44	5.68	11.36	22.64	2683	1331	665
35.2	7.1	14.2	28.3	2139	1063	532
29.3	8.53	17.06	34	1777	884	442

Table 7.3 Minimum RPM Detectable Using 2 Edges (continued)

PWM FREQUENCY	PULSE WIDTH AT DUTY CYCLE (PWM "ON" TIME)			MINIMUM RPM AT DUTY CYCLE (Note 7.5) ($30/T_{TachPulse}$)		
(HZ)	25% (MSEC)	50% (MSEC)	100% (MSEC) (Note 7.4)	25%	50%	100%
21.9	11.42	22.83	45.48	1324	660	330
14.6	17.12	34.25	68.23	881	439	220
11	22.73	45.45	90.55	663	331	166

Note 7.4 100% duty cycle is 255/256

Note 7.5 RPM=$60/T_{Revolution}$, $T_{TachPulse}$= $T_{Revolution}/2$. Using 2 edges for detection, $T_{TachPulse}$ = 2*(PWM "ON" Time-Guard Time). Minimum RPM values shown use minimum guard time (88.88usec).

7.1.4.9 Detection of a Stalled Fan

There is a fan failure bit (TACHx) in the interrupt status register used to indicate that a slow or stalled fan event has occurred. If the tach reading value exceeds the value programmed in the tach limit register the interrupt status bit is set. See Interrupt Status register 2 at offset 42h.

Notes:

- The reading register will be forced to FFFFh if a stalled event occurs (i.e., stalled event =no edges detected.)
- The reading register will be forced to either FFFFh or FFFEh if a slow fan event occurs. (i.e., slow event: 0 < #edges < programmed #edges). If the control bit, SLOW, located in the TACHx Options registers at offsets 90h - 93h, is set then FFFEh will be forced into the corresponding Tach Reading Register to indicate that the fan is spinning slowly.
- The fan tachometer reading register stays at FFFFh in the event of a stalled fan. If the fan begins to spin again, the tachometer logic will reset and latch the next valid reading into the tachometer reading register.

7.1.4.10 Fan Interrupt Status Bits

The status bits for the fan events are in Interrupt Status Register 2 (42h). These bits are set when the reading register is above the tachometer minimum and the Interrupt Enable 2 (Fan Tachs) register bits are configured to enable Fan Tach events. No interrupt status bits are set for fan events (even if the fan is stalled) if the associated tachometer minimum is set to FFFFh (registers 54h-5Bh).

Note: The Interrupt Enable 2 (Fan Tachs) register at offset 80h defaults to enabled for the individual tachometer status events bits. The group Fan Tach INT# bit defaults to disabled. This bit needs to be set if Fan Tach interrupts are to be generated on the external INT# pin.

See Figure 6.1 Interrupt Controlon page 27.

7.1.5 Linking Fan Tachometers to PWMs

The TACH/PWM Association Register at offset 81h is used to associate a Tachometer input with a PWM output. This association has three purposes:

1. The auto fan control logic supports a feature called SpinUp Reduction. If SpinUp Reduction is enabled (SUREN bit), the auto fan control logic will stop driving the PWM output high if the associated TACH input is operating within normal parameters. (Note: SUREN bit is located in the Configuration Register at offset 7Fh)

2. To measure the tachometer input in Mode 2, the tachometer logic must know when the associated PWM is ‘ON’.
3. Inhibit fan tachometer interrupts when the associated PWM is ‘OFF’.

See the description of the PWM_TACH register. The default configuration is:

PWM1 -> TACH1.

PWM2 -> TACH2.

PWM3 -> TACH3 & TACH4.

Chapter 8 Register Set

Definition for the Lock and Start columns:

Yes = Register is made read-only when the related bit is set; No = Register is **not** made read-only when the related bit is set.

Table 8.1 Register Summary

Reg Addr	Read /Write	Reg Name		Bit 7 MSb	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSb	Default Value	Lock	Start
10h	R/W	SMSC Test Register		7	6	5	4	3	2	1	0	00h	No	No
1Dh	R/W	Reserved		RES	RES	RES	RES	RES	RES	RES	RES	00h	No	No
1Eh	R/W	Reserved		RES	RES	RES	RES	RES	RES	RES	RES	00h	No	No
1Fh	R/W	Reserved		RES	RES	RES	RES	RES	RES	RES	RES	00h	No	No
20h	R	+2.5V Reading		7	6	5	4	3	2	1	0	N/A	No	No
21h	R	Vccp Reading		7	6	5	4	3	2	1	0	N/A	No	No
22h	R	VCC Reading		7	6	5	4	3	2	1	0	N/A	No	No
23h	R	+5V Reading		7	6	5	4	3	2	1	0	N/A	No	No
24h	R	+12V Reading		7	6	5	4	3	2	1	0	N/A	No	No
25h	R	Remote Diode 1 Temp Reading		7	6	5	4	3	2	1	0	N/A	No	No
26h	R	Internal Temp Reading		7	6	5	4	3	2	1	0	N/A	No	No
27h	R	Remote Diode 2 Temp Reading		7	6	5	4	3	2	1	0	N/A	No	No
28h	R	Tach1 LSB		7	6	5	4	3	2	1	0	N/A	No	No
29h	R	Tach1 MSB		15	14	13	12	11	10	9	8	N/A	No	No
2Ah	R	Tach2 LSB		7	6	5	4	3	2	1	0	N/A	No	No
2Bh	R	Tach2 MSB		15	14	13	12	11	10	9	8	N/A	No	No
2Ch	R	Tach3 LSB		7	6	5	4	3	2	1	0	N/A	No	No
2Dh	R	Tach3 MSB		15	14	13	12	11	10	9	8	N/A	No	No
2Eh	R	Tach4 LSB		7	6	5	4	3	2	1	0	N/A	No	No
2Fh	R	Tach4 MSB		15	14	13	12	11	10	9	8	N/A	No	No
30h	R/W Note 8.1	PWM1 Current Duty Cycle		7	6	5	4	3	2	1	0	N/A	Yes Note 8.1	No
31h	R/W Note 8.1	PWM2 Current Duty Cycle		7	6	5	4	3	2	1	0	N/A	Yes Note 8.1	No
32h	R/W Note 8.1	PWM3 Current Duty Cycle		7	6	5	4	3	2	1	0	N/A	Yes Note 8.1	No

Table 8.1 Register Summary (continued)

Reg Addr	Read /Write	Reg Name		Bit 7 MSb	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSb	Default Value	Lock	Start
3Eh	R	Company ID		7	6	5	4	3	2	1	0	5Ch	No	No
3Fh	R	Version / Stepping		VER3	VER2	VER1	VER0	STP3	STP2	STP1	STP0	6Ah	No	No
40h	R/W Note 8.2	Ready/Lock/Start		RES	RES	RES	RES	OVRID	READY	LOCK	START	00h	Yes Note 8.2	No
41h	R-C Note 8.3	Interrupt Status Register 1		INT2	D2	AMB	D1	5V	VCC	Vccp	2.5V	00h	No	No
42h	R-C Note 8.3	Interrupt Status Register 2		ERR2	ERR1	TACH4	TACH3	TACH2	TACH1	RES	12V	00h	No	No
43h	R	VID0-4		RES	RES	RES	VID4	VID3	VID2	VID1	VID0	N/A	No	No
44h	R/W	2.5V Low Limit		7	6	5	4	3	2	1	0	00h	No	No
45h	R/W	2.5V High Limit		7	6	5	4	3	2	1	0	FFh	No	No
46h	R/W	Vccp Low Limit		7	6	5	4	3	2	1	0	00h	No	No
47h	R/W	Vccp High Limit		7	6	5	4	3	2	1	0	FFh	No	No
48h	R/W	VCC Low Limit		7	6	5	4	3	2	1	0	00h	No	No
49h	R/W	VCC High Limit		7	6	5	4	3	2	1	0	FFh	No	No
4Ah	R/W	5V Low Limit		7	6	5	4	3	2	1	0	00h	No	No
4Bh	R/W	5V High Limit		7	6	5	4	3	2	1	0	FFh	No	No
4Ch	R/W	12V Low Limit		7	6	5	4	3	2	1	0	00h	No	No
4Dh	R/W	12V High Limit		7	6	5	4	3	2	1	0	FFh	No	No
4Eh	R/W	Remote Diode 1 Low Temp		7	6	5	4	3	2	1	0	81h	No	No
4Fh	R/W	Remote Diode 1 High Temp		7	6	5	4	3	2	1	0	7Fh	No	No
50h	R/W	Internal Low Temp		7	6	5	4	3	2	1	0	81h	No	No
51h	R/W	Internal High Temp		7	6	5	4	3	2	1	0	7Fh	No	No
52h	R/W	Remote Diode 2 Low Temp		7	6	5	4	3	2	1	0	81h	No	No
53h	R/W	Remote Diode 2 High Temp		7	6	5	4	3	2	1	0	7Fh	No	No
54h	R/W	Tach1 Minimum LSB		7	6	5	4	3	2	1	0	FFh	No	No
55h	R/W	Tach1 Minimum MSB		15	14	13	12	11	10	9	8	FFh	No	No
56h	R/W	Tach2 Minimum LSB		7	6	5	4	3	2	1	0	FFh	No	No
57h	R/W	Tach2 Minimum MSB		15	14	13	12	11	10	9	8	FFh	No	No
58h	R/W	Tach3 Minimum LSB		7	6	5	4	3	2	1	0	FFh	No	No
59h	R/W	Tach3 Minimum MSB		15	14	13	12	11	10	9	8	FFh	No	No
5Ah	R/W	Tach4 Minimum LSB		7	6	5	4	3	2	1	0	FFh	No	No
5Bh	R/W	Tach4 Minimum MSB		15	14	13	12	11	10	9	8	FFh	No	No

Table 8.1 Register Summary (continued)

Reg Addr	Read /Write	Reg Name		Bit 7 MSb	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSb	Default Value	Lock	Start
5Ch	R/W	PWM 1 Configuration		ZON2	ZON1	ZON0	INV	RES	SPIN2	SPIN1	SPIN0	62h	Yes	No
5Dh	R/W	PWM 2 Configuration		ZON2	ZON1	ZON0	INV	RES	SPIN2	SPIN1	SPIN0	62h	Yes	No
5Eh	R/W	PWM 3 Configuration		ZON2	ZON1	ZON0	INV	RES	SPIN2	SPIN1	SPIN0	62h	Yes	No
5Fh	R/W	Zone 1 Range/PWM 1 Frequency		RAN3	RAN2	RAN1	RAN0	FRQ3	FRQ2	FRQ1	FRQ0	C3h	Yes	No
60h	R/W	Zone 2 Range/PWM 2 Frequency		RAN3	RAN2	RAN1	RAN0	FRQ3	FRQ2	FRQ1	FRQ0	C3h	Yes	No
61h	R/W	Zone 3 Range/PWM 3 Frequency		RAN3	RAN2	RAN1	RAN0	FRQ3	FRQ2	FRQ1	FRQ0	C3h	Yes	No
62h	R/W	PWM1 Ramp Rate Control		RES	RES	RES	RES	RR1E	RR1-2	RR1-1	RR1-0	E0h	Yes	No
63h	R/W	PWM 2, PWM3 Ramp Rate Control		RR2E	RR2-2	RR2-1	RR2-0	RR3E	RR3-2	RR3-1	RR3-0	00h	Yes	No
64h	R/W	PWM 1 MINIMUM Duty Cycle		7	6	5	4	3	2	1	0	80h	Yes	No
65h	R/W	PWM 2 MINIMUM Duty Cycle		7	6	5	4	3	2	1	0	80h	Yes	No
66h	R/W	PWM 3 MINIMUM Duty Cycle		7	6	5	4	3	2	1	0	80h	Yes	No
67h	R/W	Zone 1 Low Temp Limit		7	6	5	4	3	2	1	0	5Ah	Yes	No
68h	R/W	Zone 2 Low Temp Limit		7	6	5	4	3	2	1	0	5Ah	Yes	No
69h	R/W	Zone 3 Low Temp Limit		7	6	5	4	3	2	1	0	5Ah	Yes	No
6Ah	R/W	Zone 1 Temp Absolute Limit		7	6	5	4	3	2	1	0	64h	Yes	No
6Bh	R/W	Zone 2 Temp Absolute Limit		7	6	5	4	3	2	1	0	64h	Yes	No
6Ch	R/W	Zone 3 Temp Absolute Limit		7	6	5	4	3	2	1	0	64h	Yes	No
6Dh	R/W	Reserved		RES	RES	RES	RES	RES	RES	RES	RES	44h	Yes	No
6Eh	R/W	Reserved		RES	RES	RES	RES	RES	RES	RES	RES	40h	Yes	No
6Fh	R/W	XOR Test Tree Enable		RES	RES	RES	RES	RES	RES	RES	XEN	00h	Yes	No
70h	R	SMSC Test Register		TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	N/A	No	No
71h	R	SMSC Test Register		TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	N/A	No	No
72h	R	SMSC Test Register		TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	N/A	No	No
73h	R	SMSC Test Register		RES	RES	RES	RES	TST3	TST2	TST1	TST0	09h	No	No
74h	R/W	SMSC Test Register		RES	RES	RES	RES	TST3	TST2	TST1	TST0	09h	Yes	No
75h	R	SMSC Test Register		RES	RES	RES	RES	TST3	TST2	TST1	TST0	09h	No	No
76h	R/W	SMSC Test Register		RES	RES	RES	RES	TST3	TST2	TST1	TST0	09h	Yes	No
77h	R	SMSC Test Register		RES	RES	RES	RES	TST3	TST2	TST1	TST0	09h	No	No
78h	R/W	SMSC Test Register		RES	RES	RES	RES	TST3	TST2	TST1	TST0	09h	Yes	No
79h	R/W	SMSC Test Register		TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	00h	Yes	No
7Ah	R	SMSC Test Register		RES	TST6	TST5	TST4	TST3	TST2	TST1	TST0	00h	No	No
7Bh	R/W	SMSC Test Register		TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	00h	Yes	No

Table 8.1 Register Summary (continued)

Reg Addr	Read /Write	Reg Name		Bit 7 MSb	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSb	Default Value	Lock	Start
7Ch	R/W Note 8.4	Special Function Register		AVG2	AVG1	AVG0	SMSC Note 8.7	SMSC Note 8.7	INTEN	MON-MD	LPMD Note 8.5	40h	Yes Note 8.4	No
7Dh	R	Reserved		RES	RES	RES	RES	RES	RES	RES	RES	00h	No	No
7Eh	R/W	Interrupt Enable 1 (Voltages)		VCC	12V	5V	RES	VCCP	25V	RES	VOLT	ECh	Yes	No
7Fh	R/W	Configuration		INIT	SMSC Note 8.7	SMSC Note 8.7	SUREN	TRDY	RES	P2INT	T3INT	10h	Yes	No
80h	R/W	Interrupt Enable 2 (Fan Tachs)		RES	RES	RES	TACH4	TACH3	TACH2	TACH1	TACH	1Eh	Yes	No
81h	R/W	TACH_PWM Association		T4H	T4L	T3H	T3L	T2H	T2L	T1H	T1L	A4h	Yes	No
82h	R/W	Interrupt Enable 3 (Temp)		RES	RES	RES	RES	D2EN	D1EN	AMB	TEMP	0Eh	Yes	No
83h	R	Reserved		RES	RES	RES	RES	RES	RES	RES	RES	00h	No	No
84h	R	Reserved		RES	RES	RES	RES	RES	RES	RES	RES	00h	No	No
85h	R	A/D Converter LSbs Reg 1		RD2.3	RD2.2	RD2.1	RD2.0	RD1.3	RD1.2	RD1.1	RD1.0	N/A	No	No
86h	R	A/D Converter LSbs Reg 2		V12.3	V12.2	V12.1	V12.0	AM.3	AM.2	AM.1	AM.0	N/A	No	No
87h	R	A/D Converter LSbs Reg 3		V50.3	V50.2	V50.1	V50.0	V25.3	V25.2	V25.1	V25.0	N/A	No	No
88h	R	A/D Converter LSbs Reg 4		VCC.3	VCC.2	VCC.1	VCC.0	VCP.3	VCP.2	VCP.1	VCP.0	N/A	No	No
89h	R	SMSC Test Register		TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	N/A	No	No
8Ah	R	SMSC Test Register		RES	TST6	TST5	TST4	TST3	TST2	TST1	TST0	40h	No	No
8Bh	R/W	SMSC Test Register		RES	TST6	TST5	TST4	TST3	TST2	TST1	TST0	40h	Yes	No
8Ch	R	SMSC Test Register		RES	RES	RES	TST4	TST3	TST2	TST1	TST0	09h	No	No
8Dh	R/W	SMSC Test Register		RES	RES	RES	TST4	TST3	TST2	TST1	TST0	09h	Yes	No
8Eh	R	SMSC Test Register		TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	N/A	No	No
8Fh	R	Reserved		RES	RES	RES	RES	RES	RES	RES	RES	00h	No	No
90h	R/W	Tach1 Option		RES	RES	RES	3EDG	MODE	EDG1	EDG0	SLOW	04h	No	No
91h	R/W	Tach2 Option		RES	RES	RES	3EDG	MODE	EDG1	EDG0	SLOW	04h	No	No

Table 8.1 Register Summary (continued)

Reg Addr	Read /Write	Reg Name		Bit 7 MSb	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSb	Default Value	Lock	Start
92h	R/W	Tach3 Option		RES	RES	RES	3EDG	MODE	EDG1	EDG0	SLOW	04h	No	No
93h	R/W	Tach4 Option		RES	RES	RES	3EDG	MODE	EDG1	EDG0	SLOW	04h	No	No
94h	R/W	PWM1 Option		RES Note 8.6	RES Note 8.6	OPP	GRD1	GRD0	SZEN	UPDT1	UPDT0	0Ch	Yes	No
95h	R/W	PWM2 Option		RES Note 8.6	RES Note 8.6	OPP	GRD1	GRD0	SZEN	UPDT1	UPDT0	0Ch	Yes	No
96h	R/W	PWM3 Option		RES Note 8.6	RES Note 8.6	OPP	GRD1	GRD0	SZEN	UPDT1	UPDT0	0Ch	Yes	No
97h	R/W	SMSC Test Register		TST7	TST 6	TST 5	TST 4	TST3	TST2	TST1	TST0	5Ah	Yes	No
98h	R/W	SMSC Test Register		TST7	TST 6	TST 5	TST 4	TST3	TST2	TST1	TST0	F1h	Yes	No
99-FEh	R	Reserved		RES	RES	RES	RES	RES	RES	RES	RES	00h	No	No
FFh	R	SMSC Test Register		TST7	TST 6	TST 5	TST 4	TST3	TST2	TST1	TST0	N/A	No	No

Note: SMSC Test Registers may be read/write registers. Writing these registers can cause unwanted results.

Note 8.1 The PWMx Current Duty Cycle Registers are only writable when the associated fan is in manual mode. In this case, the register is writable when the start bit is set, but not when the lock bit is set.

Note 8.2 The Lock bit in the Ready/Lock/Start register is locked by the Lock Bit. The START and OVRID bits are always writable, both when the start bit is set and when the lock bit is set.

Note 8.3 The Interrupt status registers are cleared on a read if no events are active

Note 8.4 The INTEN bit in register 7Ch is always writable, both when the start bit is set and when the lock bit is set.

Note 8.5 In Shutdown Mode (LPMD=1 & START=0) all the H/W Monitoring registers/bits are not accessible except for the following: Bits[2:0] in the Special Function Register (SFTR) at offset 7Ch and Bits[7:0] in the Configuration register at offset 7Fh.

Note 8.6 These Reserved bits are read/write bits. Writing these bits to a '1' has no effect on the hardware.

Note 8.7 SMSC bits may be read/write bits. Writing these bits to a value other than the default value may cause unwanted results

8.1 Undefined Registers

The registers shown in Table 8.1, "Register Summary" above are the defined registers in the part. Any reads to undefined registers always return 00h. Writes to undefined registers have no effect and do not return an error.

8.2 Defined Registers

8.2.1 Register 10h: SMSC Test Register

Table 8.2 Register 10h: SMSC Test Register

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
10h	R/W	SMSC TEST	TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	00h

Setting the Lock bit has no effect on this register.

This register must not be written. Writing this register may produce unexpected results.

8.2.2 Registers 20-24h: Voltage Reading

Table 8.3 Registers 20-24h: Voltage Reading

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
20h	R	+2.5V Reading	7	6	5	4	3	2	1	0	N/A
21h	R	Vccp Reading	7	6	5	4	3	2	1	0	N/A

Table 8.3 Registers 20-24h: Voltage Reading (continued)

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
22h	R	VCC Reading	7	6	5	4	3	2	1	0	N/A
23h	R	+5V Reading	7	6	5	4	3	2	1	0	N/A
24h	R	+12V Reading	7	6	5	4	3	2	1	0	N/A

The Voltage Reading registers reflect the current voltage of the EMC6D103 voltage monitoring inputs. Voltages are presented in the registers at ¾ full scale for the nominal voltage, meaning that at nominal voltage, each register will read C0h.

Table 8.4 Voltage vs. Register Reading

INPUT	NOMINAL VOLTAGE	REGISTER READING AT NOMINAL VOLTAGE	MAXIMUM VOLTAGE	REGISTER READING AT MAXIMUM VOLTAGE	MINIMUM VOLTAGE	REGISTER READING AT MINIMUM VOLTAGE
+2.5V	2.5V	C0h	3.32V	FFh	0V	00h
Vccp	2.25V	C0h	3.00V	FFh	0V	00h
VCC	3.3V	C0h	4.38V	FFh	0V	00h
+5V	5.0V	C0h	6.64V	FFh	0V	00h
+12V	12.0V	C0h	16.00V	FFh	0V	00h

The Voltage Reading registers will be updated automatically by the EMC6D103 Chip with a minimum frequency of 4Hz. These registers are read only – a write to these registers has no effect.

8.2.3 Registers 25-27h: Temperature Reading

Table 8.5 Registers 25-27h: Temperature Reading

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
25h	R	Remote Diode 1 Temp Reading	7	6	5	4	3	2	1	0	N/A
26h	R	Internal Temp Reading	7	6	5	4	3	2	1	0	N/A
27h	R	Remote Diode 2 Temp Reading	7	6	5	4	3	2	1	0	N/A

The Temperature Reading registers reflect the current temperatures of the internal and remote diodes. Remote Diode 1 Temp Reading register reports the temperature measured by the Remote1- and Remote1+ pins, Remote Diode 2 Temp Reading register reports the temperature measured by the Remote2- and Remote2+ pins, and the Internal Temp Reading register reports the temperature measured by the internal (ambient) temperature sensor. Current temperatures are represented as 8 bit, 2's complement, signed numbers in Celsius, as shown below in Table 8.6. The Temperature Reading register will return a value of 80h if the remote diode pins are not implemented by the board designer or are not functioning properly (this corresponds to the diode fault interrupt status bits). The Temperature Reading registers will be updated automatically by the EMC6D103 Chip with a minimum frequency of 4Hz.

Note: These registers are read only – a write to these registers has no effect.

Each of the temperature reading registers are mapped to a zone. Each PWM may be programmed to operate in the auto fan control operating mode by associating a PWM with one or more zones. The following is a list of the zone associations.

- Zone 1 is controlled by Remote Diode 1 Temp Reading
- Zone 2 is controlled by Internal Temp Reading (Ambient Temperature Sensor)
- Zone 3 is controlled by Remote Diode 2 Temp Reading

Table 8.6 Temperature vs. Register Reading

TEMPERATURE	READING (DEC)	READING (HEX)
-127°c	-127	81h
. . .	. . .	. . .
-50°c	-50	CEh
. . .	. . .	. . .
0°c	0	00h
. . .	. . .	. . .
50°c	50	32h
. . .	. . .	. . .
127°c	127	7Fh
(SENSOR ERROR)		80h

8.2.4 Registers 28-2Fh: Fan Tachometer Reading

Table 8.7 Registers 28-2Fh: Fan Tachometer Reading

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
28h	R	Tach1 LSB	7	6	5	4	3	2	1	0	N/A
29h	R	Tach1 MSB	15	14	13	12	11	10	9	8	N/A
2Ah	R	Tach2 LSB	7	6	5	4	3	2	1	0	N/A
2Bh	R	Tach2 MSB	15	14	13	12	11	10	9	8	N/A
2Ch	R	Tach3 LSB	7	6	5	4	3	2	1	0	N/A
2Dh	R	Tach3 MSB	15	14	13	12	11	10	9	8	N/A
2Eh	R	Tach4 LSB	7	6	5	4	3	2	1	0	N/A
2Fh	R	Tach4 MSB	15	14	13	12	11	10	9	8	N/A

The Fan Tachometer Reading registers contain the number of 11.111µs periods (90KHz) between full fan revolutions. Fans produce two tachometer pulses per full revolution. These registers are updated at least once every second.

This value is represented for each fan in a 16 bit, unsigned number.

The Fan Tachometer Reading registers always return an accurate fan tachometer measurement, even when a fan is disabled or non-functional, including when the start bit=0.

When one byte of a 16-bit register is read, the other byte latches the current value until it is read, in order to ensure a valid reading. The order is LSB first, MSB second.

FFFFh indicates that the fan is not spinning, or the tachometer input is not connected to a valid signal (This could be triggered by a counter overflow).

These registers are read only – a write to these registers has no effect.

8.2.5 Registers 30-32h: Current PWM Duty

Table 8.8 Registers 30-32h: Current PWM Duty

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
30h	R/W (See Note 8.8)	PWM1 Current Duty Cycle	7	6	5	4	3	2	1	0	N/A
31h	R/W (See Note 8.8)	PWM2 Current Duty Cycle	7	6	5	4	3	2	1	0	N/A
32h	R/W (See Note 8.8)	PWM3 Current Duty Cycle	7	6	5	4	3	2	1	0	N/A

Note 8.8 These registers are only writable when the associated fan is in manual mode. These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

The Current PWM Duty registers store the duty cycle that the chip is currently driving the PWM signals at. At initial power-on, the duty cycle is 100% and thus, when read, this register will return FFh. After the **Ready/Lock/Start** Register Start bit is set, this register and the PWM signals are updated based on the algorithm described in the Auto Fan Control Operating Mode section and the Ramp Rate Control logic, unless the associated fan is in manual mode – see below.

Note: When the device is configured for Manual Mode, the Ramp Rate Control logic should be disabled.

When read, the Current PWM Duty registers return the current PWM duty cycle for the respective PWM signal.

These registers are read only – a write to these registers has no effect.

Note: If the current PWM duty cycle registers are written while the part is not in manual mode or when the start bit is zero, the data will be stored in internal registers that will only be active and observable when the start bit is set and the fan is configured for manual mode. While the part is not in manual mode and the start bit is zero, the current PWM duty cycle registers will read back FFh.

Manual Mode (Test Mode)

In manual mode, when the start bit is set to 1 and the lock bit is 0, the current duty cycle registers are writable to control the PWMs.

Note: When the lock bit is set to 1, the current duty cycle registers are Read-Only.

The PWM duty cycle is represented as follows:

Table 8.9 PWM Duty vs Register Reading

CURRENT DUTY	VALUE (DECIMAL)	VALUE (HEX)
0%	0	00h
⋮	⋮	⋮
25%	64	40h
⋮	⋮	⋮
50%	128	80h
⋮	⋮	⋮
100%	255	FFh

During spin-up, the PWM duty cycle is reported as 0%.

Notes:

- The PWMx Current Duty Cycle always reflects the current duty cycle on the associated PWM pin.
- The PWMx Current Duty Cycle register is implemented as two separate registers: a read-only and a write-only. When a value is written to this register in manual mode there will be a delay before the programmed value can be read back by software. The hardware updates the read-only PWMx Current Duty Cycle register on the beginning of a PWM cycle. If Ramp Rate Control is disabled, the delay to read back the programmed value will be from 0 seconds to 1/(PWM frequency) seconds. Typically, the delay will be 1/(2*PWM frequency) seconds.

8.2.6 Register 3Eh: Company ID

Table 8.10 Register 3Eh: Company ID

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
3Eh	R	Company ID	7	6	5	4	3	2	1	0	5Ch

The Company ID register contains the company identification number. This number is a method for uniquely identifying the part manufacturer.

This register is read only – a write to this register has no effect.

8.2.7 Register 3Fh: Version / Stepping

Table 8.11 Register 3Fh: Version / Stepping

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
3Fh	R	Version / Stepping	VER3	VER 2	VER 1	VER 0	STP 3	STP 2	STP 1	STP0	6Ah

The four least significant bits of the Version / Stepping register [3:0] contain the current stepping of the EMC6D103 silicon. Stepping numbers are to begin from a value of 08h, to indicate that the register set is enhanced from previous hardware monitoring standards. The four most significant bits [7:4] reflect the version number, which will be fixed at 0110b. For the A0 stepping of this device, the register will read 01101000b. For the A1 stepping, this register will read 01101001b and so on.

The register is used by application software to identify which device has been implemented in the given system. Based on this information, software can determine which registers to read from and write to. Further, application software may use the current stepping to implement work-arounds for bugs found in a specific silicon stepping. This register is read only – a write to this register has no effect.

8.2.8 Register 40h: Ready/Lock/Start Monitoring

Table 8.12 Register 40h: Ready/Lock/Start Monitoring

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
40h	R/W	Ready/Lock/Start	RES	RES	RES	RES	OVRID	READY	LOCK	START	00h

Setting the Lock bit makes the Lock bit read only.

Table 8.13 Ready/Lock/Start Monitoring

BIT	NAME	R/W	DEFAULT	DESCRIPTION
0	START	R/W	0	When software writes a 1 to this bit, the EMC6D103 enables monitoring and PWM output control functions based on the limit and parameter registers. Before this bit is set, the part does not update register values. Whenever this bit is set to 0, the monitoring and PWM output control functions are based on the default limits and parameters, regardless of the current values in the limit and parameter registers. The EMC6D103 preserves the values currently stored in the limit and parameter registers when this bit is set or cleared. This bit is not affected by setting the Lock bit. **Note:** When this bit is 0, all fans are on full 100% duty cycle, i.e., PWM pins are high for 255 clocks, low for 1 clock. When this bit is 0, the part is not monitoring.
1	LOCK	R/W	0	Setting this bit to 1 locks specified limit and parameter registers. Once this bit is set, limit and parameter registers become read only and will remain locked until the device is powered off. This register bit becomes read only once it is set.
2	READY	R	0	The EMC6D103 sets this bit automatically after the part is fully powered up, has completed the power-up-reset process, and after all A/D converters are functioning (all bias conditions for the A/Ds have stabilized and the A/Ds are in operational mode). (Always reads back ‘1’.)
3	OVRID	R/W	0	If this bit is set to 1, all PWM outputs go to 100% duty cycle regardless of whether or not the lock bit is set.
4-7	Reserved	R	0	Reserved.

Note: There is a start-up time of up to 82ms for monitoring after the start bit is set to ‘1’, during which time the reading registers are not valid.

The following summarizes the operation of the part based on the Start bit:

1. If Start bit = '0' then:

a. Fans are set to Full On.

b. No voltage, temperature, or fan tach monitoring is performed. The values in the reading registers will be N/A (Not Applicable), which means these values will not be considered valid readings until the Start bit = '1'. The exception to this is the Tachometer reading registers, which always give the actual reading on the TACH pins.

c. No Status bits are set.

2. If Start bit = '1'

a. All fan control and monitoring will be based on the current values in the registers. There is no need to preserve the default values after software has programmed these registers because no monitoring or auto fan control will be done when Start bit = '0'.

b. Status bits may be set.

c. Setting the START bit to 1 does not prevent the limit and parameter registers from being written.

Note: Once programmed, the register values will be saved when start bit is reset to ‘0’.

8.2.9 Register 41h: Interrupt Status Register 1

Table 8.14 Register 41h: Interrupt Status Register 1

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
41h	R-C (See Note 8.9)	Interrupt Status 1	INT2	D2	AMB	D1	5V	VCC	Vccp	2.5V	00h

Note 8.9 This register is cleared on a read if no events are active.

Note: The individual enable bits for D2, AMB, and D1 are located in the Interrupt Enable 3 (Temp) register at offset 82h. The individual enable bits for 5V, VCC, Vccp, and 2.5V are located in the Interrupt Enable 1 register at offset 7Eh.

The Interrupt Status Register 1 bits are automatically set by the device, if enabled, whenever the 2.5V, Vccp, 3.3V, or 5V input voltages violate the limits set in the limit and parameter registers or when the measured temperature violates the limits set in the limit and parameter registers for any of the three thermal inputs.

This register holds a bit set until the event is read by software or until the individual enable bit is cleared (see Note below). The contents of this register are cleared (set to 0) automatically by the EMC6D103 after it is read by software, if the voltage or temperature no longer violates the limits set in the limit and parameter registers. Once set, the Interrupt Status Register 1 bits remain set until a read event occurs or until the individual enable bits is cleared, even if the voltage or temperature no longer violate the limits set in the limit and parameter registers. Note that clearing the group Temp, Fan, or Volt enable bits or the global INTEN enable bit has no effect on the status bits. See Registers 44-4Dh: Voltage Limit Registers on page 63 and on page 64.

This register contains a bit that indicates that a bit is set in the other interrupt status register. If bit 7 is set, then a status bit is set in the Interrupt Status Register 2. Therefore, S/W can poll this register, and only if bit 7 is set does the other register need to be read. This bit is cleared (set to 0) automatically by the device if there are no bits set in Interrupt Status Registers 2.

This register is read only – a write to this register has no effect.

Note: Clearing the individual enable bits:

1. An interrupt status bit will never change from a 0 to a 1 when the corresponding individual interrupt enable bit is cleared (set to 0), regardless of whether the limits are violated during a measurement.
2. If the individual enable bit is cleared while the associated status bit is 1, the status bit will be cleared when the associated reading register is updated. The reading registers only get updated when the START bit is set to ‘1’. If the enable bit is cleared when the START bit is 0, the associated interrupt status bit will not be cleared until the start bit is set to 1 and the associated reading register is updated.

Table 8.15 Interrupt Status Register 1

BIT	NAME	R/W	DEFAULT	DESCRIPTION
0	2.5V_Error	R	0	The EMC6D103 automatically sets this bit to 1 when the 2.5V input voltage is less than or equal to the limit set in the 2.5V Low Limit register or greater than the limit set in the 2.5V High Limit register.
1	Vccp_Error	R	0	The EMC6D103 automatically sets this bit to 1 when the Vccp input voltage is less than or equal to the limit set in the Vccp Low Limit register or greater than the limit set in the Vccp High Limit register.
2	VCC_Error	R	0	The EMC6D103 automatically sets this bit to 1 when the VCC input voltage is less than or equal to the limit set in the VCC Low Limit register or greater than the limit set in the VCC High Limit register.
3	5V_Error	R	0	The EMC6D103 automatically sets this bit to 1 when the 5V input voltage is less than or equal to the limit set in the 5V Low Limit register or greater than the limit set in the 5V High Limit register.
4	Remote Diode 1 Limit Error	R	0	The EMC6D103 automatically sets this bit to 1 when the temperature input measured by the Remote1- and Remote1+ is less than or equal to the limit set in the Remote Diode 1 Low Temp register or greater than the limit set in Remote Diode 1 High Temp register.
5	Internal Sensor Limit Error	R	0	The EMC6D103 automatically sets this bit to 1 when the temperature input measured by the internal temperature sensor is less than or equal to the limit set in the Internal Low Temp register or greater than the limit set in the Internal High Temp register.
6	Remote Diode 2 Limit Error	R	0	The EMC6D103 automatically sets this bit to 1 when the temperature input measured by the Remote2- and Remote2+ is less than or equal to the limit set in the Remote Diode 2 Low Temp register or greater than the limit set in the Remote Diode 1 High Temp register.
7	INT2 Event Active	R	0	The device automatically sets this bit to 1 when a status bit is set in the Interrupt Status Register 2.

8.2.10 Register 42h: Interrupt Status Register 2

Table 8.16 Register 42h: Interrupt Status Register 2

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
42h	R-C (See Note 8.10)	Interrupt Status Register 2	ERR2	ERR1	TACH4	TACH3	TACH2	TACH1	RES	12V	00h

Note 8.10 This register is cleared on a read if no events are active.

This register is read only – a write to this register has no effect.

The Interrupt Status Register 2 bits is automatically set by the device whenever a remote temperature sensor error occurs, a tach reading value is above the minimum value set in the tachometer minimum registers, or whenever the 12V input voltage violates the limits set in the limit and parameter registers. The Interrupt Status Register 2 register holds a set bit until the event is read by software or until the individual interrupt enable bit is cleared.

This register holds a bit set until the event is read by software or until the individual enable bit is cleared (see Note below). The contents of this register are cleared (set to 0) automatically by the EMC6D103 after it is read by software, if the voltage no longer violate the limits set in the limit and parameter registers, if the temperature sensor error no loner exists, or if the tach reading register is no longer above the minimum. Once set, the Interrupt Status Register 2 bits remain set until a read event occurs or until the individual interrupt enable bit is cleared, even if the voltage, Tach, or diode event no longer exists.

The remote diode fault bits do not clear on a read while the fault condition exists. If the start bit is set when a fault condition occurs, 80h will be loaded into the associated temperature reading register, which will cause the associated diode limit error bit to be set (Remote Diode 1 Limit Error or Remote Diode 2 Limit Error) in addition to the diode fault bit. Disabling the enable bit for the diode will clear both the fault bit and the error bit for that diode (see Note below).

This register is read only – a write to this register has no effect.

Note: Clearing the individual enable bits.

1. An interrupt status bit will never change from a 0 to a 1 when the corresponding individual interrupt enable bit is cleared (set to 0), regardless of whether the limits are violated during a measurement.
2. If the individual enable bit is cleared while the associated status bit is 1, the status bit will be cleared when the associated reading register is updated. The reading registers only get updated when the START bit is set to '1'. If the enable bit is cleared when the START bit is 0, the associated interrupt status bit will not be cleared until the start bit is set to 1 and the associated reading register is updated.

Table 8.17 Interrupt Status Register 2

BIT	NAME	R/W	DEFAULT	DESCRIPTION
0	+12v_Error	R	0	The EMC6D103 automatically sets this bit to 1 when the 12V input voltage is less than or equal to the limit set in the 12V Low Limit register or greater than the limit set in the 12V High Limit register.
1	Reserved	R	0	Reserved
2	TACH1 Slow/Stalled	R	0	The EMC6D103 automatically sets this bit to 1 when the TACH1 input reading is above the value set in the Tach1 Minimum MSB and LSB registers.
3	TACH2 Slow/Stalled	R	0	The EMC6D103 automatically sets this bit to 1 when the TACH2 input reading is above the value set in the Tach2 Minimum MSB and LSB registers.
4	TACH3 Slow/Stalled	R	0	The EMC6D103 automatically sets this bit to 1 when the TACH3 input reading is above the value set in the Tach3 Minimum MSB and LSB registers.
5	TACH4 Slow/Stalled	R	0	The EMC6D103 automatically sets this bit to 1 when the TACH4 input reading is above the value set in the Tach4 Minimum MSB and LSB registers.
6	Remote Diode 1 Fault	R	0	The EMC6D103 automatically sets this bit to 1 when there is either a short or open circuit fault on the Remote1+ or Remote1- thermal diode input pins as defined in the section Diode Fault on page 27. **Note:** If the START bit is set and a fault condition exists, the Remote Diode 1 reading register will be forced to 80h.
7	Remote Diode 2 Fault	R	0	The EMC6D103 automatically sets this bit to 1 when there is either a short or open circuit fault on the Remote2+ or Remote2- thermal diode input pins as defined in the section Diode Fault on page 27. **Note:** If the START bit is set and a fault condition exists, the Remote Diode 2 reading register will be forced to 80h.

8.2.11 Register 43h: VID

Table 8.18 Register 43h: VID

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
43h	R	VID0-4	RES	RES	RES	VID4	VID3	VID2	VID1	VID0	N/A

The VID register contains the values of EMC6D103 VID0-VID4 input pins. This register indicates the status of the VID lines that interconnect the processor to the Voltage Regulator Module (VRM).

Software uses the information in this register to determine the voltage that the processor is designed to operate at. With this information, software can then dynamically determine the correct values to place in the Vccp Low Limit and Vccp High Limit registers.

This register is read only – a write to this register has no effect.

8.2.12 Registers 44-4Dh: Voltage Limit Registers

Table 8.19 Registers 44-4Dh: Voltage Limit Registers

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
44h	R/W	2.5V Low Limit	7	6	5	4	3	2	1	0	00h
45h	R/W	2.5V High Limit	7	6	5	4	3	2	1	0	FFh
46h	R/W	Vccp Low Limit	7	6	5	4	3	2	1	0	00h
47h	R/W	Vccp High Limit	7	6	5	4	3	2	1	0	FFh
48h	R/W	VCC Low Limit	7	6	5	4	3	2	1	0	00h
49h	R/W	VCC High Limit	7	6	5	4	3	2	1	0	FFh
4Ah	R/W	5V Low Limit	7	6	5	4	3	2	1	0	00h
4Bh	R/W	5V High Limit	7	6	5	4	3	2	1	0	FFh
4Ch	R/W	12V Low Limit	7	6	5	4	3	2	1	0	00h
4Dh	R/W	12V High Limit	7	6	5	4	3	2	1	0	FFh

Setting the Lock bit has no effect on these registers.

If a voltage input either exceeds the value set in the voltage high limit register or falls below or equals the value set in the voltage low limit register, the corresponding bit will be set automatically by the EMC6D103 in the interrupt status registers (41-42h). Voltages are presented in the registers at ¾ full scale for the nominal voltage, meaning that at nominal voltage, each input will be C0h, as shown in Table 8.20.

Table 8.20 Voltage Limits vs. Register Setting

INPUT	NOMINAL VOLTAGE	REGISTER SETTING AT NOMINAL VOLTAGE	MAXIMUM VOLTAGE	REGISTER SETTING AT MAXIMUM VOLTAGE	MINIMUM VOLTAGE	REGISTER SETTING AT MINIMUM VOLTAGE
2.5V	2.5V	C0h	3.32V	FFh	0V	00h
Vccp	2.25V	C0h	3.00V	FFh	0V	00h
VCC	3.3V	C0h	4.38V	FFh	0V	00h
5V	5.0V	C0h	6.64V	FFh	0V	00h
12V	12.0V	C0h	16.00V	FFh	0V	00h

8.2.13 Registers 4E-53h: Temperature Limit Registers

Table 8.21 Registers 4E-53h: Temperature Limit Registers

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
4Eh	R/W	Remote Diode 1 Low Temp	7	6	5	4	3	2	1	0	81h
4Fh	R/W	Remote Diode 1 High Temp	7	6	5	4	3	2	1	0	7Fh
50h	R/W	Internal Low Temp	7	6	5	4	3	2	1	0	81h
51h	R/W	Internal High Temp	7	6	5	4	3	2	1	0	7Fh
52h	R/W	Remote Diode 2 Low Temp	7	6	5	4	3	2	1	0	81h
53h	R/W	Remote Diode 2 High Temp	7	6	5	4	3	2	1	0	7Fh

Setting the Lock bit has no effect on these registers.

If an external temperature input or the internal temperature sensor either exceeds the value set in the high limit register or is less than or equal to the value set in the low limit register, the corresponding bit will be set automatically by the EMC6D103 in the Interrupt Status Register 1 (41h). For example, if the temperature reading from the Remote1- and Remote1+ inputs exceeds the Remote Diode 1 High Temp register limit setting, Bit[4] D1 of the Interrupt Status Register 1 will be set. The temperature limits in these registers are represented as 8 bit, 2's complement, signed numbers in Celsius, as shown below in Table 8.22.

Table 8.22 Temperature Limits vs. Register Settings

TEMPERATURE	LIMIT (DEC)	LIMIT (HEX)
-127°c	-127	81h
. . .	. . .	. . .
-50°c	-50	CEh
. . .	. . .	. . .
0°c	0	00h
. . .	. . .	. . .
50°c	50	32h
. . .	. . .	. . .
127°c	127	7Fh

8.2.14 Registers 54-5Bh: Fan Tachometer Low Limit

Table 8.23 Registers 54-5Bh: Fan Tachometer Low Limit

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
54h	R/W	Tach1 Minimum LSB	7	6	5	4	3	2	1	0	FFh
55h	R/W	Tach1 Minimum MSB	15	14	13	12	11	10	9	8	FFh
56h	R/W	Tach2 Minimum LSB	7	6	5	4	3	2	1	0	FFh
57h	R/W	Tach2 Minimum MSB	15	14	13	12	11	10	9	8	FFh
58h	R/W	Tach3 Minimum LSB	7	6	5	4	3	2	1	0	FFh
59h	R/W	Tach3 Minimum MSB	15	14	13	12	11	10	9	8	FFh
5Ah	R/W	Tach4 Minimum LSB	7	6	5	4	3	2	1	0	FFh
5Bh	R/W	Tach4 Minimum MSB	15	14	13	12	11	10	9	8	FFh

Setting the Lock bit has no effect on these registers.

The Fan Tachometer Low Limit registers indicate the tachometer reading under which the corresponding bit will be set in the Interrupt Status Register 2 register. In Auto Fan Control mode, the fan can run at high speeds (100% duty cycle), so care should be taken in software to ensure that the limit is low enough not to cause sporadic alerts. Note that an interrupt status event will be generated when the tachometer reading is greater than the minimum tachometer limit.

The fan tachometer will not cause a bit to be set in the interrupt status register if the current value in the associated Current PWM Duty registers is 00h or if the PWM is disabled via the PWM Configuration Register.

Interrupts will never be generated for a fan if its tachometer minimum is set to FFFFh.

8.2.15 Registers 5C-5Eh: PWM Configuration

Table 8.24 Registers 5C-5Eh: PWM Configuration

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
5Ch	R/W	PWM 1 Configuration	ZON2	ZON1	ZON0	INV	RES	SPIN2	SPIN1	SPIN0	62h
5Dh	R/W	PWM 2 Configuration	ZON2	ZON1	ZON0	INV	RES	SPIN2	SPIN1	SPIN0	62h
5Eh	R/W	PWM 3 Configuration	ZON2	ZON1	ZON0	INV	RES	SPIN2	SPIN1	SPIN0	62h

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

Bits [7:5] Zone/Mode

Bits [7:5] of the PWM Configuration registers associate each PWM with a temperature sensor.

- When in Auto Fan Mode, the PWM will be assigned to a zone, and its PWM duty cycle will be adjusted according to the temperature of that zone. If ‘Hottest’ option is selected (101 or 110), the PWM will be controlled by the hottest of zones 2 and 3, or of zones 1, 2, and 3. If one of these options is selected, the PWM is controlled by the limits and parameters for the zone that requires the highest PWM duty cycle, as computed by the auto fan algorithm.

- When in manual control mode, the PWMx Current Duty Cycle Registers (30h-32h) become Read/Write. It is then possible to control the PWM outputs with software by writing to these registers. See PWMx Current Duty Cycle Registers description.
- When the fan is disabled (100) the corresponding PWM output is driven low (or high, if inverted).
- When the fan is Full On (011) the corresponding PWM output is driven high (or low, if inverted).

Notes:

- Zone 1 is controlled by Remote Diode 1 Temp Reading register
- Zone 2 is controlled by Internal Temp Reading Register
- Zone 3 is controlled by Remote Diode 2 Temp Reading register

Table 8.25 Fan Zone Setting

ZON[7:5]	PWM CONFIGURATION
000	Fan on zone 1 auto
001	Fan on zone 2 auto
010	Fan on zone 3 auto
011	Fan always on full
100	Fan disabled
101	Fan controlled by hottest of zones 2,3
110	Fan controlled by hottest of zones 1,2,3
111	Fan manually controlled

Bit [4] PWM Invert

Bit [4] inverts the PWM output. If set to 1, 100% duty cycle will yield an output that is low for 255 clocks and high for 1 clock. If set to 0, 100% duty cycle will yield an output that is high for 255 clocks and low for 1 clock.

Bit [3] Reserved

Bits [2:0] Spin Up

Bits [2:0] specify the ‘spin up’ time for the fan. When a fan is being started from a stationary state, the PWM output is held at 100% duty cycle for the time specified in Table 8.26, "Fan Spin-Up Register" before scaling to a lower speed. Note: during spin-up, the PWM pin is forced high for the duration of the spin-up time (i.e., 100% duty cycle = 256/256)

Note: To reduce the spin-up time, this device has implemented a feature referred to as Spin Up Reduction. Spin Up Reduction uses feedback from the tachometers to determine when each fan has started spinning properly. Spin up for a PWM will end when the tachometer reading register is below the minimum limit, or the spin-up time expires, whichever comes first. All tachs associated with a PWM must be below min. for spin-up to end prematurely. This feature can be disabled by clearing bit 4 (SUREN) of the Configuration register (7Fh). If disabled, the all fans go on full for the duration of their associated spin up time. Note that the Tachx minimum registers must be programmed to a value less than FFFFh in order for the spin-up reduction to work properly.

Table 8.26 Fan Spin-Up Register

SPIN[2:0]	SPIN UP TIME
000	0 sec
001	100ms
010	250ms (default)
011	400ms
100	700ms
101	1000ms
110	2000ms
111	4000ms

8.2.16 Registers 5F-61h: Zone Temperature Range, PWM Frequency

Table 8.27 Registers 5F-61h: Zone Temperature Range, PWM Frequency

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
5Fh	R/W	Zone 1 Range / Fan 1 Frequency	RAN3	RAN2	RAN1	RAN0	FRQ3	FRQ2	FRQ1	FRQ0	C3h
60h	R/W	Zone 2 Range / Fan 2 Frequency	RAN3	RAN2	RAN1	RAN0	FRQ3	FRQ2	FRQ1	FRQ0	C3h
61h	R/W	Zone 3 Range / Fan 3 Frequency	RAN3	RAN2	RAN1	RAN0	FRQ3	FRQ2	FRQ1	FRQ0	C3h

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

In Auto Fan Mode, when the temperature for a zone is above the Low Temperature Limit (registers 67-69h) and below the Absolute Temperature Limit (registers 6A-6Ch) the speed of a fan assigned to that zone is determined as follows by the auto fan control logic.

When the temperature reaches the temperature value programmed in the Zone x Low Temp Limit register, the PWM output assigned to that zone is at PWMx Minimum Duty Cycle. Between Zone x Low Temp Limit and (Zone x Low Temp Limit + Zone x Range), the PWM duty cycle increases linearly according to the temperature as shown in the figure below.

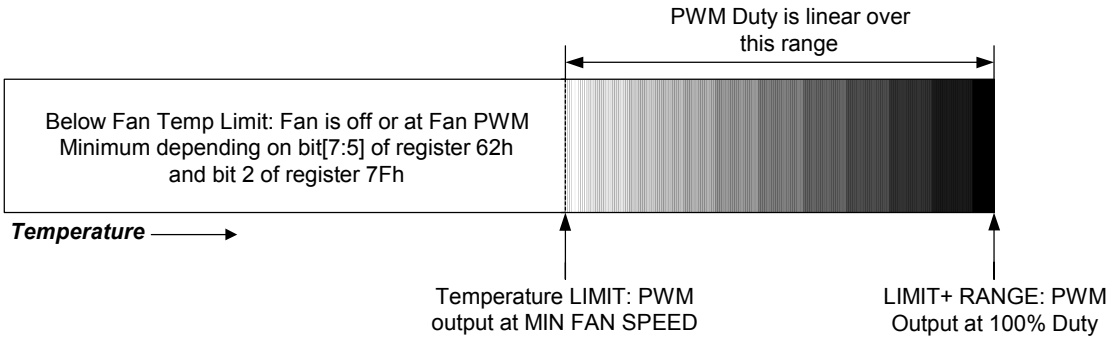


Figure 8.1 Fan Activity Above Fan Temp Limit

Example for PWM1 assigned to Zone 1:

- Zone 1 Low Temp Limit (Register 67h) is set to 50°C (32h).
- Zone 1 Range (Register 5Fh) is set to 8°C (7h)
- PWM1 Minimum Duty Cycle (Register 64h) is set to 50% (80h)

In this case, the PWM1 duty cycle will be **50% at 50°C**.

Since (**Zone 1 Low Temp Limit**) + (**Zone 1 Range**) = **50°C** + **8°C** = **58°C**, the fan controlled by PWM1 will run at 100% duty cycle when the temperature of the Zone 1 sensor is at 58°C.

Since the midpoint of the fan control range is 54°C, and the median duty cycle is 75% (Halfway between the PWM Minimum and 100%), PWM1 duty cycle would be 75% at 54°C.

Above (**Zone 1 Low Temp Limit**) + (**Zone 1 Range**), the duty cycle must be 100%.

The PWM frequency bits [3:0] determine the PWM frequency for the fan.

PWM Frequency Selection (Default =0011=29.3Hz)

Table 8.28 Register Setting vs. PWM Frequency

FREQ[3:0]	PWM FREQUENCY
0000	11.0 Hz
0001	14.6 Hz
0010	21.9 Hz
0011	29.3 Hz (default)
0100	35.2 Hz
0101	44.0 Hz
0110	58.6 Hz
0111	87.7 Hz
1000 - 1001	N/A
1010	~25 Khz
1011 - 1111	N/A

Range Selection (Default =1100=32°C)

Table 8.29 Register Setting vs. Temperature Range

RAN[3:0]	RANGE (°C)
0000	2
0001	2.5
0010	3.33
0011	4
0100	5
0101	6.67
0110	8

Table 8.29 Register Setting vs. Temperature Range (continued)

RAN[3:0]	RANGE (°C)
0111	10
1000	13.33
1001	16
1010	20
1011	26.67
1100	32
1101	40
1110	53.33
1111	80

Note: The range numbers will be used to calculate the slope of the PWM ramp up. For the fractional entries, the PWM will go on full when the temp reaches the next integer value e.g., for 3.33, PWM will be full on at (min. temp + 4).

8.2.17 Register 62h, 63h: PWM Ramp Rate Control

Table 8.30 Register 62h, 63h: Min/Off, PWM Ramp Rate Control

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
62h	R/W	PWM 1 Ramp Rate Control	RES	RES	RES	RES	RR1E	RR1-2	RR1-1	RR1-0	E0h
63h	R/W	PWM 2, PWM 3 Ramp Rate Control	RR2E	RR2-2	RR2-1	RR2-0	RR3E	RR3-2	RR3-1	RR3-0	00h

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

The duty cycle will be set to the Minimum Fan Duty Cycle when the measured temperature falls below the Temperature LIMIT register setting for the corresponding PWM.

Description of Ramp Rate Control bits:

If the Remote1 or Remote2 pins are connected to a processor or chipset, instantaneous temperature spikes may be sampled by the part. The auto fan control logic calculates the PWM duty cycle for all temperature readings. If Ramp Rate Control is disabled, the PWM output will jump or oscillate between different PWM duty cycles causing the fan to suddenly change speeds, which creates unwanted fan noise. If enabled, the PWM Ramp Rate Control logic will prevent the PWM output from jumping, instead the PWM will ramp up/down towards the new duty cycle at a pre-determined ramp rate.

Ramp Rate Control

The Ramp Rate Control logic limits the amount of change to the PWM duty cycle over a period of time. This period of time is programmable via the Ramp Rate Control bits. For a detailed description of the Ramp Rate Control bits see Table 8.31. For a description of the Ramp Rate Control logic see Ramp Rate Control Logic on page 39.

Note:

- RR1E, RR2E, and RR3E enable PWM Ramp Rate Control for PWM 1, 2, and 3 respectively.
- RR1-2, RR1-1, and RR1-0 control ramp rate time for PWM 1
- RR2-2, RR2-1, and RR2-0 control ramp rate time for PWM 2
- RR3-2, RR3-1, and RR3-0 control ramp rate time for PWM 3

Table 8.31 PWM Ramp Rate Control

RRX-[2:0]	PWM RAMP TIME (SEC) (TIME FROM 33% DUTY CYCLE TO 100% DUTY CYCLE)	PWM RAMP TIME (SEC) (TIME FROM 0% DUTY CYCLE TO 100% DUTY CYCLE)	TIME PER PWM STEP (PWM STEP SIZE = 1/255)	PWM RAMP RATE (HZ)
000	35	52.53	206 msec	4.85
001	17.6	26.52	104 msec	9.62
010	11.8	17.595	69 msec	14.49
011	7.0	10.455	41 msec	24.39
100	4.4	6.63	26 msec	38.46
101	3.0	4.59	18 msec	55.56
110	1.6	2.55	10 msec	100
111	0.8	1.275	5 msec	200

8.2.18 Registers 64-66h: Minimum PWM Duty Cycle

Table 8.32 Registers 64-66h: Minimum PWM Duty Cycle

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
64h	R/W	PWM1 Minimum Duty Cycle	7	6	5	4	3	2	1	0	80h
65h	R/W	PWM2 Minimum Duty Cycle	7	6	5	4	3	2	1	0	80h
66h	R/W	PWM3 Minimum Duty Cycle	7	6	5	4	3	2	1	0	80h

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

These registers specify the minimum duty cycle that the PWM will output when the measured temperature reaches the Temperature LIMIT register setting in Auto Fan Control Mode.

Table 8.33 PWM Duty vs. Register Setting

MINIMUM PWM DUTY	VALUE (DECIMAL)	VALUE (HEX)
0%	0	00h
. . .	. . .	. . .
25%	64	40h
. . .	. . .	. . .
50%	128	80h
. . .	. . .	. . .
100%	255	FFh

8.2.19 Registers 67-69h: Zone Low Temperature Limit

Table 8.34 Registers 67-69h: Zone Low Temperature Limit

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
67h	R/W	Zone 1 Low Temp Limit	7	6	5	4	3	2	1	0	80h
68h	R/W	Zone 2 Low Temp Limit	7	6	5	4	3	2	1	0	80h
69h	R/W	Zone 3 Low Temp Limit	7	6	5	4	3	2	1	0	80h

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

These are the temperature limits for the individual zones. When the current temperature equals this limit, the fan will be turned on if it is not already. When the temperature exceeds this limit, the fan speed will be increased according to the auto fan algorithm based on the setting in the Zone x Range / PWMx Frequency register. Default = -127°C=80h

APPLICATION NOTE: All three Zone Low Temperature Limit registers must be programmed to a valid value (other than 80h) to allow the AutoFan control to operate.

Table 8.35 Temperature Limit vs. Register Setting

LIMIT	LIMIT (DEC)	LIMIT (HEX)
-127°c	-127	81h
. . .	. . .	. . .
-50°c	-50	CEh
. . .	. . .	. . .
0°c	0	00h
. . .	. . .	. . .
50°c	50	32h
. . .	. . .	. . .
127°c	127	7Fh

8.2.20 Registers 6A-6Ch: Absolute Temperature Limit

Table 8.36 Registers 6A-6Ch: Absolute Temperature Limit

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
6Ah	R/W	Zone 1 Temp Absolute Limit	7	6	5	4	3	2	1	0	64h
6Bh	R/W	Zone 2 Temp Absolute Limit	7	6	5	4	3	2	1	0	64h
6Ch	R/W	Zone 3 Temp Absolute Limit	7	6	5	4	3	2	1	0	64h

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

In Auto Fan mode, if any zone associated with a PWM output exceeds the temperature set in the Absolute limit register, all PWM outputs will increase their duty cycle to 100% except those that are disabled via the PWM Configuration registers. This is a safety feature that attempts to cool the system if there is a potentially catastrophic thermal event.

If an absolute limit register set to 80h (-128°c), the safety feature is disabled for the associated zone. That is, if 80h is written into the Zone x Temp Absolute Limit Register, then regardless of the reading register for the zone, the fans will not turn on-full based on the absolute temp condition.

Default =100°c=64h.

When any fan is in auto fan mode, then if the temperature in any zone exceeds absolute limit, all fans go to full, including any in manual mode, except those that are disabled. Therefore, even if a zone is not associated with a fan, if that zone exceeds absolute, then all fans go to full. In this case, the absolute limit can be chosen to be 7Fh for those zones that are not associated with a fan, so that the fans won't turn on unless the temperature hits 127 degrees.

Table 8.37 Absolute Limit vs. Register Setting

ABSOLUTE LIMIT	ABS LIMIT (DEC)	ABS LIMIT (HEX)
-127°c	-127	81h
. . .	. . .	. . .
-50°c	-50	CEh
. . .	. . .	. . .
0°c	0	00h
. . .	. . .	. . .
50°c	50	32h
. . .	. . .	. . .
127°c	127	7Fh

8.2.21 Register 6F: XOR Test Register

Table 8.38 Register 6F: XOR Test Register

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
6Fh	R/W	XOR Test Register	RES	RES	RES	RES	RES	RES	RES	XEN	00h

This register becomes read only when the Lock bit is set. Any further attempts to write to this register shall have no effect.

The part incorporates an XOR tree test mode. When the test mode is enabled by setting the ‘XEN’ bit high via SMBus, the part enters XOR test mode.

The following signals are included in the XOR test tree:

- VID0, VID1, VID2, VID3, VID4

- TACH1, TACH2, TACH3, TACH4
- PWM2, PWM3

Since the test mode is XOR tree, the order of the signals in the tree is not important. SDA and SCL are not included in the test tree.

8.2.22 Register 79h: SMSC Test Register

Table 8.39 Register 79h: SMSC Test Register

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
79h	R/W	SMSC Test Register	TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	00h

This is a read/write register. Writing this register may produce unwanted results.

This register becomes read only when the Lock bit is set. Any further attempts to write to this register shall have no effect.

8.2.23 Register 7Ah: SMSC Test Register

Table 8.40 Register 7Ah: SMSC Test Register

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
7Ah	R	SMSC Test Register	RES	TST6	TST5	TST4	TST3	TST2	TST1	TST0	00h

This is a read/write register. Writing this register may produce unwanted results.

8.2.24 Register 7Bh: SMSC Test Register

Table 8.41 Register 7Bh: SMSC Test Register

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
7Bh	R/W	SMSC Test Register	TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	00h

This is a read/write register. Writing this register may produce unwanted results.

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

8.2.25 Register 7Ch: Special Function Register

Table 8.42 Register 7Ch: Special Function Register

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
7Ch	R/W	Special Function	AVG2	AVG1	AVG0	SMSC	SMSC	INTEN	MONMD	LPMD	40h

This register becomes read only when the Lock bit is set. Any further attempts to write to this register shall have no effect.

This register contains the following bits:

Bit[0] Low-Power Mode Select

0= Sleep Mode (default)

1= Shutdown Mode

Bit[1] Monitoring Mode Select

0= Continuous Monitor Mode (default)

1= Cycle Monitor Mode

Bit[2] INT# Enable

0=Disables INT# pin output function (default)

1=Enables INT# pin output function

Bit[3] SMSC Reserved

This is a read/write bit. Reading this bit has no effect. Writing this bit to '1' may cause unwanted results.

Bit [4] SMSC Reserved

This is a read/write bit. Reading this bit has no effect. Writing this bit to '1' may cause unwanted results.

Bits [7:5] AVG[2:0]

The AVG[2:0] bits determine the amount of averaging for each of the six measurements that are performed by the hardware monitor before the reading registers are updated (Table 8.43, "AVG[2:0] Bit Decoder"). The AVG[2:0] bits are priority encoded where the most significant bit has highest priority. For example, when the AVG2 bit is asserted, 32 averages will be performed for each measurement before the reading registers are updated regardless of the state of the AVG[1:0] bits.

Table 8.43 AVG[2:0] Bit Decoder

SFTR[7:5]			AVERAGES PER READING			
AVG2	**AVG1**	**AVG0**	**REM DIODE 1**	**REM DIODE 2**	**INTERNAL DIODE**	**ALL VOLTAGE READINGS (+2.5V, +5V, +12V, VCCP, AND VCC)**
0	0	0	128	128	8	8
0	0	1	16	16	1	1
0	1	X	16	16	16	16
1	X	X	32	32	32	32

Note: The default for the AVG[2:0] bits is '010'b.

8.2.26 Register 7Eh: Interrupt Enable 1 Register

Table 8.44 Register 7Eh: Interrupt Enable 1 Register

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
7Eh	R/W	Interrupt Enable 1 (Voltages)	VCC	12V	5V	RES	VCCP	25V	RES	VOLT	ECh

This register becomes read only when the Lock bit is set. Any further attempts to write to this register shall have no effect.

This register is used to enable individual voltage error events to set the corresponding status bits in the interrupt status registers. This register also contains the group voltage enable bit (Bit[0] VOLT), which is used to enable voltage events to force the interrupt pin (INT#) low if interrupts are enabled (see Bit[2] INTEN of the Special Function register at offset 7Ch).

This register contains the following bits:

Bit[0] Group INT# Voltage Enable (VOLT)

0=Out-of-limit voltages do not affect the state of the INT# pin (default)

1=Enable out-of-limit voltages to make the INT# pin active low

Bit[1] Reserved

Bit[2] 2.5V Error Enable

Bit[3] Vccp Error Enable

Bit[4] Reserved

Bit[5] 5V Error Enable

Bit[6] 12V Error Enable

Bit[7] VCC Error Enable

The individual voltage error event bits are defined as follows:

0=disable

1=enable.

See Figure 6.1 Interrupt Controlon page 27.

8.2.27 Register 7Fh: Configuration Register

Table 8.45 Register 7Fh: Configuration Register

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
7Fh	R/W	Configuration	INIT	SMSC	SMSC	SUREN	TRDY	RES	P2INT	T3INT	10h

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

This register contains the following bits:

Bit[0] TACH3/INT# pin select: 0=TACH, 1=INT#

Bit[1] PWM2/INT# pin select: 0=PWM, 1=INT#

Bit[2] Reserved

Bit[3] TRDY: Temperature Reading Ready. This bit indicates that the temperature reading registers have valid values. This bit is used after writing the start bit to '1'. 0= not valid, 1=valid.

Bit[4] SUREN: Spin-up reduction enable. This bit enables the reduction of the spin-up time based on feedback from all fan tachometers associated with each PWM. 0=disable, 1=enable (default)

Bit[5] SMSC Reserved

This is an SMSC Reserved bit. Writing this bit to a value different than the default value may cause unwanted results.

Bit[6] SMSC Reserved

This is an SMSC Reserved bit. Writing this bit to a value different than the default value may cause unwanted results.

Bit[7] Initialization

Setting the INIT bit to '1' performs a soft reset. This bit is self-clearing. Soft Reset sets all the registers except the Reading Registers to their default values.

8.2.28 Register 80h: Interrupt Enable 2 Register

Table 8.46 Register 80h: Interrupt Enable 2 Register

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
80h	R/W	Interrupt Enable 2 (Fan Tachs)	RES	RES	RES	TACH4	TACH3	TACH2	TACH1	TACH	1Eh

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

This register is used to enable individual fan tach error events to set the corresponding status bits in the interrupt status registers. This register also contains the group fan tach enable bit (Bit[0] TACH), which is used to enable fan tach events to force the interrupt pin (INT#) low if interrupts are enabled (see Bit[2] INTEN of the Special Function register at offset 7Ch).

This register contains the following bits:

Bit[0] TACH (Group TACH Enable)

0=Out-of-limit tachometer readings do not affect the state of the INT# pin (default)

1=Enable out-of-limit tachometer readings to make the INT# pin active low

Bit[1] Fan Tach 1 Event Enable

Bit[2] Fan Tach 2 Event Enable

Bit[3] Fan Tach 3 Event Enable

Bit[4] Fan Tach 4 Event Enable

Bit[5] Reserved

Bit[6] Reserved

Bit[7] Reserved

The individual fan tach error event bits are defined as follows:

0=disable

1=enable.

See Figure 6.1 Interrupt Controlon page 27.

8.2.29 Register 81h: TACH_PWM Association Register

Table 8.47 Register 81h: TACH_PWM Association Register

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
81h	R/W	TACH_PWM Association	T4H	T4L	T3H	T3L	T2H	T2L	T1H	T1L	A4h

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

This register is used to associate a PWM with a tachometer input. This association is used by the fan logic to determine when to prevent a bit from being set in the interrupt status registers.

The fan tachometer will not cause a bit to be set in the interrupt status register:

a. if the current value in Current PWM Duty registers is 00h or

b. if the fan is disabled via the Fan Configuration Register.

Note: A bit will never be set in the interrupt status for a fan if its tachometer minimum is set to FFFFh.

See bit definition below.

Bits[1:0] Tach1. These bits determine the PWM associated with this Tach. See bit combinations below.

Bits[3:2] Tach2. These bits determine the PWM associated with this Tach. See bit combinations below.

Bits[5:4] Tach3. These bits determine the PWM associated with this Tach. See bit combinations below.

Bits[7:6] Tach4. These bits determine the PWM associated with this Tach. See bit combinations below.

Table 8.48 Bit Combinations

Bits[1:0], Bits[3:2], Bits[5:4], Bits[7:6]	PWM Associated With Tachx
00	PWM1
01	PWM2
10	PWM3
11	Reserved

Notes:

- Any PWM that has no TACH inputs associated with it must be configured to operate in Mode 1.
- All TACH inputs must be associated with a PWM output. If the tach is not being driven by the associated PWM output it should be configured to operate in Mode 1 and the associated TACH interrupt must be disabled.

8.2.30 Register 82h: Interrupt Enable 3 Register

Table 8.49 Register 82h: Interrupt Enable 3 Register

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
82h	R/W	Interrupt Enable 3 (Temp)	RES	RES	RES	RES	D2EN	D1EN	AMB	TEMP	0Eh

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

This register is used to enable individual thermal error events to set the corresponding status bits in the interrupt status registers. This register also contains the group thermal enable bit (Bit[0] TEMP), which is used to enable thermal events to force the interrupt pin (INT#) low if interrupts are enabled (see Bit[2] INTEN of the Special Function register at offset 7Ch).

This register contains the following bits:
Bit[0] TEMP. Group temperature enable bit.

0=Out-of-limit temperature readings do not affect the state of the INT# pin (default)

1=Enable out-of-limit temperature readings to make the INT# pin active low

Bit[1] Ambient Temperature Status Enable bit.

Bit[2] Remote Diode 1 Temperature Status Enable bit.

Bit[3] Remote Diode 2 Temperature Status Enable bit

Bit[4] Reserved

Bit[5] Reserved

Bit[6] Reserved

Bit[7] Reserved

The individual thermal error event bits are defined as follows:

0=disable

1=enable.

See Figure 6.1 Interrupt Controlon page 27.

8.2.31 Registers 85h-88h: A/D Converter LSbs Registers

Table 8.50 Registers 85h-88h: A/D Converter LSbs Registers

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
85h	R	A/D Converter LSbs Reg 1	RD2.3	RD2.2	RD2.1	RD2.0	RD1.3	RD1.2	RD1.1	RD1.0	N/A
86h	R	A/D Converter LSbs Reg 2	V12.3	V12.2	V12.1	V12.0	AM.3	AM.2	AM.1	AM.0	N/A
87h	R	A/D Converter LSbs Reg 3	V50.3	V50.2	V50.1	V50.0	V25.3	V25.2	V25.1	V25.0	N/A
88h	R	A/D Converter LSbs Reg 4	VCC.3	VCC.2	VCC.1	VCC.0	VCP.3	VCP.2	VCP.1	VCP.0	N/A

There is a 10-bit Analog to Digital Converter (ADC) located in the hardware monitoring block that converts the measured voltages into 10-bit reading values. Depending on the averaging scheme enabled, the hardware monitor may take multiple readings and average them to create the values stored in the reading registers (i.e., 16x averaging, 32x averaging, etc.) The 8 MSb's of the reading values are placed in the Reading Registers. When the upper 8-bits located in the reading registers

are read the 4 LSb's are latched into their respective bits in the A/D Converter LSbs Register. This give 12-bits of resolution with a minimum value of 1/16th per unit measured. (i.e., Temperature Range: -127.9375 ºC < Temp < 127.9375 ºC and Voltage Range: 0 < Voltage < 256.9375) . See the DC Characteristics for the accuracy of the reading values.

The eight most significant bits of the 12-bit averaged readings are stored in Reading registers and compared with Limit registers. The Interrupt Status Register bits are asserted if the corresponding measured value(s) on the inputs violate their programmed limits.

8.2.32 Register 89h: SMSC Test Register

Table 8.51 Register 89h: SMSC Test Register

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
89h	R	SMSC Test Register	TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	N/A

8.2.33 Registers 8Ah: SMSC Test Register

Table 8.52 Registers 8Ah: SMSC Test Register

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
8Ah	R	SMSC Test Register	RES	TST6	TST5	TST4	TST3	TST2	TST1	TST0	4Dh

8.2.34 Registers 8Bh: SMSC Test Register

Table 8.53 Registers 8Bh: SMSC Test Register

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
8Bh	R/W	SMSC Test Register	RES	TST6	TST5	TST4	TST3	TST2	TST1	TST0	4Dh

This register becomes read only when the Lock bit is set. Any further attempts to write to this register shall have no effect.

This register must not be written. Writing this register may produce unexpected results.

8.2.35 Registers 8Ch: SMSC Test Register

Table 8.54 Registers 8Ch: SMSC Test Register

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
8Ch	R	SMSC Test Register	RES	RES	RES	TST4	TST3	TST2	TST1	TST0	0Eh

8.2.36 Registers 8Dh: SMSC Test Register

Table 8.55 Registers 8Dh: SMSC Test Register

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
8Dh	R/W	SMSC Test Register	RES	RES	RES	TST4	TST3	TST2	TST1	TST0	0Eh

This register becomes read only when the Lock bit is set. Any further attempts to write to this register shall have no effect.

This register must not be written. Writing this register may produce unexpected results.

8.2.37 Registers 8Eh: SMSC Test Register

Table 8.56 Registers 8Eh: SMSC Test Register

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
8Eh	R	SMSC Test Register	TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	N/A

This register is an SMSC Test register.

8.2.38 Registers 90h-93h: TachX Option Registers

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
90h	R/W	Tach1 Option	RESERVED			3EDG	MODE	EDG1	EDG0	SLOW	04h
91h	R/W	Tach2 Option	RESERVED			3EDG	MODE	EDG1	EDG0	SLOW	04h
92h	R/W	Tach3 Option	RESERVED			3EDG	MODE	EDG1	EDG0	SLOW	04h
93h	R/W	Tach4 Option	RESERVED			3EDG	MODE	EDG1	EDG0	SLOW	04h

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

Bit[0] SLOW

0=Force tach reading register to FFFEh if number of tach edges detected is greater than 0, but less than programmed number of edges.(default)

1= Force tach reading register to FFFFh if number of tach edges detected is greater than 0, but less than programmed number of edges.

Bit[2:1] The number of edges for tach1 reading:

00=2 edges

01=3 edges

10=5 edges (default)

11=9 edges

Bit[3] Tachometer Reading Mode

0=mode 1 – standard (default)

1=mode 2 – enhanced.

Bit[4] Tach (Mode 2 only)

0=Don't ignore first 3 edges (default)

1=Ignore first 3 tachometer edges after guard time

Note: This bit has been added to support a small sampling of fans that emit irregular tach pulses when the PWM transitions 'ON'. Typically, the guard time is sufficient for most fans.

Bit[7:5] RESERVED

Read to these bits return 0, writes have no affect.

8.2.39 Registers 94h-96h: PWMx Option Registers

Table 8.57 Registers 94h-96h: PWMx Option Registers

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
94h	R/W	PWM1 Option	RES	RES	OPP	GRD1	GRD0	SZEN	UPDT1	UPDT0	0Ch
95h	R/W	PWM2 Option	RES	RES	OPP	GRD1	GRD0	SZEN	UPDT1	UPDT0	0Ch
96h	R/W	PWM3 Option	RES	RES	OPP	GRD1	GRD0	SZEN	UPDT1	UPDT0	0Ch

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

Bits[1:0] Tachs reading registers associated with PWMx are updated: (Mode 2 only)

00=once a second (default)

01=twice a second

1x=every 300msec

Bit[2] Snap to Zero (SZEN)

This bit determines if the PWM output ramps down to OFF or if it is immediately set to zero.

0=Step Down the PWMx output to Off at the programmed Ramp Rate

1=Transition PWMx to Off immediately when the calculated duty cycle is 00h (default)

Bit[4:3] Guard time (Mode 2 only)

00=63 clocks (90kHz clocks ~ 700usec)

01=32 clocks (90kHz clocks ~ 356usec) (default)

10=16 clocks (90kHz clocks ~ 178usec)

11=8 clocks (90kHz clocks ~ 89usec)

Bit[5] Opportunistic Mode Enable

0= Opportunistic Mode Disabled. Update Tach Reading once per PWMx Update Period (see Bits[1:0] in this register)

1=Opportunistic Mode is Enabled. The tachometer reading register is updated any time a valid tachometer reading can be made. If a valid reading is detected prior to the Update cycle, then the Update counter is reset.

Bit[7:6] Reserved

8.2.40 Register 97h: SMSC Test Register

Table 8.58 Register 97h: SMSC Test Register

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
97h	R/W	SMSC Test Register	TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	5Ah

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

This is an SMSC Test Register. Writing to this register may cause unwanted results.

8.2.41 Register 98h:SMSC Test Register

Table 8.59 Register 98h:SMSC Test Register

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
98h	R/W	SMSC Test Register	TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	F1h

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

This is an SMSC Test Register. Writing to this register may cause unwanted results.

8.2.42 Register FFh: SMSC Test Register

Table 8.60 Register FFh: SMSC Test Register

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
98h	R	SMSC Test Register	TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	N/A

This register is an SMSC Test register.

Chapter 9 Timing Diagrams

9.1 PWM Outputs

The following section shows the timing for the PWM[1:3] outputs.

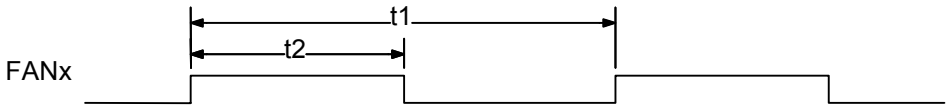


Figure 9.1 PWMx Output Timing

Table 9.1 Timing for PWM[1:3] Outputs

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	PWM Period (Note 9.1)	0.04		90.9	msec
t2	PWM High Time (Note 9.2)	0		99.6	%

Note 9.1 This value is programmable by the PWM frequency bits located in the FRFx registers.

Note 9.2 The PWM High Time is based on a percentage of the total PWM period (min=0/256*T_{PWM}, max =255/256*T_{PWM}). During Spin-up the PWM High Time can reach a 100% or Full On. (T_{PWM} = t1).

9.2 SMBus Interface

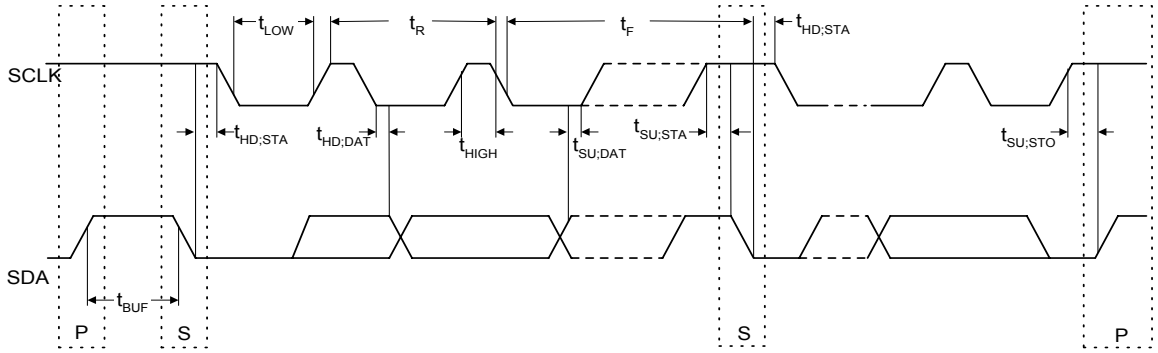


Figure 9.2 SMBus Timing

Table 9.2 SMBus Timing

SYMBOL	PARAMETER	LIMITS		UNITS	COMMENTS
		MIN	MAX		
Fsmb	SMB Operating Frequency	10	400	kHz	Note 9.3
Tsp	Spike Suppression		50	ns	Note 9.4
Tbuf	Bus free time between Stop and Start Condition	1.3		µs	
Thd:sta	Hold time after (Repeated) Start Condition. After this period, the first clock is generated.	0.6		µs	
Tsu:sta	Repeated Start Condition setup time	0.6		µs	
Tsu:sto	Stop Condition setup time	0.6		µs	
Thd:dat	Data hold time	0.3	0.9	µs	
Tsu:dat	Data setup time	100		ns	Note 9.5
Tlow	Clock low period	1.3		µs	
Thigh	Clock high period	0.6		µs	
Tf	Clock/Data Fall Time	$20+0.1C_b$	300	ns	
Tr	Clock/Data Rise Time	$20+0.1C_b$	300	ns	
C_b	Capacitive load for each bus line		400	pF	

Note 9.3 The SMBus timing (e.g., max clock frequency of 400kHz) specified exceeds that specified in the System Management Bus Specification, Rev 1.1. This corresponds to the maximum clock frequency for fast mode devices on the I^2C bus. See "The I^2C Bus Specification," version 2.0, Dec. 1998.

Note 9.4 At 400kHz, spikes of a maximum pulse width of 50ns must be suppressed by the input filter.

Note 9.5 If using 100 kHz clock frequency, the next data bit output to the SDA line will be 1250 ns (1000 ns (T_R max) + 250 ns ($T_{SU:DAT}$ min) @ 100 kHz) before the SCLK line is released.

Chapter 10 Mechanical Specifications

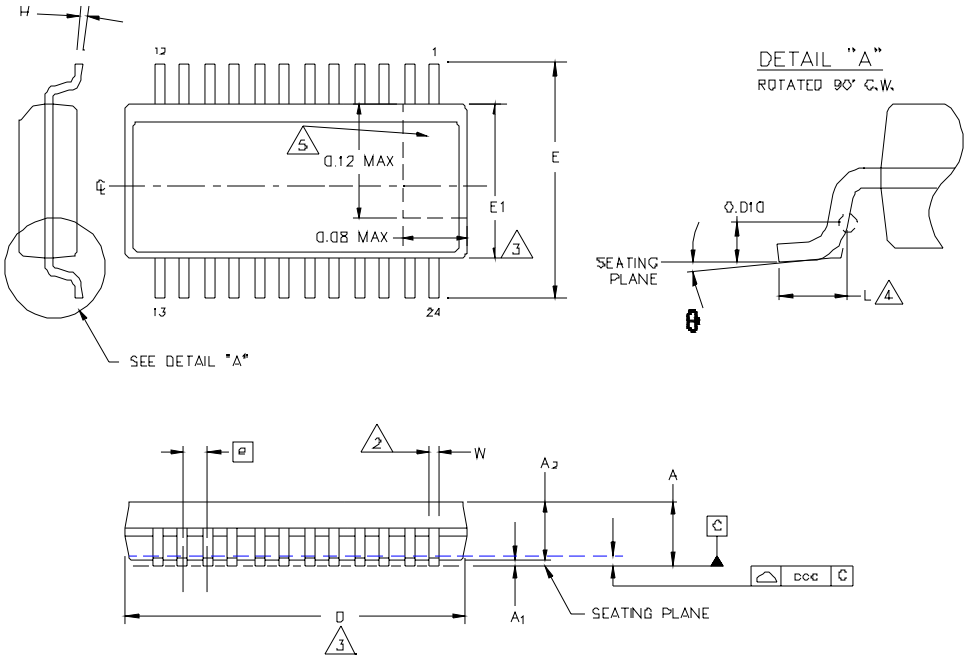


Figure 10.1 24-Pin SSOP Package Outline, 0.150” Wide Body, 0.025” Pitch

Table 10.1 24-Pin SSOP Package Parameters

	MIN	NOMINAL	MAX	REMARKS
A	0.053	~	0.069	Overall Package Height
A1	0.004	~	0.010	Standoff
A2	~	~	0.061	Body Thickness
D	0.337	~	0.344	X Body Size
E	0.228	~	0.244	Y Span
E1	0.150	~	0.157	Y body Size
H	0.007	~	0.010	Lead Frame Thickness
L	0.016	0.025	0.050	Lead Foot Length
e		0.025 Basic		Lead Pitch
è	0°	~	8°	Lead Foot Angle
W	0.008	0.010	0.012	Lead Width
ccc	~	~	0.004	Coplanarity

Notes:

1. Controlling Unit: inch.
2. Tolerance on the true position of the leads is ± 0.0035 inches maximum.
3. Package body dimensions D and E1 do not include the mold protrusion. Maximum mold protrusion is 0.006 inches for ends, and 0.010 inches for sides.
4. Dimension for foot length L measured at the gauge plane 0.010 inches above the seating plane.
5. Details of pin 1 identifier are optional but must be located within the zone indicated.

Appendix A ADC Voltage Conversion

Table A.1 Analog-to-Digital Voltage Conversions for Hardware Monitoring Block

INPUT VOLTAGE					A/D OUTPUT	
12 V_{IN}	5 V_{IN}	V_{CC}	2.5 V_{IN}	V_{CCPIN}	Decimal	Binary
<0.062	<0.026	<0.0172	<0.013	<0.012	0	0000 0000
0.062–0.125	0.026–0.052	0.017–0.034	0.013–0.026	0.012–0.023	1	0000 0001
0.125–0.188	0.052–0.078	0.034–0.052	0.026–0.039	0.023–0.035	2	0000 0010
0.188–0.250	0.078–0.104	0.052–0.069	0.039–0.052	0.035–0.047	3	0000 0011
0.250–0.313	0.104–0.130	0.069–0.086	0.052–0.065	0.047–0.058	4	0000 0100
0.313–0.375	0.130–0.156	0.086–0.103	0.065–0.078	0.058–0.070	5	0000 0101
0.375–0.438	0.156–0.182	0.103–0.120	0.078–0.091	0.070–0.082	6	0000 0110
0.438–0.500	0.182–0.208	0.120–0.138	0.091–0.104	0.082–0.093	7	0000 0111
0.500–0.563	0.208–0.234	0.138–0.155	0.104–0.117	0.093–0.105	8	0000 1000
…	…	…	…	…	…	…
4.000–4.063	1.666–1.692	1.100–1.117	0.833–0.846	0.749–0.761	64 (1/4 Scale)	0100 0000
…	…	…	…	…	…	…
8.000–8.063	3.330–3.560	2.200–2.217	1.667–1.680	1.499–1.511	128 (1/2 Scale)	1000 0000
…	…	…	…	…	…	…
12.000–12.063	5.000–5.026	3.300–3.317	2.500–2.513	2.249–2.261	192 (3/4 Scale)	1100 0000
…	…	…	…	…	…	…
15.312–15.375	6.380–6.406	4.210–4.230	3.190–3.203	2.869–2.881	245	1111 0101
15.375–15.437	6.406–6.432	4.230–4.245	3.203–3.216	2.881–2.893	246	1111 0110
15.437–15.500	6.432–6.458	4.245–4.263	3.216–3.229	2.893–2.905	247	1111 0111
15.500–15.563	6.458–6.484	4.263–4.280	3.229–3.242	2.905–2.916	248	1111 1000
15.625–15.625	6.484–6.510	4.280–4.300	3.242–3.255	2.916–2.928	249	1111 1001
15.625–15.688	6.510–6.536	4.300–4.314	3.255–3.268	2.928–2.940	250	1111 1010
15.688–15.750	6.536–6.562	4.314–4.330	3.268–3.281	2.940–2.951	251	1111 1011
15.750–15.812	6.562–6.588	4.331–4.348	3.281–3.294	2.951–2.964	252	1111 1100
15.812–15.875	6.588–6.615	4.348–4.366	3.294–3.307	2.964–2.975	253	1111 1101
15.875–15.938	6.615–6.640	4.366–4.383	3.307–3.320	2.975–2.987	254	1111 1110
>15.938	>6.640	>4.383	>3.320	>2.988	255	1111 1111

Appendix B Example Fan Circuits

The following figures show examples of circuitry on the board for the PWM outputs, tachometer inputs, and remote diodes. Figure B.1, "Fan Drive Circuitry (Apply to PWM Driving Two Fans)" shows how the part can be used to control four fans by connecting two fans to one PWM output.

Note: These examples represent the minimum required components. Some designs may require additional components.

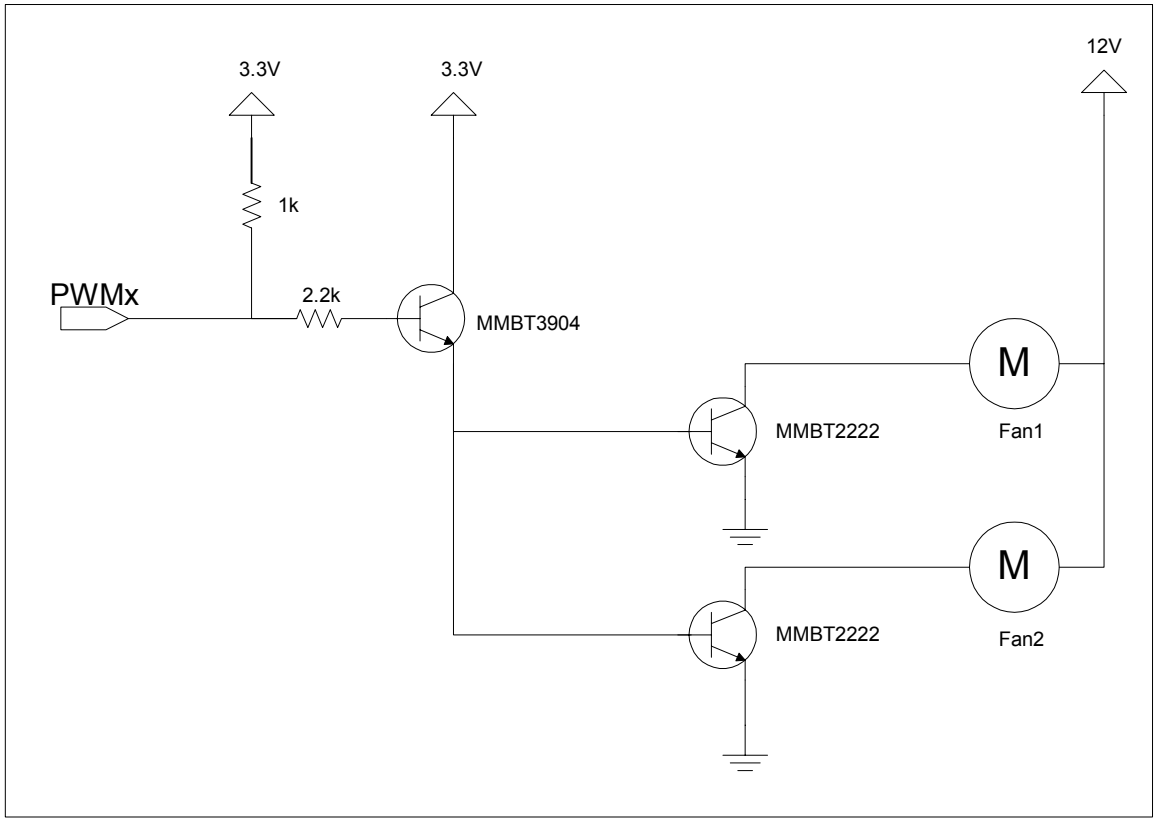


Figure B.1 Fan Drive Circuitry (Apply to PWM Driving Two Fans)

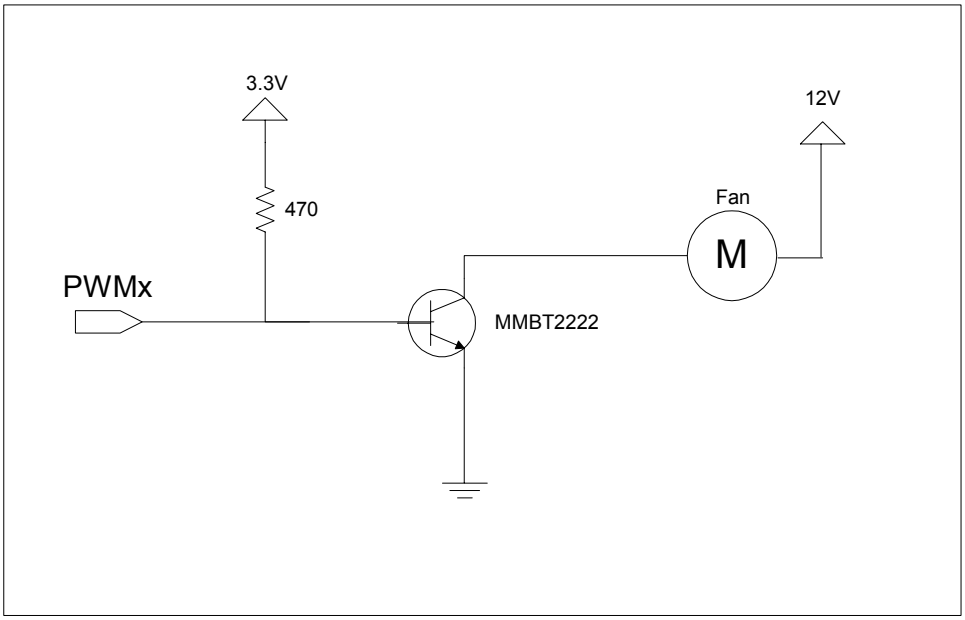
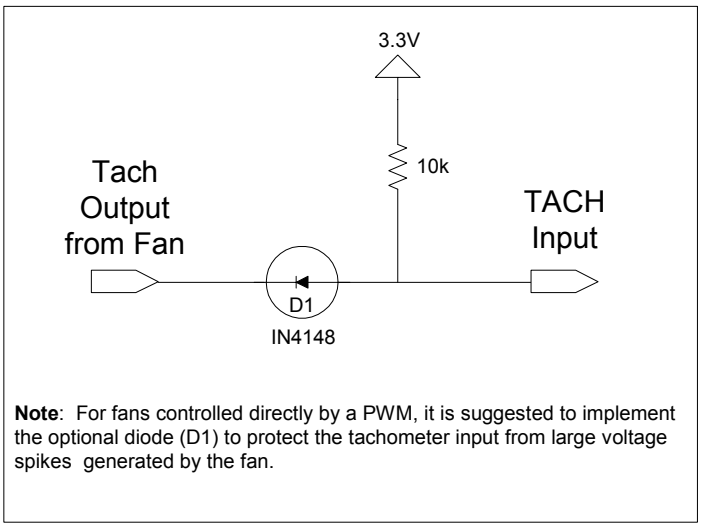


Figure B.2 Fan Drive Circuitry (Apply to PWM Driving One Fan)



Note: For fans controlled directly by a PWM, it is suggested to implement the optional diode (D1) to protect the tachometer input from large voltage spikes generated by the fan.

Figure B.3 Fan Tachometer Circuitry (Apply to Each Fan)

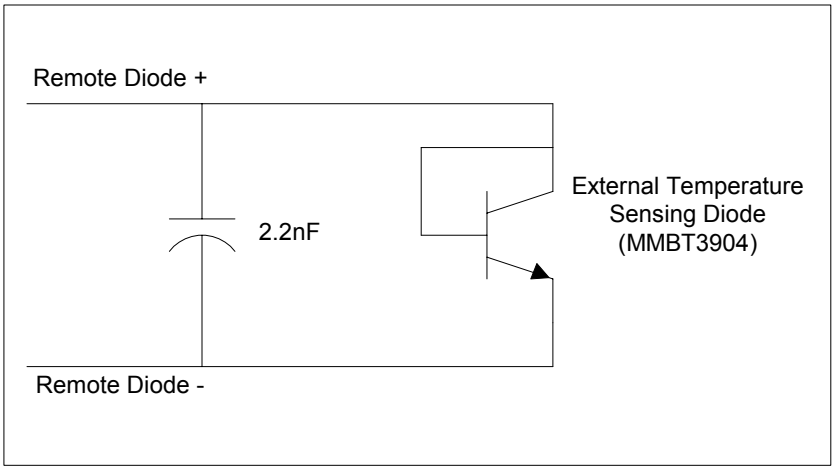


Figure B.4 Remote Diode (Apply to Remote2 Lines)

Notes:

1. 2.2nF cap is optional and should be placed close to the EMC6D103 if used.
2. The voltage at PWM3 must be at least 2.0V to avoid triggering Address Enable.
3. The Remote Diode + and Remote Diode - tracks should be kept close together, in parallel with grounded guard tracks on each side. Using wide tracks will help to minimize inductance and reduce noise pickup. A 10 mil track minimum width and spacing is recommended. See Figure B.5, "Suggested Minimum Track Width and Spacing".

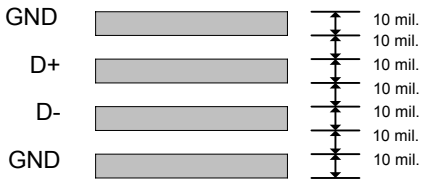


Figure B.5 Suggested Minimum Track Width and Spacing