EMC2103

RPM-Based Fan Controller with Hardware Thermal Shutdown

PRODUCT FEATURES

Datasheet

General Description

The EMC2103 is an SMBus compliant fan controller with up to up to 3 external and 1 internal temperature channels. The fan driver can be operated using two methods each with two modes. The methods include an RPM based Fan Speed Control Algorithm and a direct PWM drive setting. The modes include manually programming the desired settings or using the internal programmable temperature look-up table to select the desired setting based on measured temperature.

The temperature monitors offer ±0.5°C accuracy (for external diodes) with sophisticated features to reduce errors introduced by series resistance and beta variation of substrate thermal diode transistors commonly found in processors.

The EMC2103 also includes a hardware programmable temperature limit and dedicated system shutdown output for thermal protection of critical circuitry.

Applications

- Notebook Computers
- Projectors
- Graphics Cards
- Industrial and Networking Equipment

Features

- Programmable Fan Control circuit
  - 4-wire fan compatible
  - High and low frequency PWM
- RPM based fan control algorithm
  - 2.5% accuracy from ~500RPM to 16k RPM
  - Detects fan aging and variation
- Temperature Look-Up Table
  - Allows programmed fan response to temperature
  - Controls fan speed or PWM drive setting
  - Allows externally set temperature data to drive fan
  - Supports DTS data from CPU
- Up to Three External Temperature Channels (EMC2103-2 and EMC2103-4 only)
  - Supports 45nm, 60nm, and 90nm CPU diodes
  - Automatically detects and supports CPUs requiring BJT or Transistor models
  - Resistance error correction
  - Supports discrete transistors (i.e. 2N3904)
  - ±0.5°C accurate (60°C to 125°C)
  - 0.125°C resolution
- Hardware Programmable Thermal Shutdown Temperature
  - Cannot be altered by software
  - 65°C to 127°C Range
- Programmable High and Low Limits for all channels
- Internal Temperature Monitor
  - ±1°C accuracy
  - 0.125°C resolution
- 3.3V Supply Voltage
- SMBus 2.0 Compliant
  - SMBus Alert compatible
- Two dedicated GPIOs (EMC2103-2 and EMC2103-4 only)
- Available in 12-pin, QFN RoHS Compliant Package (EMC2103-1) or 16-pin, QFN RoHS Compliant Package (EMC2103-2 and EMC2103-4)

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ORDER NUMBERS:

ORDERING NUMBER	PACKAGE	FEATURES
EMC2103-1-KP-TR	12-pin, QFN ROHS Compliant	One external diode, RPM based Fan Speed Control Algorithm, High Frequency PWM driver, HW Thermal / Critical shutdown, EEPROM Load disabled
EMC2103-2-AP-TR	16-pin, QFN ROHS Compliant	Up to three external diodes, RPM based Fan Speed Control algorithm, High Frequency PWM driver, HW Thermal / Critical shutdown, 2 GPIOs, EEPROM Load disabled
EMC2103-4-AP-TR	16-pin, QFN ROHS Compliant	Up to three external diodes, RPM based Fan Speed Control algorithm, High Frequency PWM driver, HW Thermal / Critical shutdown, 2 GPIOs, EEPROM Load enabled

REEL SIZE IS 4,000 PIECES

This product meets the halogen maximum concentration values per IEC61249-2-21

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Chapter 1 Block Diagram

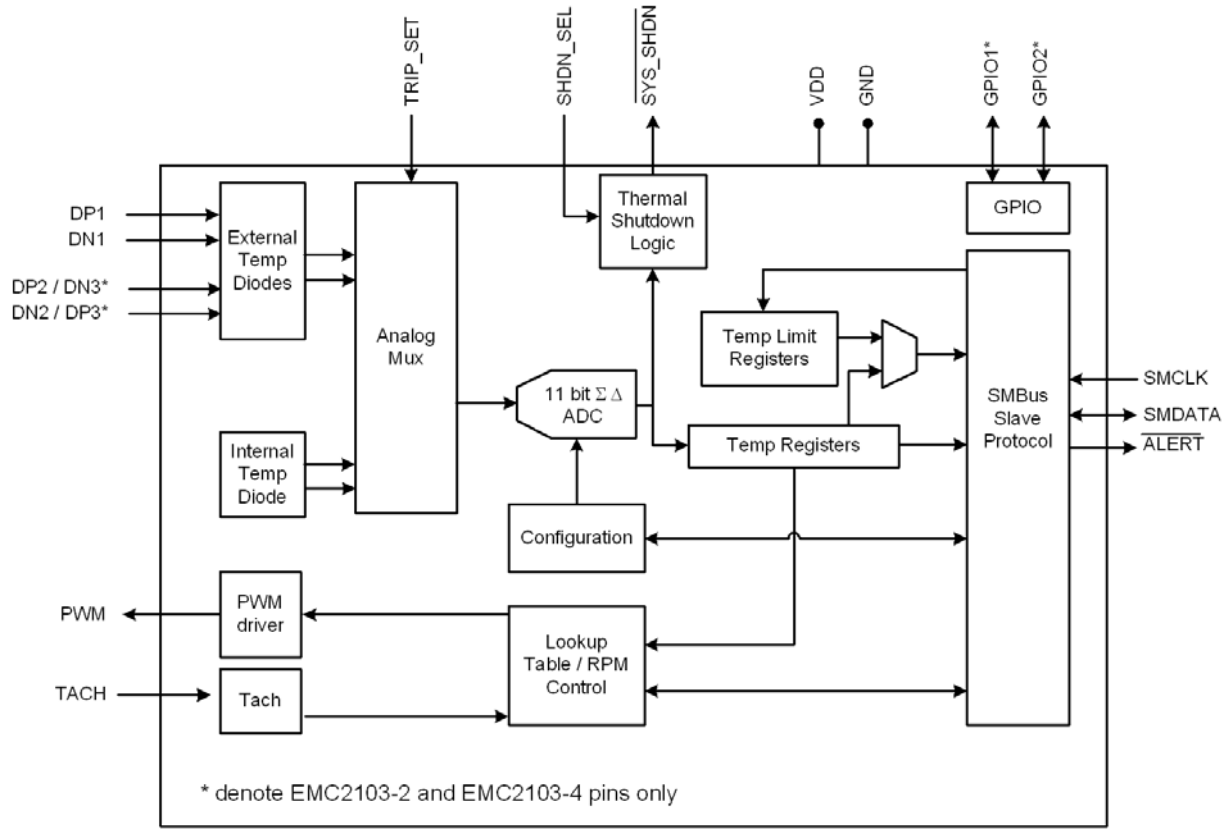


Figure 1.1 EMC2103 Block Diagram

Chapter 2 Pin Layout

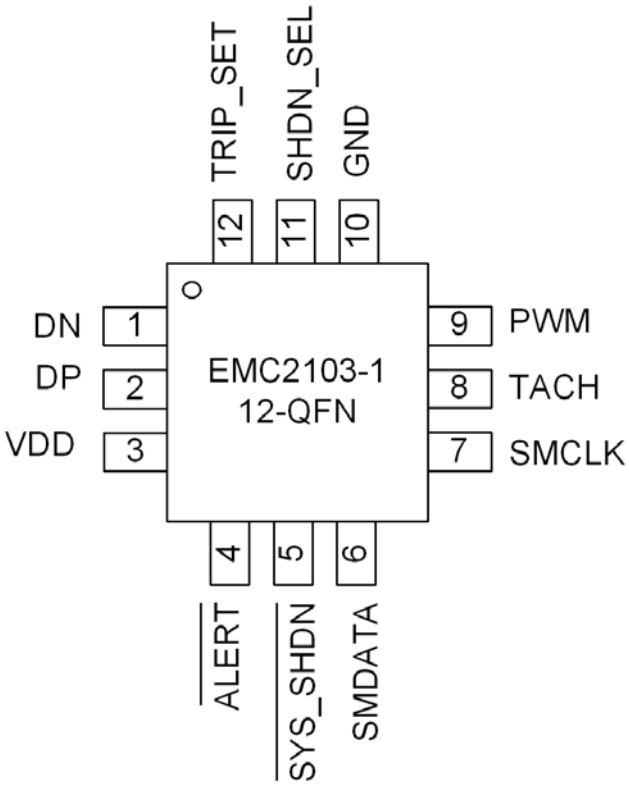


Figure 2.1 EMC2103-1 Pin Diagram (12-Pin QFN)

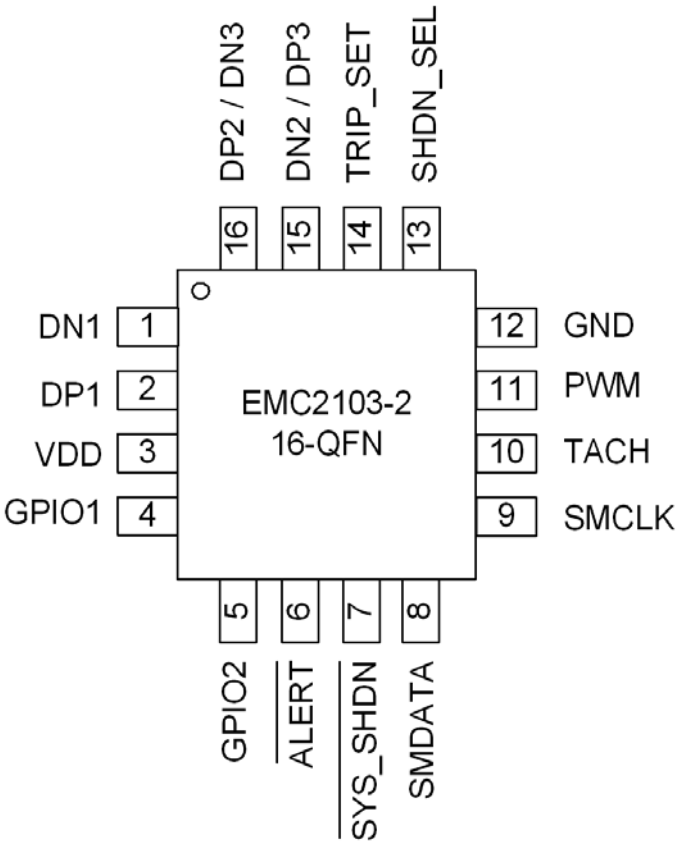


Figure 2.2 EMC2103-2 and EMC2103-4 Pin Diagram (16-Pin QFN)

Table 2.1 Pin Description for EMC2103

PIN NUMBER EMC2103-1	PIN NUMBER EMC2103-2 AND EMC2103-4	PIN NAME	PIN FUNCTION	PIN TYPE
1	1	DN1	Negative (cathode) analog input for External Diode 1.	AIO
2	2	DP1	Positive (anode) analog input for External Diode 1.	AIO
3	3	VDD	Power Supply	Power
N/A	4	GPIO1	GPI1 - General Purpose Input (default)	DI (5V)
			GPO1 - Open Drain digital output	OD (5V)
			GPO1 - Push-pull digital output	DO

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Table 2.1 Pin Description for EMC2103 (continued)

PIN NUMBER EMC2103-1	PIN NUMBER EMC2103-2 AND EMC2103-4	PIN NAME	PIN FUNCTION	PIN TYPE
N/A	5	GPIO2	GPI2 - General Purpose Input (default)	DI (5V)
			GPO2 - Open Drain digital output	OD (5V)
			GPO2 - Push-pull digital output	DO
4	6	$\overline{\text{ALERT}}$	Active low interrupt - requires external pull-up resistor.	OD (5V)
5	7	$\overline{\text{SYS_SHDN}}$	Active low Critical / Thermal Shutdown output - requires external pull-up resistor	OD (5V)
6	8	SMDATA	SMBus data input/output - requires external pull-up resistor	DIOD (5V)
7	9	SMCLK	SMBus clock input - requires external pull-up resistor	DI (5V)
8	10	TACH	Tachometer input for the Fan	DI (5V)
9	11	PWM	PWM - Open Drain PWM drive output for the Fan (default)	OD (5V)
			PWM - Push-Pull PWM drive output for the Fan	DO
10	12	GND	Ground connection	Power
11	13	SHDN_SEL	Selects the hardware shutdown channel and operating mode	AIO
12	14	TRIP_SET	Voltage input to set the Critical / Thermal Shutdown threshold	AIO
N/A	15	DN2 / DP3	Negative (cathode) analog input for External Diode 2 and positive (anode) analog input for External Diode 3	AIO
N/A	16	DP2 / DN3	Positive (anode) analog input for External Diode 2 and negative (cathode) connection for External Diode 3	AIO

The pin type are described in detail below. All pins labelled with (5V) are 5V tolerant.

APPLICATION NOTE: For the 5V tolerant pins that have a pull-up resistor, the voltage difference between VDD and the 5V tolerant pad must never be more than 3.6V.

Table 2.2 Pin Types

PIN TYPE	DESCRIPTION
Power	This pin is used to supply power or ground to the device.
DI	Digital Input - this pin is used as a digital input. This pin is 5V tolerant.
AIO	Analog Input / Output - this pin is used as an I/O for analog signals.
DO	Push / Pull Digital Output - this pin is used as a digital output. It can both source and sink current.
DIOD	Digital Input / Open Drain Output - this pin is used as a digital I/O. When it is used as an output, it is open drain and requires a pull-up resistor. This pin is 5V tolerant.
OD	Open Drain Digital Output - this pin is used as a digital output. It is open drain and requires a pull-up resistor. This pin is 5V tolerant.

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Chapter 3 Electrical Characteristics

Table 3.1 Absolute Maximum Ratings

Voltage on 5V tolerant pins (V_{5VT_pin})	-0.3 to 5.5	V
Voltage on 5V tolerant pins ($\|V_{5VT_pin} - V_{DD}\|$) (see Note 3.1)	-0.3 to 3.6	V
Voltage on VDD pin	-0.3 to 4	V
Voltage on any other pin to GND	-0.3 to V_{DD} + 0.3	V
Package Power Dissipation	0.8W up to T_A = 85°C	W
Junction to Ambient (θ_{JA})	50	°C/W
Operating Ambient Temperature Range	-40 to 125	°C
Storage Temperature Range	-55 to 150	°C
ESD Rating, All Pins, HBM	2000	V

Note: Stresses above those listed could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied. When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

Note: All voltages are relative to ground.

Note 3.1 For the 5V tolerant pins that have a pull-up resistor, the pull-up voltage must not exceed 3.6V when the EMC2103 is unpowered.

Note: θ_{JA} numbers are based on a recommended four 12 mil vias connecting the thermal pad to PCB ground.

3.1 Electrical Specifications

Table 3.2 Electrical Specifications

VDD = 3V to 3.6V, T_A = -40°C to 125°C, all Typical values at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
DC Power						
Supply Voltage	V_{DD}	3	3.3	3.6	V	
Supply Current	I_{DD}		1.3	1.8	mA	4 Conversions / second, Fan Driver active at maximum PWM frequency, Dynamic Averaging Enabled (EMC2103-2 and EMC2103-4)
			1	1.5	mA	4 Conversions / second, Fan Driver active at maximum PWM frequency, Dynamic Averaging Enabled (EMC2103-1)
			450	750	uA	1 Conversions / second, Fan Driver not active, Dynamic Averaging Disabled
First Conversion Ready	t_{CONV_T}		175	300	ms	Time after power up before all channels updated
SMBus Delay	t_{SMB_D}		10	15	ms	Time before SMBus communications should be sent by host
External Temperature Monitors						
Temperature Accuracy			±0.5	±1	°C	60°C < T_{DIODE} < 125°C 30°C < T_A < 100°C
			±1	±2	°C	-40°C < T_{DIODE} < 125°C
Temperature Resolution			0.125		°C	
Diode decoupling capacitor	C_{FILTER}		2200	2700	pF	Connected across external diode, CPU, GPU, or AMD diode
Resistance Error Corrected	R_{SERIES}		100		Ohm	Sum of series resistance in both DP and DN lines
Internal Temperature Monitor						
Temperature Accuracy	T_{DIE}		±1	±2	°C	-40°C ≤ TA ≤ 125°C
	T_{DIE}			±1.5	°C	0°C ≤ T_A ≤ 85°C
Temperature Resolution			0.125		°C	
PWM Fan Driver						
PWM Resolution	PWM		256		Steps	
PWM Duty Cycle	DUTY	0		100	%	

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Table 3.2 Electrical Specifications (continued)

VDD = 3V to 3.6V, T_A = -40°C to 125°C, all Typical values at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
TRIP_SET Measurement						
Voltage Accuracy	V_{TRIP}		0.5	1	%	
Temperature Decode Accuracy	T_{TRIP}			0.5	°C	1% external resistor
			1	2	°C	5% external resistor
RPM Based Fan Controller						
Tachometer Range	TACH	480		16000	RPM	
Tachometer Setting Accuracy	Δ_{TACH}		±2.5	±5	%	
Digital I/O pins						
Input High Voltage	V_{IH}	2.0			V	
Input Low Voltage	V_{IL}			0.8	V	
Output High Voltage	V_{OH}	VDD - 0.4			V	8 mA current drive
Output Low Voltage	V_{OL}			0.4	V	8 mA current sink
Leakage Current	I_{LEAK}			±5	uA	$\overline{ALERT}$ and $\overline{SYS_SHDN}$ pins Device powered or unpowered T_A < 85°C pull-up voltage ≤ 3.6V

3.2 SMBus Electrical Specifications (Client Mode)

Table 3.3 SMBus Electrical Specifications

VDD= 3V to 3.6V, T_A = -40°C to 125°C Typical values are at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
SMBus Interface						
Input High/Low Current	I_{IH} / I_{IL}			±5	uA	Device powered or unpowered T_A < 85°C
Input Capacitance	C_{IN}		4	10	pF	
SMBus Timing						
Clock Frequency	f_{SMB}	10		400	kHz	
Spike Suppression	t_{SP}			50	ns	
Bus free time Start to Stop	t_{BUF}	1.3			us	
Setup Time: Start	$t_{SU:STA}$	0.6			us	
Setup Time: Stop	$t_{SU:STP}$	0.6			us	

Table 3.3 SMBus Electrical Specifications (continued)

VDD= 3V to 3.6V, T_A = -40°C to 125°C Typical values are at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
Data Hold Time	$t_{HD:DAT}$	0.6		6	us	
Data Setup Time	$t_{SU:DAT}$	0.6		72	us	
Clock Low Period	t_{LOW}	1.3			us	
Clock High Period	t_{HIGH}	0.6			us	
Clock/Data Fall time	t_{FALL}			300	ns	Min = $20+0.1C_{LOAD}$ ns
Clock/Data Rise time	t_{RISE}			300	ns	Min = $20+0.1C_{LOAD}$ ns
Capacitive Load	C_{LOAD}			400	pF	Total per bus line

3.3 EEPROM Loader Electrical Specifications

The EEPROM Loader is only active in the EMC2103-4 device when enabled via the SHDN_SEL pull-up resistor (see Section 5.1.1).

Table 3.4 EEPROM Loader Electrical Specifications

V_{DD} = 3.0V to 3.6V, T_A = -40°C - 125°C, Typical values are at T_A = 27°C unless otherwise noted						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
Interface						
Input High/Low Current	I_{IH} / I_{IL}			±5	uA	Powered or unpowered
Hysteresis			420		mV	
Input Capacitance	C_{IN}			10	pF	
Timing						
Loading Delay	t_{DLY}		10		ms	Delay after power-up until EEPROM loading begins. (See Section 4.9.)
Loading Time	t_{LOAD}		50		ms	
Clock Frequency	f_{SMB}		50		kHz	
Spike Suppression	t_{SP}			50	ns	
Bus free time Start to Stop	t_{BUF}	1.3			us	
Hold Time: Start	$t_{HD:STA}$	0.6			us	
Setup Time: Start	$t_{SU:STA}$	0.6			us	
Setup Time: Stop	$t_{SU:STO}$	0.6			us	
Data Hold Time	$t_{HD:DAT}$	0.3			us	
Data Setup Time	$t_{SU:DAT}$	100			ns	

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Table 3.4 EEPROM Loader Electrical Specifications (continued)

V_{DD} = 3.0V to 3.6V, T_A = -40°C - 125°C, Typical values are at T_A = 27°C unless otherwise noted						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
Clock Low Period	t_{LOW}	1.3			us	
Clock High Period	t_{HIGH}	0.6			us	
Clock/Data Fall time	t_{FALL}			300	ns	Min = 20+0.1C_{LOAD} ns
Clock/Data Rise time	t_{RISE}			300	ns	Min = 20+0.1C_{LOAD} ns
Capacitive Load	C_{LOAD}			400	pF	Total per bus line

Chapter 4 Communications

4.1 System Management Bus Interface Protocol

The EMC2103 communicates with a host controller, such as an SIO, through the SMBus. The SMBus is a two-wire serial communication protocol between a computer host and its peripheral devices. A detailed timing diagram is shown in Figure 4.1. Stretching of the SMCLK signal is supported, however the EMC2103 will not stretch the clock signal.

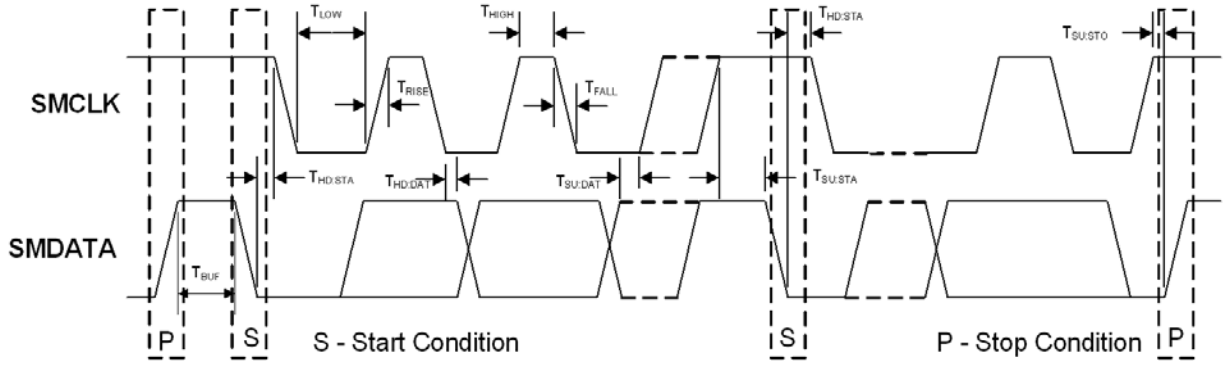


Figure 4.1 SMBus Timing Diagram

The EMC2103 contains a single SMBus interface. The EMC2103 client interfaces are SMBus 2.0 compatible and support Send Byte, Read Byte, Receive Byte and the Alert Response Address as valid protocols. These protocols are used as shown below.

All of the below protocols use the convention in Table 4.1.

Table 4.1 Protocol Format

DATA SENT TO DEVICE	DATA SENT TO THE HOST
# of bits sent	# of bits sent

4.2 Write Byte

The Write Byte is used to write one byte of data to the registers as shown below Table 4.2:

Table 4.2 Write Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	REGISTER DATA	ACK	STOP
0 -> 1	0101_110	0	0	0 -> 1	0	XXh	0	1 -> 0

4.3 Read Byte

The Read Byte protocol is used to read one byte of data from the registers as shown in Table 4.3.

Table 4.3 Read Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	START	SLAVE ADDRESS	RD	ACK	REGISTER DATA	NACK	STOP
0 -> 1	0101_110	0	0	XXh	0	0 -> 1	0101_110	1	0	XXh	1	1 -> 0

4.4 Send Byte

The Send Byte protocol is used to set the internal address register pointer to the correct address location. No data is transferred during the Send Byte protocol as shown in Table 4.4.

Table 4.4 Send Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	STOP
0 -> 1	0101_110	0	0	XXh	1	1 -> 0

4.5 Receive Byte

The Receive Byte protocol is used to read data from a register when the internal register address pointer is known to be at the right location (e.g. set via Send Byte). This is used for consecutive reads of the same register as shown in Table 4.5.

Table 4.5 Receive Byte Protocol

START	SLAVE ADDRESS	RD	ACK	REGISTER DATA	NACK	STOP
0 -> 1	0101_110	1	0	XXh	1	1 -> 0

4.6 Alert Response Address

The $\overline{\text{ALERT}}$ output can be used as a processor interrupt or as an SMBus Alert when configured to operate as an interrupt.

When it detects that the $\overline{\text{ALERT}}$ pin is asserted, the host will send the Alert Response Address (ARA) to the general address of 0001_100b. All devices with active interrupts will respond with their client address as shown in Table 4.6.

Table 4.6 Alert Response Address Protocol

START	ALERT RESPONSE ADDRESS	RD	ACK	DEVICE ADDRESS	NACK	STOP
0 -> 1	0001_100	1	0	0101_1100	1	1 -> 0

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The EMC2103 will respond to the ARA in the following way if the $\overline{\text{ALERT}}$ pin is asserted.

1. Send Slave Address and verify that full slave address was sent (i.e. the SMBus communication from the device was not prematurely stopped due to a bus contention event).
2. Set the MASK bit to clear the $\overline{\text{ALERT}}$ pin.

4.7 SMBus Address

The EMC2103 SMBus Address is fixed at 0101_110xb.

Other addresses are available. Contact Microchip for details.

Attempting to communicate with the EMC2103 SMBus interface with an invalid slave address or invalid protocol will result in no response from the device and will not affect its register contents.

4.8 SMBus Time-out

The EMC2103 includes an SMBus time-out feature. Following a 30ms period of inactivity on the SMBus, the device will time-out and reset the SMBus interface.

4.9 Programming from EEPROM

Programming from EEPROM is only available for EMC2103-4 device. When enabled via the SHDN_SEL pin (see Section 5.1.1), the EMC2103 will attempt to program itself from an EEPROM. During this time, the EMC2103 acts as a simple SMBus Master to read data from a connected EEPROM using the following procedure.

1. After power-up the EMC2103 waits for 10ms with the SMDATA and SMCLK pins tri-stated.
2. Once the wait period has elapsed, the EMC2103 sends a START signal followed by the 7 bit client address 1010_000b followed by a ‘0’ and waits for an ACK signal from the EEPROM.
3. When the EEPROM sends the ACK signal, the EMC2103 will send a second start signal and continue sending the Block Read Command (see Table 4.7) to the same slave address. It reads 256 data bytes from the EEPROM sending an ACK between each data byte. When 256 data bytes have been received, it sends a NACK signal followed by a STOP bit.
4. Resets the device as an SMBus Client with slave address 0101_110xb.

If the EMC2103 does not receive an acknowledge bit from the EEPROM then the following will occur:

1. The $\overline{\text{ALERT}}$ pin will be asserted and will remain asserted until a Host device initiates communication with the EMC2103 and reads the Status Register. The $\overline{\text{ALERT}}$ pin will be de-asserted after a single Status Register read.
2. The EMC2103 will reset its SMBus protocol as a slave interface and start operating from the default conditions with slave address 0101_110xb.

Table 4.7 Block Read Byte Protocol

START	SLAVE ADDRESS	WR	ACK	Register Address	ACK	START	SLAVE ADDRESS	RD	ACK	Register Data (00h)	. . .
0 -> 1	1010_000	0	0	00h	0	0 -> 1	1010_000	1	0	XXh	. . .
ACK	**Register Data (01h)**	**ACK**	**Register Data (02h)**	**ACK**	**Register Data (02h)**	**. . .**	**ACK**	**Register Data (FFh)**		**NACK**	**STOP**
0	XXh	0	XXh	0	XXh	. . .	0	XXh		1	1 -> 0

Note: The shaded columns represent data sent from the EMC2103 to the EEPROM device.

APPLICATION NOTE: It is recommended that the EEPROM that is used be an AT24C02B or equivalent device. The EEPROM slave address must be 1010_000xb. The device must support a block-read command, 8-bit addressing, and 8-bit data formatting using a 2-wire bus. The device must support 3.3V digital switching logic and may not pull the SMCLK and SMDATA pins above 5V. Data must be transmitted MSB first.

APPLICATION NOTE: No other SMBus Master should exist on the SMDATA and SMCLK lines. The presence of another SMBus Master will cause errors in reading from the EEPROM.

The EEPROM should be loaded to mirror the register set of the EMC2103 with the desired configuration set. All undefined registers in the EMC2103 register set should be loaded with 00h in the EEPROM. Likewise, all registers that are read-only in the EMC2103 register set should be loaded with 00h in the EEPROM.

Because of the interaction between the Fan Control Look-up Tables and the Fan Configuration Register, the EEPROM Loader stores the contents of the Fan Configuration Registers and updates these registers at the end of the EEPROM loading cycle.

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Chapter 5 General Description

The EMC2103 is an SMBus compliant fan controller with one external (EMC2103-2 and EMC2103-4 offer up to three external diode channels) and one internal temperature channels. The fan driver can be operated using two methods each with two modes. The methods include an RPM based Fan Speed Control Algorithm and a direct PWM drive setting. The modes include manually programming the desired settings or using the internal programmable temperature look-up table to select the desired setting based on measured temperature.

The temperature monitors offer 1°C accuracy (for external diodes) with sophisticated features to reduce errors introduced by series resistance and beta variation of substrate thermal diode transistors commonly found in processors (including support of the BJT or transistor model for a CPU diode).

The EMC2103 allows the user to program temperatures generated from external sources to control the fan speed. This functionality also supports DTS data from the CPU. By pushing DTS or standard temperature values into dedicated registers, the external temperature readings can be used in conjunction with the external diode(s) and internal diode to control the fan speed.

The EMC2103 also includes a hardware programmable temperature limit and dedicated system shutdown output for thermal protection of critical circuitry.

Figure 5.1 shows a system diagram of the EMC2103.

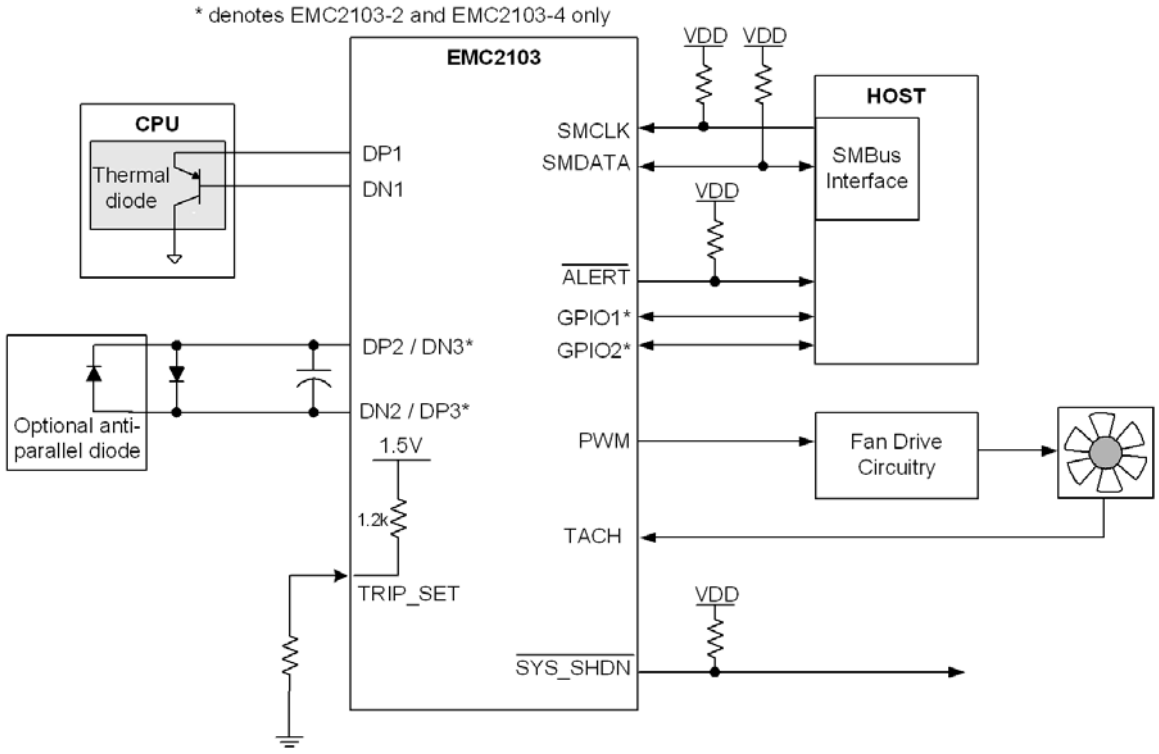


Figure 5.1 System Diagram for EMC2103

5.1 Critical/Thermal Shutdown

The EMC2103 provides a hardware Critical/Thermal Shutdown function for systems. Figure 5.2 is a block diagram of this Critical/Thermal Shutdown function. The Critical/Thermal Shutdown function accepts configuration information from the fixed states of the SHDN_SEL pin as described in Section 5.1.1.

Each of the software programmed temperature limits can be optionally configured to act as inputs to the Critical / Thermal Shutdown independent of the hardware shutdown operation. When configured to operate this way, the $\overline{\text{SYS_SHDN}}$ pin will be asserted when the temperature meets or exceeds the limit. The pin will be released when the temperature drops below the limit however the individual status bits will not be cleared if set (see Section 6.13).

The analog portion of the Critical/Thermal Shutdown function monitors the hardware determined shutdown channel (see Section 5.1.1). This measured temperature is then compared with TRIP_SET point. This TRIP_SET point is set by the system designer with a single external resistor divider as described in Section 5.1.2.

The $\overline{\text{SYS_SHDN}}$ is asserted when the indicated temperature meets or exceeds the temperature threshold (T_P) established by the TRIP_SET input pin for a number of consecutive measurements defined by the fault queue. If the HW_SHDN output is asserted and the temperature drops below the threshold, then it will be set to a logic ‘0’ state.

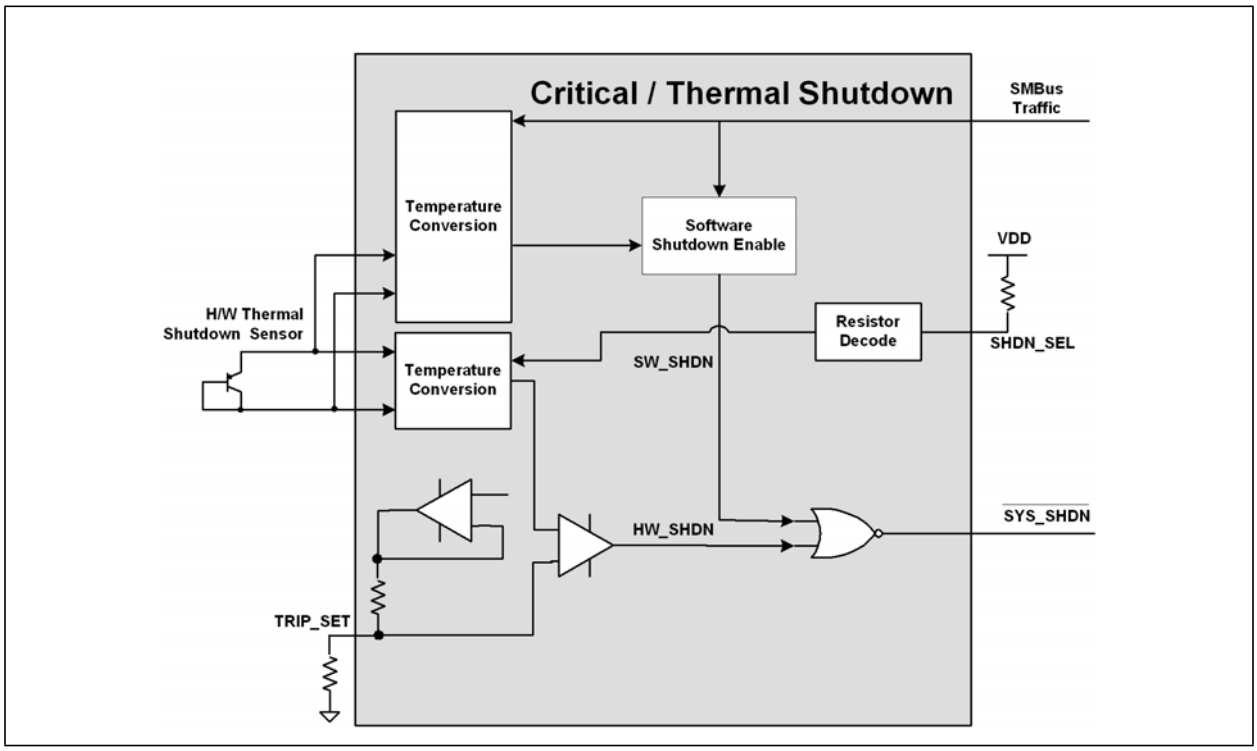


Figure 5.2 Block Diagram of Critical / Thermal Shutdown

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5.1.1 SHDN_SEL Pin

The EMC2103 has a ‘strappable’ input (SHDN_SEL) allowing for configuration of the hardware Critical/Thermal Shutdown input channel. The pull-up resistor used on this pin identifies which configuration setting is used as shown in Table 5.1.

.

Table 5.1 SHDN_SEL Pin Decode

PULL UP RESISTOR	MODE/SHUTDOWN CHANNEL	EXTERNAL DIODE 1 CONFIG	EXTERNAL DIODE 2 CONFIG
≤ 4.7k Ohm	AMD CPU on External Diode 1	Beta Compensation disabled REC disabled Beta and REC controls are locked	Beta Compensation enabled (auto) REC enabled Beta and REC controls are not locked
6.8k Ohm	2N3904 on External Diode 1	Beta Compensation disabled REC enabled Beta and REC controls are locked	Beta Compensation enabled (auto) REC enabled Beta and REC controls are not locked
10k Ohm	Intel CPU on External Diode 1	Beta Compensation enabled and set to auto REC enabled Beta and REC controls are locked	Beta Compensation enabled (auto) REC enabled Beta and REC controls are not locked
15k Ohm	Internal Diode See Note 5.2	Beta Compensation enabled (auto) REC enabled Beta and REC controls are locked	Beta Compensation enabled (auto) REC enabled Beta and REC controls are not locked
22k Ohm	Intel CPU on External Diode 2 - see Note 5.1 and Note 5.2	Beta Compensation disabled REC enabled Beta and REC controls are not locked	Beta Compensation enabled (auto) REC enabled Beta and REC controls are locked
≥ 33k Ohm	Intel CPU on External Diode 1 See Note 5.2	Beta Compensation enabled (auto) REC enabled Beta and REC controls are locked	Beta Compensation enabled (auto) REC enabled Beta and REC controls are not locked

Note 5.1 For the EMC2103-1, the decode for a 22k Ohm resistor on the SHDN_SEL pin will be to use the External Diode 1 channel in Diode Mode (the same as the decode for a 6.8k Ohm resistor) as the hardware shutdown device.

Note 5.2 Load from EEPROM enabled (EMC2103-4 only - see Section 4.9).

5.1.2 TRIP_SET Pin

The EMC2103's TRIP_SET pin is an analog input to the Critical/Thermal Shutdown block which sets the Thermal Shutdown temperature. The system designer creates a voltage level at the input through a simple resistor connected to GND as shown in Figure 5.2. The value of this resistor is used to create an input voltage on the TRIP_SET pin which is translated into a temperature ranging from 65°C to 127°C as shown in Table 5.2

APPLICATION NOTE: Current only flows when the TRIP_SET pin is being monitored. At all other times, the internal reference voltage is removed and the TRIP_SET pin will be pulled down to ground.

APPLICATION NOTE: The TRIP_SET pin circuitry is designed to use a 1% resistor externally. Using a 1% resistor will result in the Thermal / Critical Shutdown temperature being decoded correctly. If a 5% resistor is used, then the Thermal / Critical Shutdown temperature may be decoded with as much as ±1°C error.

Table 5.2 TRIP_SET Resistor Setting

T_{TRIP} (°C)	RSET (1%)	T_{TRIP} (°C)	RSET (1%)
65	0.0	97	1240
66	28.7	98	1330
67	48.7	99	1400
68	69.8	100	1500
69	90.9	101	1580
70	113	102	1690
71	137	103	1820
72	158	104	1960
73	182	105	2050
74	210	106	2210
75	237	107	2370
76	261	108	2550
77	294	109	2740
78	324.	110	2940
79	348	111	3160
80	383	112	3480
81	412	113	3740
82	453	114	4120
83	487	115	4530
84	523	116	4990
85	562	117	5490
86	604	118	6040
87	649	119	6810
88	698	120	7870
89	750	121	9090
90	787	122	10700
91	845	123	12700
92	909	124	15800
93	953	125	20500

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Table 5.2 TRIP_SET Resistor Setting (continued)

T_{TRIP} (°C)	RSET (1%)	T_{TRIP} (°C)	RSET (1%)
94	1020	126	29400
95	1100	127	49900
96	1150	65	Open

5.2 Fan Control Modes of Operation

The EMC2103 has four modes of operation for the fan driver. Each mode uses Ramp Rate control and the Spin Up Routine

1. PWM Setting Mode - in this mode of operation, the user directly controls the PWM duty cycle setting. Updating the Fan Driver Setting Register (see Section 6.20) will instantly update the fan drive.
   - This is the default mode. The PWM Setting Mode is enabled by clearing both the EN_ALGO bit in the Fan Configuration Register (see Section 6.22) and the LUT_LOCK bit in the Look Up Table Configuration Register (see Section 6.32).
   - Whenever the PWM Setting Mode is enabled the current drive will be changed to what was last written into the Fan Driver Setting Register.
2. Fan Speed Control Mode (FSC) - in this mode of operation, the user determines a fan speed and the drive setting is automatically updated to achieve this target speed.
   - This mode is enabled by clearing the LUT_LOCK bit in the Look Up Table (LUT) Configuration Register and setting the EN_ALGO bit in the Fan Configuration Register.
3. Using the Look Up Table with Fan Drive Settings (PWM Setting w/ LUT Mode) - In this mode of operation, the user programs the Look Up Table with PWM duty cycle settings and corresponding temperature thresholds. The fan drive is set based on the measured temperatures and the corresponding drive settings.
   - This mode is enabled by programming the Look Up Table then setting the LUT_LOCK bit while the RPM / PWM bit is set to a ‘1’ (see Section 6.32)
4. Using the Look Up Table with Fan Speed Control algorithm (FSC w/ LUT Mode)- In this mode of operation, the user programs the Look Up Table with fan speed target values and corresponding temperature thresholds. The TACH Target Register will be set based on the measured temperatures and the corresponding target settings. The PWM drive settings will be determined automatically based on the RPM based Fan Speed Control Algorithm
   - This mode is enabled by programming the Look Up Table then setting the LUT_LOCK bit while the RPM / PWM bit is set to ‘0’ (see Section 6.32).

Table 5.3 Fan Controls Active for Operating Mode

DIRECT PWM SETTING MODE	FSC MODE	DIRECT PWM SETTING W/ LUT MODE	FSC W/ LUT MODE
Fan Driver Setting (read / write)	Fan Driver Setting (read only)	Fan Driver Setting (read only)	Fan Driver Setting (read only)
EDGES[1:0]	EDGES[1:0] (Fan Configuration)	EDGES[1:0]	EDGES[1:0]
-	RANGE[1:0] (Fan Configuration)	-	RANGE[1:0] (Fan Configuration)
UPDATE[2:0] (Fan Configuration)	UPDATE[2:0] (Fan Configuration)	UPDATE[2:0] (Fan Configuration)	UPDATE[2:0] (Fan Configuration)

Table 5.3 Fan Controls Active for Operating Mode (continued)

DIRECT PWM SETTING MODE	FSC MODE	DIRECT PWM SETTING W/ LUT MODE	FSC W/ LUT MODE
LEVEL (Spin Up Configuration)	LEVEL (Spin Up Configuration)	LEVEL (Spin Up Configuration)	LEVEL (Spin Up Configuration)
SPINUP_TIME[1:0] (Spin Up Configuration)	SPINUP_TIME[1:0] (Spin Up Configuration)	SPINUP_TIME[1:0] (Spin Up Configuration)	SPINUP_TIME[1:0] (Spin Up Configuration)
Fan Step	Fan Step	Fan Step	Fan Step
-	Fan Minimum Drive		Fan Minimum Drive
Valid TACH Count	Valid TACH Count	Valid TACH Count	Valid TACH Count
-	TACH Target (read / write)	-	TACH Target (read only)
TACH Reading	TACH Reading	TACH Reading	TACH Reading
-	-	Look Up Table Drive / Temperature Settings (read only)	Look up Table Drive / Temperature Settings (read only)
-	DRIVE_FAIL_CNT [1:0] (Spin Up Configuration) + Fan Drive Fail Band	-	DRIVE_FAIL_CNT [1:0] (Spin Up Configuration) + Fan Drive Fail Band

5.3 PWM Fan Driver

The EMC2103 supports a high or low frequency PWM driver. The output can be configured as either push-pull or open drain and the frequency ranges from 9.5Hz to 26kHz in four programmable frequency bands.

5.4 Fan Control Look-Up Table

The EMC2103 uses a look-up table to apply a user-programmable fan control profile based on measured temperature to the fan driver. In this look-up table, each temperature channel is allowed to control the fan drive output independently (or jointly) by programming up to eight pairs of temperature and drive setting entries.

The user programs the look-up table based on the desired operation. If the RPM based Fan Speed Control Algorithm is to be used (see Section 5.5), then the user must program a fan speed target for each temperature setting of interest. Alternately, if the RPM based Fan Speed Control Algorithm is not to be used, then the user must program a PWM setting for each temperature setting of interest.

If the measured temperature on the External Diode channel meets or exceeds any of the temperature thresholds for any of the channels, the fan output will be automatically set to the desired setting corresponding to the exceeded temperature. In cases where multiple temperature channel thresholds are exceeded, the highest fan drive setting will take precedence. Figure 5.3 shows an example of this behavior using a single channel.

When the measured temperature drops to a point below a lower threshold minus the hysteresis value, the fan output will be set to the corresponding lower set point.

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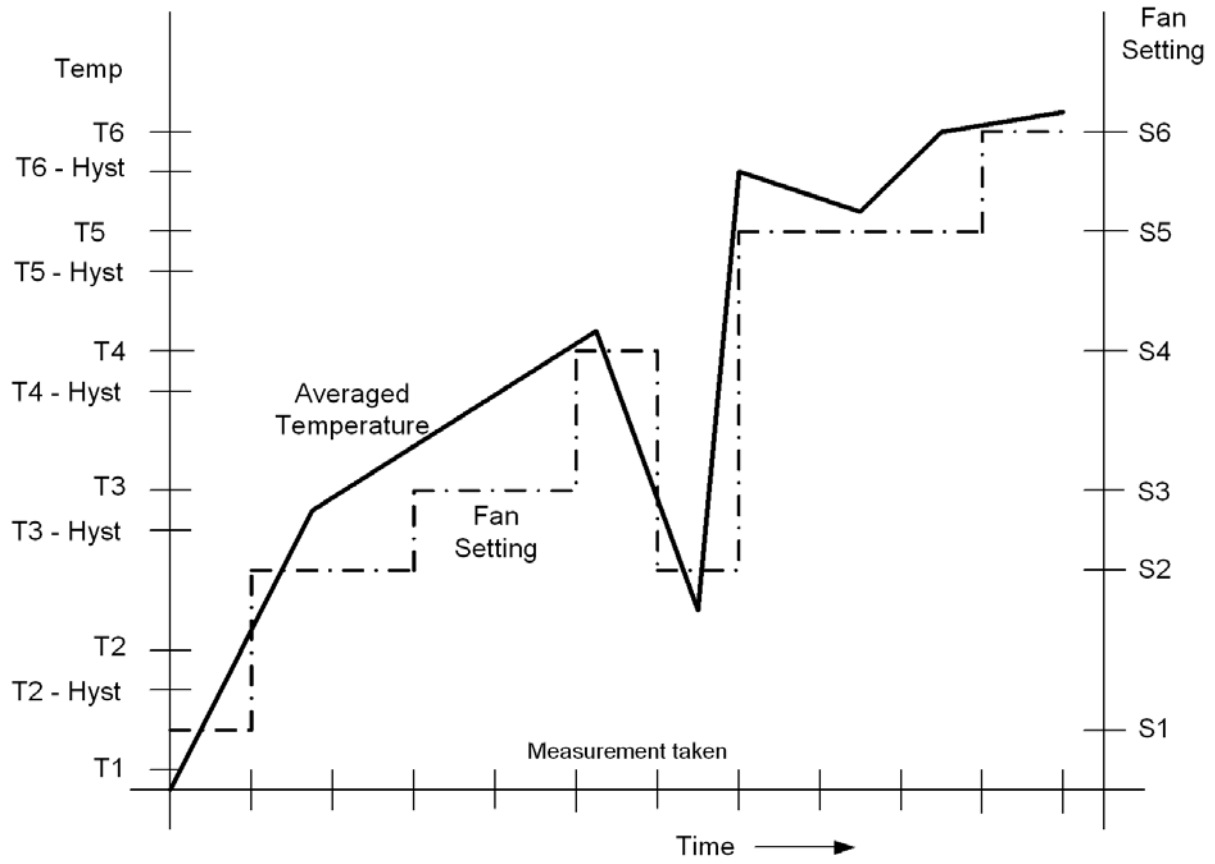


Figure 5.3 Fan Control Look-Up Table Example

5.4.1 Programming the Look Up Table

When the Look Up Table is used, it must be loaded and configured correctly based on the system requirements. The following steps outline the procedure.

1. Determine whether the Look Up Table will drive a PWM duty cycle or a tachometer target value and set the RPM / PWM bit in the Fan LUT Configuration Register (see Section 6.32).
2. Determine which measurement channels (up to four) are to be used with the Look Up Table and set the TEMP3_CFG and TEMP4_CFG bits accordingly in the Fan LUT Configuration Register.
3. For each step to be used in the LUT, set the Fan Setting (either PWM or TACH Target as set by the RPM / PWM bit). If a setting is not used, then set it to FFh (if a PWM) or 00h (if a TACH Target). Load the lowest settings first in ascending order (i.e. Fan Setting 1 is the lowest setting greater than “off”. Fan Setting 2 is the next highest setting, etc.). See Section 6.33.
4. For each step to be used in the LUT, set each of the measurement channel thresholds. These values must be set in the same data format that the data is presented. If DTS is to be used, then the format should be in temperature with a maximum threshold of 100°C (64h). If a measurement channel is not used, then set the threshold at FFh.
5. Update the threshold hysteresis to be smaller than the smallest table step.
6. Configure the RPM based Fan Speed Control Algorithm if it is to be used. See Section 5.5.1 for more details.

7. Set the LUT_LOCK bit to enable the Look Up Table and begin fan control in the Fan LUT Configuration Register.

5.4.2 DTS Support

The EMC2103 supports DTS (Intel's Digital Temperature Sensor) data in the Fan Control Look Up Table. Intel's DTS data is a positive number that represents the processor's relative temperature below a fixed value called $T_{CONTROL}$ which is generally equal to 100°C for Intel Mobile processors. For example, a DTS value of 10°C means that the actual processor temperature is 10°C below $T_{CONTROL}$ or equal to 90°C.

Either or both of the Pushed Temperature Registers can be written with DTS data and used to control the fan driver. When DTS data is entered, then the USE_DTS_Fx bit must be set in the Fan LUT Configuration register. Once this bit is set, the DTS data entered is automatically subtracted from a value of 100°C. This delta value is then used in the Look Up Table as standard temperature data.

APPLICATION NOTE: The device is designed with the assumption that $T_{CONTROL}$ is 100°C. As such, all DTS related conversions are done based on this value including Look Up Table comparisons. If $T_{CONTROL}$ is adjusted (i.e. $T_{CONTROL}$ is shifted to 105°C), then all of the Look Up Table thresholds should be adjusted by a value equal to $T_{CONTROL}$ - 100°C.

5.5 RPM based Fan Speed Control Algorithm (FSC)

The EMC2103 includes an RPM based Fan Speed Control Algorithm.

This fan control algorithm uses Proportional, Integral, and Derivative terms to automatically approach and maintain the system's desired fan speed to an accuracy directly proportional to the accuracy of the clock source. Figure 5.4 shows a simple flow diagram of the RPM based Fan Speed Control Algorithm operation.

The desired tachometer count is set by the user inputting the desired number of 32.768KHz cycles that occur per fan revolution. This is done by either manually setting the TACH Target Register or by programming the Temperature Look-Up Table. The user may change the target count at any time. The user may also set the target count to FFh in order to disable the fan driver for lower current operation.

For example, if a desired RPM rate for a 2-pole fan is 3000 RPM then the user would input the hexidecimal equivalent of 1296 (51h in the TACH Target Register). This number represents the number of 32.768KHz cycles that would occur during the time it takes the fan to complete a single revolution when it is spinning at 3000RPMs. See Section 6.31, "TACH Reading Register" for more information.

The EMC2103's RPM based Fan Speed Control Algorithm has programmable configuration settings for parameters such as ramp-rate control and spin up conditions. The fan driver automatically detects and attempts to alleviate a stalled/stuck fan condition while also asserting the $\overline{ALERT}$ pin. The EMC2103 works with fans that operate up to 16,000 RPMs and provides a valid tachometer signal.

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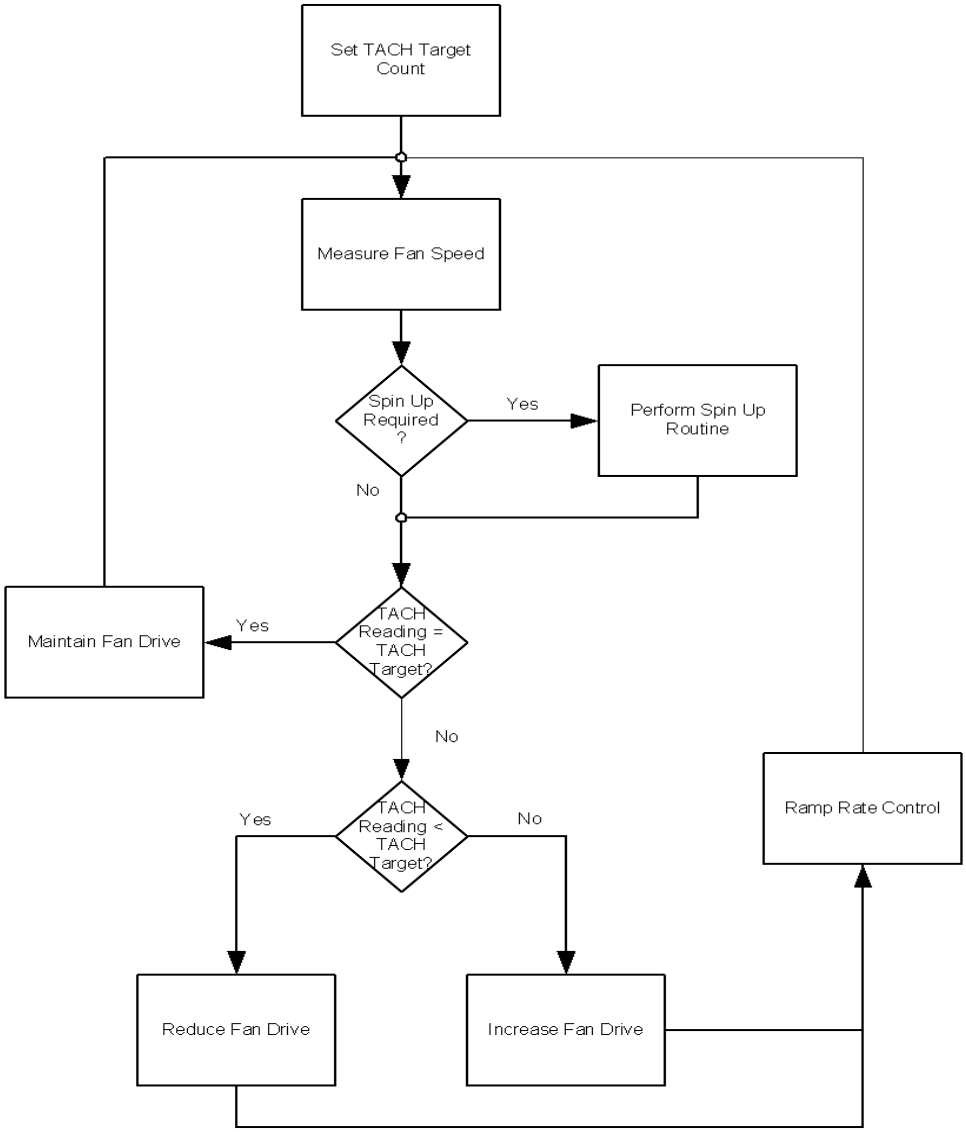


Figure 5.4 RPM based Fan Speed Control Algorithm

5.5.1 Programming the RPM Based Fan Speed Control Algorithm

The RPM based Fan Speed Control Algorithm powers-up disabled. The following registers control the algorithm. The EMC2103 fan control registers are pre-loaded with defaults that will work for a wide variety of fans so only the TACH Target Register is required to set a fan speed. The other fan control registers can be used to fine-tune the algorithm behavior based on application requirements.

Note that steps 1 - 7 are optional and need only be performed if the default settings do not provide the desired fan response.

1. Set the Valid TACH Count Register to maximum number of tach counts to indicate the fan is spinning.
2. Set the Spin Up Configuration Register to the Spin Up Level and Spin Time desired.
3. Set the Fan Step Register to the desired step size.

4. Set the Fan Minimum Drive Register to the minimum drive value that will maintain fan operation.
5. Set the Update Time, and Edges options in the Fan Configuration Register.
6. Set the valid TACH count setting at the highest count that indicates that the fan is spinning.
7. Set the TACH Target Register to the desired tachometer count.
8. Enable the RPM based Fan Speed Control Algorithm by setting the EN_ALGO bit.

5.6 Tachometer Measurement

The tachometer measurement circuitry is used in conjunction with the RPM based Fan Speed Control Algorithm to update the fan driver output. Additionally, it can be used in Direct Setting mode as a diagnostic for host based fan control.

This method monitors the TACH signal in real time. It constantly updates the tachometer measurement by reporting the number of clocks between a user programmed number of edges on the TACH signal.

Using the Tach Period Measurement method provides fast response times for the RPM based Fan Speed Control Algorithm and the data is presented as a count value that represents the fan RPM period. When this method is used, all fan target values must be input as a count value for proper operation.

APPLICATION NOTE: The Tach Period Measurement method works independently of the drive settings. If the device is put into Direct Setting and the fan drive is set at a level that is lower than the fan can operate (including zero drive), then the tachometer measurement may signal a Stalled Fan condition and assert an interrupt.

5.6.1 Stalled Fan

A Stalled fan is detected differently based on which tach method is enabled. If the Tach Period Measurement measurement method is implemented, and if the tach counter exceeds the user-programmable Valid TACH Count setting then it will flag the fan as stalled and trigger an interrupt.

If the RPM based Fan Speed Control Algorithm is enabled, the algorithm will automatically attempt to restart the fan until it detects a valid tachometer level or is disabled.

The FAN_STALL Status bit indicates that a stalled fan was detected. This bit is checked conditionally depending on the mode of operation.

- When the Direct Setting Mode or Direct Setting with LUT Mode are enabled or the Spin Up Routine is initiated, the FAN_STALL interrupt will be masked for the duration of the programmed Spin Up Time. This is to allow the fan opportunity to reach a valid speed without generating unnecessary interrupts.
- When the Direct Setting Mode or Direct Setting w/ LUT Mode are activated then whenever the TACH Reading Register value exceeds the Valid TACH Count Register setting, the FAN_STALL status bit will be set.
- When using the RPM based Fan Speed Control Algorithm (either FSC Mode or LUT with FSC Mode), the stalled fan condition is checked whenever the Update Time is met and the fan drive setting is updated. It is not a continuous check.

5.6.2 Aging Fan or Invalid Drive Detection

The EMC2103 contains circuitry that detects that the programmed fan speed can be reached by the fan. If the target fan speed cannot be reached within a user defined band of tach counts at maximum drive then the DRIVE_FAIL status bit is and the $\overline{\text{ALERT}}$ pin is asserted. This is useful to detect aging fan conditions (where the fan's natural maximum speed degrades over time) or incorrect fan speed settings.

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5.7 Spin Up Routine

The EMC2103 also contains programmable circuitry to control the spin up behavior of the fan driver to ensure proper fan operation. The Spin Up Routine is initiated under the following conditions when the Tach Period Measurement method of tach measurement is used. This applies to either the RPM based Fan Speed Control Algorithm mode or the Direct Setting mode (with or without the Look Up Table).

1. The TACH Target Register value changes from a value of FFh to a value that is less than the Valid TACH Count.
2. The RPM based Fan Speed Control Algorithm's measured TACH Reading Register value is greater than the Valid TACH Count setting.

When the Spin Up Routine is operating, the fan driver is set to full scale (optional) for one quarter of the total user defined spin up time. For the remaining spin up time, the fan driver output is set a a user defined level (30% through 65% drive).

After the Spin Up Routine has finished, the EMC2103 measures the TACH signal. If the measured TACH Reading Register value is higher than the Valid TACH Count Register setting, the FAN_SPIN status bit is set and the Spin Up Routine will automatically attempt to restart the fan.

Figure 5.5 shows an example of the Spin Up Routine in response to a programmed fan speed change based on the first condition above.

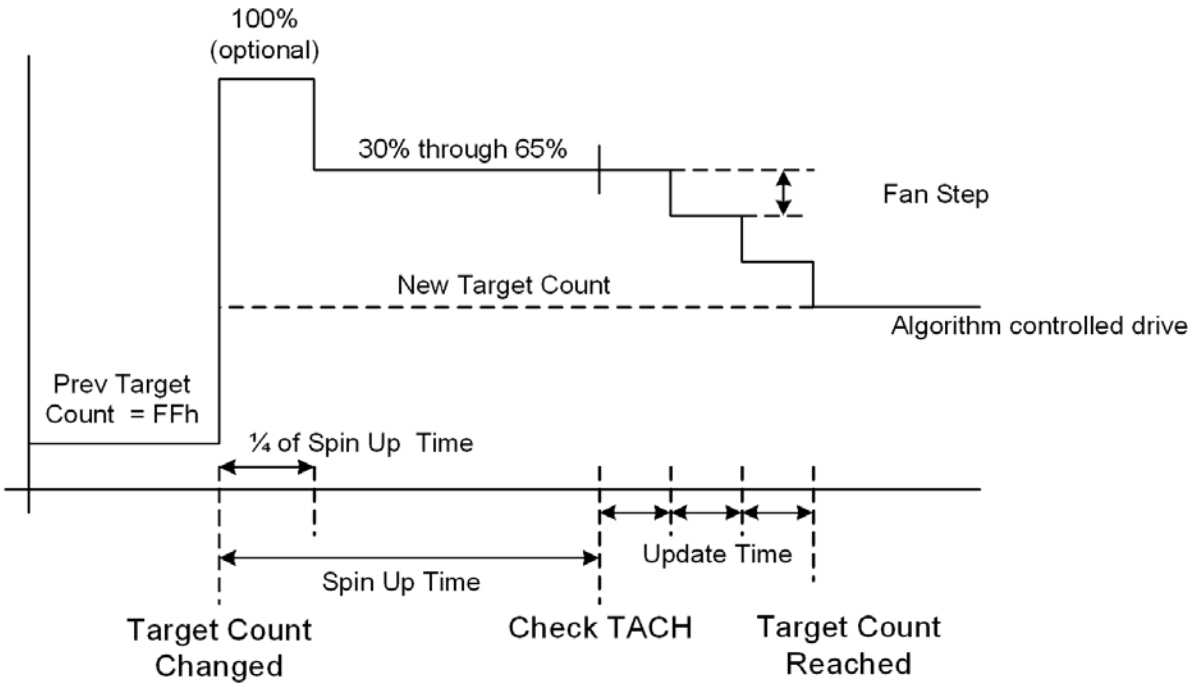


Figure 5.5 Spin Up Routine

5.8 Ramp Rate Control

The PWM output drive can be configured with automatic ramp rate control. If the RPM based Fan Speed Control Algorithm is used, then this ramp rate control is automatically used based on the fan control derivative option settings. See Section 6.23, "Fan Configuration 2 Register". The user programs a maximum step size for the PWM setting and an update time. The update time varies from 100ms to 1.6s while the PWM maximum step can vary from 1 PWM count to 31 PWM counts.

When a new PWM is entered, the delta from the next PWM and the previous PWM is determined. If this delta is greater than the Max Step settings, then the PWM is incrementally adjusted every 100ms to 1.6s as determined by the Update Time until the target PWM setting is reached. See Figure 5.6.

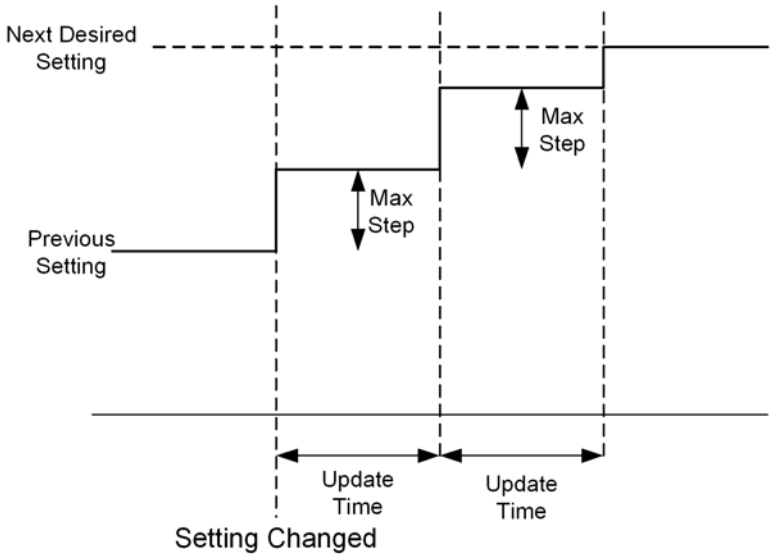


Figure 5.6 Ramp Rate Control

5.9 Watchdog Timer

The EMC2103 contains an internal Watchdog Timer. Once the device has powered up the watchdog timer monitors the bus traffic for signs of activity. The Watchdog Timer starts when the internal supply has reached its operating point. The Watchdog Timer only starts immediately after power-up and once it has been triggered or deactivated will not restart.

If four (4) seconds elapse without the system host programming the device, then the watchdog will be triggered and the following will occur:

1. The WATCH status bit will be set.
2. The fan driver will be set to full scale drive. It will remain at full scale drive until one of the three conditions listed below are met.

If the Watchdog Timer is triggered, the following three operations will disable the timer and return the device to normal operation. Alternately, if the Watchdog Timer has not yet been triggered performing any one of the following will disable it.

1. Writing the Fan Setting Register will disable the Watchdog Timer.
2. Enabling the RPM based Fan Speed Control Algorithm by setting the EN_ALGO bit will disable the Watchdog Timer. The fan driver will be set based on the RPM based Fan Speed Control Algorithm.

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3. Setting the LUT_LOCK bit will disable the Watchdog Timer. The fan driver will be set based on the Look Up Table settings.

Writing any other configuration registers will not disable the Watchdog Timer.

APPLICATION NOTE: Disabling the Watchdog will not automatically set the fan drive. This must be done manually (or via the Look Up Table).

5.10 Fault Queue

The EMC2103 contains a programmable fault queue on all fault conditions. The fault queue defines how many consecutive out-of-limit conditions must be reported before the corresponding status bit is set (and the $\overline{\text{ALERT}}$ pin asserted).

5.11 Temperature Monitoring

The EMC2103 can monitor the temperature of up to three (3) externally connected diodes as well as the internal or ambient temperature. Each channel is configured with the following features enabled or disabled based on user settings and system requirements.

5.11.1 Dynamic Averaging

The EMC2103 supports dynamic averaging. When enabled, this feature changes the conversion time for all channels based on the selected conversion rate. This essentially increases the averaging factor as shown in Table 5.4. The benefits of Dynamic Averaging are improved noise rejection due to the longer integration time as well as less random variation on the temperature measurement.

Table 5.4 Dynamic Averaging Behavior

CONVERSION RATE	AVERAGING FACTOR (RELATIVE TO 11-BIT CONVERSI0N)	
	DYNAMIC AVERAGING ENABLED	DYNAMIC AVERAGING DISABLED
1 / sec	8x	1x
2 / sec	4x	1x
4 / sec	2x	1x
Continuous	1x	1x

5.11.2 Resistance Error Correction

The EMC2103 includes active Resistance Error Correction to remove the effect of up to 100 ohms of series resistance. Without this automatic feature, voltage developed across the parasitic resistance in the remote diode path causes the temperature to read higher than the true temperature is. The error induced by parasitic resistance is approximately +0.7°C per ohm. Sources of parasitic resistance include bulk resistance in the remote temperature transistor junctions, series resistance in the CPU, and resistance in the printed circuit board traces and package leads. Resistance error correction in the EMC2103 eliminates the need to characterize and compensate for parasitic resistance in the remote diode path.

5.11.3 Beta Compensation

The forward current gain, or beta, of a transistor is not constant as emitter currents change. As well, it is not constant over changes in temperature. The variation in beta causes an error in temperature reading that is proportional to absolute temperature. This correction is done by implementing the BJT or transistor model for temperature measurement.

For discrete transistors configured with the collector and base shorted together, the beta is generally sufficiently high such that the percent change in beta variation is very small. For example, a 10% variation in beta for two forced emitter currents with a transistor whose ideal beta is 50 would contribute approximately 0.25°C error at 100°C. However for substrate transistors where the base-emitter junction is used for temperature measurement and the collector is tied to the substrate, the proportional beta variation will cause large error. For example, a 10% variation in beta for two forced emitter currents with a transistor whose ideal beta is 0.5 would contribute approximately 8.25°C error at 100°C.

The Beta Compensation circuitry in the EMC2103 corrects for this beta variation to eliminate any error which would normally be induced. It automatically detects the appropriate beta setting to use.

5.11.4 Digital Averaging

The external diode channels support a 4x digital averaging filter. Every cycle, this filter updates the temperature data based an a running average of the last 4 measured temperature values. The digital averaging reduces temperature flickering and increases temperature measurement stability.

The digital averaging can be disabled by setting the DIS_AVG bit in the Configuration 2 Register (see Section 6.11).

5.12 Diode Connections

The External Diode 1 channel can support a diode-connected transistor (such as a 2N3904) or a substrate transistor requiring the BJT or transistor model (such as those found in a CPU or GPU) as shown in Figure 5.7.

The External Diode 2 channel (EMC2103-2 and EMC2103-4 only) supports any diode connection shown or it can be configured to operate in anti-parallel diode (APD) mode. When configured in APD mode, a third temperature channel is available that shares the DP2 and DN2 pins. When in this mode, both the external diode 2 channel and external diode 3 channel thermal diodes must be connected as diodes.

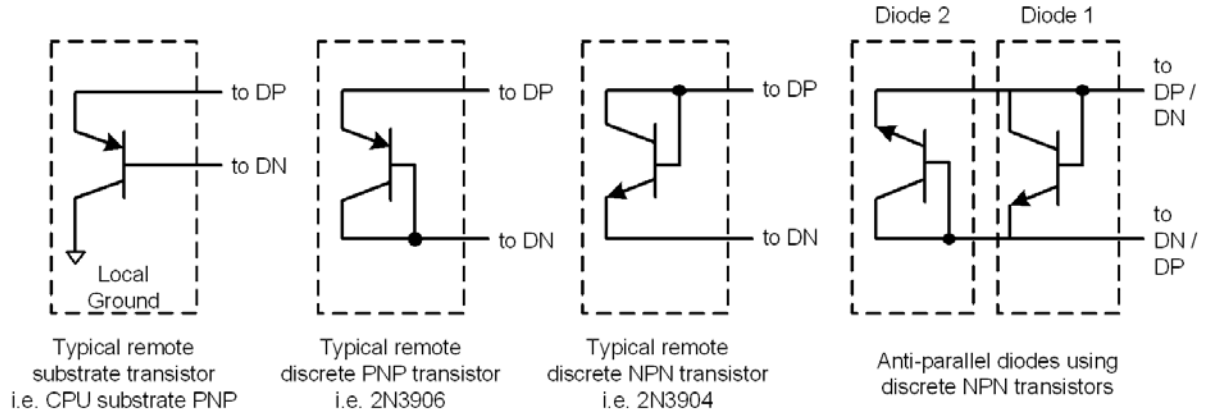


Figure 5.7 Diode Connections

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5.12.1 Diode Faults

The EMC2103 actively detects an open and short condition on each measurement channel. When a diode fault is detected, the temperature data MSByte is forced to a value of 80h and the FAULT bit is set in the Status Register. When the External Diode 2 channel is configured to operate in APD mode, the circuitry will detect independent open fault conditions, however a short condition will be shared between the External Diode 2 and External Diode 3 channels.

If a diode fault occurs on the hardware defined shutdown channel, then no temperature comparison is performed. The $\overline{\text{SYS_SHDN}}$ pin will not be asserted.

5.13 GPIOs

The EMC2103-2 and EMC2103-4 contain two dedicated GPIO pins. The GPIO pins can be individually configured as an input or an output and as a push-pull or open-drain output. Additionally, each GPIO pin, when configured as an input, can be individually enabled to trigger an interrupt when they change states.

Chapter 6 Register Set

6.1 Register Map

The following registers are accessible through the SMBus Interface. All register bits marked as '-' will always read '0'. A write to these bits will have no effect.

APPLICATION NOTE: All registers denoted with a ** are specific to the EMC2103-2 and EMC2103-4 only. Writing to these registers by the EMC2103-1 will have no effect and reading from them will return '00h'.

Table 6.1 EMC2103 Register Set

ADDR	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	LOCK	PAGE
Temperature Registers						
00h	R	Internal Temp Reading High Byte	Stores the integer data of the Internal Diode	00h	No	Page 44
01h	R	Internal Temp Reading Low Byte	Stores the fractional data of the Internal Diode	00h	No	Page 44
02h	R	External Diode 1 Temp Reading High Byte	Stores the integer data of External Diode 1	00h	No	Page 44
03h	R	External Diode 1 Temp Reading Low Byte	Stores the fractional data of External Diode 1	00h	No	Page 44
04h **	R	External Diode 2 Temp Reading High Byte **	Stores the integer data of External Diode 2	00h	No	Page 44
05h **	R	External Diode 2 Temp Reading Low Byte **	Stores the fractional data of External Diode 2	00h	No	Page 44
06h **	R	External Diode 3 Temp Reading High Byte **	Stores the integer data of External Diode 3	00h	No	Page 44
07h **	R	External Diode 3 Temp Reading Low Byte **	Stores the fractional data of External Diode 3	00h	No	Page 44
0Ah	R	Critical/Thermal Shutdown Temperature	Stores the calculated Critical/Thermal Shutdown temperature high limit derived from TRIP_SET pin voltage	N/A	No	Page 45
0Ch	R/W	Pushed Temperature 1	Stores the integer data for Pushed Temperature 1 to drive the LUT	00h	No	Page 45
0Dh	R/W	Pushed Temperature 2	Stores the integer data for Pushed Temperature 2 to drive the LUT	00h	No	Page 45
10h	R	TRIP_SET Voltage	Stores the measured voltage on the TRIP_SET pin	FFh	No	Page 46

Table 6.1 EMC2103 Register Set (continued)

ADDR	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	LOCK	PAGE
Diode Configuration						
11h	R/W	External Diode 1 Ideality Register	Stores the Ideality Factor used for External Diode 1	12h	SWL	Page 46
12h **	R/W	External Diode 2 Ideality Register **	Stores the Ideality factor used for External Diode 2 and External Diode 3	12h	SWL	Page 46
14h	See Text	External Diode 1 Beta Configuration	Configures the beta compensation settings for External Diode 1	See Text	SWL	Page 47
15h **	See Text	External Diode 2 Beta Configuration **	Configures the beta compensation settings for External Diode 2	See Text	SWL	Page 47
17h	R/W	External Diode REC Configuration	Configures the Resistance Error Correction functionality for all external diodes	See Text	SWL	Page 48
19h	R/W once	External Diode 1 Tcrit Limit	Stores the critical temperature limit for External Diode 1	64h (100°C)	Write Once	Page 49
1Ah **	R/W once	External Diode 2 Tcrit Limit **	Stores the critical temperature limit for External Diode 2	64h (100°C)	Write Once	Page 49
1Bh **	R/W once	External Diode 3 Tcrit Limit **	Stores the critical temperature limit for External Diode 3	64h (100°C)	Write Once	Page 49
1Dh	R/W once	Internal Diode Tcrit Limit	Stores the critical temperature limit for the Internal Diode	64h (100°C)	Write Once	Page 49
Configuration and control						
1Fh	R	Tcrit Status	Stores the status bits for all temperature channel tcrit limits	00h	No	Page 53
20h	R/W	Configuration	Configures the Thermal / Critical Shutdown masking options	00h	SWL	Page 50
21h	R/W	Configuration 2	Controls the conversion rate for monitoring of all channels	0Eh	SWL	Page 51
23h	R-C	Interrupt Status	Stores the status bits for temperature channels	00h	No	Page 52
24h	R-C	High Limit Status	Stores the status bits for all temperature channel high limits	00h	No	Page 53
25h	R-C	Low Limit Status	Stores the status bits for all temperature channel low limits	00h	No	Page 53
26h	R-C	Diode Fault	Stores the status bits for all temperature channel diode faults	00h	No	Page 53
27h	R-C	Fan Status	Stores the status bits for the RPM based Fan Speed Control Algorithm	00h	No	Page 53
28h	R/W	Interrupt Enable Register	Controls the masking of interrupts on all temperature channels	00h	No	Page 54
29h	R/W	Fan Interrupt Enable Register	Controls the masking of interrupts for the Fan Driver	00h	No	Page 54

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Table 6.1 EMC2103 Register Set (continued)

ADDR	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	LOCK	PAGE
2Ah	R/W	PWM Config	Configures the PWM driver	00h	No	Page 55
2Bh	R/W	PWM Base Frequency	Controls the base frequency of the PWM driver	03h	No	Page 55
Temperature Limit Registers						
30h	R/W	External Diode 1 Temp High Limit	High limit for External Diode 1	55h (+85°C)	SWL	Page 56
31h **	R/W	External Diode 2 Temp High Limit **	High limit for External Diode 2	55h (+85°C)	SWL	Page 56
32h **	R/W	External Diode 3 Temp High Limit **	High limit for External Diode 3	55h (+85°C)	SWL	Page 56
34h	R/W	Internal Diode High Limit	High Limit for Internal Diode	55h (85°C)	SWL	Page 56
38h	R/W	External Diode 1 Temp Low Limit	Low Limit for External Diode 1	00h (0°C)	SWL	Page 56
39h **	R/W	External Diode 2 Temp Low Limit **	Low Limit for External Diode 2	00h (0°C)	SWL	Page 56
3Ah **	R/W	External Diode 3 Temp Low Limit **	Low Limit for External Diode 3	00h (0°C)	SWL	Page 56
3Ch	R/W	Internal Diode Low Limit	Low Limit for Internal Diode	00h (0°C)	SWL	Page 56
Fan Control Registers						
40h	R/W	Fan Setting	Always displays the most recent fan driver input setting for Fan. If the RPM based Fan Speed Control Algorithm is disabled, allows direct user control of the fan driver.	00h	No	Page 57
41h	R/W	PWM Divide	Stores the divide ratio to set the frequency for the Fan	01h	No	Page 57
42h	R/W	Fan Configuration 1	Sets configuration values for the RPM based Fan Speed Control Algorithm for the Fan	2Bh	No	Page 57
43h	R/W	Fan Configuration 2	Sets additional configuration values for the Fan driver	38h	SWL	Page 59
45h	R/W	Gain	Holds the gain terms used by the RPM based Fan Speed Control Algorithm for the Fan	2Ah	SWL	Page 60
46h	R/W	Fan Spin Up Configuration	Sets the configuration values for Spin Up Routine of the Fan driver	19h	SWL	Page 61
47h	R/W	Fan Step	Sets the maximum change per update for the Fan	10h	SWL	Page 63
48h	R/W	Fan Minimum Drive	Sets the minimum drive value for the the Fan driver	66h (40%)	SWL	Page 63

Table 6.1 EMC2103 Register Set (continued)

ADDR	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	LOCK	PAGE
49h	R/W	Fan Valid TACH Count	Holds the minimum tachometer reading that indicates the fan is spinning properly	F5h	SWL	Page 63
4Ah	R/W	Fan Drive Fail Band Low Byte	Stores the number of Tach counts used to determine how the actual fan speed must match the target fan speed at full scale drive	00h	SWL	Page 64
4Bh	R/W	Fan Drive Fail Band High Byte		00h	SWL	
4Ch	R/W	TACH Target Low Byte	Holds the target tachometer reading low byte for the Fan	F8h	No	Page 64
4Dh	R/W	TACH Target High Byte	Holds the target tachometer reading for the Fan	FFh	No	Page 64
4Eh	R	TACH Reading High Byte	Holds the tachometer reading for the Fan	FFh	No	Page 65
4Fh	R	TACH Reading Low Byte	Holds the tachometer reading low byte for the Fan	F8h	No	Page 65
Look Up Table (LUT)						
50h	R/W	LUT Configuration	Stores and controls the configuration for the LUT	00h	No	Page 65
51h	R/W	LUT Drive 1	Stores the lowest programmed drive setting for the LUT	FBh	LUT Lock	Page 66
52h	R/W	LUT Temp 1 Setting 1	Stores the threshold level for the External Diode 1 channel that is associated with the Drive 1 value	7Fh (127°C)	LUT Lock	Page 66
53h	R/W	LUT Temp 2 Setting 1	Stores the threshold level for the External Diode 2 channel that is associated with the Drive 1 value	7Fh (127°C)	LUT Lock	Page 66
54h	R/W	LUT Temp 3 Setting 1	Stores the threshold level for the External Diode 3 channel (or Pushed Temp 1 temp) that is associated with the Drive 1 value	7Fh (127°C)	LUT Lock	Page 66
55h	R/W	LUT Temp 4 Setting 1	Stores the threshold level for the Internal Diode channel (or Pushed Temp 2 temp) that is associated with the Drive 1 value	7Fh (127°C)	LUT Lock	Page 66
56h	R/W	LUT Drive 2	Stores the second programmed drive setting for the LUT	E6h	LUT Lock	Page 66
57h	R/W	LUT Temp 1 Setting 2	Stores the threshold level for the External Diode 1 channel that is associated with the Drive 2 value	7Fh (127°C)	LUT Lock	Page 66
58h	R/W	LUT Temp 2 Setting 2	Stores the threshold level for the External Diode 2 channel that is associated with the Drive 2 value	7Fh (127°C)	LUT Lock	Page 66
59h	R/W	LUT Temp 3 Setting 2	Stores the threshold level for the External Diode 3 channel (or Pushed Temp 1 temp) that is associated with the Drive 2 value	7Fh (127°C)	LUT Lock	Page 66

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Table 6.1 EMC2103 Register Set (continued)

ADDR	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	LOCK	PAGE
5Ah	R/W	LUT Temp 4 Setting 2	Stores the threshold level for the Internal Diode channel (or Pushed Temp 2 temp) that is associated with the Drive 2 value	7Fh (127°C)	LUT Lock	Page 66
5Bh	R/W	LUT Drive 3	Stores the third programmed drive setting for the LUT	D1h	LUT Lock	Page 66
5Ch	R/W	LUT Temp 1 Setting 3	Stores the threshold level for the External Diode 1 channel that is associated with the Drive 3 value	7Fh (127°C)	LUT Lock	Page 66
5Dh	R/W	LUT Temp 2 Setting 3	Stores the threshold level for the External Diode 2 channel that is associated with the Drive 3 value	7Fh (127°C)	LUT Lock	Page 66
5Eh	R/W	LUT Temp 3 Setting 3	Stores the threshold level for the External Diode 3 channel (or Pushed Temp 1 temp) that is associated with the Drive 3 value	7Fh (127°C)	LUT Lock	Page 66
5Fh	R/W	LUT Temp 4 Setting 3	Stores the threshold level for the Internal Diode channel (or Pushed Temp 2 temp) that is associated with the Drive 3 value	7Fh (127°C)	LUT Lock	Page 66
60h	R/W	LUT Drive 4	Stores the fourth programmed drive setting for the LUT	BCh	LUT Lock	Page 66
61h	R/W	LUT Temp 1 Setting 4	Stores the threshold level for the External Diode 1channel that is associated with the Drive 4 value	7Fh (127°C)	LUT Lock	Page 66
62h	R/W	LUT Temp 2 Setting 4	Stores the threshold level for the External Diode 2 channel that is associated with the Drive 4 value	7Fh (127°C)	LUT Lock	Page 66
63h	R/W	LUT Temp 3 Setting 4	Stores the threshold level for the External Diode 3 channel (or Pushed Temp 1 temp) that is associated with the Drive 4 value	7Fh (127°C)	LUT Lock	Page 66
64h	R/W	LUT Temp 4 Setting 4	Stores the threshold level for the Internal Diode channel (or Pushed Temp 2 temp) that is associated with the Drive 4 value	7Fh (127°C)	LUT Lock	Page 66
65h	R/W	LUT Drive 5	Stores the fifth programmed drive setting for the LUT	A7h	LUT Lock	Page 66
66h	R/W	LUT Temp 1 Setting 5	Stores the threshold level for the External Diode 1 channel that is associated with the Drive 5 value	7Fh (127°C)	LUT Lock	Page 66
67h	R/W	LUT Temp 2 Setting 5	Stores the threshold level for the External Diode 2 channel that is associated with the Drive 5 value	7Fh (127°C)	LUT Lock	Page 66
68h	R/W	LUT Temp 3 Setting 5	Stores the threshold level for the External Diode 3 channel (or Pushed Temp 1 temp) that is associated with the Drive 5 value	7Fh (127°C)	LUT Lock	Page 66

Table 6.1 EMC2103 Register Set (continued)

ADDR	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	LOCK	PAGE
69h	R/W	LUT Temp 4 Setting 5	Stores the threshold level for the Internal Diode channel (or Pushed Temp 2 temp) that is associated with the Drive 5 value	7Fh (127°C)	LUT Lock	Page 66
6Ah	R/W	LUT Drive 6	Stores the sixth programmed drive setting for the LUT	92h	LUT Lock	Page 66
6Bh	R/W	LUT Temp 1 Setting 6	Stores the threshold level for the External Diode 1 channel that is associated with the Drive 6 value	7Fh (127°C)	LUT Lock	Page 66
6Ch	R/W	LUT Temp 2 Setting 6	Stores the threshold level for the External Diode 2 channel that is associated with the Drive 6 value	7Fh (127°C)	LUT Lock	Page 66
6Dh	R/W	LUT Temp 3 Setting 6	Stores the threshold level for the External Diode 3 channel (or Pushed Temp 1 temp) that is associated with the Drive 6 value	7Fh (127°C)	LUT Lock	Page 66
6Eh	R/W	LUT Temp 4 Setting 6	Stores the threshold level for the Internal Diode channel (or Pushed Temp 2 temp) that is associated with the Drive 6 value	7Fh (127°C)	LUT Lock	Page 66
6Fh	R/W	LUT Drive 7	Stores the seventh programmed drive setting for the LUT	92h	LUT Lock	Page 66
70h	R/W	LUT Temp 1 Setting 7	Stores the threshold level for the External Diode 1 channel that is associated with the Drive 7 value	7Fh (127°C)	LUT Lock	Page 66
71h	R/W	LUT Temp 2 Setting 7	Stores the threshold level for the External Diode 2 channel that is associated with the Drive 7 value	7Fh (127°C)	LUT Lock	Page 66
72h	R/W	LUT Temp 3 Setting 7	Stores the threshold level for the External Diode 3 channel (or Pushed Temp 1 temp) that is associated with the Drive 7 value	7Fh (127°C)	LUT Lock	Page 66
73h	R/W	LUT Temp 4 Setting 7	Stores the threshold level for the Internal Diode channel (or Pushed Temp 2 temp) that is associated with the Drive 7 value	7Fh (127°C)	LUT Lock	Page 66
74h	R/W	LUT Drive 8	Stores the highest programmed drive setting for the LUT	92h	LUT Lock	Page 66
75h	R/W	LUT Temp 1 Setting 8	Stores the threshold level for the External Diode 1 channel that is associated with the Drive 8 value	7Fh (127°C)	LUT Lock	Page 66
76h	R/W	LUT Temp 2 Setting 8	Stores the threshold level for the External Diode 2 channel that is associated with the Drive 8 value	7Fh (127°C)	LUT Lock	Page 66
77h	R/W	LUT Temp 3 Setting 8	Stores the threshold level for the External Diode 3 channel (or Pushed Temp 1 temp) that is associated with the Drive 8 value	7Fh (127°C)	LUT Lock	Page 66

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Table 6.1 EMC2103 Register Set (continued)

ADDR	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	LOCK	PAGE
78h	R/W	LUT Temp 4 Setting 8	Stores the threshold level for the Internal Diode channel (or Pushed Temp 2 temp) that is associated with the Drive 8 value	7Fh (127°C)	LUT Lock	Page 66
79h	R/W	LUT Temp Hysteresis	Stores the hysteresis that is shared for all temperature inputs	0Ah (10°C)	LUT Lock	Page 66
E1h **	R/W	GPIO Direction Register **	Controls the GPIO direction for GPIOs 1 and 2	00h	No	Page 68
E2h **	R/W	GPIO Output Configuration Register **	Controls the output type of GPIOs 1 and 2	00h	No	Page 68
E3h **	R/W	GPIO Input Register **	Stores the inputs for GPIOs 1 and 2	00h	No	Page 68
E4h **	R/W	GPIO Output Register **	Controls the output state of GPIOs 1 and 2	00h	No	Page 69
E5h **	R/W	GPIO Interrupt Enable Register **	Enables interrupts for GPIOs 1 and 2	00h	No	Page 69
E6h **	R/W	GPIO Status **	Indicates when the GPIOs change state	00h	No	Page 70
Lock Register						
EF	R/W	Software Lock	Locks all SWL registers	00h	SWL	Page 70
Revision Registers						
FCh	R	Product Features	Indicates which pin selected options are enabled	00h	No	Page 70
FDh	R	Product ID EMC2103-1	Stores the unique Product ID	24h	No	Page 71
		Product ID EMC2103-2 and EMC2103-4		26h	No	
FEh	R	Manufacturer ID	Manufacturer ID	5Dh	No	Page 71
FFh	R	Revision	Revision	00h	No	Page 72

During Power-On-Reset (POR), the default values are stored in the registers. A POR is initiated when power is first applied to the part and the voltage on the VDD supply surpasses the POR level as specified in the electrical characteristics. Any reads to undefined registers will return 00h. Writes to undefined registers will not have an effect.

6.1.1 Lock Entries

The Lock Column describes the locking mechanism, if any, used for individual registers. All SWL registers are Software Locked and therefore made read-only when the LOCK bit is set.

6.2 Temperature Data Registers

Table 6.2 Temperature Data Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
00h	R	Internal Diode High Byte	Sign	64	32	16	8	4	2	1	00h
01h	R	Internal Diode Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
02h	R	External Diode 1 High Byte	Sign	64	32	16	8	4	2	1	00h
03h	R	External Diode 1 Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
04h **	R	External Diode 2 High Byte **	Sign	64	32	16	8	4	2	1	00h
05h **	R	External Diode 2 Low Byte **	0.5	0.25	0.125	-	-	-	-	-	00h
06h **	R	External Diode 3 High Byte **	Sign	64	32	16	8	4	2	1	00h
07h **	R	External Diode 3 Low Byte **	0.5	0.25	0.125	-	-	-	-	-	00h

The temperature measurement range is from -64°C to +127.875°C. The data format is a signed two's complement number as shown in Table 6.3.

Table 6.3 Temperature Data Format

TEMPERATURE (°C)	BINARY	HEX (AS READ BY REGISTERS)
Diode Fault	1000_0000_000b	80_00h
-63.875	1100_0000_001b	C0_20h
-63	1100_0001_000b	C1_00h
-1	1111_1111_000b	FF_00h
-0.125	1111_1111_111b	FF_E0h
0	0000_0000_000b	00_00h
0.125	0000_0000_001b	00_20h
1	0000_0001_000b	01_00h
63	0011_1111_000b	3F_00h
64	0100_0000_000b	40_00h

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Table 6.3 Temperature Data Format (continued)

TEMPERATURE (°C)	BINARY	HEX (AS READ BY REGISTERS)
65	0100_0001_000b	41_00h
127	0111_1111_000b	7F_00h
127.875	0111_1111_111b	7F_E0h

6.3 Critical/Thermal Shutdown Temperature Register

Table 6.4 Critical/Thermal Shutdown Temperature Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
0Ah	R	Critical/Thermal Shutdown Temperature	128	64	32	16	8	4	2	1	7Fh (+127°C)

The Critical/Thermal Shutdown Temperature Register is a read-only register that stores the Voltage Programmable Threshold temperature used in the Thermal / Critical Shutdown circuitry. The contents of the register reflect the calculated temperature determined by the voltage on the TRIP_SET pin (see Section 5.1.2).

The data format is shown in Table 6.5.

Table 6.5 Critical / Thermal Shutdown Data Format

TEMPERATURE (°C)	BINARY	HEX
0	0000_0000b	00h
1	0000_0001b	01h
63	0011_1111b	3Fh
64	0100_0000b	40h
65	0100_0001b	41h
127	0111_1111b	7Fh

6.4 Pushed Temperature Registers

Table 6.6 Pushed Temperature Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
0Ch	R/W	Pushed Temperature 1	Sign	64	32	16	8	4	2	1	00h
0Dh	R/W	Pushed Temperature 2	Sign	64	32	16	8	4	2	1	00h

The Pushed Temperature Registers store user programmed temperature values that can be used by the look-up table to update the fan control algorithm. Data written in these registers is not compared against any limits and must match the data format shown in Table 6.3.

6.5 TRIP_SET Voltage Register

Table 6.7 TRIP_SET Voltage Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
10h	R/W	TRIP_SET Voltage Register	750.0	375.0	187.5	93.75	46.88	23.43	11.72	5.89	FFh

The TRIP_SET Voltage Register stores data that is measured on the TRIP_SET Voltage input. Each bit weight represents mV of resolution so that the final voltage can be determined by adding the weighting of the set bits together.

6.6 Ideality Factor Registers

Table 6.8 Ideality Factor Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
11h	R/W	External Diode 1 Ideality	0	0	0	1	0	B2	B1	B0	12h
12h **	R/W	External Diode 2 Ideality **	0	0	0	1	0	B2	B1	B0	12h

These registers store the ideality factors that are applied to the external diodes.

The External Diode 3 channel will use the settings for the External Diode 2 channel.

Beta Compensation and Resistance Error Correction automatically correct for most diode ideality errors, therefore it is not recommended that these settings be updated without consulting Microchip.

For CPU substrate transistors that require the BJT transistor model, the ideality factor behaves slightly differently than for discrete diode-connected transistors. Refer to Table 6.10 when using a CPU substrate transistor.

Only the lower three bits can be written. Writing to any other bit will be ignored.

The Ideality Factor Registers are software locked.

Table 6.9 Ideality Factor Look-Up Table

SETTING	FACTOR
10h	1.0053
11h	1.0066
12h	1.0080
13h	1.0093

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Table 6.9 Ideality Factor Look-Up Table (continued)

SETTING	FACTOR
14h	1.0106
15h	1.0119
16h	1.0133
17h	1.0146

Table 6.10 Substrate Diode Ideality Factor Look-Up Table (BJT Model)

SETTING	FACTOR
10h	0.9973
11h	0.9986
12h	1.0000
13h	1.0013
14h	1.0026
15h	1.0039
16h	1.0053
17h	1.0066

APPLICATION NOTE: When measuring a 65nm Intel CPUs, the Ideality Setting should be the default 12h. When measuring 45nm Intel CPUs, the Ideality Setting should be 15h.

6.7 Beta Configuration Register

Table 6.11 Beta Configuration Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
14h	R/W - see Table 5.1	External Diode 1 Beta Configuration	-	-	-	AUTO1	-	BETA1[2:0]			see Table 5.1
15h **	R/W - see Table 5.1	External Diode 2 Beta Configuration **	-	-	-	AUTO2	-	BETA2[2:0]			see Table 5.1

The Beta Configuration Register controls advanced temperature measurement features of the External Diode channels.

If External Diode 1 is selected as the hardware shutdown measurement channel (see Section 5.1.1) then the External Diode 1 Beta register will be read only. If the internal diode is selected, then this register can be written normally. Likewise, if the External Diode 2 channel is selected (EMC2103-2 and EMC2103-4 only) then this register can be written normally. Finally, if External Diode 2 is selected as the hardware shutdown measurement channel (EMC2103-2 and EMC2103-4 only), then the External Diode 2 Beta Configuration Register will be read only.

Writing to a read only register will have no affect. The data will be ignored.

Bit 4 - AUTOx - Enables the Automatic Beta detection algorithm for the External Diode X channel.

- '0' - The Automatic Beta detection algorithm is disabled. The BETAx[3:0] bit settings will be used to control the beta compensation circuitry. This bit is set to '0' automatically if Beta Compensation is disabled - see Table 5.1.
- '1' - The Automatic Beta detection algorithm is enabled. The circuitry will automatically detect the transistor type and beta values and configure the BETAx[3:0] bits for optimal performance.

Bits 2 - 0 - BETAx[2:0] - hold a value that corresponds to a range of betas that the Beta Compensation circuitry can compensate for. These three bits will always show the current beta setting used by the circuitry. If the AUTO bit is set (default), then these bits may be overwritten with every temperature conversion. If the AUTO bit is not set, then the value of these bits is used to drive the beta compensation circuitry. In this case, these bits should be set with a value corresponding to the lowest expected value of beta for the PNP transistor being used as a temperature sensing device.

See Table 6.12 for supported beta ranges. A value of 111b indicates that the beta compensation circuitry is disabled. In this condition, the diode channels will function with default current levels and will not automatically adjust for beta variation. This mode is used when measuring a discrete 2N3904 transistor or AMD thermal diode.

If the External Diode 3 channel is enabled, it will always use a beta setting of 111b.

These bits will be set to 111b if Beta Compensation is disabled - see Table 5.1

The Beta Configuration Registers are Software Locked.

Table 6.12 Beta Compensation Look Up Table

BETAX[2:0]			MINIMUM BETA
2	**1**	**0**	
0	0	0	≤ 0.08
0	0	1	≤ 0.111
0	1	0	≤ 0.176
0	1	1	≤ 0.29
1	0	0	≤ 0.48
1	0	1	≤ 0.9
1	1	0	≤ 2.33
1	1	1	Disabled

6.8 REC Configuration Register

Table 6.13 REC Configuration Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
17h	R/W - see Table 5.1	REC Configuration	-	-	-	-	-	REC3	REC2	REC1	0000_01XXb see Table 5.1

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The REC Configuration Register determines whether Resistance Error Correction is used for each external diode channel.

Bit 2 - REC3 (EMC2102-2 and EMC2103-4 only) - Controls the Resistance Error Correction functionality of External Diode 3 (if enabled)

- '0' - the REC functionality for External Diode 3 is disabled
- '1' (default) - the REC functionality for External Diode 3 is enabled.

Bit 1 - REC2 (EMC2103-2 and EMC2103-4 only) - Controls the Resistance Error Correction functionality of External Diode 2. If External Diode 2 is selected as the hardware shutdown channel then this bit is read only and determined by the SHDN_SEL pin (see Section 5.1.1).

- '0' - the REC functionality for External Diode 2 is disabled
- '1' - the REC functionality for External Diode 2 is enabled.

Bit 0 - REC1 - Indicates the Resistance Error Correction functionality of External Diode 1. If External Diode 1 is selected as the hardware shutdown channel then this bit is read only and determined by the SHDN_SEL pin (see Section 5.1.1).

- '0' - the REC functionality for External Diode 1 is disabled
- '1' - the REC functionality for External Diode 1 is enabled.

The REC Configuration Register is software locked.

6.9 Critical Temperature Limit Registers

Table 6.14 Critical Temperature Limit Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
19h	R/W once	External Diode 1 Tcrit Limit	Sign	64	32	16	8	4	2	1	64h (+100°C)
1Ah	R/W once	External Diode 2 Tcrit Limit	Sign	64	32	16	8	4	2	1	64h (+100°C)
1Bh	R/W once	External Diode 3 Tcrit Limit	Sign	64	32	16	8	4	2	1	64h (+100°C)
1Dh	R/W once	Internal Diode Tcrit Limit	Sign	64	32	16	8	4	2	1	64h (+100°C)

The Critical Temperature Limit Registers store the Critical Temperature Limit. At power up, none of the respective channels are linked to the SYS_SHDN pin or the Hardware set Thermal/Critical Shutdown circuitry.

Whenever one of the registers is updated, two things occur. First, the register is locked so that it cannot be updated again without a power on reset. Second, the respective temperature channel is linked to the SYS_SHDN pin and the Hardware set Thermal/Critical Shutdown Circuitry. At this point, if the measured temperature channel exceeds the Critical limit, the SYS_SHDN pin will be asserted, the appropriate bit set in the Tcrit Status Register, and the TCRIT bit in the Interrupt Status Register will be set.

6.10 Configuration Register

Table 6.15 Configuration Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
20h	R/W	Configuration	MASK	-	-	-	SYS3	SYS2	SYS1	APD	00h

The Configuration Register controls the basic functionality of the EMC2103. The bits are described below.

Bit 7 - MASK - Blocks the $\overline{\text{ALERT}}$ pin from being asserted.

- '0' (default) - The $\overline{\text{ALERT}}$ pin is unmasked. If any bit in either status register is set, the $\overline{\text{ALERT}}$ pin will be asserted (unless individually masked via the Mask Register)
- '1' - The $\overline{\text{ALERT}}$ pin is masked and will not be asserted.

Bit 3 - SYS3 (EMC2103-2 and EMC2103-4 only) - Enables the high temperature limit for the External Diode 3 channel to trigger the Critical / Thermal Shutdown circuitry (see Section 5.1).

- '0' (default) - the External Diode 3 channel high limit will not be linked to the $\overline{\text{SYS_SHDN}}$ pin. If the temperature meets or exceeds the limit, the $\overline{\text{ALERT}}$ pin will be asserted normally.
- '1' - the External Diode 3 channel high limit will be linked to the $\overline{\text{SYS_SHDN}}$ pin. If the temperature meets or exceeds the limit then the $\overline{\text{SYS_SHDN}}$ pin will be asserted. The $\overline{\text{SYS_SHDN}}$ pin will be released when the temperature drops below the high limit. The $\overline{\text{ALERT}}$ pin will be asserted normally.

Bit 2 - SYS2 (EMC2103-2 and EMC2103-4 only) - Enables the high temperature limit for the External Diode 2 channel to trigger the Critical / Thermal Shutdown circuitry (see Section 5.1).

- '0' (default) - the External Diode 2 channel high limit will not be linked to the $\overline{\text{SYS_SHDN}}$ pin. If the temperature meets or exceeds the limit, the $\overline{\text{ALERT}}$ pin will be asserted normally.
- '1' - the External Diode 2 channel high limit will be linked to the $\overline{\text{SYS_SHDN}}$ pin. If the temperature meets or exceeds the limit then the $\overline{\text{SYS_SHDN}}$ pin will be asserted. The $\overline{\text{ALERT}}$ pin will be asserted normally.

Bit 1 - SYS1 - Enables the high temperature limit for the External Diode 1 channel to trigger the Critical / Thermal Shutdown circuitry (see Section 5.1).

- '0' (default) - The External Diode 1 channel high limit will not be linked to the $\overline{\text{SYS_SHDN}}$ pin. If the temperature meets or exceeds the limit, the $\overline{\text{ALERT}}$ pin will be asserted normally.
- '1' - The External Diode 1 channel high limit will be linked to the $\overline{\text{SYS_SHDN}}$ pin. If the temperature meets or exceeds the limit then the $\overline{\text{SYS_SHDN}}$ pin will be asserted. The $\overline{\text{ALERT}}$ pin will be asserted normally.

Bit 0 - APD (EMC2103-2 and EMC2103-4 only) - This bit enables the Anti-parallel diode functionality on the External Diode 3 pins (DP3 and DN3).

- '0' (default) - The Anti-parallel diode functionality is disabled. The External Diode 2 channel can be configured for any type of diode
- '1' - The Anti-parallel diode functionality is enabled. Both the External Diode 2 and 3 channels are configured to support a diode or diode connected transistor (such as a 2N3904).

APPLICATION NOTE: When the APD diode is enabled, there will be a delay of a full temperature update before any comparisons and functionality associated with the External Diode 3 channel will be implemented. This includes the SYS3 bit operation, limit comparisons, and look up table comparisons.

The Configuration Register is software locked.

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6.11 Configuration 2 Register

Table 6.16 Configuration 2 Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
21h	R/W	Config 2	-	DIS_DYN	DIS_TO	DIS_AVG	QUEUE[1:0]		CONV[1:0]		0Eh

The Configuration 2 Register controls conversion rate of the temperature monitoring as well as the fault queue.

Bit 6 - DIS_DYN - Disables the Dynamic Averaging Feature.

- '0' (default) - The Dynamic Averaging function is enabled. The conversion time for all temperature channels is scaled based on the chosen conversion rate to maximize accuracy and immunity to random temperature measurement variation.
- '1' - The Dynamic Averaging function is disabled. The conversion time for all temperature channels is fixed regardless of the chosen conversion rate.

Bit 5 - DIS_TO - Disables the SMBus time out function.

- '0' (default) - The SMBus time out function is enabled.
- '1' - The SMBus time out function is disabled allowing the device to be fully I^2C compliant.

Bit 4 - DIS_AVG - Disables digital averaging of the External Diode channels.

- '0' (default) - The External Diode channels have digital averaging enabled. The temperature data is the average of the previous four measurements.
- '1' - The External Diode channels have digital averaging disabled. The temperature data is the last measured data.

Bits 3-2 - QUEUE[1:0] - Determines the number of consecutive out of limit conditions that are necessary to trigger an interrupt. Each measurement channel has a separate fault queue associated with the high limit, low limit, and diode fault condition.

APPLICATION NOTE: If the fault queue for any channel is currently active (i.e. an out of limit condition has been detected and caused the fault queue to increment) then changing the settings will not take effect until the fault queue is zeroed. This occurs by the $\overline{\text{ALERT}}$ pin asserting or the out of limit condition being removed.

Table 6.17 Fault Queue

QUEUE[1:0]		NUMBER OF CONSECUTIVE OUT OF LIMIT CONDITIONS
1	**0**	
0	0	1 (disabled)
0	1	2
1	0	3
1	1	4 (default)

Bit 1 - 0 - CONV[1:0] - determines the conversion rate of the temperature monitoring. This conversion rate does not affect the fan driver. The supply current from VDD_3V is nominally dependent upon the conversion rate and the average current will increase as the conversion rate increases.

Table 6.18 Conversion Rate

CONV[1:0]		CONVERSION RATE
1	**0**	
0	0	1 / sec
0	1	2 / sec
1	0	4 / sec (default)
1	1	Continuous

The Configuration 2 Register is software locked.

6.12 Interrupt Status Register

Table 6.19 Interrupt Status Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
23h	R-C	Interrupt Status Register	EEP ROM	-	TCRIT	GPIO	FAN	HIGH	LOW	FAULT	00h

The Interrupt Status Register reports the operating condition of the EMC2103. If any of the bits are set to a logic ‘1’ (other than HWS) then the $\overline{\text{ALERT}}$ pin will be asserted low if the corresponding channel is enabled. Reading from the status register clears all status bits if the error conditions is removed. If there are no set status bits, then the $\overline{\text{ALERT}}$ pin will be released.

The bits that cause the $\overline{\text{ALERT}}$ pin to be asserted can be masked based on the channel they are associated with unless stated otherwise.

Bit 7 - EEPROM (EMC2103-4 only) - This bit is set to ‘1’ if the EEPROM loader circuitry detects an error when writing data from the EEPROM. This bit is cleared when the register is read. This bit is not masked except via the MASK bit.

Bit 5 - TCRIT - This bit is set to ‘1’ if any bit in the Tcrit Status Register is set. This bit is automatically cleared when the Tcrit Status Register is read and the bits are cleared.

Bit 4 - GPIO (EMC2103-2 and EMC2103-4 only) - This bit is set to ‘1’ if any bit in the GPIO Status Register is set. This bit is automatically cleared when the GPIO Status Register is read.

Bit 3 - FAN - This bit is set to ‘1’ if any bit in the Fan Status Register is set. This bit is automatically cleared when the Fan Status Register is read and the bits are cleared.

Bit 2 - HIGH - This bit is set to ‘1’ if any bit in the High Status Register is set. This bit is automatically cleared when the High Status Register is read and the bits are cleared.

Bit 1- LOW - This bit is set to ‘1’ if any bit in the Low Status Register is set. This bit is automatically cleared when the Low Status Register is read and the bits are cleared.

Bit 0 - FAULT - This bit is set to ‘1’ if any bit in the Diode Fault Register is set. This bit is automatically cleared when the Diode Fault Register is read and the bits are cleared.

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6.13 Error Status Registers

Table 6.20 Error Status Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
1Fh	R-C	Tcrit Status	HWS				EXT3_TCRIT	EXT2_TCRIT	EXT1_TCRIT	INT_TCRIT	00h
24h	R-C	High Status	-	-	-	-	EXT3_HI	EXT2_HI	EXT1_HI	INT_HI	00h
25h	R-C	Low Status	-	-	--	-	EXT3_LO	EXT2_LO	EXT1_LO	INT_LO	00h
26h	R-C	Diode Fault	-	-	-	-	EXT3_FLT	EXT2_FLT	EXT1_FLT	-	00h

The Error Status Registers report the specific error condition for all measurement channels with limits. If any bit is set in the High, Low, or Diode Fault Status register, the corresponding High, Low, or Fault bit is set in the Interrupt Status Register.

Reading the Interrupt Status Register does not clear the Error Status bit. Reading from any Error Status Register that has bits set will clear the register and the corresponding bit in the Interrupt Status Register if the error condition has been removed. If the error condition is persistent, reading the Error Status Registers will have no affect.

6.13.1 Tcrit Status Register

The Tcrit Status Register stores the event that caused the $\overline{\text{SYS_SHDN}}$ pin to be asserted. Each of the temperature channels must be associated with the $\overline{\text{SYS_SHDN}}$ pin before they can be set (see Section 6.9). Once the $\overline{\text{SYS_SHDN}}$ pin is asserted, it will be released when the temperature drops below the threshold level however the individual status bit will not be cleared until read.

6.14 Fan Status Register

Table 6.21 Fan Status Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
27h	R-C	Fan Status Register	WATCH	-	DRIVE_FAIL	-	-	-	FAN_SPIN	FAN_STALL	00h

The Fan Status Register contains the status bits associated with each fan driver.

Bit 7 - WATCH - This bit is asserted ‘1’ if the host has not programmed the fan driver within four (4) seconds after power up (i.e. the Watchdog Timer has timed out. See Section 5.9.

Bit 5 - DRIVE_FAIL - Indicates that the RPM based Fan Speed Control Algorithm cannot drive the Fan to the desired target setting at maximum drive. This bit can be masked from asserting the $\overline{\text{ALERT}}$ pin.

- ‘0’ - The RPM based Fan Speed Control Algorithm can drive Fan to the desired target setting.
- ‘1’ - The RPM based Fan Speed Control Algorithm cannot drive Fan to the desired target setting at maximum drive.

Bit 1- FAN_SPIN - This bit is asserted '1' if the Spin up Routine for the Fan cannot detect a valid tachometer reading within its maximum time window. This bit can be masked from asserting the $\overline{\text{ALERT}}$ pin.

Bit 0 - FAN_STALL - This bit is asserted '1' if the tachometer measurement on the Fan detects a stalled fan. This bit can be masked from asserting the $\overline{\text{ALERT}}$ pin.

6.15 Interrupt Enable Register

Table 6.22 Interrupt Enable Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
28	R/W	Interrupt Enable	-	-	-	-	EXT3_INT_EN	EXT2_INT_EN	EXT1_INT_EN	INT_INT_EN	00h

The Interrupt Enable Register controls the masking for each temperature channel. When a channel is masked, it will not cause the $\overline{\text{ALERT}}$ pin to be asserted when an error condition is detected.

Bit 3 - EXT3_INT_EN (EMC2103-2 and EMC2103-4 only) - Allows the External Diode 3 to assert the $\overline{\text{ALERT}}$ pin.

- '0' (default) - The $\overline{\text{ALERT}}$ pin will not be asserted for any error condition associated with External Diode 3 channel.
- '1' - The $\overline{\text{ALERT}}$ pin will be asserted for an error condition associated with External Diode 3 channel.

Bit 2 - EXT2_INT_EN (EMC2103-2 and EMC2103-4 only) - Allows the External Diode 2 to assert the $\overline{\text{ALERT}}$ pin.

- '0' (default) - The $\overline{\text{ALERT}}$ pin will not be asserted for any error condition associated with External Diode 2 channel.
- '1' - The $\overline{\text{ALERT}}$ pin will be asserted for an error condition associated with External Diode 2 channel.

Bit 1 - EXT1_INT_EN - Allows the External Diode 1 to assert the $\overline{\text{ALERT}}$ pin.

- '0' (default) - The $\overline{\text{ALERT}}$ pin will not be asserted for any error condition associated with External Diode 1 channel.
- '1' - The $\overline{\text{ALERT}}$ pin will be asserted for an error condition associated with External Diode 1 channel.

Bit 0 - INT_INT_EN - Allows the Internal Diode to assert the $\overline{\text{ALERT}}$ pin.

- '0' (default) - The $\overline{\text{ALERT}}$ pin will not be asserted for any error condition associated with the Internal Diode.
- '1' - The $\overline{\text{ALERT}}$ pin will be asserted for an error condition associated with the Internal Diode.

6.16 Fan Interrupt Enable Register

Table 6.23 Fan Interrupt Enable Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
29	R/W	Fan Interrupt Enable	-	-	-	-	-	-	SPIN_INT_EN	STALL_INT_EN	00h

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The Fan Interrupt Enable Register controls the masking for errors generated by the Fan Driver. When a channel is masked, it will not cause the $\overline{\text{ALERT}}$ pin to be asserted when an error condition is detected.

Bit 1 - SPIN_INT_EN - Allows the FAN_SPIN bit to assert the $\overline{\text{ALERT}}$ pin.

- '0' (default) - the FAN_SPIN bit will not assert the $\overline{\text{ALERT}}$ pin though it will still update the Status Register normally.
- '1' - the FAN_SPIN bit will assert the $\overline{\text{ALERT}}$ pin.

Bit 0 - STALL_INT_EN - Allows the FAN_STALL bit or DRIVE_FAIL bit to assert the $\overline{\text{ALERT}}$ pin.

- '0' (default) - the FAN_STALL bit or DRIVE_FAIL bit will not assert the $\overline{\text{ALERT}}$ pin though will still update the Status Register normally.
- '1' - the FAN_STALL bit will assert the $\overline{\text{ALERT}}$ pin.

6.17 PWM Configuration Register

Table 6.24 PWM Configuration Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
2Ah	R/W	PWM Config	-	-	-	PWM_OT	-	-	-	POLARITY	00h

The PWM Config Register controls the output type and polarity of the PWM output.

Bit 4 - PWM_OT - Determines the output type for the PWM pin.

- '0' (default) - The PWM pin is configured as an open drain output.
- '1' - The PWM pin is configured as a push-pull output.

Bit 0 - POLARITY1 - Determines the polarity of PWM1 (if enabled).

- '0' (default) - the Polarity of the PWM driver is normal. A drive setting of 00h will cause the output to be set at 0% duty cycle and a drive setting of FFh will cause the output to be set at 100% duty cycle.
- '1' - The Polarity of the PWM driver is inverted. A drive setting of 00h will cause the output to be set at 100% duty cycle and a drive setting of FFh will cause the output to be set at 0% duty cycle.

6.18 PWM Base Frequency Register

Table 6.25 PWM Base Frequency Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
2Bh	R/W	PWM Base Frequency	-	-	-	-	-	-	PWM_BASE[1:0]		03h

The PWM Base Frequency Register controls base frequency of the PWM output.

Bits 1-0 - PWM_BASE[1:0] - Determines the base frequency of the PWM driver (PWM).

Table 6.26 PWM_BASEx[1:0] it Decode

PWM_BASE[1:0]		BASE FREQUENCY
1	**0**	
0	0	26.00kHz
0	1	19.531kHz
1	0	4,882Hz
1	1	2,441Hz (default)

6.19 Limit Registers

Table 6.27 Limit Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
30h	R/W	External Diode 1 High Limit	Sign	64	32	16	8	4	2	1	55h (+85°C)
31h **	R/W	External Diode 2 High Limit **	Sign	64	32	16	8	4	2	1	55h (+85°C)
32h **	R/W	External Diode 3 High Limit **	Sign	64	32	16	8	4	2	1	55h (+85°C)
34h	R/W	Internal Diode High Limit	Sign	64	32	16	8	4	2	1	55h (+85°C)
38h	R/W	External Diode 1 Low Limit	Sign	64	32	16	8	4	2	1	00h (0°C)
39h **	R/W	External Diode 2 Low Limit **	Sign	64	32	16	8	4	2	1	00h (0°C)
3Ah **	R/W	External Diode 3 Low Limit **	Sign	64	32	16	8	4	2	1	00h (0°C)
3Ch	R/W	Internal Diode Low Limit	Sign	64	32	16	8	4	2	1	00h (0°C)

The EMC2103 contains high limits for all temperature channels. If any measurement meets or exceeds the high limit then the appropriate status bit is set and the $\overline{\text{ALERT}}$ pin is asserted (if enabled).

Additionally, the EMC2103 contains low limits for all temperature channels. If the temperature channel drops below the low limit, then the appropriate status bit is set and the $\overline{\text{ALERT}}$ pin is asserted (if enabled).

All Limit Registers are Software Locked.

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6.20 Fan Setting Registers

Table 6.28 Fan Driver Setting Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
40h	R/W	Fan Setting	128	64	32	16	8	4	2	1	00h

The Fan Setting Register always displays the current setting of the Fan Driver. Reading from the register will report the current fan speed setting of the fan driver regardless of the operating mode. Therefore it is possible that reading from this register will not report data that was previously written into this register.

While the RPM based Fan Speed Control Algorithm or the Look Up Table are active (or both), then the register is read only. Writing to the register will have no affect and the data will not be stored.

If both the RPM based Fan Control Algorithm and the Look Up Table are disabled, then the register will be set with the previous value that was used. The register is read / write and writing to this register will affect the fan speed.

The contents of the register represent the weighting of each bit in determining the final duty cycle. The output drive for a PWM output is given by Equation [1].

$$Drive = \left(\frac{VALUE}{255}\right) \times 100\% \quad \textbf{[1]}$$

6.21 PWM Divide Register

Table 6.29 PWM Divide Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
41h	R/W	PWM Divide	128	64	32	16	8	4	2	1	01h

The PWM Divide Register determines the final frequency of the PWM driver. The driver base frequency is divided by the value of the PWM Divide Register to determine the final frequency. The duty cycle settings are not affected by these settings, only the final frequency of the PWM driver. A value of 00h will be decoded as 01h.

The final PWM frequency is derived as the base frequency divided by the value of this register as shown in Equation [2].

$$f_{PWM} = \frac{PWM\ base\ freqeuncy}{PWM\ \text{Divide Setting}} \quad \textbf{[2]}$$

6.22 Fan Configuration 1 Register

Table 6.30 Fan Configuration 1 Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
42h	R/W	Fan Configuration 1	EN_ ALGO	RANGE[1:0]		EDGES[1:0]		UPDATE[2:0]			2Bh

The Fan Configuration 1 Register controls the general operation of the RPM based Fan Speed Control Algorithm used on the PWM pin.

Bit 7 - EN_ALGO - enables the RPM based Fan Speed Control Algorithm. Based on the setting of the RPM / PWM bit, this bit is automatically set or cleared when the LUT_LOCK bit is set (see Section 6.32).

- '0' - (default) the control circuitry is disabled and the fan driver output is determined by the Fan Driver Setting Register.
- '1' - the control circuitry is enabled and the Fan Driver output will be automatically updated to maintain the programmed fan speed as indicated by the TACH Target Register.

Bits 6- 5 - RANGE[1:0] - Adjusts the range of reported and programmed tachometer reading values. The RANGE bits determine the weighting of all TACH values (including the Valid TACH Count, TACH Target, and TACH reading) as shown in Table 6.31.

Table 6.31 Range Decode

RANGE[1:0]		REPORTED MINIMUM RPM	TACH COUNT MULTIPLIER
1	**0**		
0	0	500	1
0	1	1000 (default)	2
1	0	2000	4
1	1	4000	8

Bits 4-3 - EDGES[1:0] - determines the minimum number of edges that must be detected on the TACH signal to determine a single rotation. A typical fan measured 5 edges (for a 2-pole fan). For more accurate tachometer measurement, the minimum number of edges measured may be increased.

Increasing the number of edges measured with respect to the number of poles of the fan will cause the TACH Reading registers to indicate a fan speed that is higher or lower than the actual speed. In order for the FSC Algorithm to operate correctly, the TACH Target must be updated by the user to accommodate this shift. The Effective Tach Multiplier shown in Table 6.32 is used as a direct multiplier term that is applied to the Actual RPM to achieve the Reported RPM. It should only be applied if the number of edges measured does not match the number of edges expected based on the number of poles of the fan (which is fixed for any given fan).

Contact Microchip for recommended settings when using fans with more or less than 2 poles.

Table 6.32 Minimum Edges for Fan Rotation

EDGES[1:0]		MINIMUM TACH EDGES	NUMBER OF FAN POLES	EFFECTIVE TACH MULTIPLIER (BASED ON 2 POLE FANS)
1	**0**			
0	0	3	1 pole	0.5
0	1	5	2 poles (default)	1
1	0	7	3 poles	1.5
1	1	9	4 poles	2

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Bit 2-0 - UPDATE - determines the base time between fan driver updates. The Update Time, along with the Fan Step Register, is used to control the ramp rate of the drive response to provide a cleaner transition of the actual fan operation as the desired fan speed changes. The Update Time is set as shown in Table 6.33.

Table 6.33 Update Time

UPDATE[2:0]			UPDATE TIME
2	**1**	**0**	
0	0	0	100ms
0	0	1	200ms
0	1	0	300ms
0	1	1	400ms (default)
1	0	0	500ms
1	0	1	800ms
1	1	0	1200ms
1	1	1	1600ms

6.23 Fan Configuration 2 Register

Table 6.34 Fan Configuration 2 Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
43h	R/W	Fan Configuration 2	-	EN_RRC	GLITCH_EN	DER_OPT [1:0]		ERR_RNG:0]		-	38h

The Fan Configuration 2 Register controls the tachometer measurement and advanced features of the RPM based Fan Speed Control Algorithm.

Bit 6 - EN_RRC - Enables ramp rate control when the fan driver is operated in the Direct Setting mode or the Direct Setting with LUT mode.

- '0' (default) - Ramp rate control is disabled. When the fan driver is operating in Direct Setting mode or Direct Setting with LUT mode, the PWM setting will instantly transition to the next programmed setting.
- '1' - Ramp rate control is enabled. When the fan driver is operating in Direct Setting mode or Direct Setting with LUT mode, the PWM setting will follow the ramp rate controls as determined by the Fan Step and Update Time settings. The maximum PWM step is capped at the Fan Step setting and is updated based on the Update Time as given by Table 6.33.

Bit 5 - GLITCH_EN - Disables the low pass glitch filter that removes high frequency noise injected on the TACH pin.

- '0' - The glitch filter is disabled.
- '1' (default) - The glitch filter is enabled.

Bits 4 - 3 - DER_OPT[1:0] - Control some of the advanced options that affect the derivative portion of the RPM based Fan Speed Control Algorithm as shown in Table 6.35. Note that the default derivative

options disable the ramp rate control maximum step settings. To take advantage of the full ramp rate control, limit derivative options to the disabled or basic derivative settings.

Table 6.35 Derivative Options

DER_OPT[1:0]		OPERATION
1	**0**	
0	0	No derivative terms used
0	1	Basic derivative. The derivative of the error from the current drive setting and the target is added to the iterative Fan Drive setting (in addition to proportional and integral terms)
1	0	Step derivative. The derivative of the error from the current drive setting and the target is added to the iterative Fan Drive setting and is not capped by the maximum Fan Step Register setting.
1	1	Both the basic derivative and the step derivative are used effectively causing the derivative term to have double the effect of the derivative term (default).

Bit 2 - 1 - ERR_RNG[1:0] - Control some of the advanced options that affect the error window. When the measured fan speed is within the programmed error window around the target speed, then the fan drive setting is not updated. The algorithm will continue to monitor the fan speed and calculate necessary drive setting changes based on the error, however these changes are ignored.

Table 6.36 Error Range Options

ERR_RNG[1:0]		OPERATION
1	**0**	
0	0	0 RPM (default)
0	1	50 RPM
1	0	100 RPM
1	1	200 RPM

The Fan Configuration 2 Register is Software Locked.

6.24 Gain Register

Table 6.37 Gain Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
45h	R/W	Gain Register	-	-	GAIND[1:0]		GAINI[1:0]		GAINP[1:0]		2Ah

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The Gain Register stores the gain terms used by the proportional and integral portions of the RPM based Fan Speed Control Algorithm. These terms will affect the FSC closed loop acquisition, overshoot, and settling as would be expected in a classic PID system.

Table 6.38 Gain Decode

GAIND OR GAINP OR GAINI [1:0]		RESPECTIVE GAIN FACTOR
1	**0**	
0	0	1x
0	1	2x
1	0	4x (default)
1	1	8x

6.25 Fan Spin Up Configuration Register

Table 6.39 Fan Spin Up Configuration Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
46h	R/W	Fan Spin Up Configuration	DRIVE_FAIL_CNT [1:0]		NOK ICK	SPIN_LVL[2:0]			SPINUP_TIME [1:0]		19h

The Fan Spin Up Configuration Register controls the settings of Spin Up Routine.

Bit 7 - 6 - DRIVE_FAIL_CNT[1:0] - Determines how many update cycles are used for the Drive Fail detection function as shown in Table 6.40. This circuitry determines whether the fan can be driven to the desired tach target.

Table 6.40 DRIVE_FAIL_CNT[1:0] Bit Decode

DRIVE_FAIL_CNT[1:0]		NUMBER OF UPDATE PERIODS
1	**0**	
0	0	Disabled - the Drive Fail detection circuitry is disabled
0	1	16 - the Drive Fail detection circuitry will count for 16 update periods
1	0	32 - the Drive Fail detection circuitry will count for 32 update periods
1	1	64 - the Drive Fail detection circuitry will count for 64 update periods

Bit 5 - NOKICK - Determines if the Spin Up Routine will drive the fan to 100% duty cycle for 1/4 of the programmed spin up time before driving it at the programmed level.

- '0' (default) - The Spin Up Routine will drive the PWM to 100% for 1/4 of the programmed spin up time before reverting to the programmed spin level.

- '1' - The Spin Up Routine will not drive the PWM to 100%. It will set the drive at the programmed spin level for the entire duration of the programmed spin up time.

Bits 4 - 2 - SPIN_LVL[2:0] - Determines the final drive level that is used by the Spin Up Routine as shown in Table 6.41.

Table 6.41 Spin Level

SPIN_LVL[2:0]			SPIN UP DRIVE LEVEL
2	**1**	**0**	
0	0	0	30%
0	0	1	35%
0	1	0	40%
0	1	1	45%
1	0	0	50%
1	0	1	55%
1	1	0	60% (default)
1	1	1	65%

Bit 1 -0 - SPINUP_TIME[1:0] - determines the maximum Spin Time that the Spin Up Routine will run for (see Section 5.7). If a valid tachometer measurement is not detected before the Spin Time has elapsed, then an interrupt will be generated. When the RPM based Fan Speed Control Algorithm is active, the fan driver will attempt to re-start the fan immediately after the end of the last spin up attempt.

The Spin Time is set as shown in Table 6.42.

Table 6.42 Spin Time

SPINUP_TIME[1:0]		TOTAL SPIN UP TIME
1	**0**	
0	0	250 ms
0	1	500 ms (default)
1	0	1 sec
1	1	2 sec

The Fan Spin Up Configuration Register is software locked.

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6.26 Fan Step Register

Table 6.43 Fan Step Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
47h	R/W	Fan Max Step	-	-	32	16	8	4	2	1	10h

The Fan Step Register, along with the Update Time, control the ramp rate of the fan driver response. The value of the registers represents the maximum step size each fan driver will take between update times (see Section 6.22).

All modes of operation have the options to use the Fan Step Register (and update times) for ramp rate control based on the Fan Configuration 2 Register settings. The Fan Speed Control Algorithm will always use the Fan Step Register settings (but see application note below).

APPLICATION NOTE: If the Fan Speed Control Algorithm is used, the default settings in the Fan Configuration 2 Register will cause the maximum fan step settings to be ignored.

The Fan Step Register is software locked.

6.27 Fan Minimum Drive Register

Table 6.44 Minimum Fan Drive Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
48h	R/W	Fan Minimum Drive	128	64	32	16	8	4	2	1	66h (40%)

The Fan Minimum Drive Register stores the minimum drive setting for the RPM based Fan Speed Control Algorithm. This register is not used if the FSC is not active. The RPM based Fan Speed Control Algorithm will not drive the fan at a level lower than the minimum drive unless the target TACH Target is set at FFh (see Section 6.30)

During normal operation, if the fan stops for any reason (including low drive), the RPM based Fan Speed Control Algorithm will attempt to restart the fan. Setting the Fan Minimum Drive Registers to a setting that will maintain fan operation is a useful way to avoid potential fan oscillations as the control circuitry attempts to drive it at a level that cannot support fan operation.

The Fan Minimum Drive Register is software locked.

6.28 Valid TACH Count Register

Table 6.45 Valid TACH Count Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
49h	R/W	Valid TACH Count	4096	2048	1024	512	256	128	64	32	F5h

The Valid TACH Count Register store the maximum TACH Reading Register value to indicate that the the fan is spinning properly. The value is referenced at the end of the Spin Up Routine to determine if the fan has started operating and decide if the device needs to retry.

See Equation [4] for translating the count to an RPM.

If the TACH Reading Register value exceeds the Valid TACH Count Register (indicating that the Fan RPM is below the threshold set by this count), then a stalled fan is detected. In this condition, the algorithm will automatically begin its Spin Up Routine.

APPLICATION NOTE: The automatic invoking of the Spin Up Routine only applies if the Fan Speed Control Algorithm is used. If the FSC is disabled, then the device will only invoke the Spin Up Routine when the PWM setting changes from 00h.

If a TACH Target setting is set above the Valid TACH Count setting, then that setting will be ignored and the algorithm will use the current fan drive setting.

The Valid TACH Count Register is software locked.

6.29 Fan Drive Fail Band Registers

Table 6.46 Fan Drive Fail Band Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
4Ah	R/W	Fan Drive Fail Band Low Byte	16	8	4	2	1	-	-	-	00h
4Bh	R/W	Fan Drive Fail Band High Byte	4096	2048	1024	512	256	128	64	32	00h

The Fan Drive Fail Band Registers store the number of tach counts used by the Fan Drive Fail detection circuitry. This circuitry is activated when the fan drive setting high byte is at FFh. When it is enabled, the actual measured fan speed is compared against the target fan speed.

This circuitry is used to indicate that the target fan speed at full drive is higher than the fan is actually capable of reaching. If the measured fan speed does not exceed the target fan speed minus the Fan Drive Fail Band Register settings for a period of time longer than set by the DRIVE_FAIL_CNTx[1:0] bits then the DRIVE_FAIL status bit will be set and an interrupt generated.

6.30 TACH Target Register

Table 6.47 TACH Target Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
4Ch	R/W	Fan TACH Target Low Byte	16	8	4	2	1	-	-	-	F8h
4Dh	R/W	TACH Target	4096	2048	1024	512	256	128	64	32	FFh

The TACH Target Register holds the target tachometer value that is maintained by the RPM based Fan Speed Control Algorithm.

The value in the TACH Target Register will always reflect the current TACH Target value. If the Look Up Table is active and configured to operate in RPM Mode, then this register will be read only. Writing to this register will have no affect and the data will not be stored.

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If the algorithm is enabled then setting the TACH Target Register to FFh will disable the fan driver (set the PWM duty cycle to 0%). Setting the TACH Target to any other value (from a setting of FFh) will cause the algorithm to invoke the Spin Up Routine after which it will function normally.

6.31 TACH Reading Register

Table 6.48 TACH Reading Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
4Eh	R	Fan TACH	4096	2048	1024	512	256	128	64	32	FFh
4Fh	R	Fan TACH Low Byte	16	8	4	2	1	-	-	-	F8h

The TACH Reading Register contents describe the current tachometer reading for the fan. By default, the data represents the fan speed as the number of 32kHz clock periods that occur for a single revolution of the fan.

Equation [3] shows the detailed conversion from TACH measurement (COUNT) to RPM while Equation [4] shows the simplified translation of TACH Reading Register count to RPM assuming a 2-pole fan, measuring 5 edges, with a frequency of 32.768kHz.

These equations are solved and tabulated for ease of use in AN17.4 RPM to TACH Counts Conversion.

$$RPM = \frac{1}{(poles)} \times \frac{(n-1)}{COUNT \times \frac{1}{m}} \times 1{,}966{,}080 \quad \textbf{[3]}$$

where:

poles = number of poles of the fan (typically 2)

n = number of edges measured (typically 5)

m = the multiplier defined by the RANGE bits

COUNT = TACH Reading Register value (in decimal)

$$RPM = \frac{3{,}932{,}160 \times m}{COUNT} \quad \textbf{[4]}$$

6.32 Look Up Table Configuration Register

Table 6.49 Look Up Table Configuration Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
50h	R/W	LUT Configuration	USE_DTS_F1	USE_DTS_F2	LUT_LOCK	RPM / PWM	-	TEMP3_CFG	-	TEMP4_CFG	00h

The Look Up Table Configuration Register controls the setup information for the temperature to fan drive look up table.

Bit 7 - USE_DTS_F1 - This bit determines whether the Pushed Temperature 1 Register is using DTS data.

- '0' (default) - The Pushed Temperature 1 Register is not using DTS data. The contents of the Pushed Temperature 1 registers is standard temperature data.
- '1' - The Pushed Temperature 1 Register is loaded with DTS data. The contents of this register is automatically subtracted from a fixed value of 100°C before being compared to the Look Up Table threshold levels.

Bit 6 - USE_DTS_F2 - This bit determines whether the Pushed Temperature 2 Register is using DTS data.

- '0' (default) - The Pushed Temperature 2 Register is not using DTS data. The contents of this register is standard 2's complement temperature data.
- '1' - The Pushed Temperature 2 Register is loaded with DTS data. The contents of this register is automatically subtracted from a fixed value of 100°C before being compared to the Look Up Table threshold levels.

Bit 5 - LUT_LOCK - This bit locks updating the Look Up Table entries and determines whether the look up table is being used.

- '0' (default) - The Look Up Table entries can be updated normally. The Look Up Table will not be used while the Look Up Table entries are unlocked. During this condition, the PWM output will not change states regardless of temperature or tachometer variation.
- '1' - The Look Up Table entries are locked and cannot be updated. The Look Up Table is fully active and will be used based on the loaded values. The PWM output will be updated depending on the temperature and / or TACH variations.

APPLICATION NOTE: When the LUT_LOCK bit is set at a logic '0', the PWM drive setting will be set at whatever value was last used by the RPM based Fan Speed Control Algorithm or the Look Up Table.

Bit 4 - RPM / PWM - This bit selects the data format for the LUT drive settings.

- '0' (default) - The Look Up Table drive settings are RPM TACH count values for use by the RPM based Fan Speed Control Algorithm. The Look Up Table drive settings should be loaded highest value to lowest value (to coincide with the inversion between TACH counts and actual RPM).
- '1' - The Look Up Table drive settings are PWM duty cycle values and are used directly. The drive settings should be loaded lowest value to highest value.

Bit 2 - TEMP3_CFG - Determine the temperature channel that is used for the Temperature 3 inputs to the Look Up Table. If the External Diode 3 channel is not enabled, then the Temperature 3 inputs are not used by the Look Up Table.

- '0' (default) - The External Diode 3 channel is used by the Fan Look Up Table (if enabled).
- '1' - The data written into the Pushed Temperature 1 Register is used by the Fan Look Up Table.

Bit 0 - TEMP4_CFG - Determine the temperature channel that is used for the Temperature 4 inputs to the Look Up Table.

- '0' (default) - The Internal channel is used by the Fan Look Up Table.
- '1' - The data written into the Pushed Temperature 2 Register is used by the Fan Look Up Table.

6.33 Look Up Table Registers

Table 6.50 Look Up Table Registers

ADDR	R/W	REGISTER	RPM / PWM	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
51h	R/W	LUT Drive Setting 1	'0'	4096	2048	1024	512	256	128	64	32	FBh
			'1'	128	64	32	16	8	4	2	1	

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Table 6.50 Look Up Table Registers (continued)

ADDR	R/W	REGISTER	RPM / PWM	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
52h	R/W	LUT Ext Diode 1 Setting 1	X	-	64	32	16	8	4	2	1	7Fh (127°C)
53h	R/W	LUT Ext Diode 2 Setting 1	X	-	64	32	16	8	4	2	1	7Fh (127°C)
54h	R/W	LUT Temp 3 Setting 1	X	-	64	32	16	8	4	2	1	7Fh (127°C)
55h	R/W	LUT Temp 4 Setting 1	X	-	64	32	16	8	4	2	1	7Fh (127°C)
. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .
74h	R/W	LUT Drive Setting 8	‘0’	4096	2048	1024	512	256	128	64	32	92h
			‘1’	128	64	32	16	8	4	2	1	
75h	R/W	LUT Ext Diode 1 Setting 8	X	-	64	32	16	8	4	2	1	7Fh (127°C)
76h	R/W	LUT Ext Diode 2 Setting 8	X	-	64	32	16	8	4	2	1	7Fh (127°C)
77h	R/W	LUT Temp 3 Setting 8	X	-	64	32	16	8	4	2	1	7Fh (127°C)
78h	R/W	LUT Temp 4 Setting 8	X	-	64	32	16	8	4	2	1	7Fh (127°C)
79h	R/W	LUT Temp Hysteresis	X	-	-	-	16	8	4	2	1	0Ah

The Look Up Table Registers hold the 40 entries of the Look Up Table that controls the drive of the PWM. As the temperature channels are updated, the measured value for each channel is compared against the respective entries in the Look Up Table and the associated drive setting is loaded into an internal shadow register and stored.

The bit weighting for temperature inputs represents °C and is compared against the measured data. Note that the LUT entry does not include a sign bit. The Look Up Table does not support negative temperature values and the MSBit should not be set for a temperature input.

Each temperature channel threshold shares the same hysteresis value. When the measured temperature for any of the channels meets or exceeds the programmed threshold, the drive setting associated with that threshold is used. The temperature must drop below the threshold minus the hysteresis value before the drive setting will be set to the previous value.

If the RPM based Fan Speed Control Algorithm is used, the TACH Target is updated after every conversion. It is always set to the minimum TACH Target that is stored by the Look Up Table. The PWM duty cycle is updated based on the RPM based Fan Speed Control Algorithm configuration settings.

If the RPM based Fan Speed Control Algorithm is not used, then the PWM duty cycle is updated after every conversion. It is set to the maximum duty cycle that is stored by the Look Up Table.

6.34 GPIO Direction Register (EMC2103-2 and EMC2103-4 Only)

Table 6.51 GPIO Direction Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
E1h	R/W	GPIO Direction 1	-	-					GPIO 2_DIR	GPIO 1_DIR	00h

The GPIO Direction Register controls the direction of GPIOs 1 and 2.

Bit 1 - GPIO2_DIR - Determines the direction of GPIO2.

- '0' (default) - GPIO2 is configured as an input.
- '1' - GPIO1 is configured as an output.

Bit 0 - GPIO2_DIR - Determines the direction of GPIO1.

- '0' (default) - GPIO1 is configured as an input.
- '1' - GPIO1 is configured as an output.

6.35 GPIO Output Configuration Register (EMC2103-2 and EMC2103-4 Only)

Table 6.52 GPIO Output Configuration Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
E2	R/W	GPIO Output Config	-						GPIO 2_OT	GPIO 1_OT	00h

The GPIO Output Configuration Register controls the output pin type of each GPIO pin.

Bit 1 - GPIO2_OT - Determines the output type for GPIO2.

- '0' (default) - GPIO2 is configured as an open drain output (if enabled as an output).
- '1' - GPIO2 is configured as a push-pull output (if enabled as an output).

Bit 0 - GPIO1_OT - Determines the output type for GPIO1.

- '0' (default) - GPIO1 is configured as an open drain output (if enabled as an output).
- '1' - GPIO1 is configured as a push-pull output (if enabled as an output).

6.36 GPIO Input Register (EMC2103-2 and EMC2103-4 Only)

Table 6.53 GPIO Input Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
E3h	R	GPIO Input	-	-					GPIO 2_IN	GPIO 1_IN	00h

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The GPIO Input Register indicates the state of the corresponding GPIO pin. When a GPIO is configured as an input, any change of state will assert the $\overline{\text{ALERT}}$ pin (unless GPIO interrupts are masked, see Section 6.15).

Bit 1 - GPIO2_IN - Indicates the pin state of the GPIO2 pin regardless of the pin functionality.

Bit 0 - GPIO1_IN - Indicates the pin state of the GPIO1 pin regardless of the pin functionality.

6.37 GPIO Output Register (EMC2103-2 and EMC2103-4 Only)

Table 6.54 GPIO Output Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
E4h	R/W	GPIO Output 1	-	-					GPIO2_OUT	GPIO1_OUT	00h

The GPIO Output Register controls the state of the corresponding pins when they are configured as outputs.

If the output is configured as an open-drain output, then it requires a pull-up resistor to VDD. Setting the corresponding bit to a '1' will act to disable the output allowing the pull-up resistor to pull the output high. Setting the corresponding bit to a '0' will enable the output and drive the pin to a logical '0' state.

If the output is configured as a push-pull output, then output pin will immediately be driven to match the corresponding bit setting.

Bit 1 - GPIO2_OUT - Controls the pin state of the GPIO2 pin when it is configured as a GPIO output.

Bit 0 - GPIO1_OUT - Controls the pin state of the GPIO1 pin when it is configured as a GPIO output.

6.38 GPIO Interrupt Enable Register (EMC2103-2 and EMC2103-4 Only)

Table 6.55 GPIO Interrupt Enable Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
E5h	R/W	GPIO Interrupt Enable	-	-					GPIO2_INT_EN	GPIO1_INT_EN	00h

The GPIO Interrupt Enable Register enables the GPIOs to assert the $\overline{\text{ALERT}}$ pin when they change state. When the GPIO pins are configured as outputs, then these bits are ignored.

Bit 1 - GPIO2_INT_EN - Allows the $\overline{\text{ALERT}}$ pin to be asserted when the GPIO2 pin changes state (when configured as an input).

- '0' (default) - The $\overline{\text{ALERT}}$ pin will not be asserted when the GPIO2 pin changes state (when configured as an input).
- '1' - The $\overline{\text{ALERT}}$ pin will be asserted when the GPIO2 pin changes state (when configured as an input)

Bit 0 - GPIO1_INT_EN - Allows the $\overline{\text{ALERT}}$ pin to be asserted when the GPIO1 pin changes state (when configured as an input).

- '0' (default) - The $\overline{\text{ALERT}}$ pin will not be asserted when the GPIO1 pin changes state (when configured as an input).
- '1' - The $\overline{\text{ALERT}}$ pin will be asserted when the GPIO1 pin changes state (when configured as an input)

6.39 GPIO Status Register (EMC2103-2 and EMC2103-4 Only)

Table 6.56 GPIO Status Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
E6h	R-C	GPIO Status	-	-					GPIO2_ STS	GPIO1_ STS	00h

The GPIO Status Register indicates which GPIO has changed states to cause the ALERT pin to be asserted. This register is cleared when it is read. The bits in this register are set whenever the corresponding GPIO changes states regardless if the ALERT pins are asserted. Once a bit is set, it will remain set until read.

If any bit in this register is set, then the GPIO status bit will be set.

Bit 1 - GPIO2_STS - Indicates that the GPIO2 pin has changed states from a '0' to a '1' or a '1' to a '0' (when configured as a GPIO input).

Bit 0 - GPIO1_STS - Indicates that the GPIO1 pin has changed states from a '0' to a '1' or a '1' to a '0' (when configured as a GPIO input).

6.40 Software Lock Register

Table 6.57 Software Lock

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
EFh	R/W	Software Lock	-	-	-	-	-	-	-	LOCK	00h

The Software Lock Register controls the software locking of critical registers. This register is software locked.

Bit 0 - LOCK - this bit acts on all registers that are designated SWL. When this bit is set, the locked registers become read only and cannot be updated.

- '0' (default) - all SWL registers can be updated normally.
- '1' - all SWL registers cannot be updated and a hard-reset is required to unlock them.

6.41 Product Features Register

Table 6.58 Product Features Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
FCh	R	Product Features	-	-	-	-	-	SHDN_SEL[2:0]			00h

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The Product Features Register indicates which pin selected functionality is enabled.

Table 6.59 SHDN_SEL[2:0] Encoding

SHDN_SEL[2:0]			DIODE MODE	OTHER FEATURES
2	1	0		
0	0	0	External Diode 1 Simple Mode - Beta compensation disabled, REC disabled - recommended for AMD CPU diodes	none
0	0	1	External Diode 1 Diode Mode - Beta compensation disabled, REC enabled	none
0	1	0	External Diode 1 Transistor Mode - Beta compensation enabled, REC enabled - - recommended for Intel 45nm and 65mn CPU diodes	none
0	1	1	Internal Diode Transistor Mode - Beta compensation enabled, REC enabled	none
1	0	0	External Diode 2 Transistor Mode - Beta compensation enabled, REC enabled (EMC2103-2 and EMC2103-4 only) External Diode 1 Diode mode (EMC2103-1 only)	none
1	0	1	External Diode 1 Transistor Mode - Beta compensation enabled, REC enabled	none

6.42 Product ID Register

Table 6.60 Product ID Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
FDh	R	Product ID Register (EMC2103-1)	0	0	1	0	0	1	0	0	24h
		Product ID Register (EMC2103-2 and EMC2103-4)	0	0	1	0	0	1	1	0	26h

The Product ID Register contains a unique 8-bit word that identifies the product.

6.43 Manufacturer ID Register

Table 6.61 Manufacturer ID Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
FEh	R	Manufacturer ID	0	1	0	1	1	1	0	1	5Dh

The Manufacturer ID Register contains an 8-bit word that identifies Microchip.

6.44 Revision Register

Table 6.62 Revision Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
FFh	R	Revision	0	0	0	0	0	0	0	1	01h

The Revision Register contains an 8-bit word that identifies the die revision.

- '0' - The lower 3 bits are writable for a range of 1.0053 to 1.0146
- '1' - The lower 4 bits are writable for a range of 1.0053 to 1.0253

DBh - IDCF Trim Register - sets the default value for the IDCF1 Register.

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Chapter 7 Package Drawing

7.1 EMC2103-1 Package Information

COMMON DIMENSIONS					
SYMBOL	MIN	NOM	MAX	NOTE	REMARK
A	0.80	0.85	0.90	-	OVERALL PACKAGE HEIGHT
A1	0	0.02	0.05	-	STANDOFF
A3		0.20 REF		-	LEAD-FRAME THICKNESS
D/E	3.90	4.00	4.10	-	X/Y BODY SIZE
D2/E2	2.00	2.10	2.20	2	X/Y EXPOSED PAD SIZE
L	0.45	0.50	0.55	-	TERMINAL LENGTH
b	0.25	0.30	0.35	2	TERMINAL WIDTH
K	0.20	-	-	-	TERMINAL TO PAD DISTANCE
e		0.80 BSC		-	TERMINAL PITCH

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. POSITION TOLERANCE OF EACH TERMINAL AND EXPOSED PAD IS ± 0.05mm AT MAXIMUM MATERIAL CONDITION. DIMENSIONS "b" APPLIES TO PLATED TERMINALS AND IT IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
3. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE AREA INDICATED.

Figure 7.1 12-Pin QFN 4mm x 4mm Package Dimensions

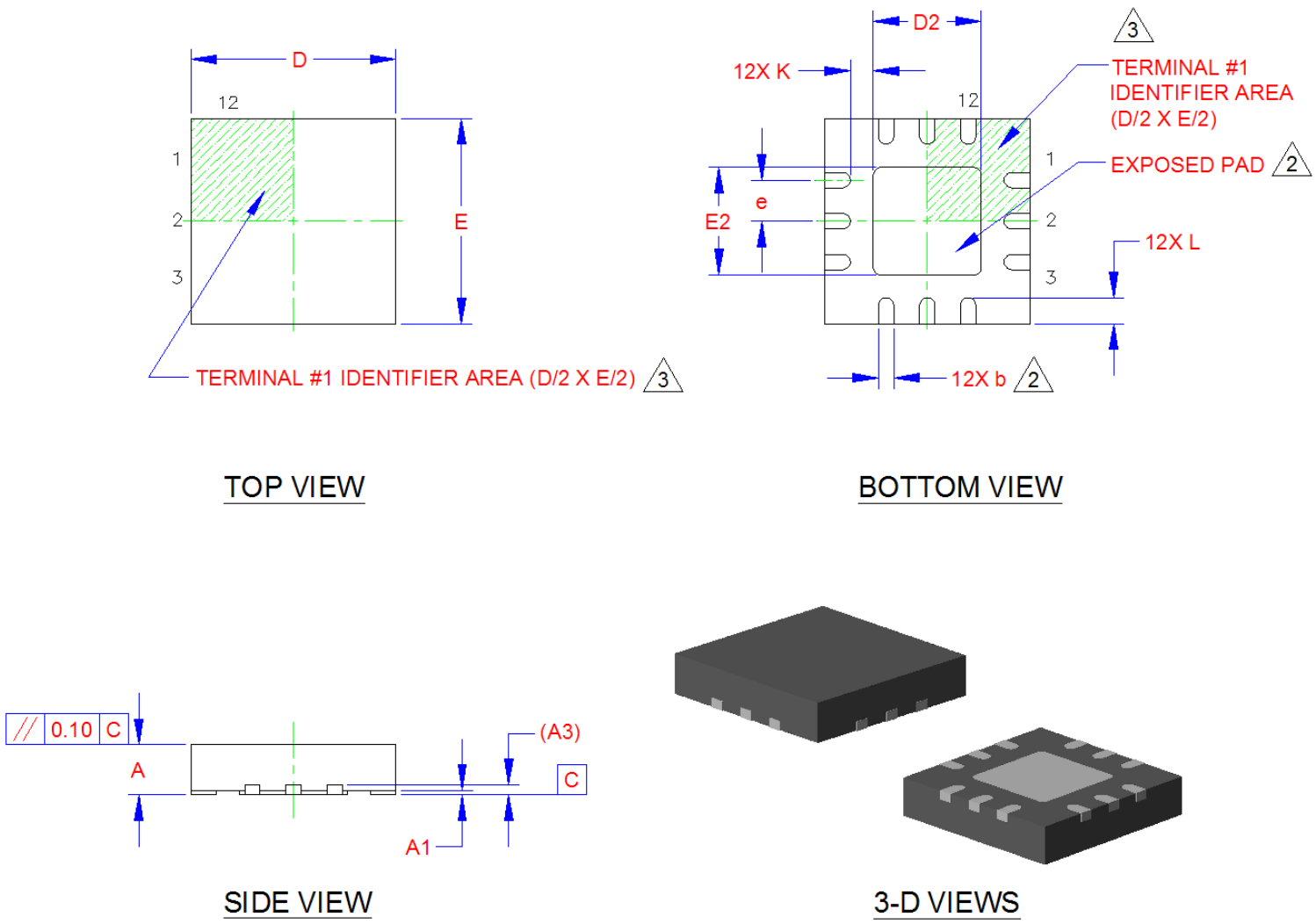
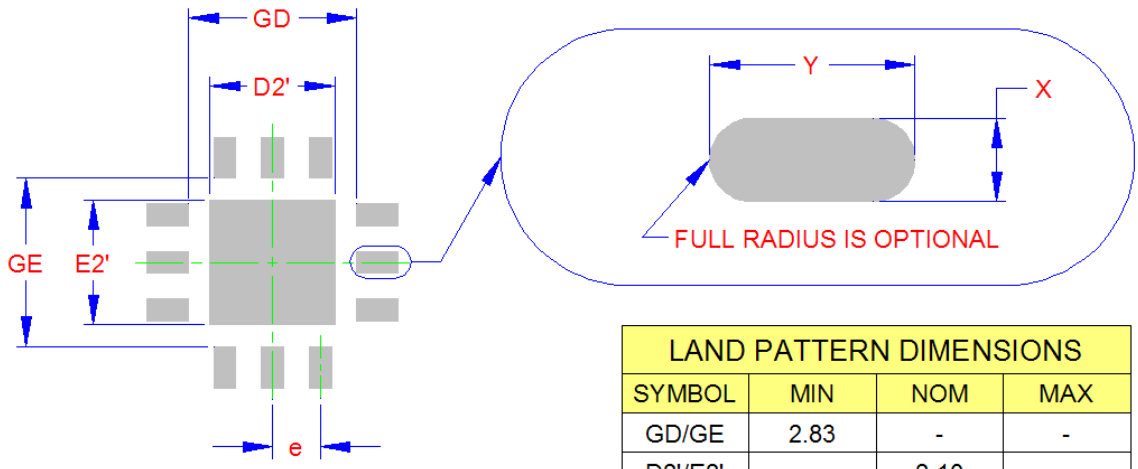


Figure 7.2 12-Pin QFN 4mm x 4mm Package Drawing

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LAND PATTERN DIMENSIONS			
SYMBOL	MIN	NOM	MAX
GD/GE	2.83	-	-
D2'/E2'	-	2.10	-
X	-	-	0.37
Y	-	-	0.69
e		0.80	

RECOMMENDED PCB LAND PATTERN

Figure 7.3 Recommended PCB Footprint 12-Pin QFN 4mm x 4mm

7.2 EMC2103-2 and EMC2103-4 Package Information

COMMON DIMENSIONS					
SYMBOL	MIN	NOM	MAX	NOTE	REMARK
A	0.80	0.85	0.90	-	OVERALL PACKAGE HEIGHT
A1	0	0.02	0.05	-	STANDOFF
A3		0.20 REF		-	LEAD-FRAME THICKNESS
D/E	3.90	4.00	4.10	-	X/Y BODY SIZE
D2/E2	2.00	2.10	2.20	2	X/Y EXPOSED PAD SIZE
L	0.45	0.50	0.55	-	TERMINAL LENGTH
b	0.25	0.30	0.35	2	TERMINAL WIDTH
K	0.20	-	-	-	TERMINAL TO PAD DISTANCE
e		0.65 BSC		-	TERMINAL PITCH

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. POSITION TOLERANCE OF EACH TERMINAL AND EXPOSED PAD IS ± 0.05mm AT MAXIMUM MATERIAL CONDITION. DIMENSIONS "b" APPLIES TO PLATED TERMINALS AND IT IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
3. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE AREA INDICATED.

Figure 7.4 16-Pin QFN 4mm x 4mm Package Dimensions

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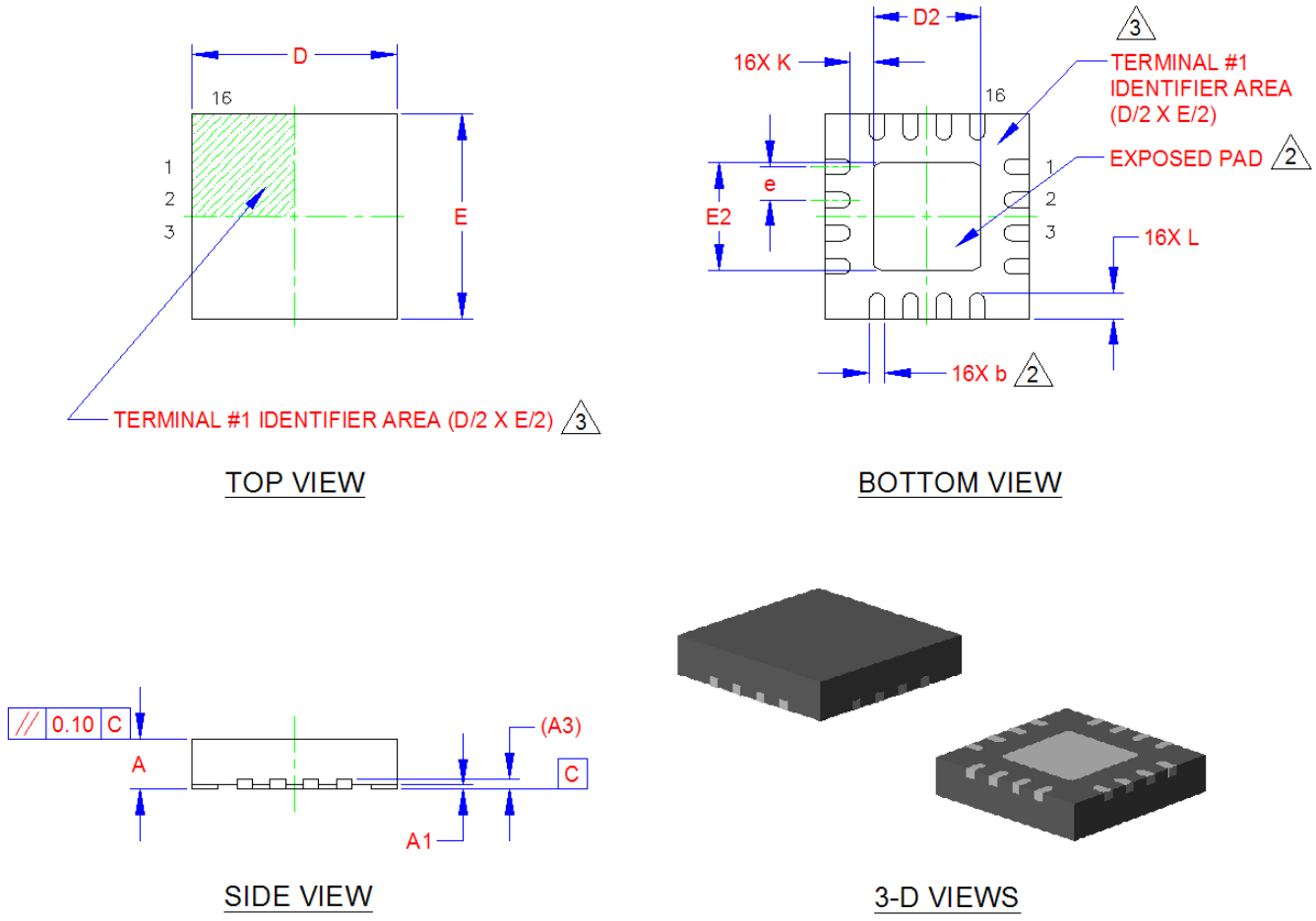
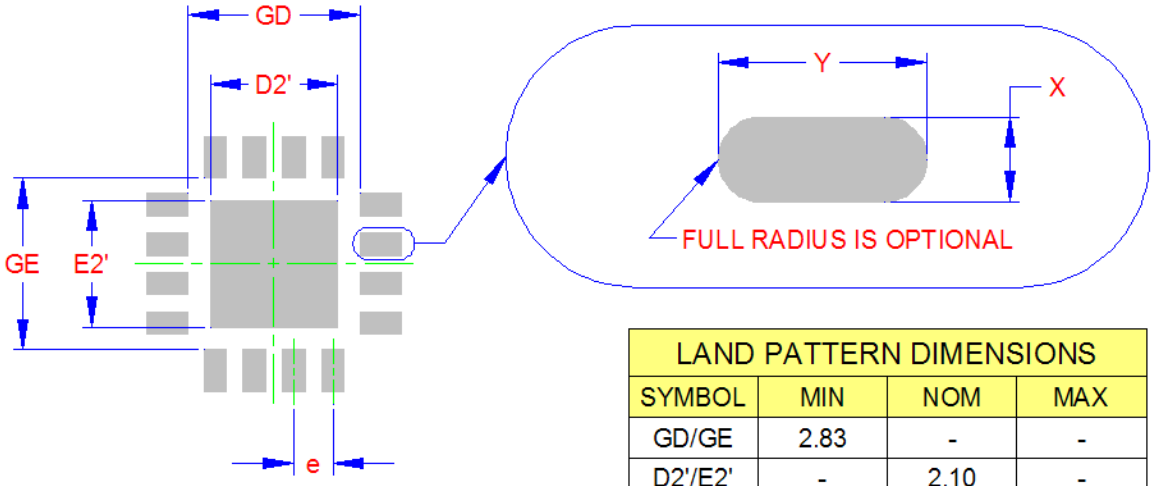


Figure 7.5 16-Pin QFN 4mm x 4mm Package Drawing

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LAND PATTERN DIMENSIONS			
SYMBOL	MIN	NOM	MAX
GD/GE	2.83	-	-
D2'/E2'	-	2.10	-
X	-	-	0.37
Y	-	-	0.69
e		0.65	

RECOMMENDED PCB LAND PATTERN

Figure 7.6 Recommended PCB Footprint 16-Pin QFN 4mm x 4mm

7.3 Package Markings

All devices are marked on the first line with “2103” followed by the dash number of the respective device. On the second line, they will be marked with the Lot Number. on the third line, they will be marked with the functional revision “B” and the Country Code.

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Appendix A Look Up Table Operation

The EMC2103 uses a look-up table to apply a user-programmable fan control profile based on measured temperature to the fan driver. In this look-up table, each temperature channel is allowed to control the fan drive output independently (or jointly) by programming up to eight pairs of temperature and drive setting entries.

The user programs the look-up table based on the desired operation. If the RPM based Fan Speed Control Algorithm is to be used (see Section 5.5), then the user must program an RPM target for each temperature setting of interest. Alternately, if the RPM based Fan Speed Control Algorithm is not to be used, then the user must program a drive setting for each temperature setting of interest.

If the measured temperature on the External Diode channel meets or exceeds any of the temperature thresholds for any of the channels, the fan output will be automatically set to the desired setting corresponding to the exceeded temperature. In cases where multiple temperature channel thresholds are exceeded, the highest fan drive setting will take precedence.

When the measured temperature drops to a point below a lower threshold minus the hysteresis value, the fan output will be set to the corresponding lower set point.

The following sections show examples of how the Look Up Table is used and configured. Each Look Up Table Example uses the Fan 1 Look Up Table Registers configured as shown in Table A.1.

Table A.1 Look Up Table Format

STEP	TEMP 1	TEMP 2	TEMP 3	TEMP 4	LUT DRIVE
1	LUT Temp 1 Setting 1 (52h)	LUT Temp 2 Setting 1 (53h)	LUT Temp 3 Setting 1 (54h)	LUT Temp 4 Setting 1 (55h)	LUT Drive Setting 1 (51h)
2	LUT Temp 1 Setting 2 (57h)	LUT Temp 2 Setting 2 (58h)	LUT Temp 3 Setting 2 (59h)	LUT Temp 4 Setting 2 (5Ah)	LUT Drive Setting 2 (56h)
3	LUT Temp 1 Setting 3 (5Ch)	LUT Temp 2 Setting 3 (5Dh)	LUT Temp 3 Setting 3 (5Eh)	LUT Temp 4 Setting 3 (5Fh)	LUT Drive Setting 3 (5Bh)
4	LUT Temp 1 Setting 4 (61h)	LUT Temp 2 Setting 4 (62h)	LUT Temp 3 Setting 4 (63h)	LUT Temp 4 Setting 4 (64h)	LUT Drive Setting 4 (60h)
5	LUT Temp 1 Setting 5 (66h)	LUT Temp 2 Setting 5 (67h)	LUT Temp 3 Setting 5 (68h)	LUT Temp 4 Setting 5 (69h)	LUT Drive Setting 5 (65h)
6	LUT Temp 1 Setting 6 (6Bh)	LUT Temp 2 Setting 6 (6Ch)	LUT Temp 3 Setting 6 (6Dh)	LUT Temp 4 Setting 6 (6Eh)	LUT Drive Setting 6 (6Ah)
7	LUT Temp 1 Setting 7 (70h)	LUT Temp 2 Setting 7 (71h)	LUT Temp 3 Setting 7 (72h)	LUT Temp 4 Setting 7 (73h)	LUT Drive Setting 7 (6Fh)
8	LUT Temp 1 Setting 8 (75h)	LUT Temp 2 Setting 8 (76h)	LUT Temp 3 Setting 8 (77h)	LUT Temp 4 Setting 8 (78h)	LUT Drive Setting 8 (74h)

A.1 Example #1

This example does not use the RPM based Fan Speed Control Algorithm. Instead, the Look Up Table is configured to directly set a PWM setting based on the temperature of four of its measured inputs. The configuration is set as shown in Table A.2.

Once configured, the Look Up Table is loaded as shown in Table A.3. Table A.3 shows three temperature configurations using the settings in Table A.3 and the final PWM output drive setting that the Look Up Table will select.

Table A.2 Look Up Table Example #1 Configuration

ADDR	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	SETTING
50h	LUT 1 Configuration	USE_DTS_F1	USE_DTS_F2	LUT_LOCK	RPM / PWM	-	TEMP3_CFG	-	TEMP4_CFG	C0h
		0	0	1	1	0	0	0	0	

Table A.3 Fan Speed Control Table Example #1

FAN SPEED STEP #	EXTERNAL DIODE 1 TEMPERATURE (CPU)	EXTERNAL DIODE 2 TEMPERATURE (GPU)	EXTERNAL DIODE 3 TEMPERATURE (SKIN)	INTERNAL DIODE TEMPERATURE (AMBIENT)	PWM SETTINGS
1	35°C	60°C	30°C	40°C	0%
2	40°C	70°C	35°C	45°C	30%
3	50°C	75°C	40°C	50°C	40%
4	60°C	80°C	45°C	55°C	50%
5	70°C	85°C	50°C	60°C	60%
6	80°C	90°C	55°C	65°C	70%
7	90°C	95°C	60°C	70°C	80%
8	100°C	100°C	65°C	75°C	100%

Note: The values shown in Table A.3 are example settings. All the cells in the look-up table are programmable via SMBus.

Table A.4 Fan Speed Determination for Example #1 (using settings in Table A.3)

	EXTERNAL DIODE 1 TEMPERATURE (CPU)	EXTERNAL DIODE 2 TEMPERATURE (GPU)	EXTERNAL DIODE 3 TEMPERATURE (SKIN)	INTERNAL DIODE TEMPERATURE (AMBIENT)	PWM RESULT
Example 1:	**82°C**	82°C	48°C	58°C	70% (CPU temp requires highest drive)
Example 2:	82C°	**97°C**	**62°C**	58°C	80% (GPU and Skin require highest drive)
Example 3:	82°C	97°C	62°C	**75°C**	100% (Internal temp requires highest drive)

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A.2 Example #2

This example uses the RPM based Fan Speed Control Algorithm. The Spin Level (used by the Spin Up Routine) should be changed to 50% drive for a total Spin Time of 1 second. For all other RPM configuration settings, the default conditions are used.

For control inputs, it uses the External Diode 1 channel normally, the External Diode 2 channel normally, and both Pushed Temperature registers in DTS format. The configuration is set as shown in Table A.5 while Table A.6 shows how the table is loaded.

Note that when using DTS data, the USE_DTS_F1 and / or USE_DTS_F2 bits should be set. The Pushed Temperature Registers are loaded with the normal DTS values as received by the processor. When the DTS value is used by the Look Up Table, the value that is stored in the Pushed Temperature Register is subtracted from a fixed temperature of 100°C. This resultant value is then compared against the Look Up Table thresholds normally. When programming the Look Up Table, it is necessary to take this translation into account or else incorrect settings may be selected.

Table A.5 Look Up Table Example #2 Configuration

ADDR	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	SETTING
42h	Fan 1 Configuration 1	EN_ ALGO	RANGE[1:0]		EDGES[1:0]		UPDATE[2:0]			CBh
		1	1	0	0	1	0	1	1	
46h	Fan 1 Spin Up Configuration	DRIVE_FAIL_CNT1 [1:0]		NOKICK 1	SPIN_LVL[2:0]			SPINUP_TIME [1:0]		0Ah
		0	0	0	0	1	0	1	0	
50h	LUT 1 Configuration	USE_DT S_F1	USE_D TS_F2	LUT_LO CK	RPM / PWM	-	TEMP3 _CFG		TEMP 3_CFG	E5h
		1	1	1	0	0	1	0	1	

Table A.6 Fan Speed Control Table Example #2

FAN SPEED STEP #	EXTERNAL DIODE 1 TEMPERATURE (CPU)	EXTERNAL DIODE 2 TEMPERATURE (GPU)	PUSHED TEMPERATURE SETTING (DTS1)	PUSHED TEMPERATURE SETTING (DTS2)	TACH TARGET
1	35°C	65°C	50°C	40°C	F4h (2014 RPM)
2	40°C	75°C	55°C	45°C	C4h (2508 RPM)
3	50°C	85°C	60°C	50°C	A0h (3072 RPM)
4	60°C	90°C	65°C	55°C	78h (4096 RPM)
5	70°C	95°C	70°C	60°C	60h (5120 RPM)
6	80°C	100°C	75°C	65°C	52h (5994 RPM)

Table A.6 Fan Speed Control Table Example #2 (continued)

FAN SPEED STEP #	EXTERNAL DIODE 1 TEMPERATURE (CPU)	EXTERNAL DIODE 2 TEMPERATURE (GPU)	PUSHED TEMPERATURE SETTING (DTS1)	PUSHED TEMPERATURE SETTING (DTS2)	TACH TARGET
7	90°C	105°C	80°C	80°C	46h (7022 RPM)
8	100°C	110°C	85°C	100°C	3Dh (8058 RPM)

Note: The values shown in Table A.6 are example settings. All the cells in the look-up table are programmable via SMBus.

Table A.7 Fan Speed Determination for Example #2 (using settings in Table A.6)

	EXTERNAL DIODE 1 TEMPERATURE (CPU)	EXTERNAL DIODE 2 TEMPERATURE (GPU)	PUSHED TEMPERATURE (DTS1)	PUSHED TEMPERATURE (DTS2)	PWM RESULT
Example 1:	**75°C**	75°C	35°C (translated as 65°C)	50°C (translated as 50°C)	0Ch (5120 RPM) - CPU requires highest target
Example 2:	75°C	90°C	**15°C (translated as 85°C)**	20°C (translated as 80°C)	08h (7680 RPM) - DTS1 requires highest target
Example 3:	75°C	97.25°C	30°C (translated as 70°C)	**5°C (translated as 95°C)**	09h (6826 RPM) - DTS2 requires highest target

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Datasheet Revision History

Revision History

REVISION LEVEL & DATE	SECTION/FIGURE/ENTRY	CORRECTION
REV A	Replaces the previous SMSC version Rev. 0.93	
Rev. 0.93 (01-08-10)	Table A.6, "Fan Speed Control Table Example #2"	Recalculated RPM values using Equation 3 to correct math errors.
Rev. 0.92 (5-17-09)	Section Chapter 2, "Pin Layout"	Added app note: For the 5V tolerant pins that have a pull-up resistor (SMCLK, SMDATA, ALERT, and SYS_SHDN), the voltage difference between VDD and the 5V tolerant pad must never be more than 3.6V.
	Table 3.1, "Absolute Maximum Ratings"	Updated voltage limits for 5V tolerant pins with pull-up resistors.
	Table 3.2, "Electrical Specifications"	Qualified leakage current (pull-up voltage ≤ 3.6V)
Rev. 0.91 (04-09-09)	Appendix B "RPM to Tachometer Count Look Up Tables"	Removed
	Section 6.31, "TACH Reading Register"	Added reference to AN17.4 “RPM to TACH Counts Conversion” which includes more information.
Rev. 0.89 (07-02-08)	Table 5.1, "SHDN_SEL Pin Decode"	Added note for EEPROM loading for EMC2103-4
	Section 4.9, "Programming from EEPROM"	Added section for EEPROM loading description
	Table 3.4, "EEPROM Loader Electrical Specifications"	Added specifications for EEPROM loading description

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