HV Start-up Green-mode PWM Convertor with Brown-Out Protection

General Description

EM8569A is a high performance, low cost, HV Start-up, current mode PWM controller with green mode power saving. The EM8569A integrates functions of Soft Start (SS), Under Voltage Lockout (UVLO), Leading Edge Blanking (LEB), internal Over Temperature Protection (OTP), and internal slope compensation. The EM8569A also features more protection like Over Load Protection (OLP) and Over Voltage Protection (OVP) to prevent circuit damage occurred under abnormal conditions. The EM8569A also has line under-voltage protection (Brown-out Protection).

Features

- 700V High Voltage Start up Circuit
- Current Mode Control
- Soft Start Function
- Built-in Slope Compensation
- Internal Leading-edge Blanking
- Brown in/out Protection
- Over Voltage Protection (OVP) on VCC pin
- Over Load Protection (OLP)
- Cycle-by-cycle Current Limit
- Feedback Open Protection
- Internal Over Temperature Protection (OTP)
- Constant Output Power Limit (Full AC Input Range)
- Excellent EMI performance

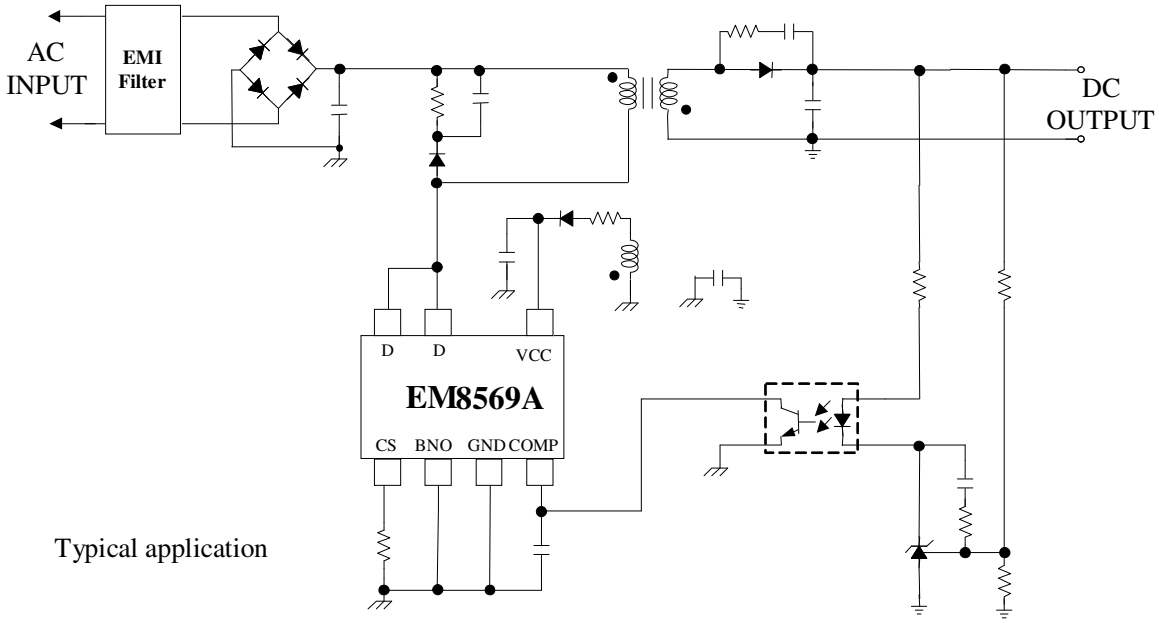
Ordering Information

Part Number	Package	Remark
EM8569AS7	DIP-7	

Applications

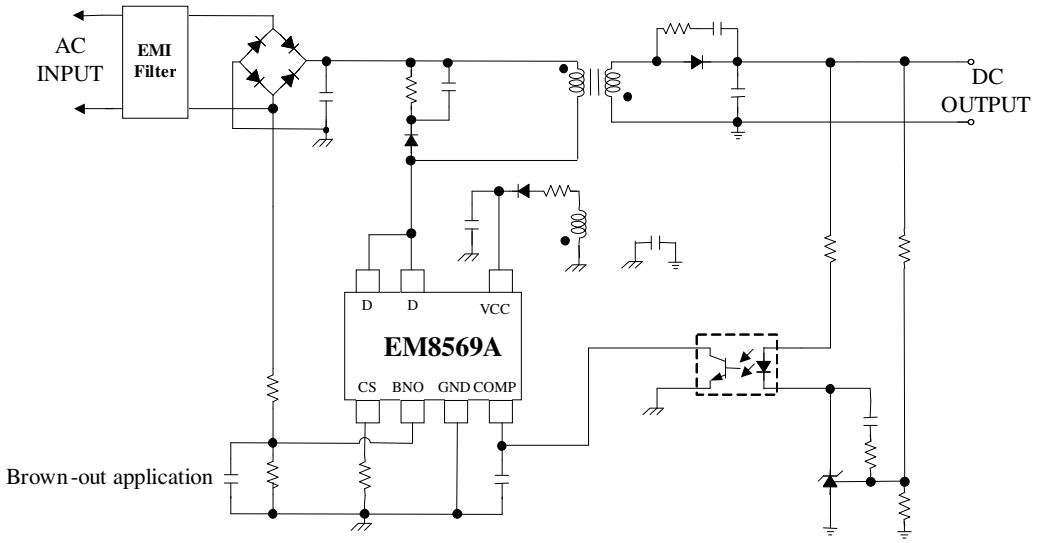
- LCD Monitor Power Supply
- Open-Frame SMPS

Typical Application Circuit 1

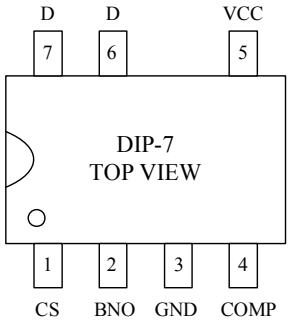


Typical application

Typical Application Circuit 2



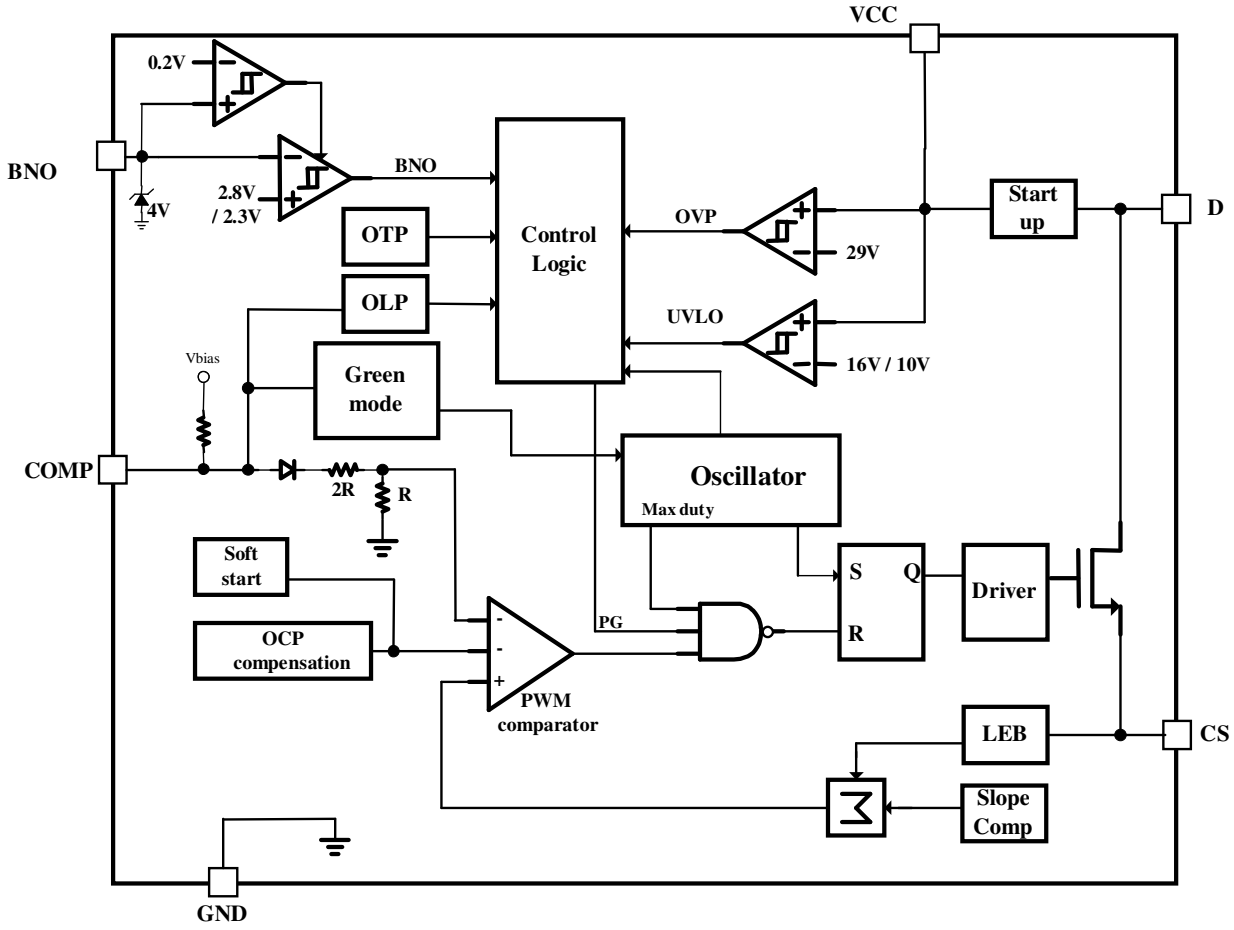
Pin Configuration



Pin Assignment

Pin Name	Pin Number	Pin Function
CS	1	Senses the primary current.
BNO	2	Line voltage detection. Use for brown-out protection.
GND	3	Ground.
COMP	4	Voltage feedback pin. By connecting a photo-coupler to close the control loop and achieve the regulation.
VCC	5	IC Power Supply Pin.
D	6,7	For start-up, the pin is also HV Power MOSFET drain Pin.

Function Block Diagram



Absolute Maximum Ratings (Note1)

- Supply Input Voltage, VCC ---------- 30V
- D pin---------- 700V
- BNO, COMP, CS Pin ---------- - 0.3V to 6.5V
- Power Dissipation, PD @ TA = 25℃
  DIP 7 ---------- 1.5W
- Package Thermal Resistance
  DIP 7 ---------- 80℃/W
- Junction Temperature ---------- 150℃
- Lead Temperature (Soldering, 10 sec.) ---------- 260℃
- Storage Temperature Range ---------- -65℃ to 150℃
- ESD Susceptibility (Note2)
  HBM (Human Body Mode) ---------- 2KV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note3)

- Supply Input Voltage, VCC ---------- 11V to 25V
- V_{CC} Capacitor ---------- 4.7uF to 47uF
- Junction Temperature Range---------- -40℃ to 125℃
- Ambient Temperature Range---------- -40℃ to 85℃

Electrical Characteristics

(V_{CC}=16V, T_A=25℃, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
VCC Section						
VCC OVP Protect voltage	V_{OVP}		27	29	31	V
Start up current	I_{START}	VCC=V_{TH-ON}-0.5V	-	45	65	uA
VCC On Threshold Voltage	V_{TH-ON}		15	16	17	V
VCC Off Threshold Voltage	V_{TH-OFF}		9	10	11	V
Operating Supply Current 1	I_{CC-OP1}	VCC=15V, V_{COMP}=0V,	-	0.7	2	mA
Operating Supply Current 2	I_{CC-OP2}	VCC=15V, V_{COMP}=3V,	-	2.5	-	mA
Operating Supply Current 3	I_{CC-OP3}	VCC=15V, Protection triggerred	-	0.3	-	mA
D Section						
HV Current Source		VCC=V_{TH-ON}-0.5V V_D=50V		1		mA
Drain to Source Breakdown voltage			700			V
Drain leakage current		VCC=V_{TH-ON}+0.5V V_D=700V, PWM off			300	uA
ON-Resistance				6		Ω
Switching time	T_F				250	nS
Current-Sense Section						
Maximum Internal Current Setpoint	V_{CSLim}	OCP at 36% Duty	0.81	0.9	0.99	V
		OCP at Zero on-Duty	0.70	0.78	0.86	V
Leading Edge Blanking Time	T_{LEB}		300	380	460	nS
Propagation Delay Time	T_{PD}			100		nS
Soft-Start Period	T_{SS}			3.5		mS
Internal Oscillator						
Oscillation Frequency	f_{OSC}		90	100	110	KHz
Jitter Percentage				+/-4		%
Jitter Period				2.6		mS
Maximum Duty	D_{max}			75		%
Green mode minimum frequency				22		KHz
Frequency variation vs. VCC		VCC=11V to 25V			3	%
Frequency variation vs. Temperature		-20℃ to 105℃(Note4)			3	%
COMP Section						
COMP short to GND current	I_{COMP}	V_{COMP}=0V	150	250	350	uA
Open loop COMP voltage	V_{COMP}	COMP pin open		5.2		V
COMP voltage to CS voltage Attenuation	Av		1 / 2.5	1 / 3	1 / 3.5	V/V

Green mode COMP Threshold Voltage	V_{Green}			1.8		V
COMP voltage for zero duty	$V_{COMP-ZD}$			1.3		V
BNO Section						
Brown-in threshold	V_{BNO-IN}		2.6	2.8	3	V
Brown-out threshold	$V_{BNO-OUT}$		2.1	2.3	2.5	V
BNO function disable threshold	$V_{BNO-DIS}$		0.15	0.2	0.25	V
Protection Section						
Open loop protection delay time	T_{delay}			56		mS
Open loop protection COMP Trip voltage	V_{OLP}			4.0		V
Internal Temperature Shutdown	T_{SD}			150		℃

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution is recommended.

Note 3. The device is not guaranteed to function outside its operating conditions.

Note 4. Guaranteed by design.

Typical Operating Characteristics

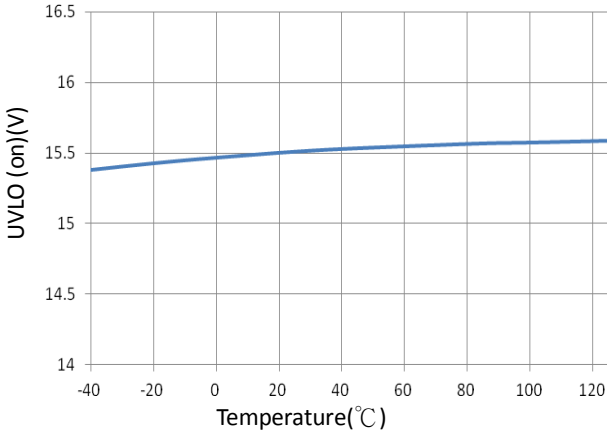


Fig1. UVLO (on) vs. Temperature.

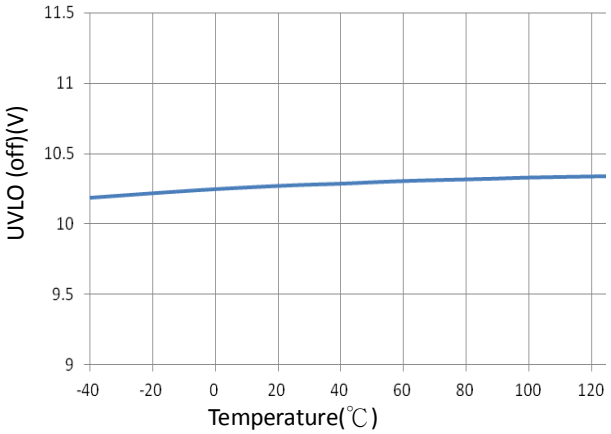


Fig2. UVLO (off) vs. Temperature

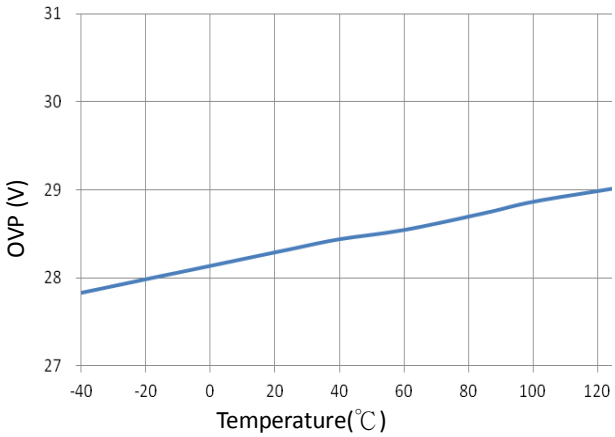


Fig3. OVP vs. Temperature.

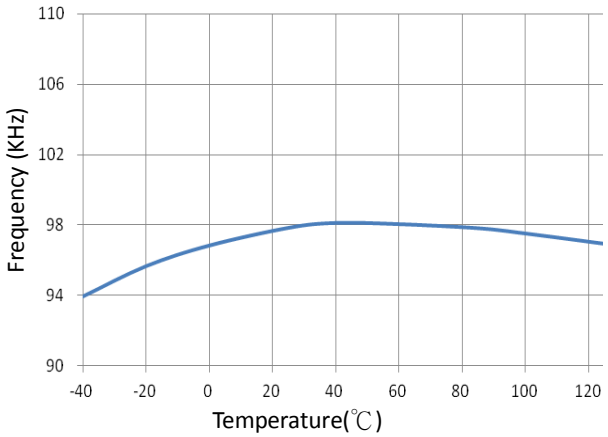


Fig4. Frequency vs. Temperature.

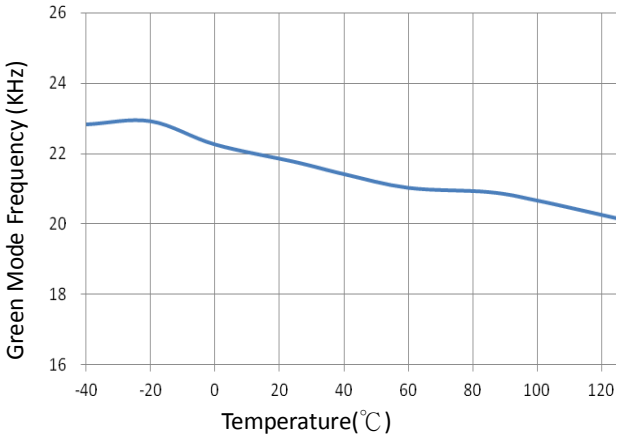


Fig5. Green Mode Frequency vs. Temperature.

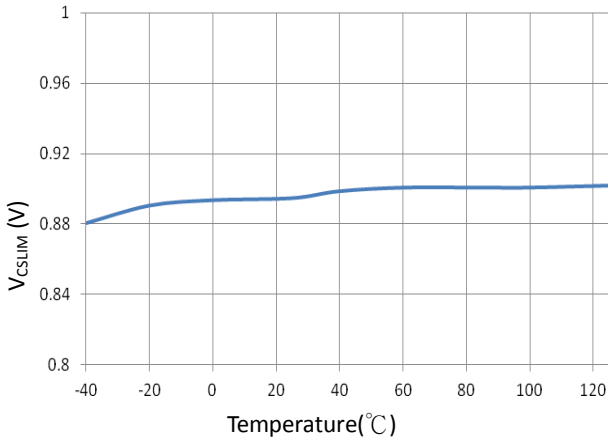


Fig6. V_{CSLIM} vs. Temperature.

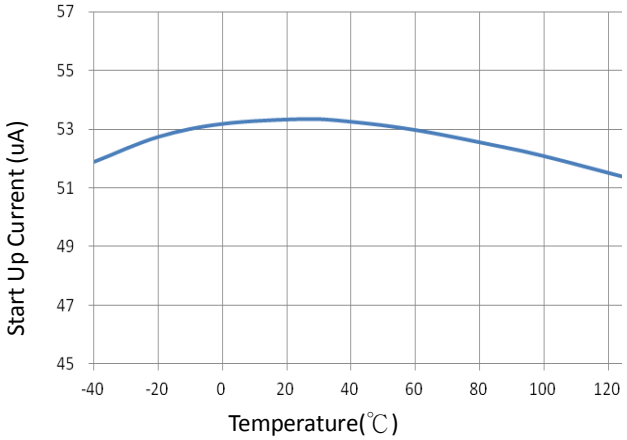


Fig7. Start Up Current vs. Temperature.

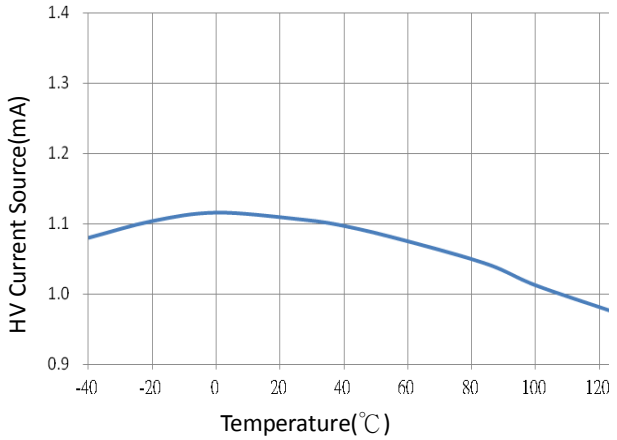


Fig8. HV Current Source vs. Temperature.

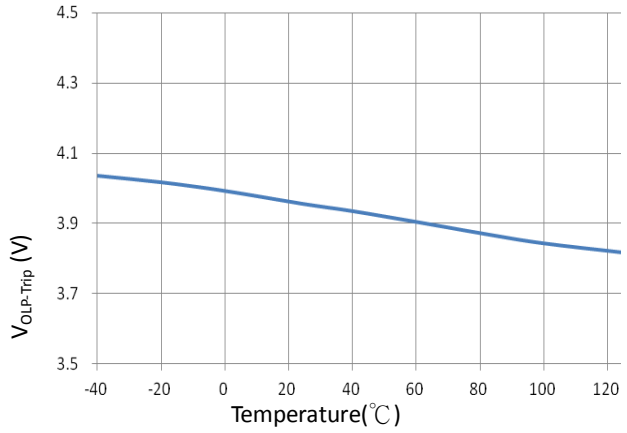


Fig9. $V_{OLP-Trip}$ vs. Temperature.

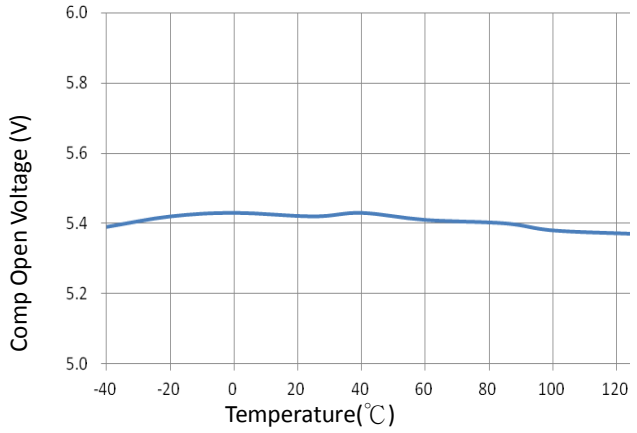


Fig10. Comp Open Voltage vs. Temperature.

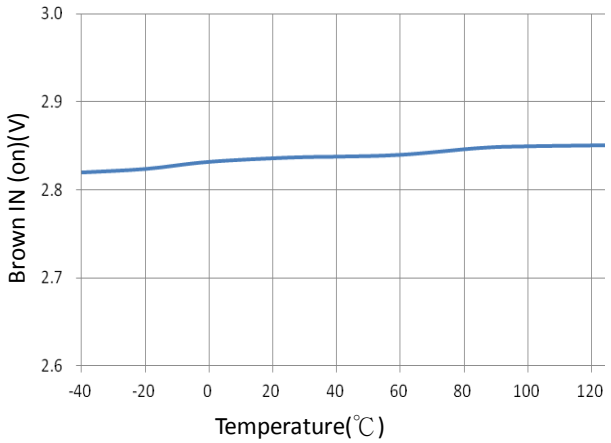


Fig11. Brown In (on) vs. Temperature

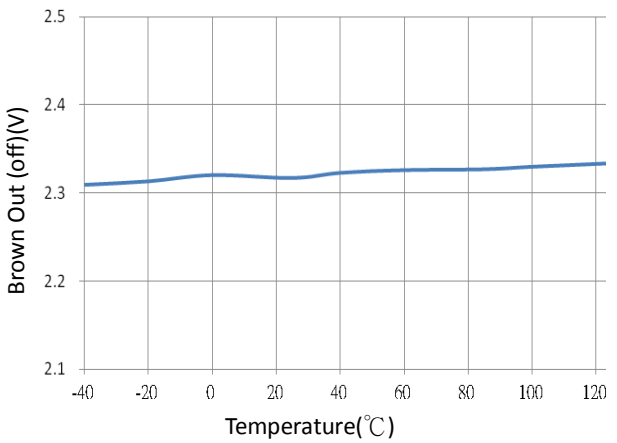


Fig12. Brown Out (off) vs. Temperature

Functional Description

UVLO

An UVLO comparator is implemented in EM8569A to monitor the VCC pin voltage. As shown in Fig. 13, a hysteresis is built in to prevent the shutdown from the voltage drop during startup. The UVLO (on) and UVLO (off) are setting at 16V and 10V, respectively.

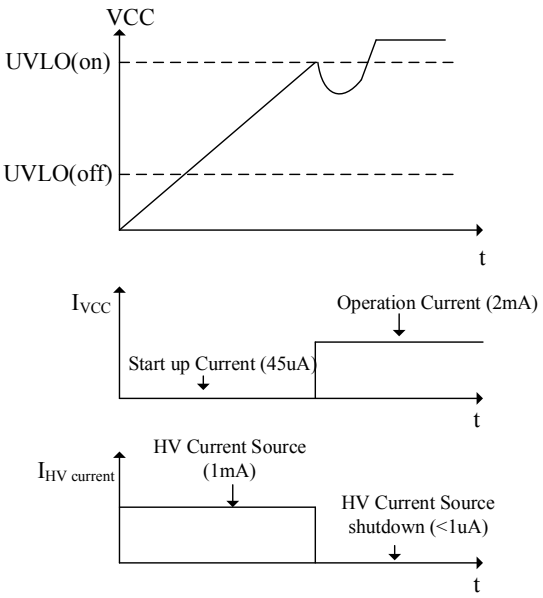


Fig. 13

Startup Operation

Fig. 14 shows a typical HV startup circuit and transformer auxiliary winding for the EM8569A application, it consumes only startup current (typical 45uA) and the startup current drawn from the HV pin to charge the VCC capacitor (C_{VCC}). When VCC reaches UVLO (on) voltage, EM8569A begins switching and the HV startup current switches off. Then, the power required is supplied from the transformer auxiliary winding. The hysteresis of UVLO (off) provides more holdup time, which allows using a small capacitor for VCC.

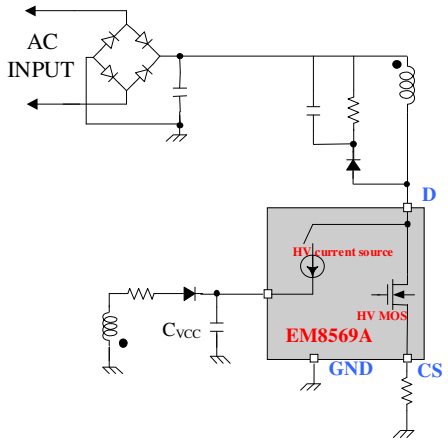


Fig. 14

Switching Frequency

To guarantee accurate frequency, EM8569A is trimmed to 10% tolerance. The internal oscillator also generates slope compensation, 75% maximum duty limit.

Leading Edge Blanking (LEB)

Fig.15 shows an each time the power MOSFET turn on, the MOSFET C_{OSS}, secondary rectifier reverse recovery current and gate driver sourcing current comprise the current spike. To avoid premature termination of the switching pulse, a leading edge blanking time is built in. During the blanking time (380nS), the PWM comparator is off and cannot switch off the gate driver.

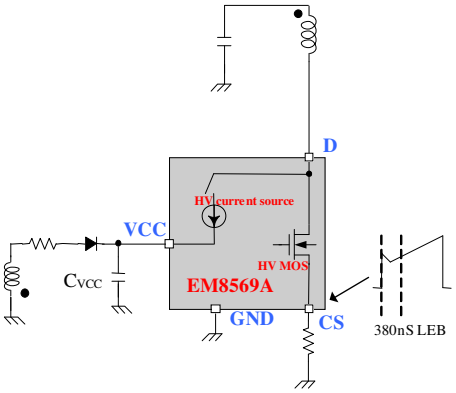


Fig. 15

Soft Start

The EM8569A has an internal soft-start circuit that increases cycle-by-cycle current limit comparator inverting input voltage slowly after it starts. The typical soft-start time is 3.5mS. The pulse width to the power MOSFET is progressively increased to establish the correct working conditions for transformers, rectifier diodes and capacitors. The voltage on the output capacitors is progressively increased with the intention of smoothly establishing the required output voltage. It also helps prevent transformer saturation and reduces the stress on the secondary diode during startup.

Slope compensation

In the conventional application, the problem of the stability is a critical issue for current mode controlling, when it operates in high than 50% of the duty cycle. The EM8569A built in saw-tooth slope compensation. So it requires no extra component.

Brown-In/Out Function

The EM8569A has a built-in internal brown-in/out protection comparator monitoring voltage of BNO pin. Fig. 16 shows a resistive divider with low-pass filtering for line-voltage detection on the BNO pin.

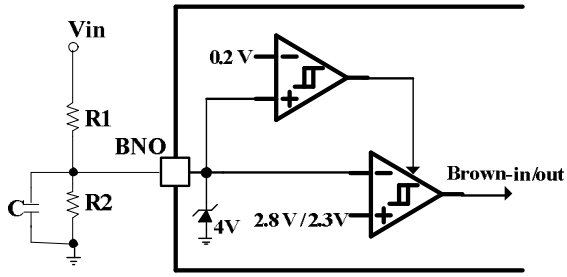


Fig. 16

If the BNO pin voltage is lower than 2.3V, the PWM gate is disabled to protect the system from over current. If the BNO pin increases above 2.8V, the EM8569A starts up.

If the BNO pin voltage is lower than 0.2V, the Brown-in/out function is disabled to allow the EM8569A to start up.

Deep Burst Mode Operation

At no load or light load condition, majority of the power dissipation in switching power supply is form switching loss on the power MOSFET, the core loss of the transformer and the loss on the snubber. The magnitude of power loss is in proportion to the number of switching events within a fixed period of time. Reducing switching events leads reduction on the power loss and conserves the energy.

The EM8569A adjusts the switching mode according to the load condition, the COMP pin voltage drops below Deep Burst mode in-threshold level (typical 1.3V). Device enters Deep Burst Mode Control. The Gate drive output remains at off state to minimize the switching loss and reduces the standby power consumption. And when the COMP pin voltage exceed the burst mode on threshold level (typical 1.4V). The Gate drive output starts active. The COMP pin voltage immediately increases if there is a high load. When the COMP pin voltage exceed the Deep Burst mode out-threshold level (typical 1.5V), the device goes to normal mode. During the Deep Burst mode, the CS level is controlled to 0.3V. Fig. 17 shows the signals of Deep Burst mode.

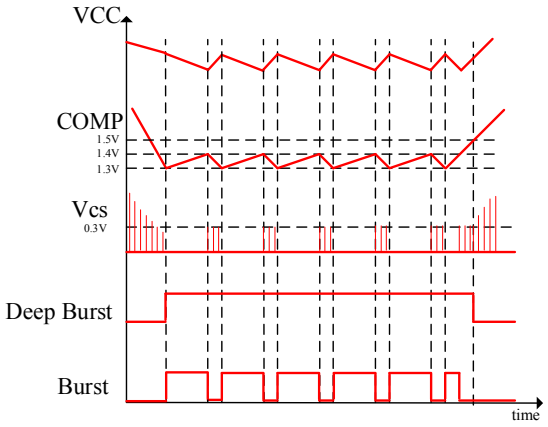


Fig. 17

Protection

The EM8569A provides many protection functions that intend to protect system from being damaged. All the protection functions are listed as below:

- **Cycle-by-cycle current limit**

  The EM8569A has over-current protection thresholds. It is for cycle-by-cycle current limit, which turns off MOSFET for the remainder of the switching cycle when the sensing voltage of MOSFET current reaches the threshold.

- **Over-load / Open-loop Protection (OLP)**

  When feedback loop is open, as shown in Fig. 18, no current flows through the opto-coupler transistor, the EM8569A pulls up the COMP pin voltage to 5.2V.

  When the COMP pin voltage is above 4.0V longer than 56mS, OLP is triggered. This protection is also triggered when the SMPS output drops below the normal value longer than 56mS due to the overload condition.

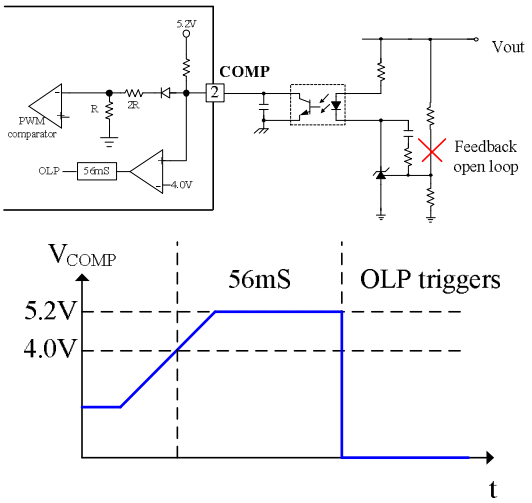


Fig. 18

- **Over Voltage Protection (OVP) on VCC**

  The EM8569A are implemented an Over-Voltage-Protection (OVP) on VCC. Whenever the VCC voltage is high than the OVP threshold voltage (29V), the output gate drive will be shutdown to stop the switching of the power MOSFET until the next UVLO (on).

  The Over-Voltage-Protection on VCC function in EM8569A is an auto-restart type protection. If the OVP condition is not released, the VCC will tripped the OVP level again and re-shutdown the gate output. The VCC is working as a hiccup mode as shown in Fig. 19. On the other hand, if the OVP condition is removed, the VCC level will go back to normal level and the output will automatically return to the normal operation.

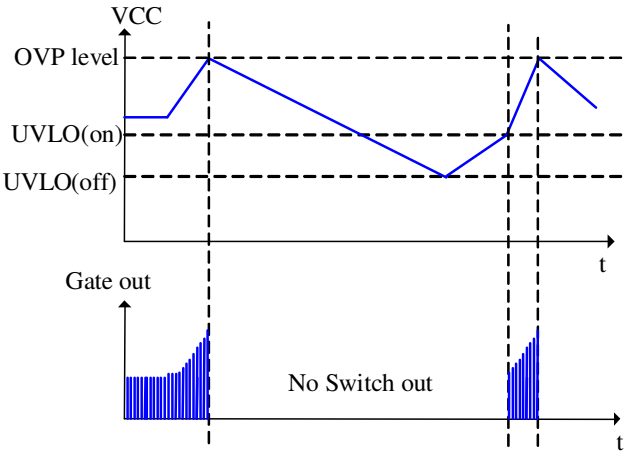


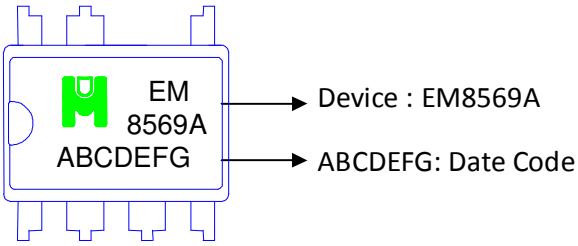
Fig. 19

- **Internal Over-Temperature Protection (OTP)**

  Internal 150℃ comparator will provide over temperature protection (OTP). OTP will not shutdown system. It stops the system from switching until the VCC is below the UVLO (off) threshold voltage, the system will hiccup.

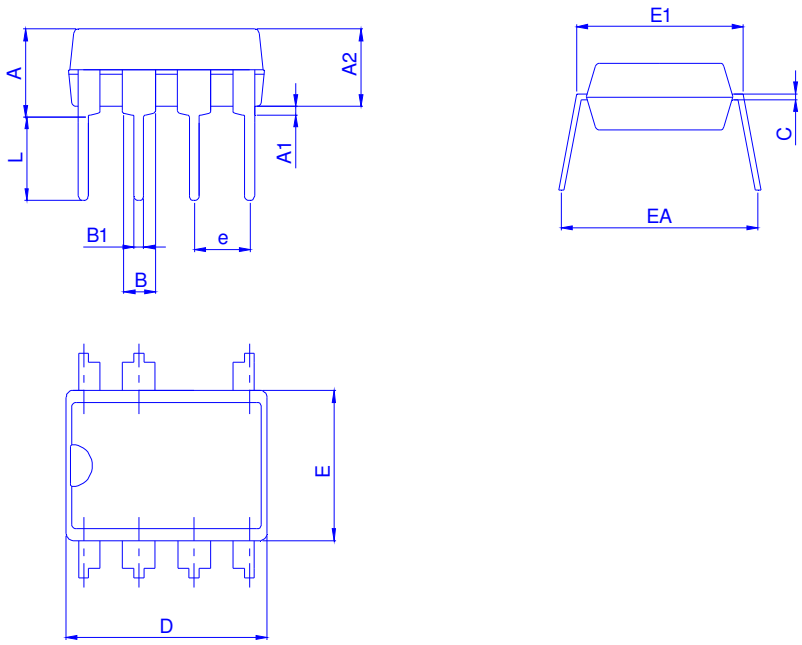
Ordering & Marking Information

Device Name: EM8569AS7 for DIP-7



Outline Drawing

DIP-7



Dimension in mm

Dimension	A	A1	A2	B	B1	C	D	E	E1	EA	e	L
Min.		0.381	3.17				9.01	6.22	7.36	8.5		2.92
Typ.				1.524	0.457	0.254					2.54	
Max.	5.334		3.429				10.16	6.53	7.87	9.53		3.81