Document Title

512K x8 bit Super Low Power and Low Voltage Full CMOS Static RAM

Revision History

Revision No.	History		Draft Date	Remark
0.0	Initial Draft		October 24,2002	Preliminary
0.1	2' nd Draft	Changed Icc, Icc1 value	November 11 , 2002	
0.2	3'rd Draft	Changed I_{SB1} test conditions, Changed VDR & IDR measurement condition	December 23 , 2002	
0.3	4' th Draft	Add Pb-free part number	February 13 , 2004	

Emerging Memory & Logic Solutions Inc.
IT Venture Tower Eastside 11F, 78, Karac-Dong, Songpa-Ku, Seoul, Rep.of Korea Zip Code : 138-160
Tel : +82-2-2142-1759~1766 Fax : +82-2-2142-1769 / Homepage : www.emlsi.com

FEATURES

- Process Technology : 0.18µm Full CMOS
- Organization : 512K x 8 bit
- Power Supply Voltage : 1.65V ~ 2.2V
- Low Data Retention Voltage : 1.0V(Min)
- Three state outputs
- Package Type : 36-FPBGA 6.0x7.0

GENERAL DESCRIPTION

The EM640FP8 families are fabricated by EMLSI's advanced full CMOS process technology. The families support industrial temperature range and Chip Scale Package for user flexibility of system design. The families also supports low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (I_{SB1}, Typ)	Operating (I_{CC1}.Max)	
EM640FP8	Industrial (-40 ~ 85°C)	1.65~2.2V	70ns [1)]	1 µA	2 mA	36 FPBGA (6.0x7.0)

1. The parameter is measured with 30pF test load.

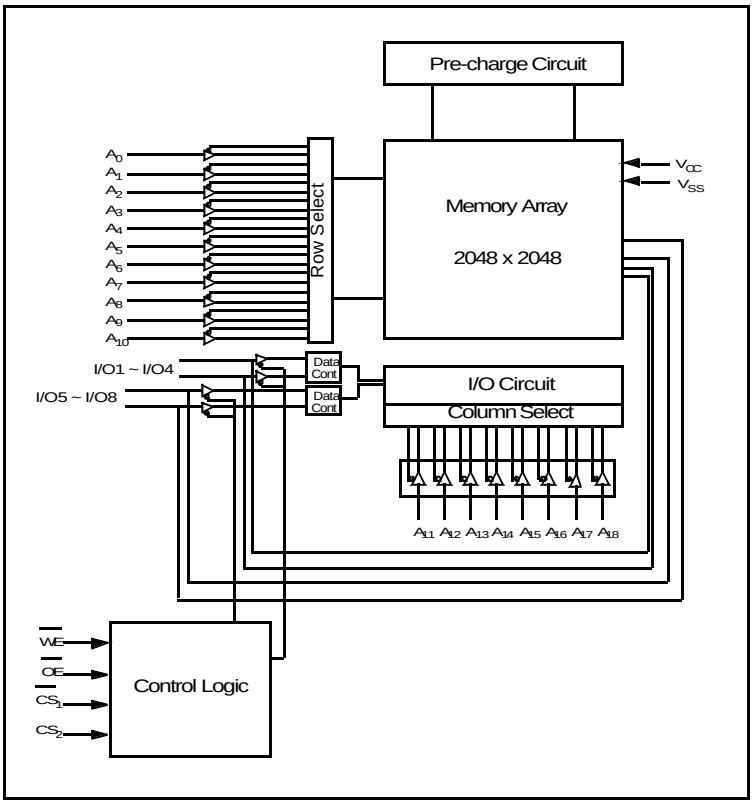
PIN DESCRIPTION

	1	2	3	4	5	6
A	A_0	A_1	CS_2	A_3	A_6	A_8
B	I/O_5	A_2	$\overline{WE}$	A_4	A_7	I/O_1
C	I/O_6		DNU	A_5		I/O_2
D	V_{SS}					V_{CC}
E	V_{CC}					V_{SS}
F	I/O_7		A_{18}	A_{17}		I/O_3
G	I/O_8	$\overline{OE}$	$\overline{CS_1}$	A_{16}	A_{15}	I/O_4
H	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}

36-FPBGA : Top view (ball down)

Name	Function	Name	Function
$\overline{CS_1}$,CS_2	Chip select inputs	$\overline{WE}$	Write Enable input
$\overline{OE}$	Output Enable input	Vcc	Power Supply
A_0~A_{18}	Address Inputs	Vss	Ground
I/O_1~I/O_8	Data Inputs/outputs	DNU	Do Not Use

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Parameter	Symbol	Ratings	Unit
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-0.5V to VCC+0.3V (Max.2.5V)	V
Voltage on Vcc supply relative to Vss	V_{CC}	-0.3V to 2.5V	V
Power Dissipation	P_D	1.0	W
Operating Temperature	T_A	-40 to 85	^oC

***** Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

FUNCTIONAL DESCRIPTION

$\overline{CS}_1$	CS_2	$\overline{OE}$	$\overline{WE}$	I/O	Mode	Power
H	X	X	X	High-Z	Deselected	Stand by
X	L	X	X	High-Z	Deselected	Stand by
L	H	H	H	High-Z	Output Disabled	Active
L	H	L	H	Data Out	Read	Active
L	H	X	L	Data In	Write	Active

Note: X means don't care. (Must be low or high state)

RECOMMENDED DC OPERATING CONDITIONS [1)]

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	1.65	1.8	2.2	V
Ground	V_{SS}	0	0	0	V
Input high voltage	V_{IH}	1.4	-	V_{CC} + 0.3[2)]	V
Input low voltage	V_{IL}	-0.3[3)]	-	0.4	V

1. TA= -40 to 85°C, otherwise specified
2. Overshoot: V_{CC} +1.0 V in case of pulse width ≤ 20ns
3. Undershoot: -1.0 V in case of pulse width ≤ 20ns
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE [1)] (f =1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	8	pF
Input/Ouput capacitance	C_{IO}	V_{IO}=0V	-	10	pF

1. Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

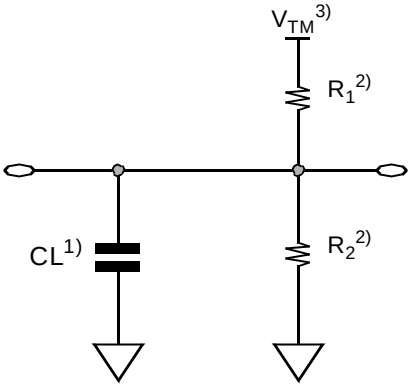
Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Input leakage current	I_{LI}	V_{IN}=V_{SS} to V_{CC}		-1	-	1	µA
Output leakage current	I_{LO}	$\overline{CS_1}$=V_{IH}, CS_2=V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{IO}=V_{SS} to V_{CC}		-1	-	1	µA
Operating power supply	I_{CC}	I_{IO}=0mA, $\overline{CS_1}$=V_{IL}, CS_2=$\overline{WE}$=V_{IH}, V_{IN}=V_{IH} or V_{IL}		-	-	2	mA
Average operating current	I_{CC1}	Cycle time=1µs, 100% duty, I_{IO}=0mA, $\overline{CS_1}$≤0.2V, CS_2≥V_{CC}-0.2V, V_{IN}≤0.2V or V_{IN}≥V_{CC}-0.2V		-	-	2	mA
	I_{CC2}	Cycle time = Min, I_{IO}=0mA, 100% duty, $\overline{CS_1}$=V_{IL}, CS_2=V_{IH}, V_{IN}=V_{IL} or V_{IH}	70ns	-	-	12	mA
Output low voltage	V_{OL}	I_{OL} = 0.1mA		-	-	0.2	V
Output high voltage	V_{OH}	I_{OH} = -0.1mA		1.4	-	-	V
Standby Current (CMOS)	I_{SB1}	$\overline{CS_1}$≥V_{CC}-0.2V, CS_2≥V_{CC}-0.2V ($\overline{CS_1}$ controlled) or 0V≤CS_2≤0.2V (CS_2 controlled), Other inputs=0 ~ V_{CC} (Typ. condition : V_{CC}=1.8V @ 25°C) (Max. condition : V_{CC}=2.2V @ 85°C)	LL LF	-	1	5	µA

AC OPERATING CONDITIONS

Test Conditions (Test Load and Test Input/Output Reference)

Input Pulse Level : 0.2V to VCC-0.2V
Input Rise and Fall Time : 5ns
Input and Output reference Voltage : 0.9V
Output Load (See right) : CL = 100pF+ 1 TTL
$CL^{1)}$ = 30pF + 1 TTL

1. Including scope and Jig capacitance
2. R_1=3070Ω, R_2=3150Ω
3. V_{TM}=1.8V



READ CYCLE (V_{cc} =1.65 to 2.2V, Gnd = 0V, T_A = -40°C to +85°C)

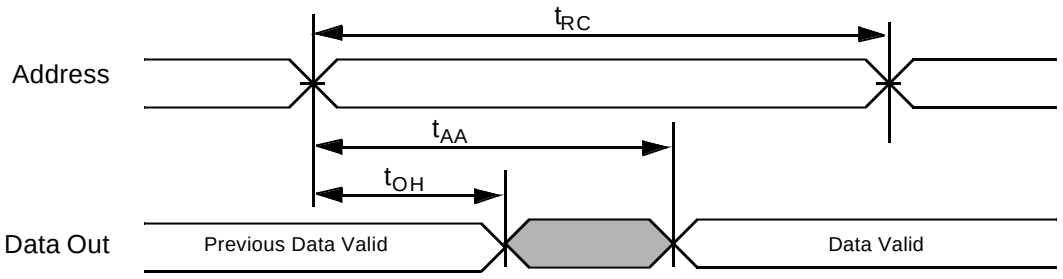
Parameter	Symbol	70ns		Unit
		Min	Max	
Read cycle time	t_{RC}	70	-	ns
Address access time	t_{AA}	-	70	ns
Chip select to output	t_{co1}, t_{co2}	-	70	ns
Output enable to valid output	t_{OE}	-	35	ns
Chip select to low-Z output	t_{LZ1}, t_{LZ2}	10	-	ns
Output enable to low-Z output	t_{OLZ}	5	-	ns
Chip disable to high-Z output	t_{HZ1}, t_{HZ2}	0	25	ns
Output disable to high-Z output	t_{OHZ}	0	25	ns
Output hold from address change	t_{OH}	10	-	ns

WRITE CYCLE (V_{cc} =1.65 to 2.2V, Gnd = 0V, T_A = -40°C to +85°C)

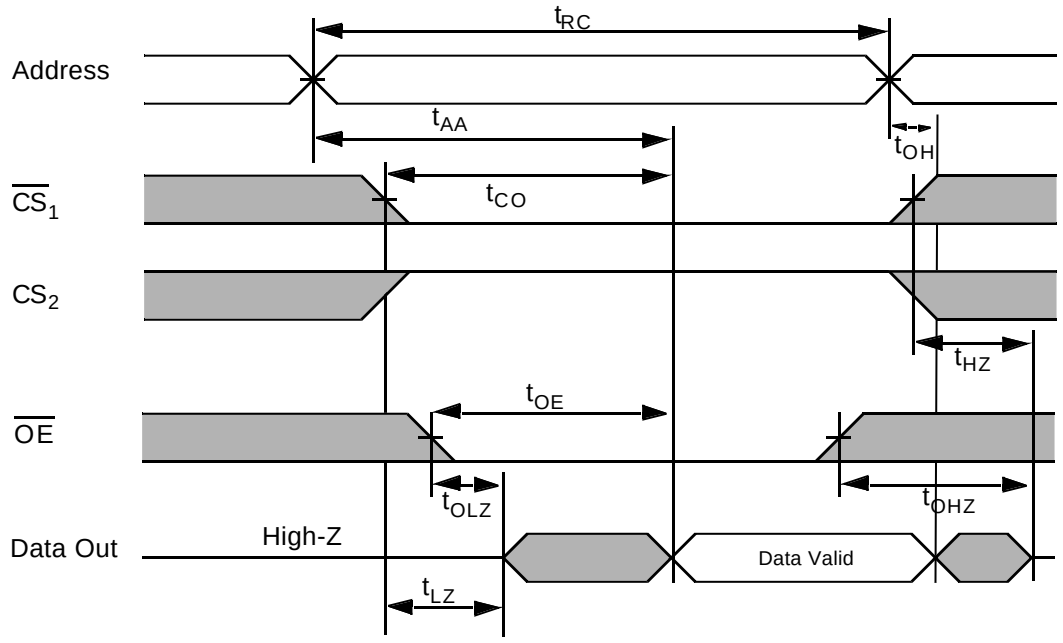
Parameter	Symbol	70ns		Unit
		Min	Max	
Write cycle time	t_{WC}	70	-	ns
Chip select to end of write	t_{CW1}, t_{CW2}	60	-	ns
Address setup time	t_{As}	0	-	ns
Address valid to end of write	t_{AW}	60	-	ns
Write pulse width	t_{WP}	55	-	ns
Write recovery time	t_{WR}	0	-	ns
Write to ouput high-Z	t_{WHZ}	0	25	ns
Data to write time overlap	t_{DW}	30		ns
Data hold from write time	t_{DH}	0	-	ns
End write to output low-Z	t_{OW}	5	-	ns

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1). (Address Controlled, $\overline{CS_1}$=$\overline{OE}$=V_{IL}, CS_2=$\overline{WE}$=V_{IH})



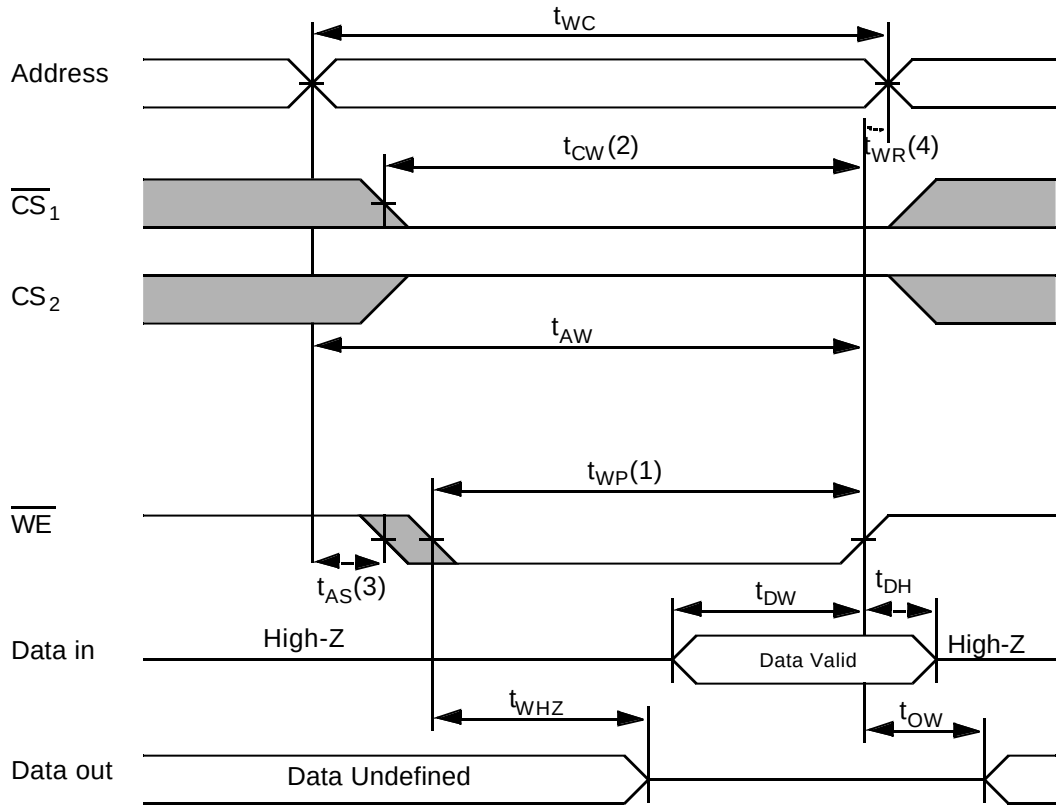
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$ = V_{IH})



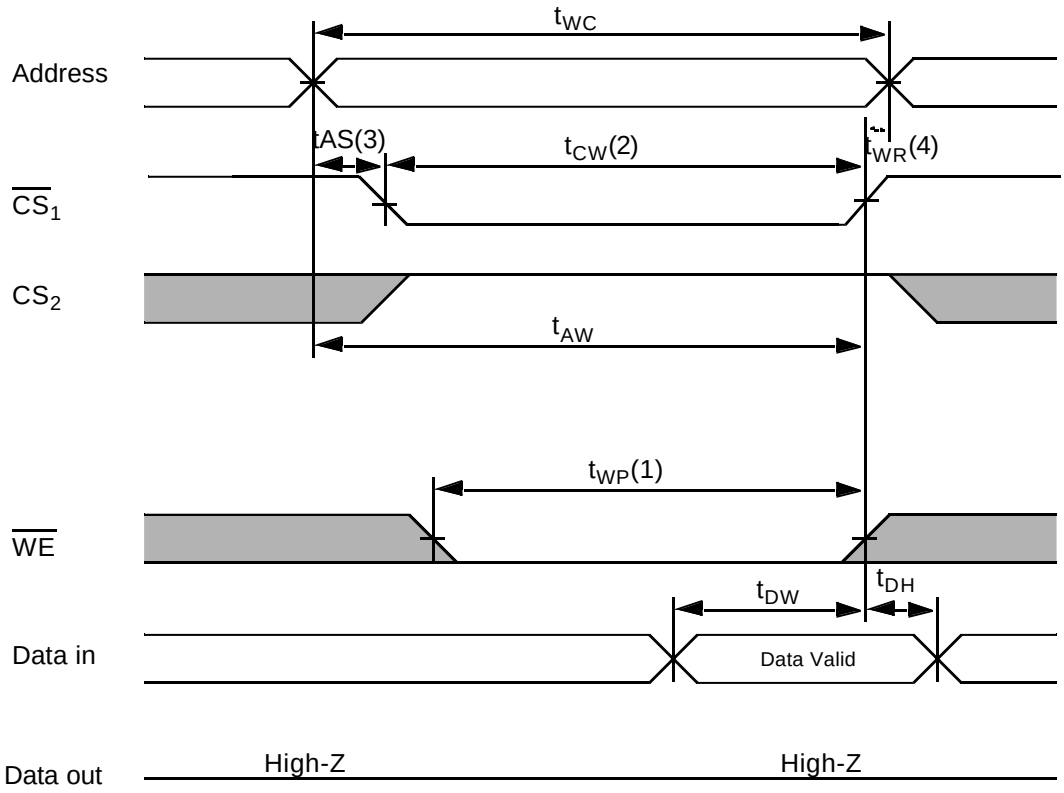
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the outputs achieve the open circuit conditions and are not referanced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device interconnection.

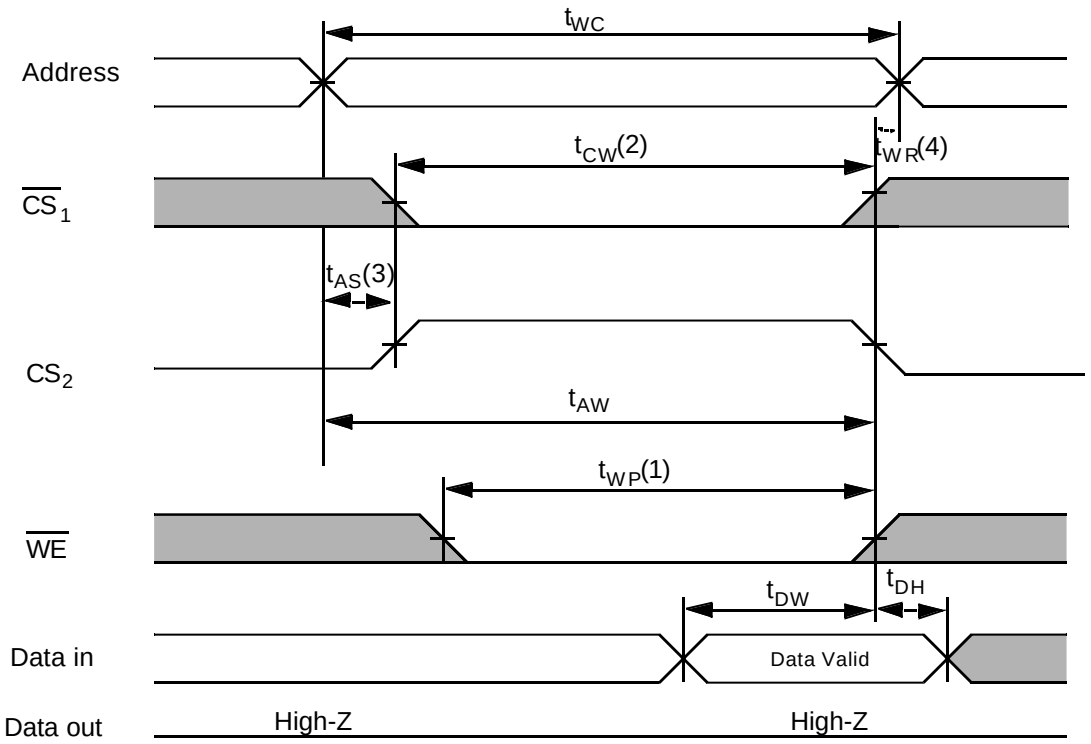
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{WE}$ CONTROLLED)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS_1}$ CONTROLLED)



TIMING WAVEFORM OF WRITE CYCLE(3) (CS_2 CONTROLLED)



NOTES (WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of low $\overline{CS_1}$, a high CS_2 and low $\overline{WE}$. A write begins at the latest transition among $\overline{CS_1}$ goes low, CS_2 goes high and $\overline{WE}$ goes low. A write ends at the earliest transition when $\overline{CS_1}$ goes high, CS_2 goes hagh and $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS_1}$ going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end or write to the address change. t_{WR} applied in case a write ends as $\overline{CS_1}$ or $\overline{WE}$ going high.

DATA RETENTION CHARACTERISTICS

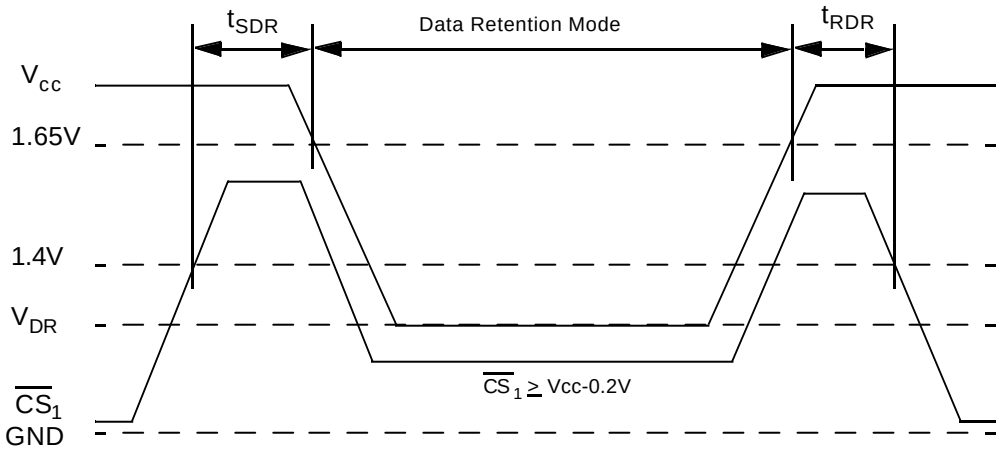
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{CC} for Data Retention	V_{DR}	I_{SB1} Test Condition (Chip Disabled) 1)	1.0	-	2.2	V
Data Retention Current	I_{DR}	V_{CC}=1.2V, I_{SB1} Test Condition (Chip Disabled) 1)	-	0.5	2	µA
Chip Deselect to Data Retention Time	t_{SDR}	See data retention wave form	0	-	-	ns
Operation Recovery Time	t_{RDR}		t_{RC}	-	-	

NOTES

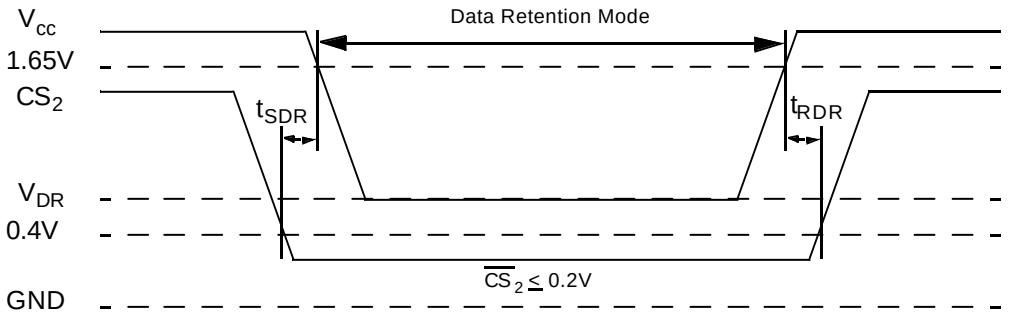
1. See the I_{SB1} measurement condition of datasheet page 4.

DATA RETENTION WAVE FORM

$\overline{CS_1}$ Controlled



CS_2 Controlled

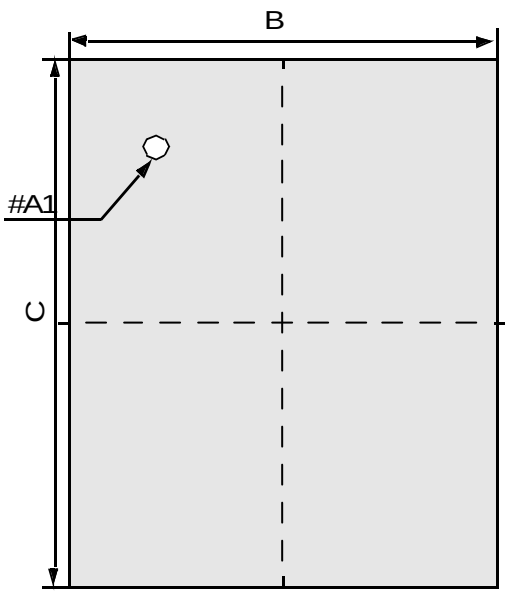


Unit: millimeters

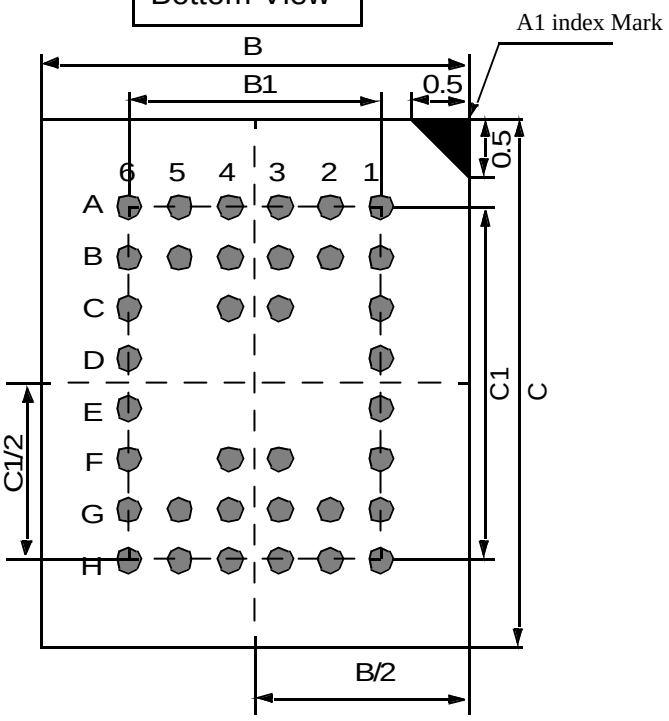
PACKAGE DIMENSION

36 Ball Fine Pitch BGA (0.75mm ball pitch)

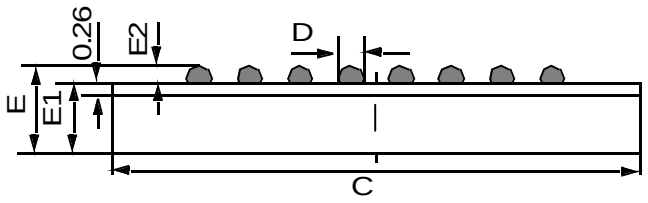
Top View



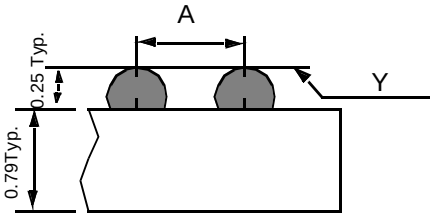
Bottom View



Side View



Detail A

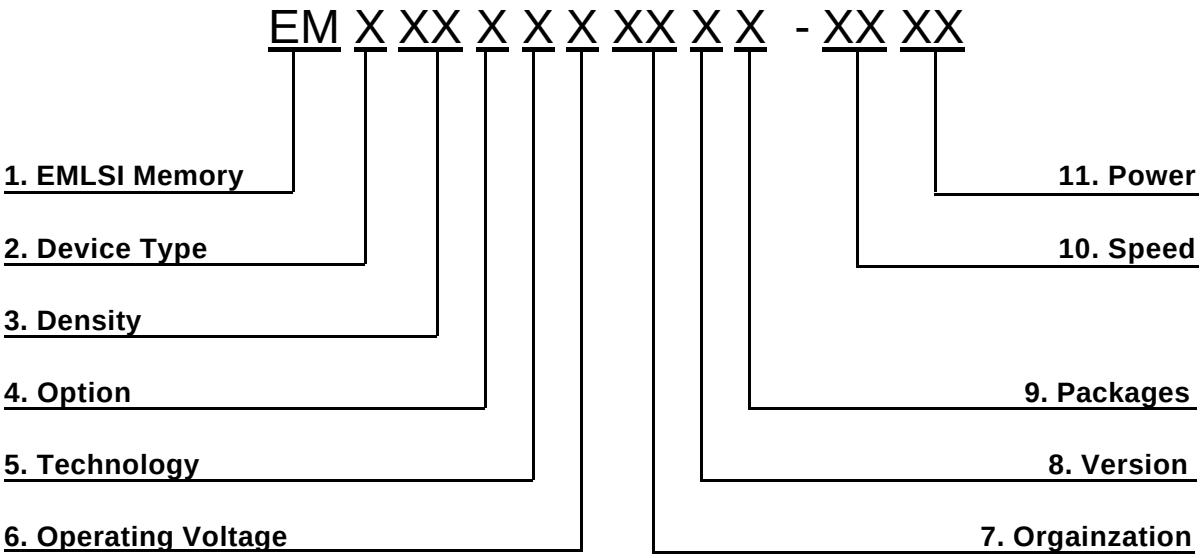


	Min	Typ	Max
A	-	0.75	-
B	5.95	6.00	6.05
B1	-	3.75	-
C	6.95	7.00	7.05
C1	-	5.25	-
D	0.30	0.35	0.40
E	1.00	1.04	1.10
E1	-	0.79	-
E2	-	0.25	-
Y	-	-	0.08

NOTES.

1. Bump counts : 36(8row x 6column)
2. Bump pitch : (x,y)=(0.75x0.75) (typ.)
3. All tolerence are +/-0.050 unless otherwise specified.
4. Typ : Typical
5. Y is coplanarity : 0.08(Max)

MEMORY FUNCTION GUIDE



1. Memory Component

2. Device Type
- 6 ---------- Low Power SRAM
- 7 ---------- STRAM

3. Density
- 1 ---------- 1M
- 2 ---------- 2M
- 4 ---------- 4M
- 8 ---------- 8M
- 16 ---------- 16M
- 32 ---------- 32M
- 64 ---------- 64M

4. Option
- 0 ---------- Dual CS
- 1 ---------- Single CS

5. Technology
- Blank ---------- CMOS
- F ---------- Full CMOS

6. Operating Voltage
- Blank ---------- 5V
- V ---------- 3.3V
- U ---------- 3.0V
- S ---------- 2.5V
- R ---------- 2.0V
- P ---------- 1.8V

7. Orginzation
- 8 ---------- x8 bit
- 16 ---------- x16 bit
- 32 ---------- x32 bit

8. Version
- Blank ---------- Mother Die
- A ---------- First revision
- B ---------- Second revision
- C ---------- Third revision
- D ---------- Fourth revision

9. Package
- Blank ---------- Package
- W ---------- Wafer

10. Speed
- 45 ---------- 45ns
- 55 ---------- 55ns
- 70 ---------- 70ns
- 85 ---------- 85ns
- 10 ---------- 100ns
- 12 ---------- 120ns

11. Power
- LL ---------- Low Low Power
- LF ---------- Low Low Power(Pb-Free)
- L ---------- Low Power
- S ---------- Standard Power