

ELM77xxxxxC CMOS Dual voltage detector

■General description

ELM77xxxxxC is CMOS dual voltage detector which consists of two comparator circuits watching Vdetn2 (Vdd level) and Vdetn1(Vdet input level) simultaneously and independently. This configuration enables output to maintain the state of detection even when voltage of the Vdet input level drops to 0V.

■Features

- Detection voltage range : Vdetn1 (Vdet) 0.8V to 5.0V (by0.1V)
Vdetn2 (Vdd) 1.1V to 5.0V (by0.1V)
- Low current consumption : Typ.0.6μA(Vdd=3.0V)
- High accuracy of detection voltage : ±2.0%(Vdetn1,2>1.5V)
±30mV(Vdetn1,2≤1.5V)
- High input resistance : Typ.10MΩ
- Low temperature coefficient : Typ.±100ppm/°C
- Output configuration : N-ch open-drain
- Small package : SOT-25

■Application

- Reset for microcomputers
- Power voltage shortage detectors
- Switch of backup power source
- Battery checkers

■Maximum absolute ratings

Parameter	Symbol	Limit	Unit
Power supply voltage	Vdd	Vss-0.3 to 10.0	V
Input voltage(for detection voltage)	Vdet	Vss-0.3 to 10.0	V
Output voltage	Vout1	Vss-0.3 to 10.0	V
	Vout2		
Output current	Iout1	25	mA
	Iout2		
Power dissipation	Pd	250	mW
Operating temperature	Top	-40 to +85	°C
Storage temperature	Tstg	-55 to +125	°C

■Selection guide

ELM77xxxxxC-x

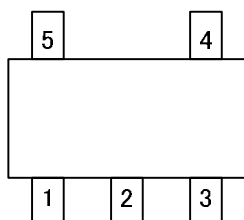
Symbol		
a, b	Detection voltage2	e.g.) 22: Vdetn2=2.2V, 24: Vdetn2=2.4V 27: Vdetn2=2.7V
c, d	Detection voltage1	e.g.) 09: Vdetn1=0.9V, 11: Vdetn1=1.1V
e	Package	B: SOT-25
f	Product version	C
g	Taping direction	S: Refer to PKG file N: Refer to PKG file

ELM77 x x x x x C - x
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 a b c d e f g

ELM77xxxxxC CMOS Dual voltage detector

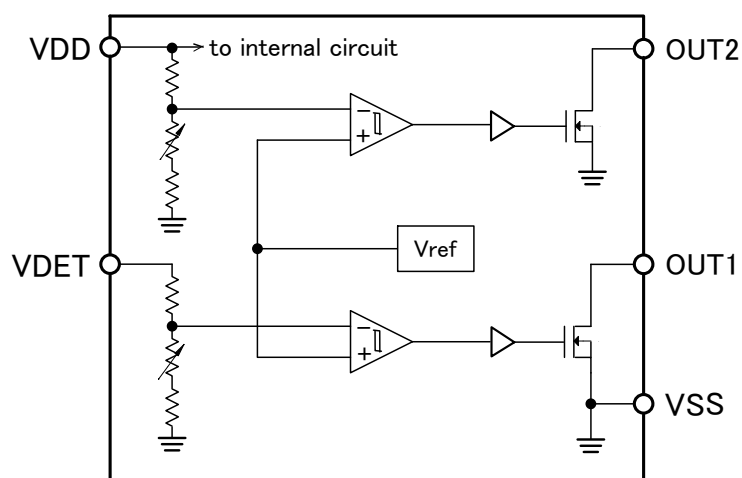
■Pin configuration

SOT-25(TOP VIEW)

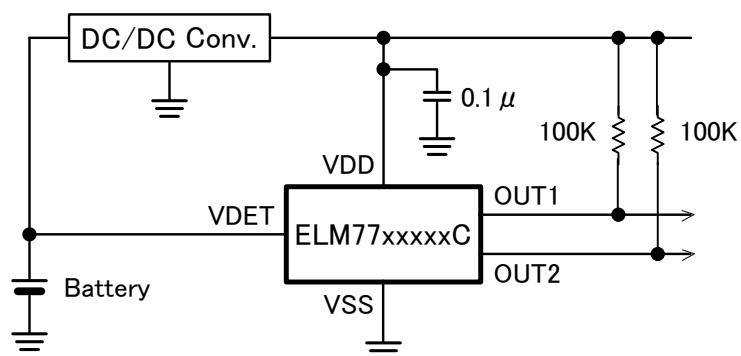


Pin No.	Pin name
1	OUT1
2	VDD
3	VSS
4	VDET
5	OUT2

■Block diagram

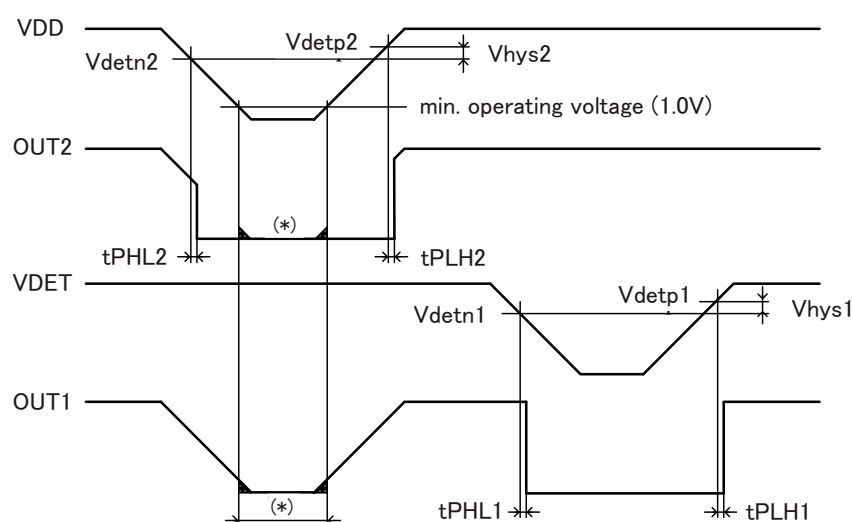


■Typical application



ELM77xxxxxC CMOS Dual voltage detector

■Operating timing chart



* Output status is undefined when Vdd is lower than min. operating voltage.

■Electrical characteristics

ELM772211BC(Vdetn1=1.1V, Vdetn2=2.2V) Rpullup=100K, Vpullup=3V unless otherwise specified. Top=25°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Operating voltage	Vdd		1.0		6.0	V	-
Detection voltage1	Vdetn1	Vdd=1.5V, Vdet=Voltage detected	1.070	1.100	1.130	V	1
Detection voltage2	Vdetn2	Vdd=Voltage detected	2.156	2.200	2.244	V	1
Hysteresis width1	Vhys1		Vdetn1 ×0.04	Vdetn1 ×0.08	Vdetn1 ×0.12	V	1
Hysteresis width2	Vhys2		Vdetn2 ×0.02	Vdetn2 ×0.04	Vdetn2 ×0.06	V	1
Current consumption	Idd	Vdd=3.0V, Vdet=0V, OUT1,2:Open		0.6	2.0	μA	2
Output current1	Ioutn1	Vdd=1.0V, Vdet=0V, Vout1=0V	1	3		mA	3
Output current2	Ioutn2	Vdd=1.0V, Vout2=0.5V	1	3		mA	3
Open drain leakage current1	Ileak1	Vdd=6.0V, Vdet=6.0V, Vout1=6.0V		0.001	0.400	μA	3
Open drain leakage current2	Ileak2	Vdd=6.0V, Vdet=6.0V, Vout2=6.0V		0.001	0.400	μA	3
Input resistance	Rdet	Vdet=5.0V, Vdd=0V		10		MΩ	4
Detect delay 1	tPHL1	Vdd=6.0V, Vdet=6.0V→0V		160		μs	5
Detect delay 2	tPHL2	Vdd=6.0V→1.0V		70		μs	6
Release delay 1	tPLH1	Vdd=6.0V, Vdet=0V→6.0V		120		μs	5
Release delay 2	tPLH2	Vdd=1.0V→6.0V		60		μs	6
Temperature coefficient of Vdetn	$\frac{\Delta V_{detn}}{\Delta T_{op}}$	Top=-40°C to +85°C		±100		ppm/°C	-

Note : test circuit No.

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ELM772409BC(Vdetn1=0.9V, Vdetn2=2.4V) Rpullup=100K, Vpullup=3V unless otherwise specified. Top=25°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Operating voltage	Vdd		1.0		6.0	V	-
Detection voltage1	Vdetn1	Vdd=1.5V, Vdet=Voltage detected	0.870	0.900	0.930	V	1
Detection voltage2	Vdetn2	Vdd=Voltage detected	2.352	2.400	2.448	V	1
Hysteresis width1	Vhys1		Vdetn1 ×0.04	Vdetn1 ×0.08	Vdetn1 ×0.12	V	1
Hysteresis width2	Vhys2		Vdetn2 ×0.02	Vdetn2 ×0.04	Vdetn2 ×0.06	V	1
Current consumption	Idd	Vdd=3.0V, Vdet=0V, OUT1,2:Open		0.6	2.0	μA	2
Output current1	Ioutn1	Vdd=1.0V, Vdet=0V, Vout1=0V	1	3		mA	3
Output current2	Ioutn2	Vdd=1.0V, Vout2=0.5V	1	3		mA	3
Open drain leakage current1	Ileak1	Vdd=6.0V, Vdet=6.0V, Vout1=6.0V		0.001	0.400	μA	3
Open drain leakage current2	Ileak2	Vdd=6.0V, Vdet=6.0V, Vout2=6.0V		0.001	0.400	μA	3
Input resistance	Rdet	Vdet=5.0V, Vdd=0V		10		MΩ	4
Detect delay 1	tPHL1	Vdd=6.0V, Vdet=6.0V→0V		160		μs	5
Detect delay 2	tPHL2	Vdd=6.0V→1.0V		70		μs	6
Release delay 1	tPLH1	Vdd=6.0V, Vdet=0V→6.0V		120		μs	5
Release delay 2	tPLH2	Vdd=1.0V→6.0V		60		μs	6
Temperature coefficient of Vdetn	$\frac{\Delta V_{detn}}{\Delta Top}$	Top=-40°C to +85°C		±100		ppm/°C	-

Note : test circuit No.

ELM772709BC(Vdetn1=0.9V, Vdetn2=2.7V) Rpullup=100K, Vpullup=3V unless otherwise specified. Top=25°C

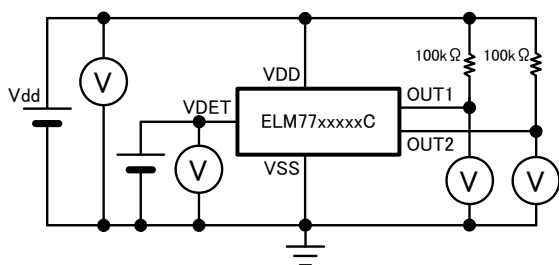
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Operating voltage	Vdd		1.0		6.0	V	-
Detection voltage1	Vdetn1	Vdd=1.5V, Vdet=Voltage detected	0.870	0.900	0.930	V	1
Detection voltage2	Vdetn2	Vdd=Voltage detected	2.645	2.700	2.754	V	1
Hysteresis width1	Vhys1		Vdetn1 ×0.04	Vdetn1 ×0.08	Vdetn1 ×0.12	V	1
Hysteresis width2	Vhys2		Vdetn2 ×0.02	Vdetn2 ×0.04	Vdetn2 ×0.06	V	1
Current consumption	Idd	Vdd=3.0V, Vdet=0V, OUT1,2:Open		0.6	2.0	μA	2
Output current1	Ioutn1	Vdd=1.0V, Vdet=0V, Vout1=0V	1	3		mA	3
Output current2	Ioutn2	Vdd=1.0V, Vout2=0.5V	1	3		mA	3
Open drain leakage current1	Ileak1	Vdd=6.0V, Vdet=6.0V, Vout1=6.0V		0.001	0.400	μA	3
Open drain leakage current2	Ileak2	Vdd=6.0V, Vdet=6.0V, Vout2=6.0V		0.001	0.400	μA	3
Input resistance	Rdet	Vdet=5.0V, Vdd=0V		10		MΩ	4
Detect delay 1	tPHL1	Vdd=6.0V, Vdet=6.0V→0V		160		μs	5
Detect delay 2	tPHL2	Vdd=6.0V→1.0V		70		μs	6
Release delay 1	tPLH1	Vdd=6.0V, Vdet=0V→6.0V		120		μs	5
Release delay 2	tPLH2	Vdd=1.0V→6.0V		60		μs	6
Temperature coefficient of Vdetn	$\frac{\Delta V_{detn}}{\Delta Top}$	Top=-40°C to +85°C		±100		ppm/°C	-

Note : test circuit No.

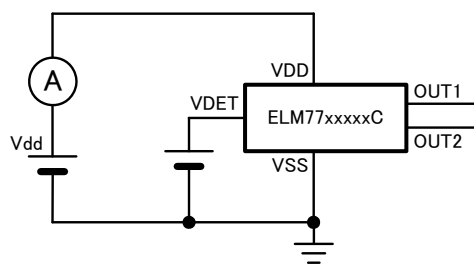
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■ Test circuits

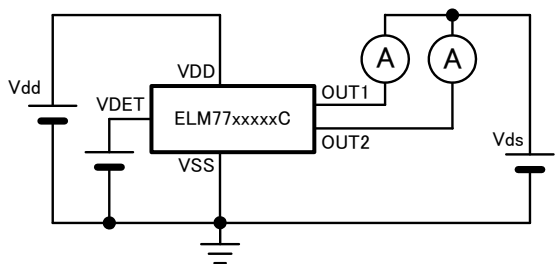
1) Detection voltage & hysteresis width



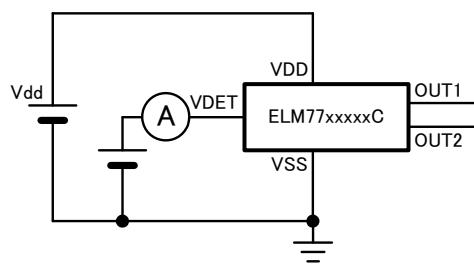
2) Current consumption



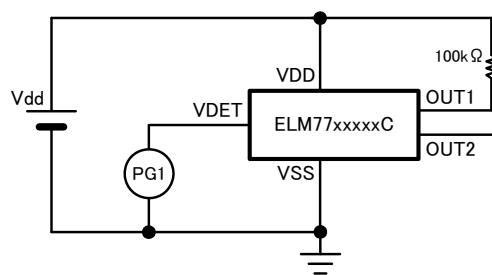
3) Output current & leakage current



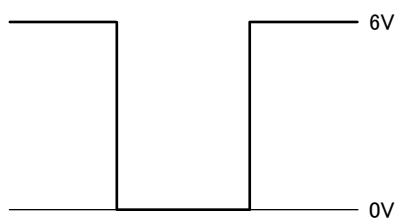
4) Input resistance



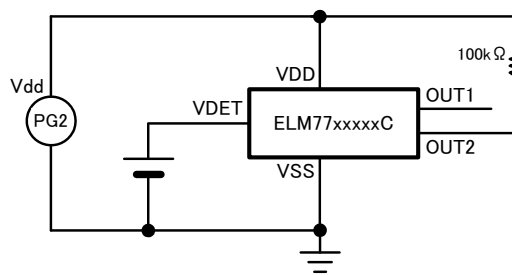
5) Delay time 1 & release time 1



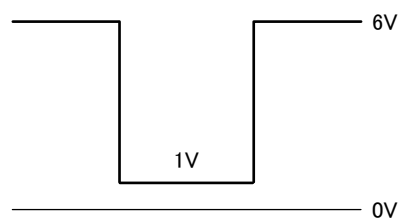
PG1 wave form



6) Delay time 2 & release time 2



PG2 wave form



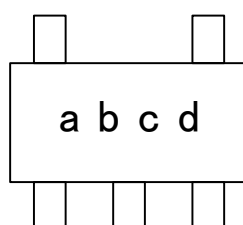
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■Detection voltage accuracy reference

Target (V)		Accuracy (mV, %)	Detection Voltage (V)		Target (V)		Accuracy (mV, %)	Detection Voltage (V)	
Vdetn1	Vdetn2		Min.	Max.	Vdetn1	Vdetn2		Min.	Max.
0.8	-	±30mV	0.770	0.830	3.0	3.0	±2%	2.940	3.060
0.9	-		0.870	0.930	3.1	3.1		3.038	3.162
1.0	-		0.970	1.030	3.2	3.2		3.136	3.264
1.1	1.1		1.070	1.130	3.3	3.3		3.234	3.366
1.2	1.2		1.170	1.230	3.4	3.4		3.332	3.468
1.3	1.3		1.270	1.330	3.5	3.5		3.430	3.570
1.4	1.4		1.370	1.430	3.6	3.6		3.528	3.672
1.5	1.5	±2%	1.470	1.530	3.7	3.7		3.626	3.774
1.6	1.6		1.568	1.632	3.8	3.8		3.724	3.876
1.7	1.7		1.666	1.734	3.9	3.9		3.822	3.978
1.8	1.8		1.764	1.836	4.0	4.0		3.920	4.080
1.9	1.9		1.862	1.938	4.1	4.1		4.018	4.182
2.0	2.0		1.960	2.040	4.2	4.2		4.116	4.284
2.1	2.1		2.058	2.142	4.3	4.3		4.214	4.386
2.2	2.2		2.156	2.244	4.4	4.4		4.312	4.488
2.3	2.3		2.254	2.346	4.5	4.5		4.410	4.590
2.4	2.4		2.352	2.448	4.6	4.6		4.508	4.692
2.5	2.5		2.450	2.550	4.7	4.7		4.606	4.794
2.6	2.6		2.548	2.652	4.8	4.8		4.704	4.896
2.7	2.7		2.646	2.754	4.9	4.9		4.802	4.998
2.8	2.8		2.744	2.856	5.0	5.0		4.900	5.100
2.9	2.9		2.842	2.958					

■Marking

SOT-25



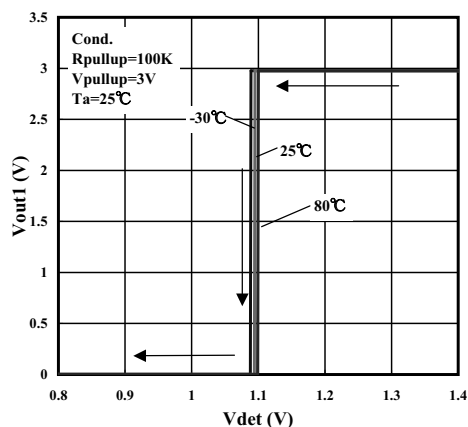
a to d : Assembly lot No. ———
A to Z (I, O, X excepted) and 0 to 9

ELM77xxxxxC CMOS Dual voltage detector

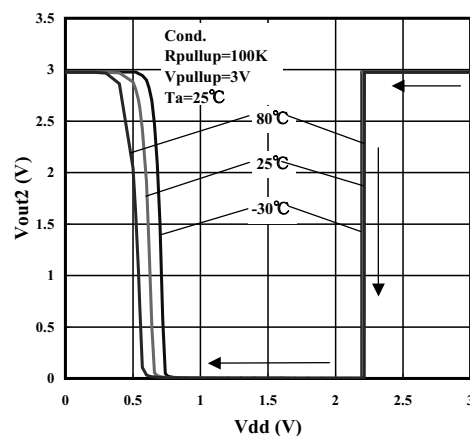
■ Typical performance characteristics

- ELM772211BC

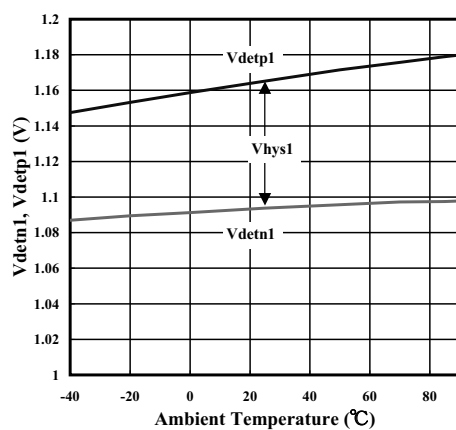
Vout1 vs Vdet



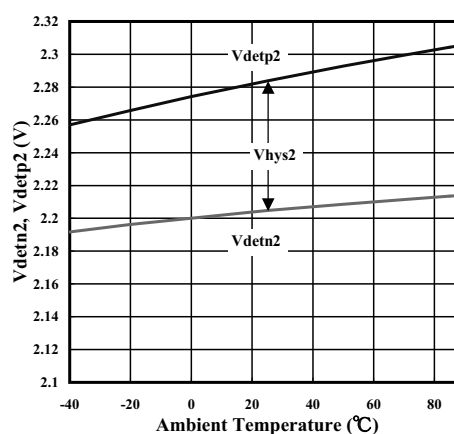
Vout2 vs Vdd



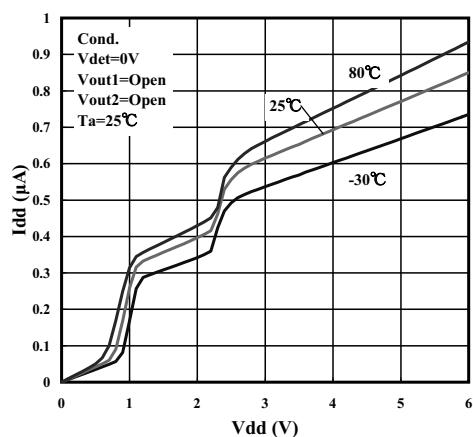
Vdetn1, Vdetp1 vs Ta



Vdetn2, Vdetp2 vs Ta



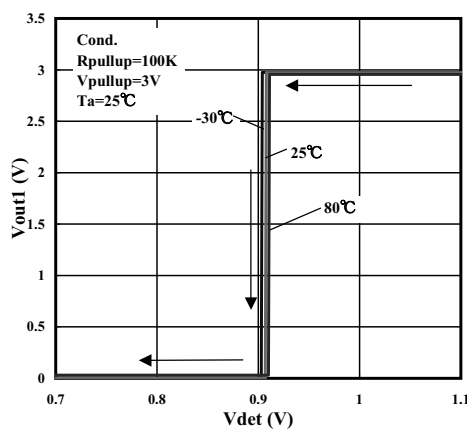
Idd vs Vdd



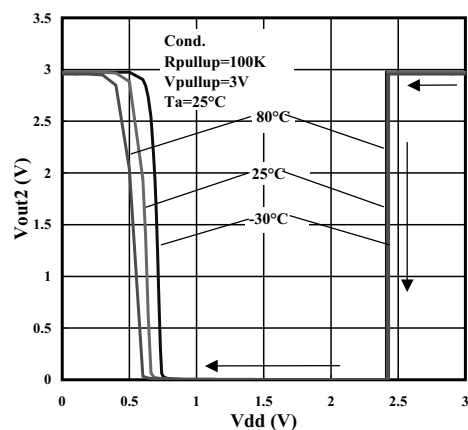
ELM77xxxxxC CMOS Dual voltage detector

- ELM772409BC

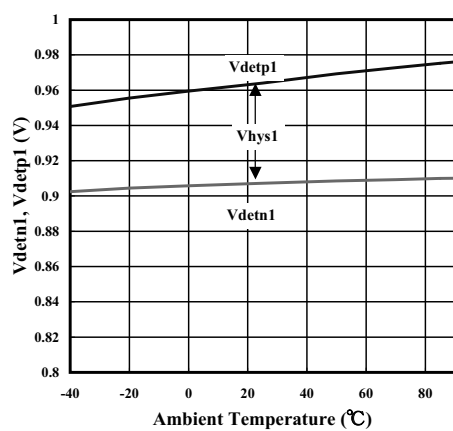
Vout1 vs Vdet



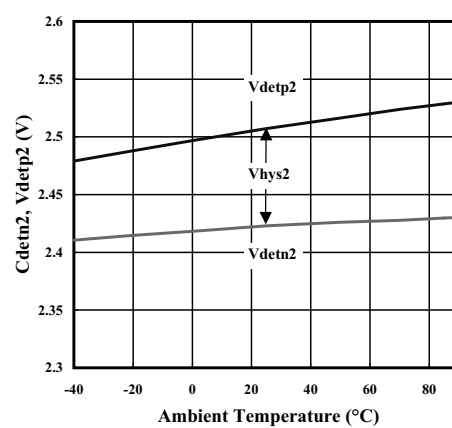
Vout2 vs Vdd



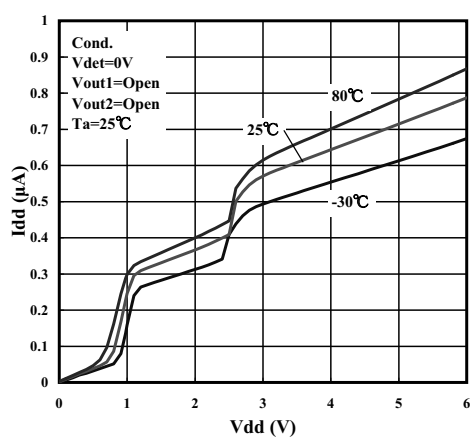
Vdetn1, Vdetp1 vs Ta



Vdetn2, Vdetp2 vs Ta



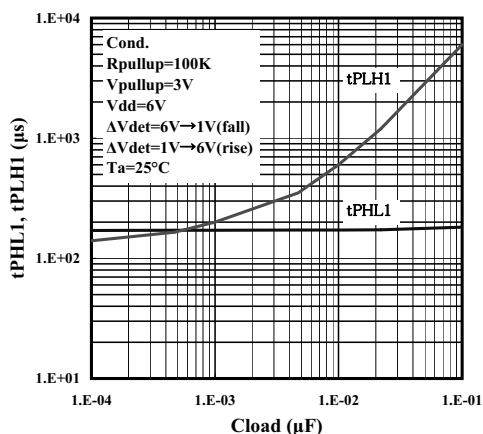
Idd vs Vdd



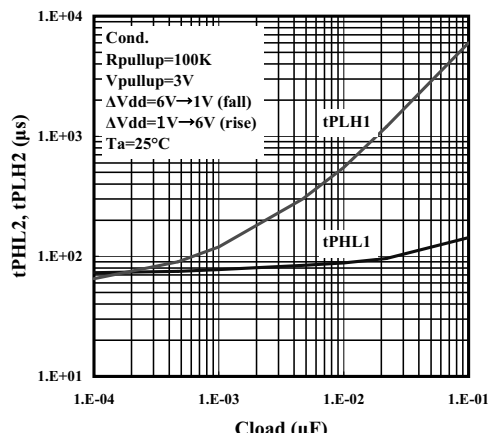
ELM77xxxxxC CMOS Dual voltage detector

- ELM77xxxxBC

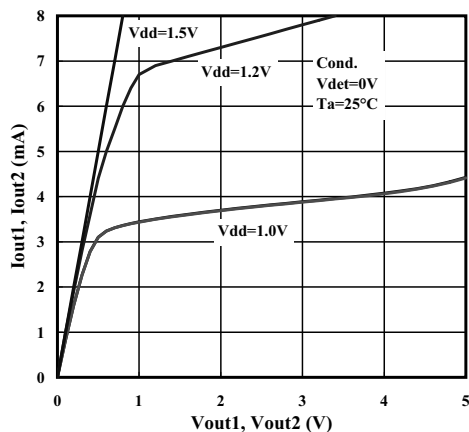
tPHL1, tPLH1 vs Cload



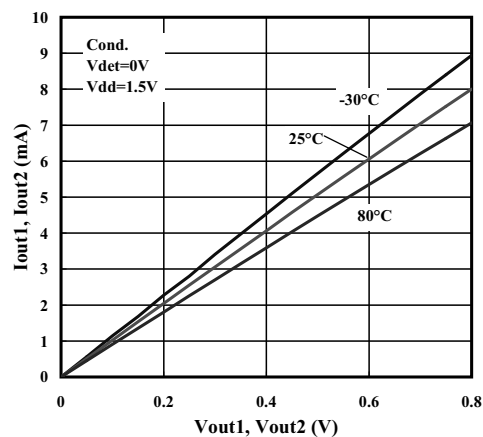
tPHL2, tPLH2 vs Cload



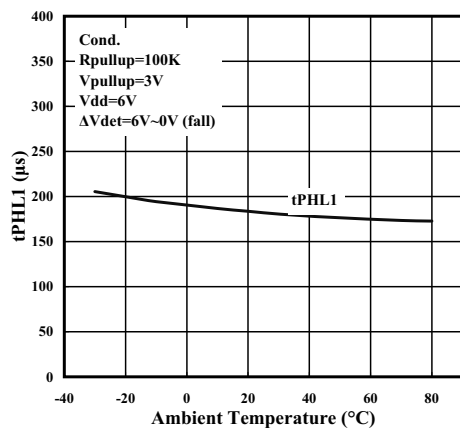
Iout-Vout



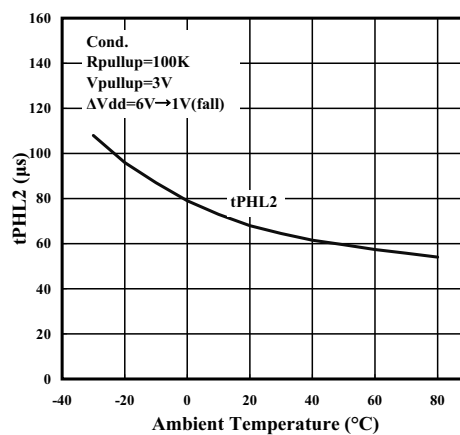
Iout vs Vout



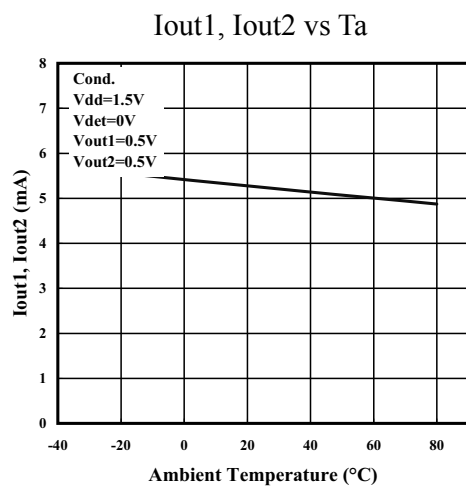
tPHL1 vs Ta



tPHL2 vs Ta



ELM77xxxxxC CMOS Dual voltage detector



- ELM77xx11BC

