

30MHz Rail-to-Rail Input-Output Op Amps

The EL5210 and EL5410 are low power, high voltage rail-to-rail input-output amplifiers. The EL5210 contains two amplifiers in one package and the EL5410 contains four amplifiers. Operating on supplies ranging from 5V to 15V, while consuming only 2.5mA per amplifier, the EL5410 and EL5210 have a bandwidth of 30MHz (-3dB). They also provide common mode input ability beyond the supply rails, as well as rail-to-rail output capability. This enables these amplifiers to offer maximum dynamic range at any supply voltage.

The EL5410 and EL5210 also feature fast slewing and settling times, as well as a high output drive capability of 30mA (sink and source). These features make these amplifiers ideal for high speed filtering and signal conditioning application. Other applications include battery power, portable devices, and anywhere low power consumption is important.

The EL5410 is available in a space-saving 14-Pin TSSOP package, as well as the industry-standard 14-Pin SOIC. The EL5210 is available in the 8-Pin MSOP and 8-Pin SOIC packages. Both feature a standard operational amplifier pin out. These amplifiers operate over a temperature range of -40°C to +85°C.

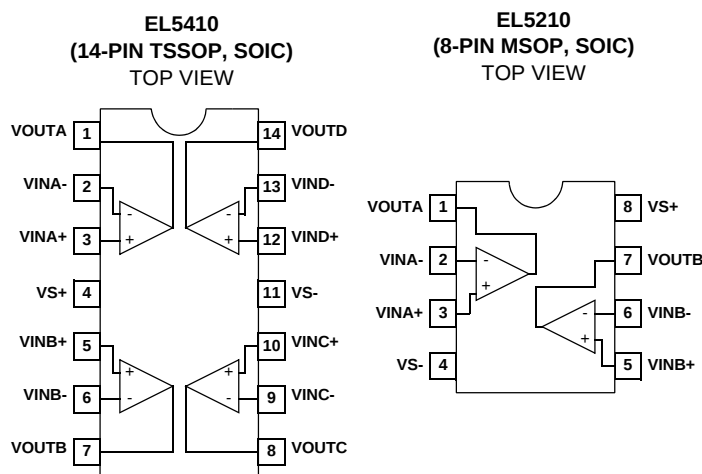
Features

- 30MHz -3dB bandwidth
- Supply voltage = 4.5V to 16.5V
- Low supply current (per amplifier) = 2.5mA
- High slew rate = 33V/μs
- Unity-gain stable
- Beyond the rails input capability
- Rail-to-rail output swing
- Available in both standard and space-saving fine pitch packages
- Pb-Free available (RoHS compliant)

Applications

- Driver for A-to-D Converters
- Data Acquisition
- Video Processing
- Audio Processing
- Active Filters
- Test Equipment
- Battery Powered Applications
- Portable Equipment

Pinouts



Ordering Information

PART NUMBER	PACKAGE	TAPE & REEL	PKG. DWG. #
EL5210CS	8-Pin SOIC	-	MDP0027
EL5210CS-T7	8-Pin SOIC	7"	MDP0027
EL5210CS-T13	8-Pin SOIC	13"	MDP0027
EL5210CSZ (See Note)	8-Pin SOIC (Pb-free)	-	MDP0027
EL5210CSZ-T7 (See Note)	8-Pin SOIC (Pb-free)	7"	MDP0027
EL5210CSZ-T13 (See Note)	8-Pin SOIC (Pb-free)	13"	MDP0027
EL5210CY	8-Pin MSOP	-	MDP0043
EL5210CY-T7	8-Pin MSOP	7"	MDP0043
EL5210CY-T13	8-Pin MSOP	13"	MDP0043
EL5210CYZ (See Note)	8-Pin MSOP (Pb-free)	-	MDP0043
EL5210CYZ-T7 (See Note)	8-Pin MSOP (Pb-free)	7"	MDP0043
EL5210CYZ-T13 (See Note)	8-Pin MSOP (Pb-free)	13"	MDP0043
EL5410CS	14-Pin SOIC	-	MDP0027
EL5410CS-T7	14-Pin SOIC	7"	MDP0027
EL5410CS-T13	14-Pin SOIC	13"	MDP0027
EL5410CSZ (See Note)	14-Pin SOIC (Pb-free)	-	MDP0027
EL5410CSZ-T7 (See Note)	14-Pin SOIC (Pb-free)	7"	MDP0027
EL5410CSZ-T13 (See Note)	14-Pin SOIC (Pb-free)	13"	MDP0027
EL5410CR	14-Pin TSSOP	-	MDP0044
EL5410CR-T7	14-Pin TSSOP	7"	MDP0044
EL5410CR-T13	14-Pin TSSOP	13"	MDP0044
EL5410CRZ (See Note)	14-Pin TSSOP (Pb-free)	-	MDP0044
EL5410CRZ-T7 (See Note)	14-Pin TSSOP (Pb-free)	7"	MDP0044
EL5410CRZ-T13 (See Note)	14-Pin TSSOP (Pb-free)	13"	MDP0044

Add "-T" suffix for tape and reel.

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)

Supply Voltage between V_{S+} and V_{S-} +18V
 Input Voltage $V_{S-} - 0.5\text{V}$, $V_{S+} + 0.5\text{V}$
 Maximum Continuous Output Current 30mA
 Maximum Die Temperature +125°C

Storage Temperature -65°C to +150°C
 Operating Temperature -40°C to +85°C
 Power Dissipation See Curves

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications $V_{S+} = +5\text{V}$, $V_{S-} = -5\text{V}$, $R_L = 1\text{k}\Omega$ and $C_L = 12\text{pF}$ to 0V, $T_A = 25^\circ\text{C}$ unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage	$V_{CM} = 0\text{V}$		3	15	mV
TCV_{OS}	Average Offset Voltage Drift (Note 1)			7		$\mu\text{V}/^\circ\text{C}$
I_B	Input Bias Current	$V_{CM} = 0\text{V}$		2	60	nA
R_{IN}	Input Impedance			1		G Ω
C_{IN}	Input Capacitance			2		pF
$CMIR$	Common-Mode Input Range		-5.5		+5.5	V
$CMRR$	Common-Mode Rejection Ratio	for V_{IN} from -5.5V to 5.5V	50	70		dB
A_{VOL}	Open-Loop Gain	$-4.5\text{V} \leq V_{OUT} \leq 4.5\text{V}$	65	80		dB
OUTPUT CHARACTERISTICS						
V_{OL}	Output Swing Low	$I_L = -5\text{mA}$		-4.9	-4.8	V
V_{OH}	Output Swing High	$I_L = 5\text{mA}$	4.8	4.9		V
I_{SC}	Short Circuit Current			± 120		mA
I_{OUT}	Output Current			± 30		mA
POWER SUPPLY PERFORMANCE						
$PSRR$	Power Supply Rejection Ratio	V_S is moved from $\pm 2.25\text{V}$ to $\pm 7.75\text{V}$	60	80		dB
I_S	Supply Current (Per Amplifier)	No Load		2.5	3.75	mA
DYNAMIC PERFORMANCE						
SR	Slew Rate (Note 2)	$-4.0\text{V} \leq V_{OUT} \leq 4.0\text{V}$, 20% to 80%		33		V/ μs
t_S	Settling to +0.1% ($A_V = +1$)	($A_V = +1$), $V_O = 2\text{V}$ Step		140		ns
BW	-3dB Bandwidth			30		MHz
$GBWP$	Gain-Bandwidth Product			20		MHz
PM	Phase Margin			50		°
CS	Channel Separation	$f = 5\text{MHz}$		110		dB
d_G	Differential Gain (Note 3)	$R_F = R_G = 1\text{k}\Omega$ and $V_{OUT} = 1.4\text{V}$		0.12		%
d_P	Differential Phase (Note 3)	$R_F = R_G = 1\text{k}\Omega$ and $V_{OUT} = 1.4\text{V}$		0.17		°

NOTES:

1. Measured over operating temperature range
2. Slew rate is measured on rising and falling edges
3. NTSC signal generator used

Electrical Specifications $V_{S+} = 5V$, $V_{S-} = 0V$, $R_L = 1k\Omega$ and $C_L = 12pF$ to 2.5V, $T_A = 25^\circ C$ unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage	$V_{CM} = 2.5V$		3	15	mV
TCV_{OS}	Average Offset Voltage Drift (Note 1)			7		$\mu V/^\circ C$
I_B	Input Bias Current	$V_{CM} = 2.5V$		2	60	nA
R_{IN}	Input Impedance			1		$G\Omega$
C_{IN}	Input Capacitance			2		pF
CMIR	Common-Mode Input Range		-0.5		+5.5	V
CMRR	Common-Mode Rejection Ratio	for V_{IN} from -0.5V to 5.5V	45	66		dB
A_{VOL}	Open-Loop Gain	$0.5V \leq V_{OUT} \leq 4.5V$	65	80		dB
OUTPUT CHARACTERISTICS						
V_{OL}	Output Swing Low	$I_L = -5mA$		100	200	mV
V_{OH}	Output Swing High	$I_L = 5mA$	4.8	4.9		V
I_{SC}	Short Circuit Current			± 120		mA
I_{OUT}	Output Current			± 30		mA
POWER SUPPLY PERFORMANCE						
PSRR	Power Supply Rejection Ratio	V_S is moved from 4.5V to 15.5V	60	80		dB
I_S	Supply Current (Per Amplifier)	No Load		2.5	3.75	mA
DYNAMIC PERFORMANCE						
SR	Slew Rate (Note 2)	$1V \leq V_{OUT} \leq 4V$, 20% o 80%		33		V/ μs
t_S	Settling to +0.1% ($A_V = +1$)	($A_V = +1$), $V_O = 2V$ Step		140		ns
BW	-3dB Bandwidth			30		MHz
GBWP	Gain-Bandwidth Product			20		MHz
PM	Phase Margin			50		°
CS	Channel Separation	$f = 5MHz$		110		dB
d_G	Differential Gain (Note 3)	$R_F = R_G = 1k\Omega$ and $V_{OUT} = 1.4V$		0.30		%
d_P	Differential Phase (Note 3)	$R_F = R_G = 1k\Omega$ and $V_{OUT} = 1.4V$		0.66		°

NOTES:

1. Measured over operating temperature range
2. Slew rate is measured on rising and falling edges
3. NTSC signal generator used

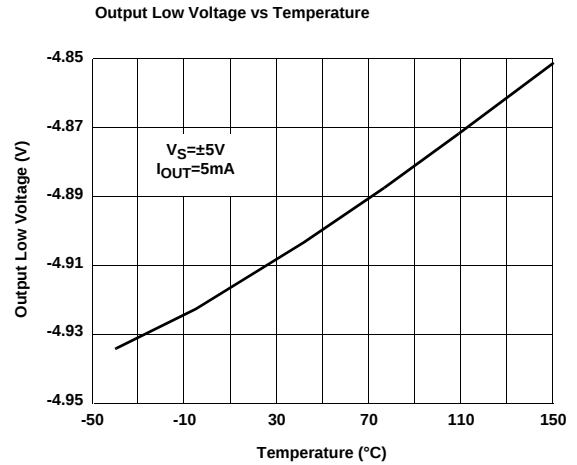
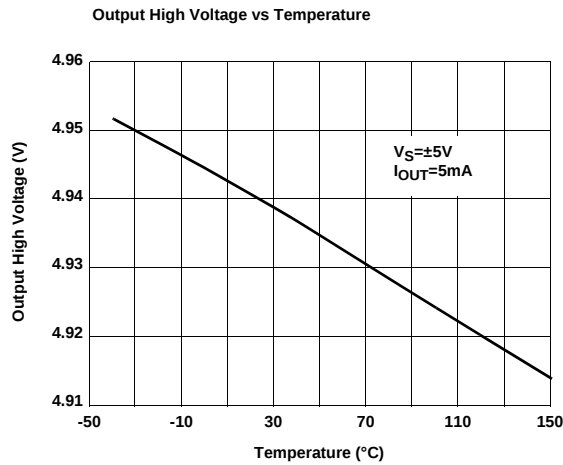
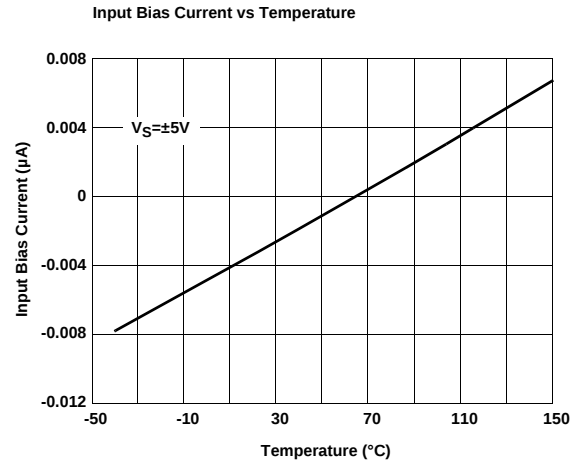
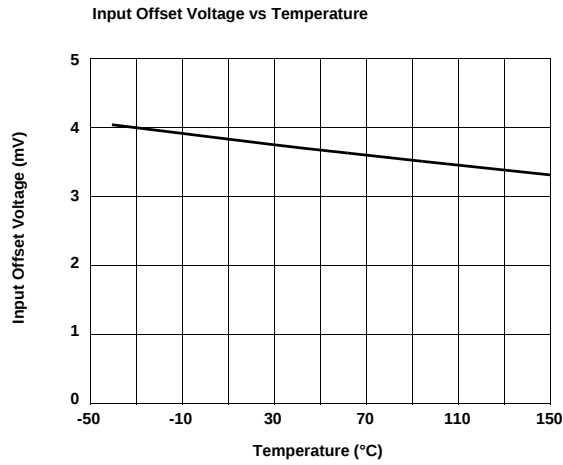
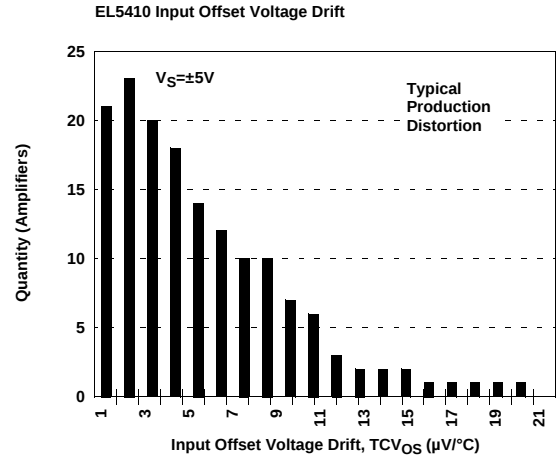
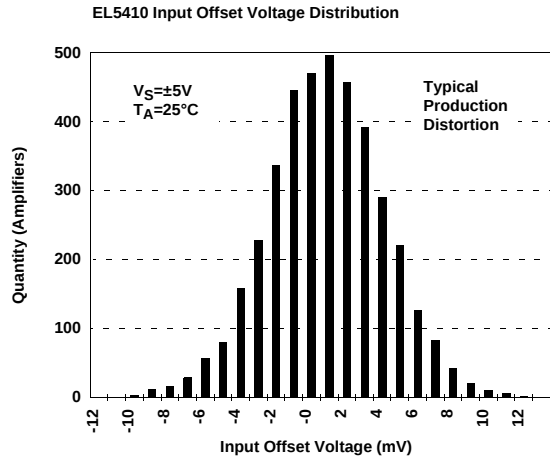
Electrical Specifications $V_{S+} = 15V$, $V_{S-} = 0V$, $R_L = 1k\Omega$ and $C_L = 12pF$ to 7.5V, $T_A = 25^\circ C$ unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage	$V_{CM} = 7.5V$		3	15	mV
TCV_{OS}	Average Offset Voltage Drift (Note 1)			7		$\mu V/^\circ C$
I_B	Input Bias Current	$V_{CM} = 7.5V$		2	60	nA
R_{IN}	Input Impedance			1		$G\Omega$
C_{IN}	Input Capacitance			2		pF
CMIR	Common-Mode Input Range		-0.5		+15.5	V
CMRR	Common-Mode Rejection Ratio	for V_{IN} from -0.5V to 15.5V	53	72		dB
A_{VOL}	Open-Loop Gain	$0.5V \leq V_{OUT} \leq 14.5V$	65	80		dB
OUTPUT CHARACTERISTICS						
V_{OL}	Output Swing Low	$I_L = -7.5mA$		170	350	mV
V_{OH}	Output Swing High	$I_L = 7.5mA$	14.65	14.83		V
I_{SC}	Short Circuit Current			± 120		mA
I_{OUT}	Output Current			± 30		mA
POWER SUPPLY PERFORMANCE						
PSRR	Power Supply Rejection Ratio	V_S is moved from 4.5V to 15.5V	60	80		dB
I_S	Supply Current (Per Amplifier)	No Load		2.5	3.75	mA
DYNAMIC PERFORMANCE						
SR	Slew Rate (Note 2)	$1V \leq V_{OUT} \leq 14V$, 20% o 80%		33		V/ μs
t_S	Settling to +0.1% ($A_V = +1$)	($A_V = +1$), $V_O = 2V$ Step		140		ns
BW	-3dB Bandwidth			30		MHz
GBWP	Gain-Bandwidth Product			20		MHz
PM	Phase Margin			50		°
CS	Channel Separation	$f = 5MHz$		110		dB
d_G	Differential Gain (Note 3)	$R_F = R_G = 1k\Omega$ and $V_{OUT} = 1.4V$		0.10		%
d_P	Differential Phase (Note 3)	$R_F = R_G = 1k\Omega$ and $V_{OUT} = 1.4V$		0.11		°

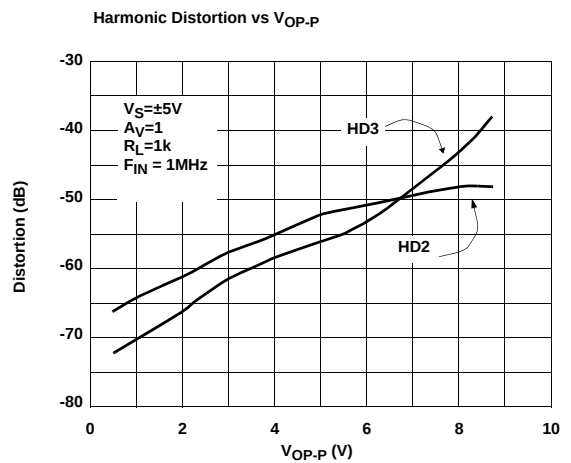
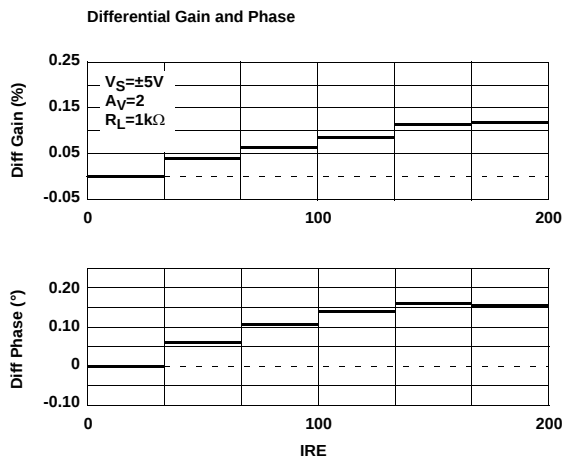
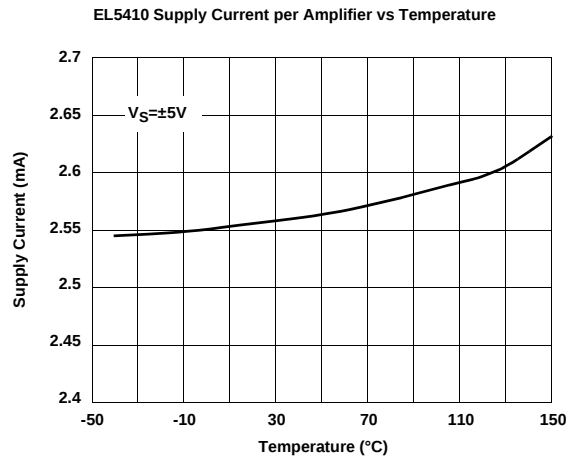
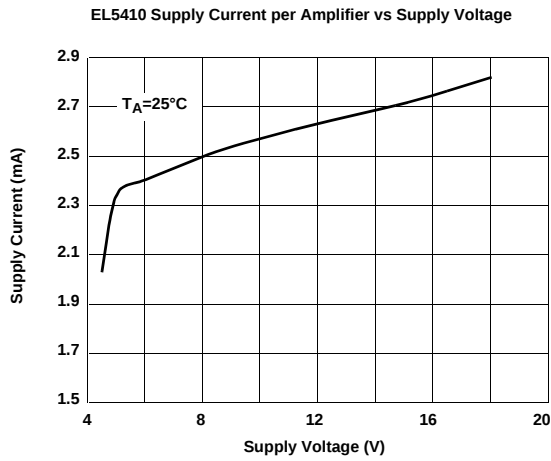
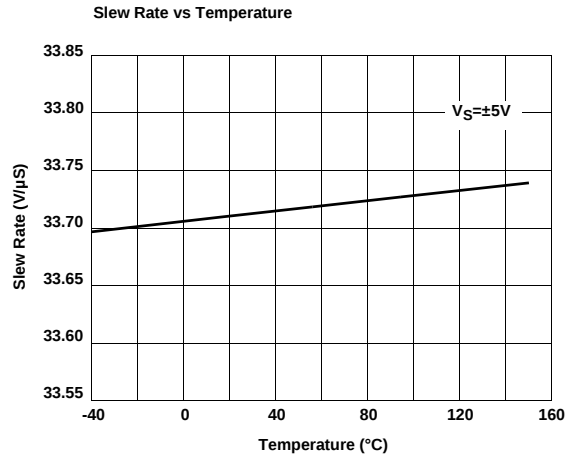
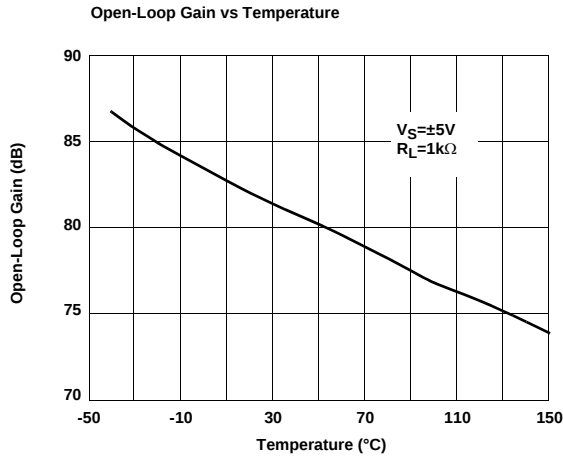
NOTES:

1. Measured over operating temperature range
2. Slew rate is measured on rising and falling edges
3. NTSC signal generator used

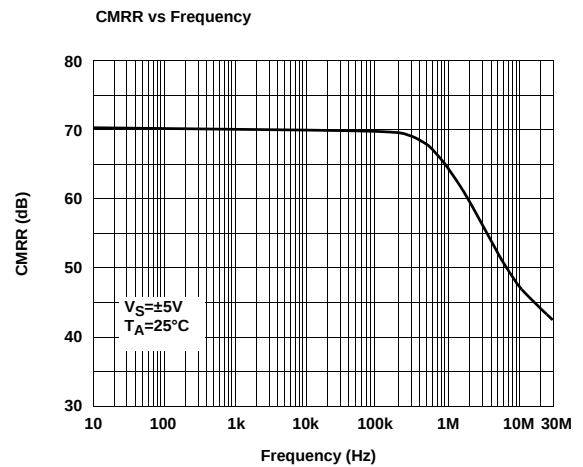
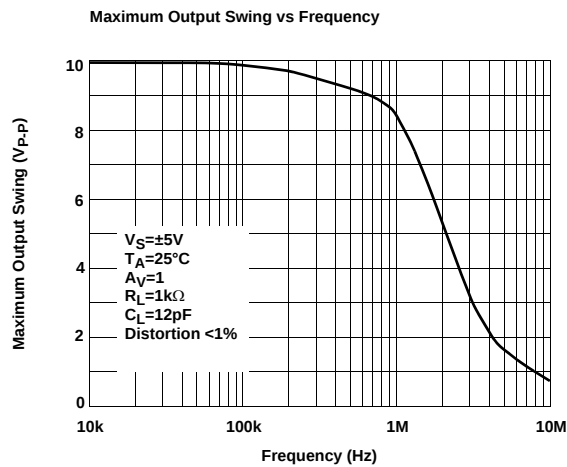
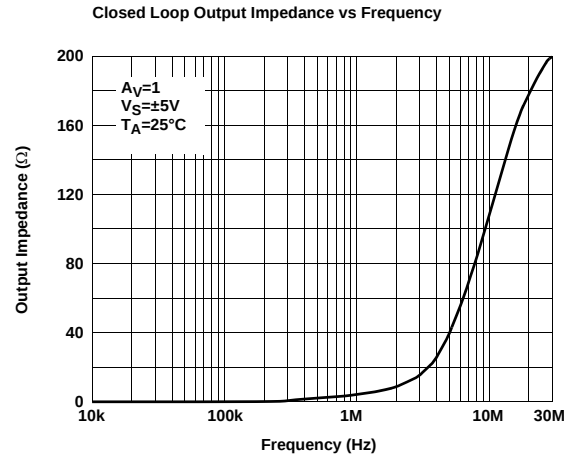
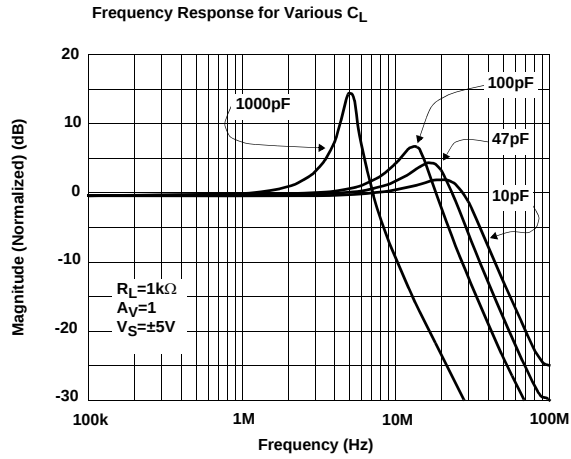
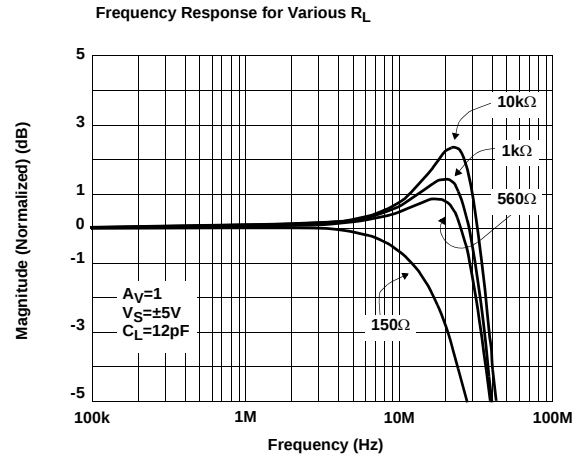
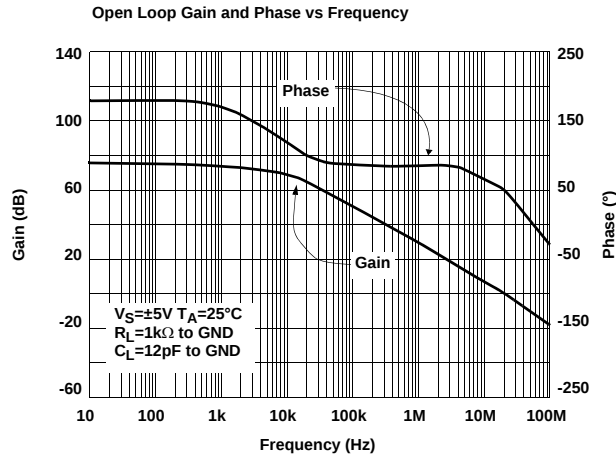
Typical Performance Curves



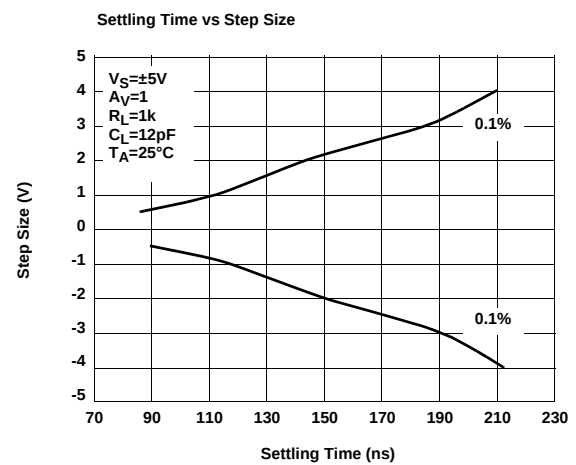
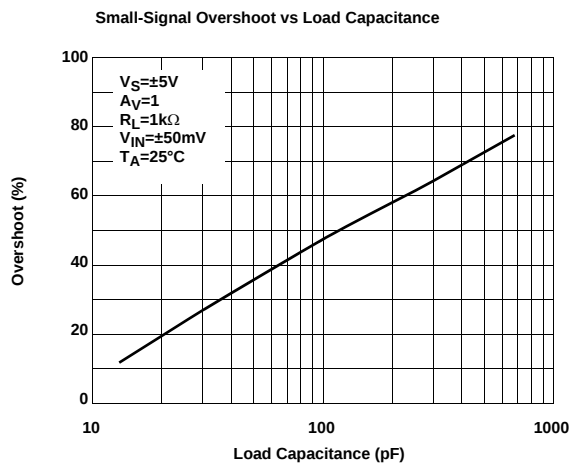
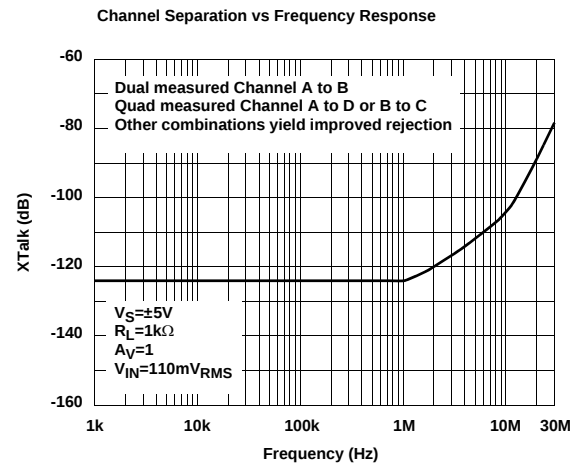
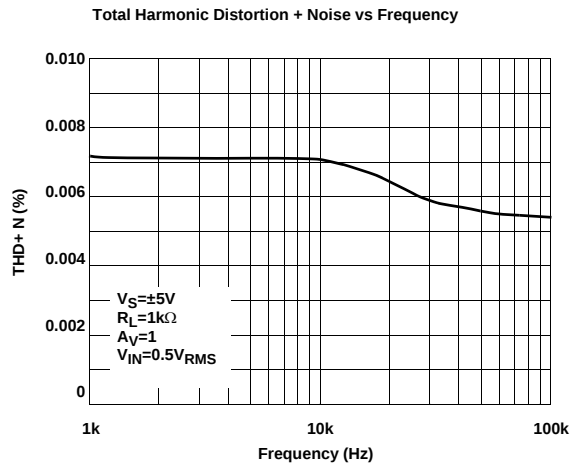
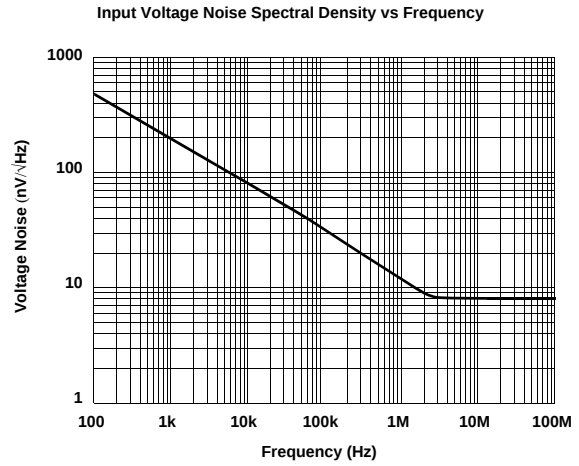
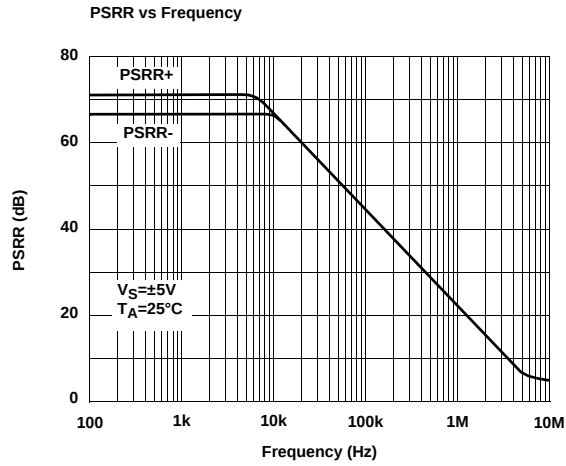
Typical Performance Curves (Continued)



Typical Performance Curves (Continued)

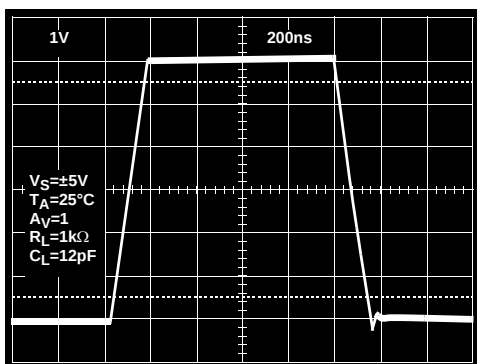


Typical Performance Curves (Continued)

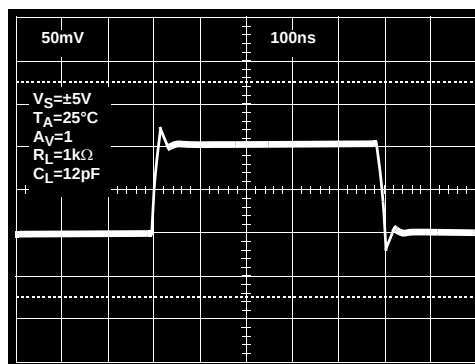


Typical Performance Curves (Continued)

Large Signal Transient Response



Small Signal Transient Response



Pin Descriptions

EL5210	EL5410	NAME	FUNCTION	EQUIVALENT CIRCUIT
1	1	V_{OUTA}	Amplifier A Output	Circuit 1
2	2	V_{INA-}	Amplifier A Inverting Input	Circuit 2
3	3	V_{INA+}	Amplifier A Non-Inverting Input	(Reference Circuit 2)
8	4	V_{S+}	Positive Power Supply	
5	5	V_{INB+}	Amplifier B Non-Inverting Input	(Reference Circuit 2)
6	6	V_{INB-}	Amplifier B Inverting Input	(Reference Circuit 2)
7	7	V_{OUTB}	Amplifier B Output	(Reference Circuit 1)
	8	V_{OUTC}	Amplifier C Output	(Reference Circuit 1)
	9	V_{INC-}	Amplifier C Inverting Input	(Reference Circuit 2)
	10	V_{INC+}	Amplifier C Non-Inverting Input	(Reference Circuit 2)
4	11	V_{S-}	Negative Power Supply	
	12	V_{IND+}	Amplifier D Non-Inverting Input	(Reference Circuit 2)
	13	V_{IND-}	Amplifier D Inverting Input	(Reference Circuit 2)
	14	V_{OUTD}	Amplifier D Output	(Reference Circuit 1)

Applications Information

Product Description

The EL5210 and EL5410 voltage feedback amplifiers are fabricated using a high voltage CMOS process. They exhibit Rail-to-Rail input and output capability, are unity gain stable and have low power consumption (2.5mA per amplifier). These features make the EL5210 and EL5410 ideal for a wide range of general-purpose applications. Connected in voltage follower mode and driving a load of 1k Ω and 12pF, the EL5210 and EL5410 have a -3dB bandwidth of 30MHz while maintaining a 33V/ μ s slew rate. The EL5210 is a dual amplifier while the EL5410 is a quad amplifier.

Operating Voltage, Input, and Output

The EL5210 and EL5410 are specified with a single nominal supply voltage from 5V to 15V or a split supply with its total range from 5V to 15V. Correct operation is guaranteed for a supply range of 4.5V to 16.5V. Most EL5210 and EL5410 specifications are stable over both the full supply range and operating temperatures of -40°C to +85°C. Parameter variations with operating voltage and/or temperature are shown in the typical performance curves.

The input common-mode voltage range of the EL5210 and EL5410 extends 500mV beyond the supply rails. The output swings of the EL5210 and EL5410 typically extend to within 100mV of positive and negative supply rails with load currents of 5mA. Decreasing load currents will extend the output voltage range even closer to the supply rails. Figure 1 shows the input and output waveforms for the device in the unity-gain configuration. Operation is from ± 5 V supply with a 1k Ω load connected to GND. The input is a 10V_{P-P} sinusoid. The output voltage is approximately 9.8V_{P-P}.

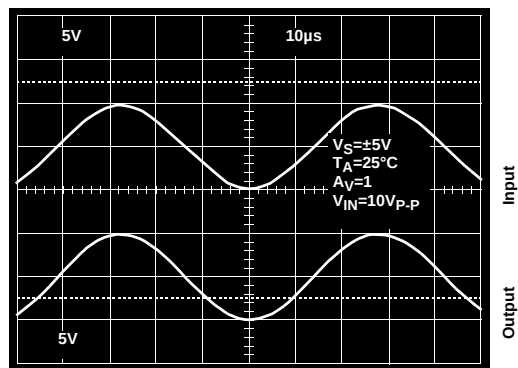


FIGURE 1. OPERATION WITH RAIL-TO-RAIL INPUT AND OUTPUT

Short Circuit Current Limit

The EL5210 and EL5410 will limit the short circuit current to ± 120 mA if the output is directly shorted to the positive or the negative supply. If an output is shorted indefinitely, the power dissipation could easily increase such that the device may be damaged. Maximum reliability is maintained if the

output continuous current never exceeds ± 30 mA. This limit is set by the design of the internal metal interconnects.

Output Phase Reversal

The EL5210 and EL5410 are immune to phase reversal as long as the input voltage is limited from $V_S - 0.5$ V to $V_S + 0.5$ V. Figure 2 shows a photo of the output of the device with the input voltage driven beyond the supply rails. Although the device's output will not change phase, the input's overvoltage should be avoided. If an input voltage exceeds supply voltage by more than 0.6V, electrostatic protection diodes placed in the input stage of the device begin to conduct and overvoltage damage could occur.

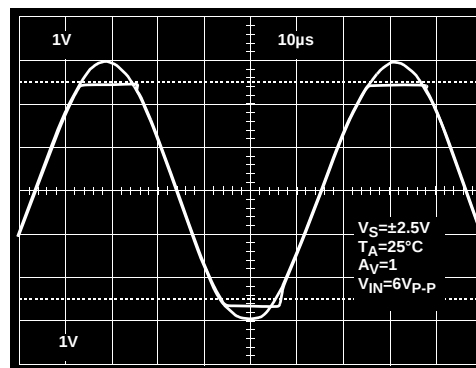


FIGURE 2. OPERATION WITH BEYOND-THE-RAILS INPUT

Power Dissipation

With the high-output drive capability of the EL5210 and EL5410 amplifiers, it is possible to exceed the 125°C 'absolute-maximum junction temperature' under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for the application to determine if load conditions need to be modified for the amplifier to remain in the safe operating area.

The maximum power dissipation allowed in a package is determined according to:

$$P_{DMAX} = \frac{T_{JMAX} - T_{AMAX}}{\Theta_{JA}}$$

Where:

T_{JMAX} = Maximum Junction Temperature

T_{AMAX} = Maximum Ambient Temperature

Θ_{JA} = Thermal Resistance of the Package

P_{DMAX} = Maximum Power Dissipation in the Package.

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the loads, or:

$$P_{DMAX} = \Sigma i[V_S \times I_{SMAX} + (V_S - V_{OUTi}) \times I_{LOADi}]$$

when sourcing, and

$$P_{D_{MAX}} = \sum_i [V_S \times I_{S_{MAX}} + (V_{OUT_i} - V_S) \times I_{LOAD_i}]$$

when sinking.

Where:

$i = 1$ to 2 for Dual and 1 to 4 for Quad

V_S = Total Supply Voltage

$I_{S_{MAX}}$ = Maximum Supply Current Per Amplifier

V_{OUT_i} = Maximum Output Voltage of the Application

I_{LOAD_i} = Load current

If we set the two $P_{D_{MAX}}$ equations equal to each other, we can solve for R_{LOAD_i} to avoid device overheat. Figure 3 and Figure 4 provide a convenient way to see if the device will overheat. The maximum safe power dissipation can be found graphically, based on the package type and the ambient temperature. By using the previous equation, it is a simple matter to see if $P_{D_{MAX}}$ exceeds the device's power derating curves. To ensure proper operation, it is important to observe the recommended derating curves shown in Figure 3 and Figure 4.

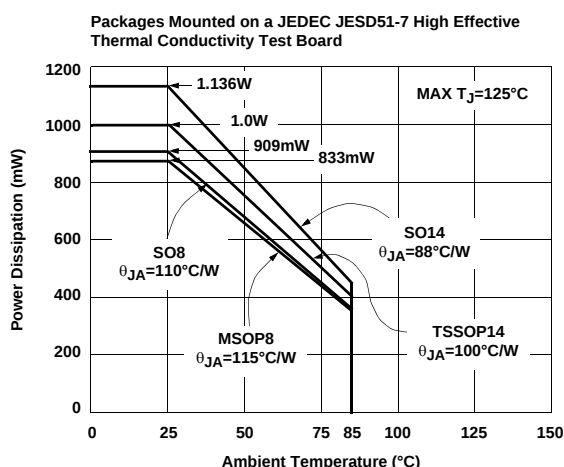


FIGURE 3. PACKAGE POWER DISSIPATION VS AMBIENT TEMPERATURE

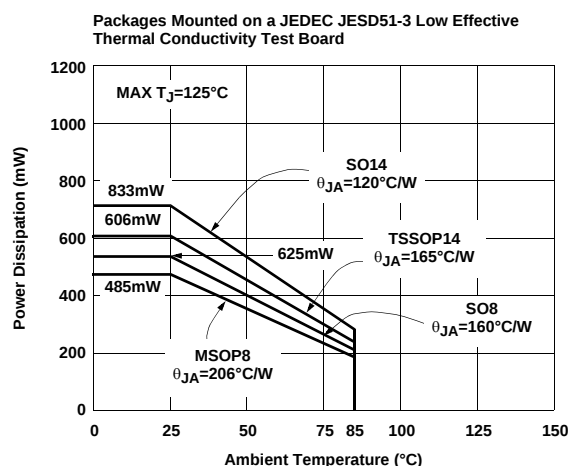


FIGURE 4. PACKAGE POWER DISSIPATION VS AMBIENT TEMPERATURE

Unused Amplifiers

It is recommended that any unused amplifiers in a dual and a quad package be configured as a unity gain follower. The inverting input should be directly connected to the output and the non-inverting input tied to the ground plane.

Driving Capacitive Loads

The EL5210 and EL5410 can drive a wide range of capacitive loads. As load capacitance increases, however, the -3dB bandwidth of the device will decrease and the peaking increase. The amplifiers drive 10pF loads in parallel with 1kΩ with just 1.2dB of peaking, and 100pF with 6.5dB of peaking. If less peaking is desired in these applications, a small series resistor (usually between 5Ω and 50Ω) can be placed in series with the output. However, this will obviously reduce the gain slightly. Another method of reducing peaking is to add a "snubber" circuit at the output. A snubber is a shunt load consisting of a resistor in series with a capacitor. Values of 150Ω and 10nF are typical. The advantage of a snubber is that it does not draw any DC load current or reduce the gain.

Power Supply Bypassing and Printed Circuit Board Layout

The EL5210 and EL5410 can provide gain at high frequency. As with any high-frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended, lead lengths should be as short as possible and the power supply pins must be well bypassed to reduce the risk of oscillation. For normal single supply operation, where the V_{S-} pin is connected to ground, a 0.1μF ceramic capacitor should be placed from V_{S+} to pin to V_{S-} pin. A 4.7μF tantalum capacitor should then be connected in parallel, placed in the region of the amplifier. One 4.7μF capacitor may be used for multiple devices. This same capacitor combination should be placed at each supply pin to ground if split supplies are to be used.

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems.
Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com