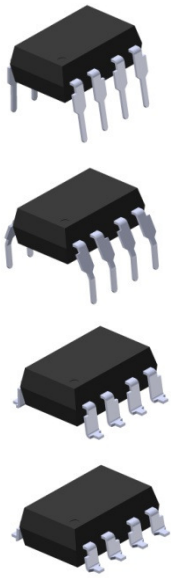
EVERLIGHT

8 PIN DIP HIGH SPEED 10MBit/s LOGIC GATE PHOTOCOUPLER

6N137
EL26XX series

Features:

- High speed 10Mbit/s
- 10kV/μs min. common mode transient immunity (EL2611)
- Guaranteed performance from -40 to 85℃
- Logic gate output
- High isolation voltage between input and output (Viso=5000 V rms)
- Pb free and RoHS compliant.
- UL approved (No. 214129)
- VDE approved (No. 132249)
- SEMKO approved
- NEMKO approved
- DEMKO approved
- FIMKO approved
- CSA approved (No. 2037145)



Description

The 6N137, EL2601 and EL2611 are consists of an infrared emitting diode optically coupled to a high speed integrated photo detector logic gate with a strobable output.

It is packaged in a 8-pin DIP package and available in wide-lead spacing and SMD options.

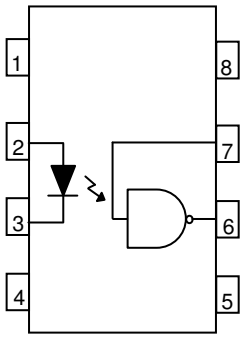
Applications

- Ground loop elimination
- LSTTL to TTL, LSTTL or 5 volt CMOS
- Line receiver, data transmission
- Data multiplexing
- Switching power supplies
- Pulse transformer replacement
- Computer peripheral interface

Truth Table (Positive Logic)

Input	Enable	Output
H	H	L
L	H	H
H	L	H
L	L	H
H	NC	L
L	NC	H

Schematic



A 0.1μF bypass capacitor must be connected between pins 8 and 5 *3

Pin Configuration

1, No Connection
2, Anode
3, Cathode
4. No Connection
5, Gnd
6, Vout
7, V_E
8, V_{CC}

Absolute Maximum Ratings (T_a=25℃)

Parameter		Symbol	Rating	Unit
Input	Forward current	I_F	50	mA
	Enable input voltage Not exceed V_{CC} by more than 500mV	V_E	5.5	V
	Reverse voltage	V_R	5	V
	Power dissipation	P_D	100	mW
Output	Power dissipation	P_C	85	mW
	Output current	I_O	50	mA
	Output voltage	V_O	7.0	V
	Supply voltage	V_{CC}	7.0	V
Output Power Dissipation		P_O	100	mW
Isolation voltage *1		V_{ISO}	5000	V rms
Operating temperature		T_{OPR}	-40 ~ +85	℃
Storage temperature		T_{STG}	-55 ~ +125	℃
Soldering temperature *2		T_{SOL}	260	℃

Notes

*1 AC for 1 minute, R.H.= 40 ~ 60% R.H. In this test, pins 1, 2, 3 & 4 are shorted together, and pins 5, 6, 7 & 8 are shorted together.

*2 For 10 seconds.

Electrical Characteristics (T_a=-40 to 85℃ unless specified otherwise)

Input

Parameter	Symbol	Min.	Typ.*	Max.	Unit	Condition
Forward voltage	V_F	-	1.4	1.8	V	I_F = 10mA
Reverse voltage	V_R	5.0	-	-	V	I_R = 10μA
Temperature coefficient of forward voltage	$\Delta V_F/\Delta T_A$	-	-1.8	-	mV/℃	I_F =10mA
Input capacitance	C_{IN}	-	60	-	pF	V_F=0, f=1MHz

Output

Parameter	Symbol	Min.	Typ.*	Max.	Unit	Condition
High level supply current	I_{CCH}	-	7	10	mA	I_F=10mA, V_E=0.5V, V_{CC}=5.5V
Low level supply current	I_{CCL}	-	9	13	mA	I_F=0mA, V_E=0.5V, V_{CC}=5.5V
High level enable current	I_{EH}	-	- 0.6	-1.6	mA	V_E=0.5V, V_{CC}=5.5V
Low level enable current	I_{EL}	-	- 0.8	-1.6	mA	V_E=2.0V, V_{CC}=5.5V
High level enable voltage	V_{EH}	2.0	-	-	V	I_F=10mA, V_{CC}=5.5V
Low level enable voltage*4	V_{EL}	-	-	0.8	V	I_F=10mA, V_{CC}=5.5V

Transfer Characteristics (T_a=-40 to 85℃ unless specified otherwise)

Parameter	Symbol	Min.	Typ.*	Max.	Unit	Condition
HIGH Level Output Current	I_{OH}	-	2.1	100	uA	V_{CC}=5.5V, V_O=5.5V, I_F=250μA, V_E=2.0V
LOW Level Output Current	V_{OL}	-	0.35	0.6	V	V_{CC} = 5.5V, I_F=5mA, V_E=2.0V,I_{CL}=13mA
Input Threshold Current	I_{FT}	-	2.5	5	mA	V_{CC}= 5.5V, V_O=0.6V, V_E =2.0V,I_{OL}=13mA

Switching Characteristics (T_a=-40 to 85℃, V_{CC}=5V, I_F=7.5mA unless specified otherwise)

Parameter	Symbol	Min.	Typ.*	Max.	Unit	Condition
Propagation delay time to output High level*5 (Fig.12)	T_{PHL}	-	35	75	ns	C_L = 15pF, R_L=350Ω, TA=25℃
Propagation delay time to output Low level*6 (Fig.12)	T_{PLH}	-	40	75	ns	C_L = 15pF, R_L=350Ω, TA=25℃
Pulse width distortion	|Tphl – Tplh|	-	5	35	ns	C_L = 15pF, R_L=350Ω
Output rise time*7 (Fig.12)	tr	-	40	-	ns	C_L = 15pF, R_L=350Ω
Output fall time*8 (Fig.12)	tf	-	10	-	ns	C_L = 15pF, R_L=350Ω

Switching Characteristics (T_a=-40 to 85℃, V_{CC}=5V, I_F=7.5mA unless specified otherwise)

Enable Propagation Delay Time to Output High Level*9 (Fig.13)		t_{ELH}	-	15	-	ns	I_F = 7.5mA , V_{EH}=3.5V, C_L = 15pF, R_L=350Ω
Enable Propagation Delay Time to Output Low Level*10 (Fig.13)		t_{EHL}	-	15	-	ns	I_F = 7.5mA , V_{EH}=3.5V, C_L = 15pF, R_L=350Ω
Common Mode Transient Immunity at Logic High *11	6N137	CM_H	-	-	-	V/μS	I_F = 7.5mA , V_{OH}=2.0V, R_L=350Ω, TA=25℃ V_{CM}=10Vp-p (Fig.14)
	EL2601		5,000	-	-		I_F = 7.5mA , V_{OH}=2.0V, R_L=350Ω, TA=25℃ V_{CM}=50Vp-p (Fig.14)
	EL2611		10,000	-	-		I_F = 7.5mA , V_{OH}=2.0V, R_L=350Ω, TA=25℃ V_{CM}=400Vp-p (Fig.14)
	EL2611		20,000	-	-		I_F = 7.5mA , V_{OH}=2.0V, R_L=350Ω, TA=25℃ V_{CM}=400Vp-p (Fig.15)
Common Mode Transient Immunity at Logic Low *12	6N137	CM_L	-	-	-	V/μS	I_F = 0mA , V_{OL}=0.8V, R_L=350Ω, TA=25℃ V_{CM}=10Vp-p (Fig.14)
	EL2601		5,000	-	-		I_F = 0mA , V_{OL}=0.8V, R_L=350Ω, TA=25℃ V_{CM}=50Vp-p (Fig.14)
	EL2611		10,000	-	-		I_F = 0mA , V_{OL}=0.8V, R_L=350Ω, TA=25℃ V_{CM}=400Vp-p (Fig.14)
	EL2611		20,000	-	-		I_F = 7.5mA , V_{OH}=2.0V, R_L=350Ω, TA=25℃ V_{CM}=400Vp-p (Fig.15)

Typical Performance Curves

Fig.1 Input Diode Forward Voltage vs. Forward Current

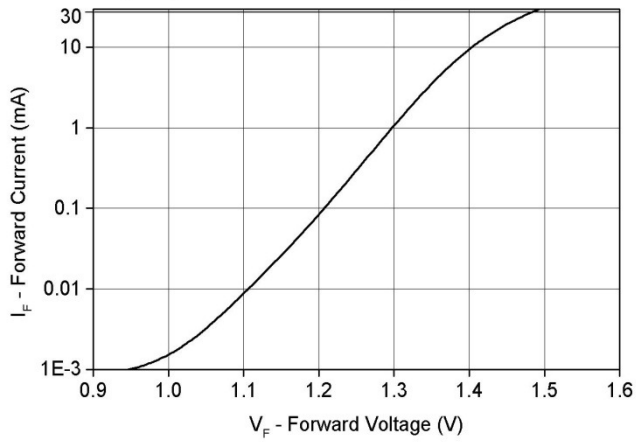


Fig.2 Low Level Output Voltage vs. Ambient Temperature

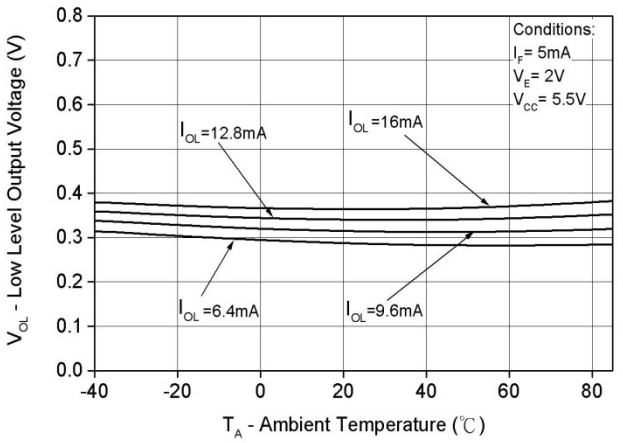


Fig.3 Low Level Output Current vs. Ambient Temperature

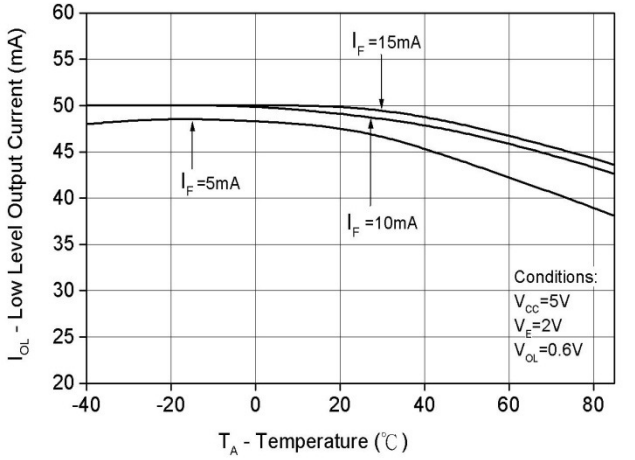


Fig.4 Input Threshold Current vs. Ambient Temperature

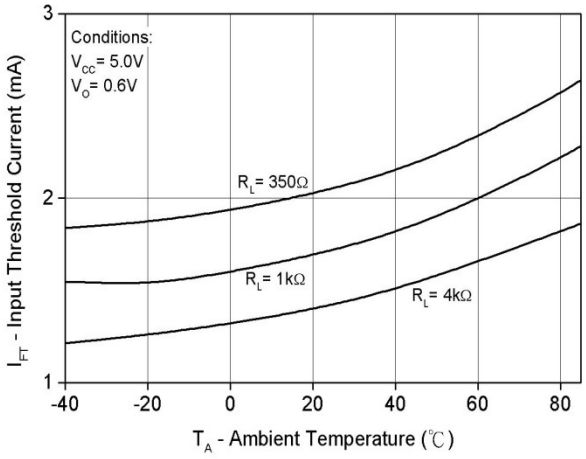


Fig.5 Output Voltage vs. Input Forward Current

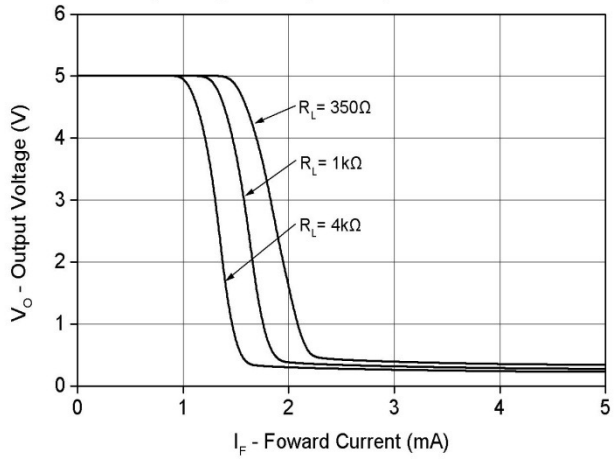


Fig.6 High Level Output Current vs. Temperature

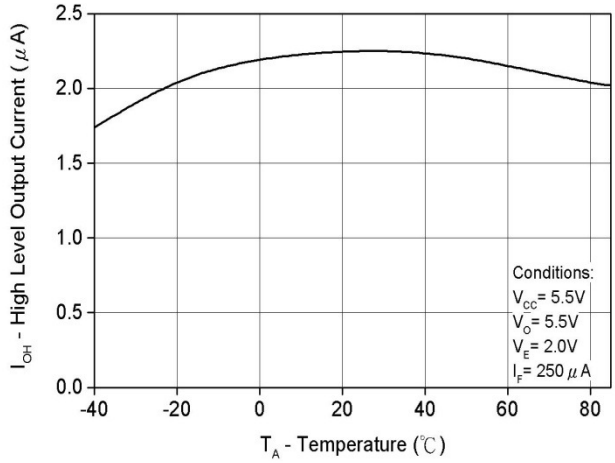


Fig.7 Switching Time vs. Forward Current

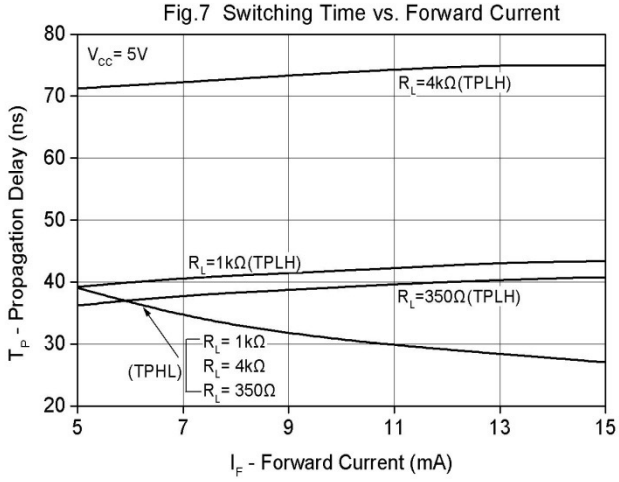


Fig.8 Switching Time vs. Temperature

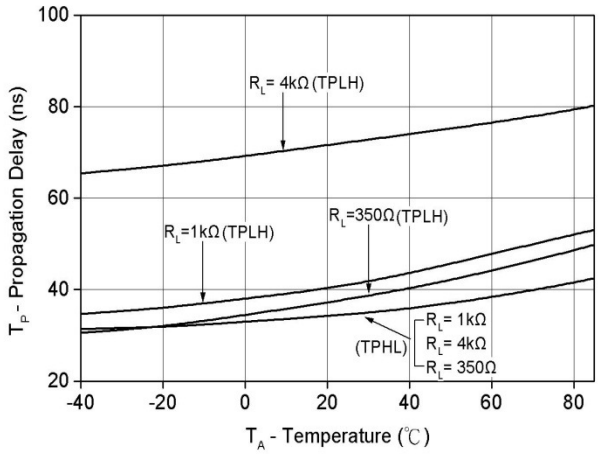


Fig.9 Pulse Width Distortion vs. Temperature

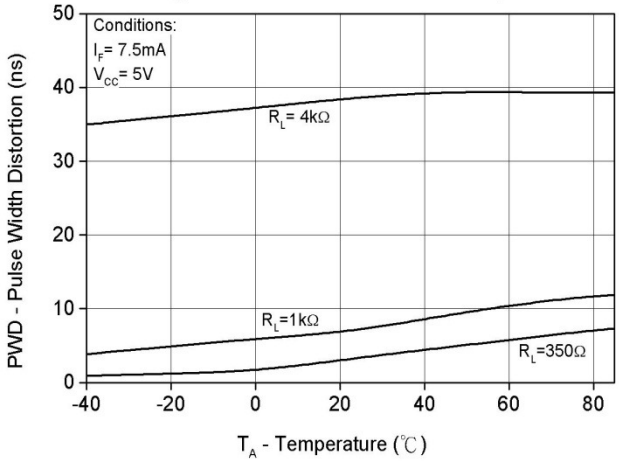


Fig.10 Rise and Fall Time vs. Temperature

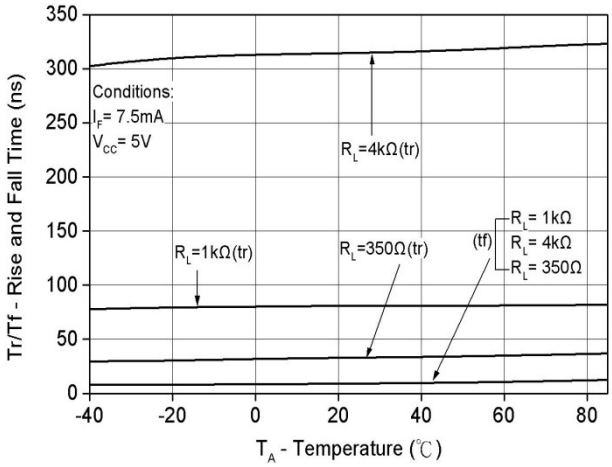
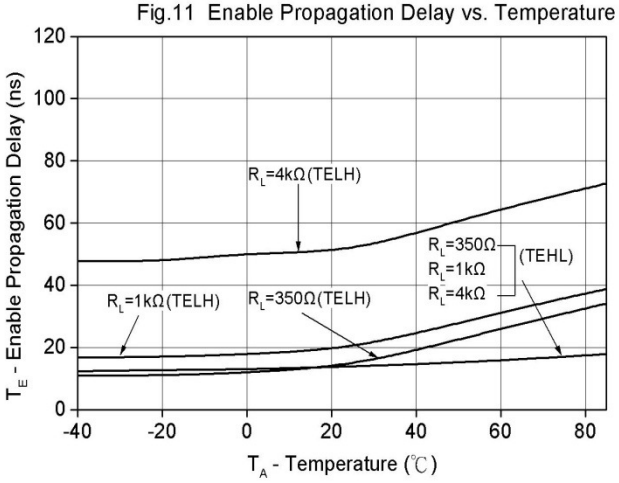


Fig.11 Enable Propagation Delay vs. Temperature



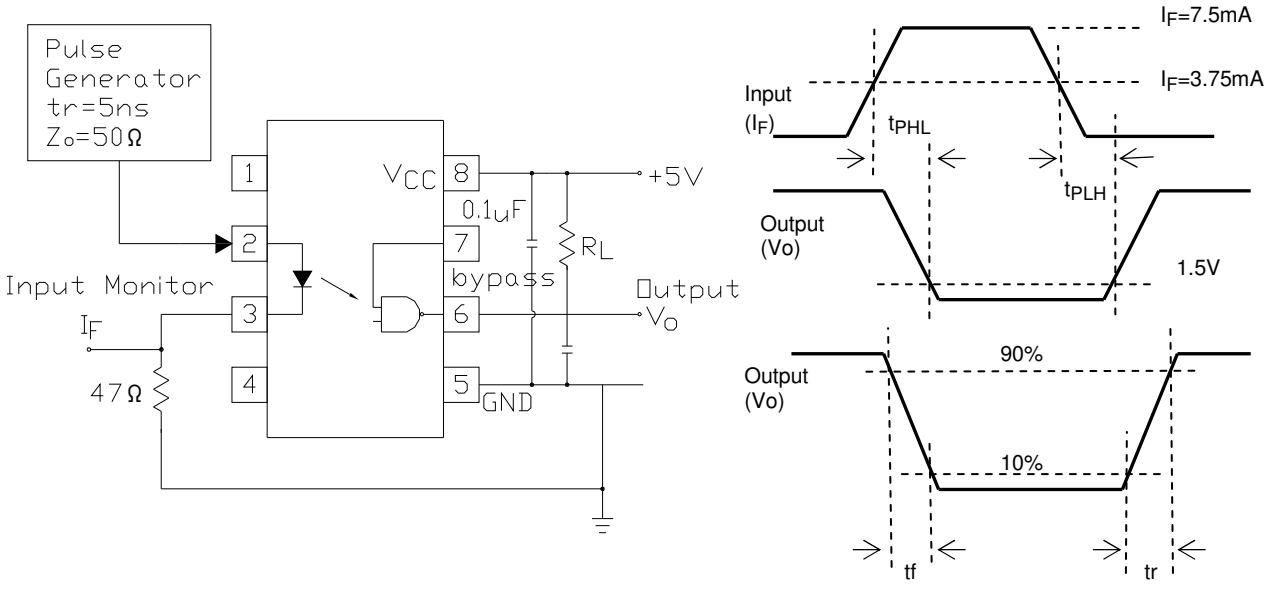


Fig. 12 Test circuit and waveforms for t_{PHL}, t_{PLH}, t_r, and t_f

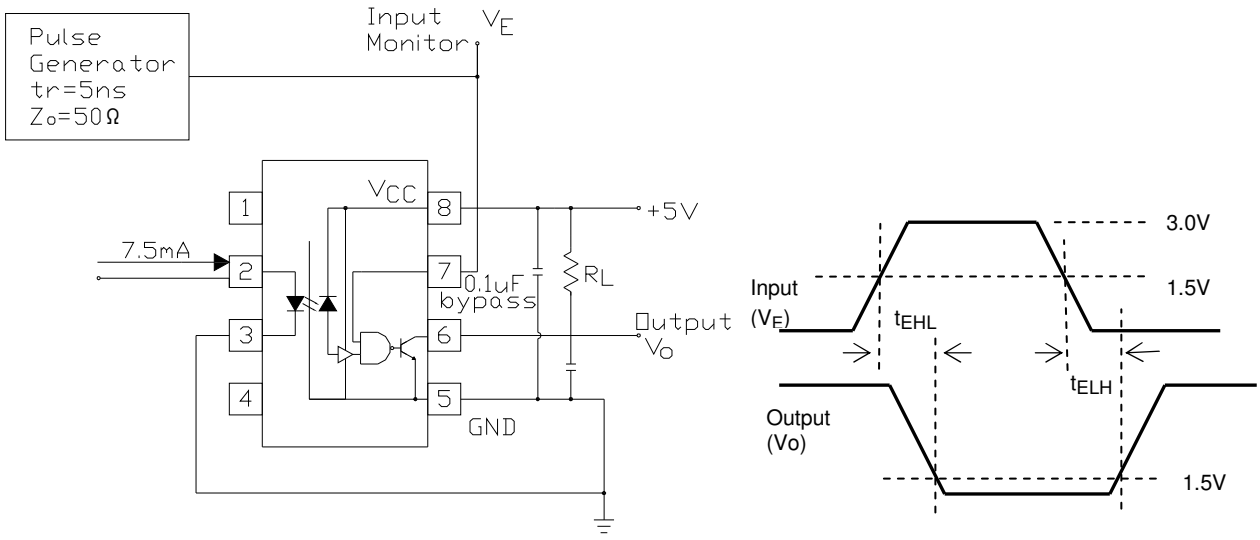


Fig. 13 Test circuit and waveform for $t_{EHL}$and t_{ELH}

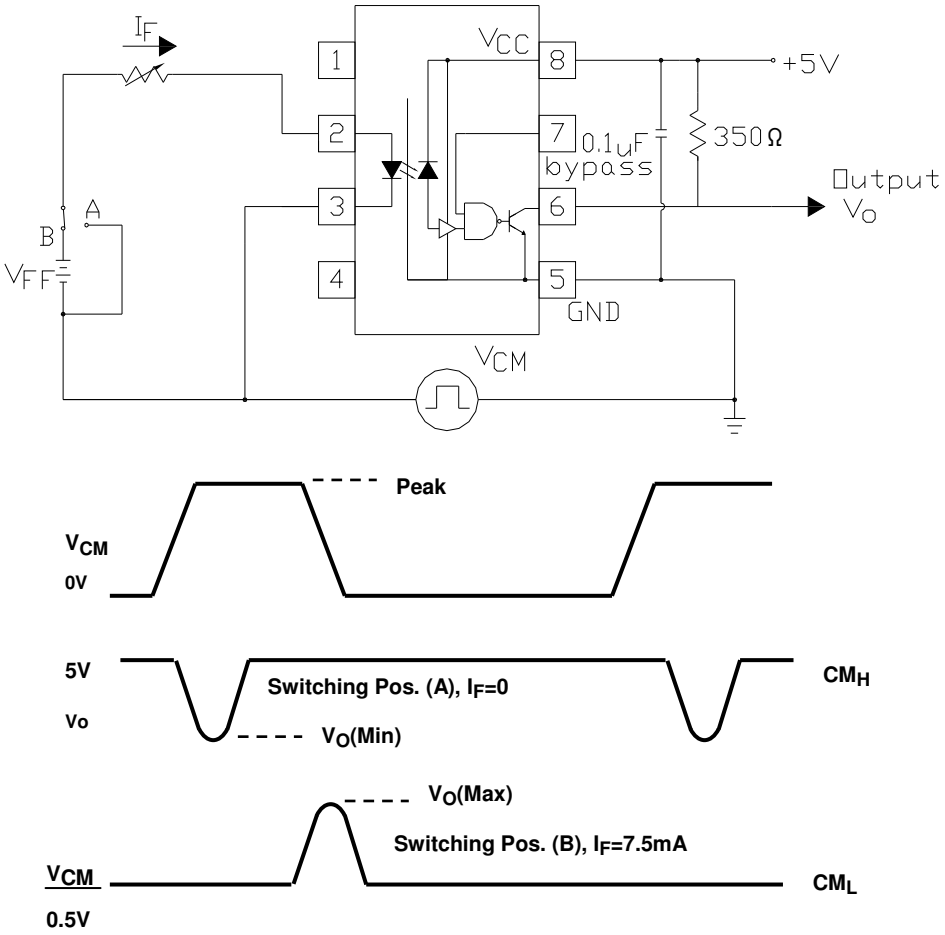


Fig. 14 Test circuit Common mode Transient Immunity

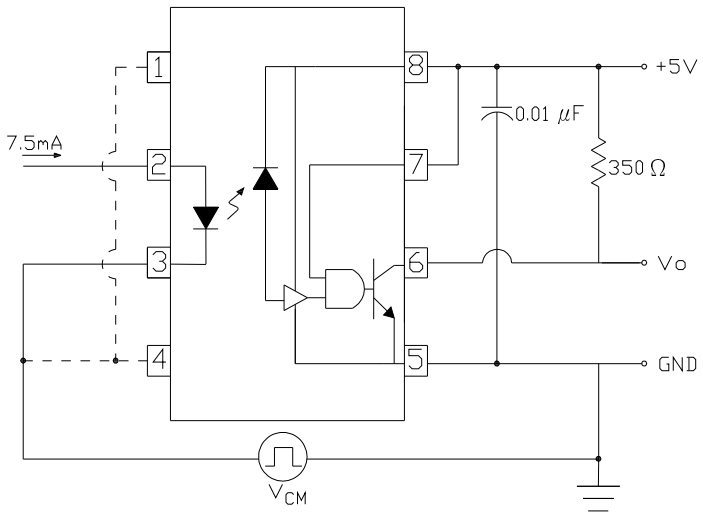


Fig. 15 Recommended drive circuit for ELW2611 families for high-CMR

Notes:

*3 The VCC supply must be bypassed by a 0.1μF capacitor or larger. This can be either a ceramic or solid tantalum capacitor with good high frequency characteristic and should be connected as close as possible to the package VCC and GND pins

*4. Enable Input – No pull up resistor required as the device has an internal pull up resistor.

*5. tPLH – Propagation delay is measured from the 3.75mA level on the HIGH to LOW transition of the input current pulse to the 1.5 V level on the LOW to HIGH transition of the output voltage pulse.

*6. tPHL – Propagation delay is measured from the 3.75mA level on the LOW to HIGH transition of the input current pulse to the 1.5 V level on the HIGH to LOW transition of the output voltage pulse.

*7. tr – Rise time is measured from the 90% to the 10% levels on the LOW to HIGH transition of the output pulse.

*8. tf – Fall time is measured from the 10% to the 90% levels on the HIGH to LOW transition of the output pulse.

*9. tELH – Enable input propagation delay is measured from the 1.5V level on the HIGH to LOW transition of the input voltage pulse to the 1.5V level on the LOW to HIGH transition of the output voltage pulse.

*10. tEHL – Enable input propagation delay is measured from the 1.5V level on the LOW to HIGH transition of the input voltage pulse to the 1.5V level on the HIGH to LOW transition of the output voltage pulse.

*11 CMH– The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the HIGH state (i.e., VOUT > 2.0V).

*12 CML– The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the LOW output state (i.e., VOUT < 0.8V).

Order Information

Part Number

6N137Y(Z)-V

Or

EL26XXY(Z)-V

Note

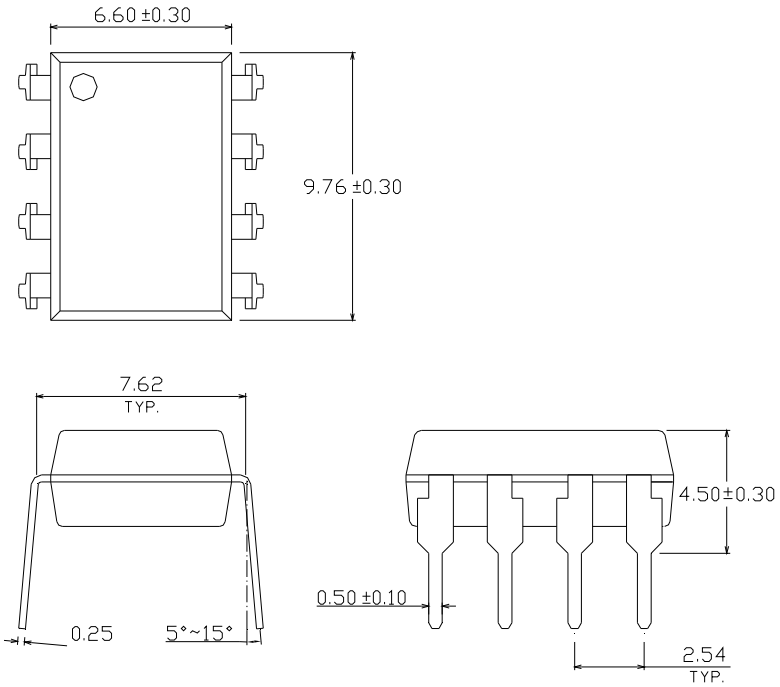
X = (01 or 11) for EL26 part no.
Y = Lead form option (S, S1, M or none)
Z = Tape and reel option (TA, TB or none).
V = VDE (optional)

Option	Description	Packing quantity
None	Standard DIP-8	45 units per tube
M	Wide lead bend (0.4 inch spacing)	45 units per tube
S (TA)	Surface mount lead form + TA tape & reel option	1000 units per reel
S (TB)	Surface mount lead form + TB tape & reel option	1000 units per reel
S1 (TA)	Surface mount lead form (low profile) + TA tape & reel option	1000 units per reel
S1 (TB)	Surface mount lead form (low profile) + TB tape & reel option	1000 units per reel

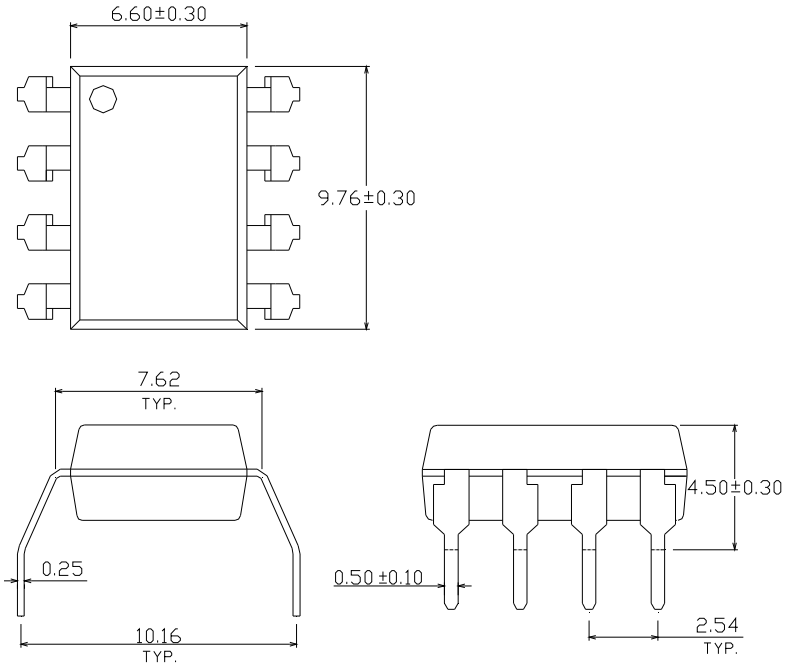
Package Drawing

(Dimensions in mm)

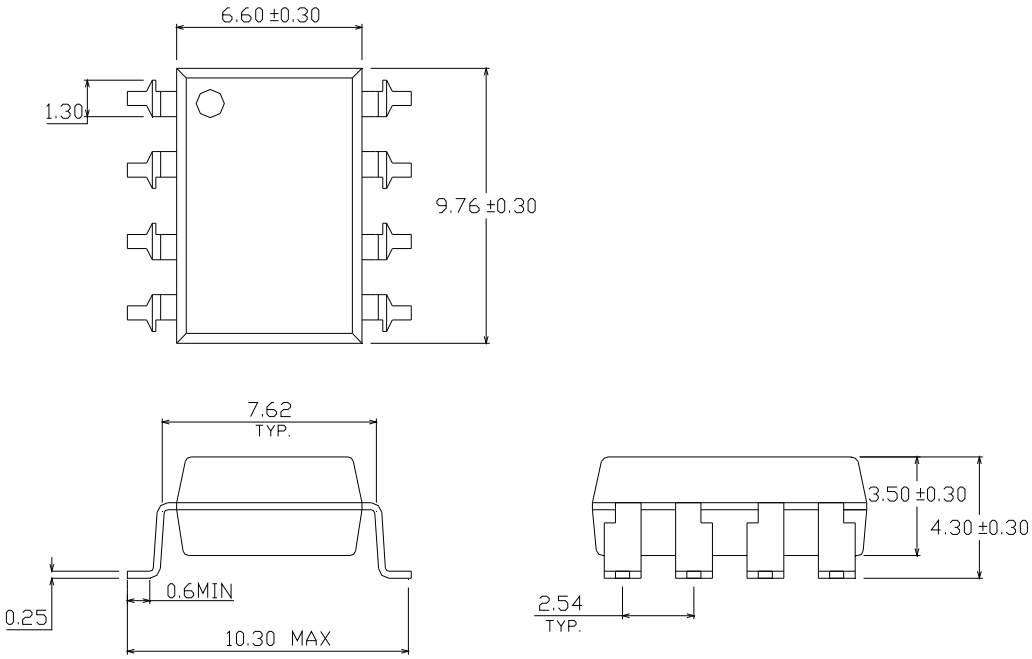
Standard DIP Type



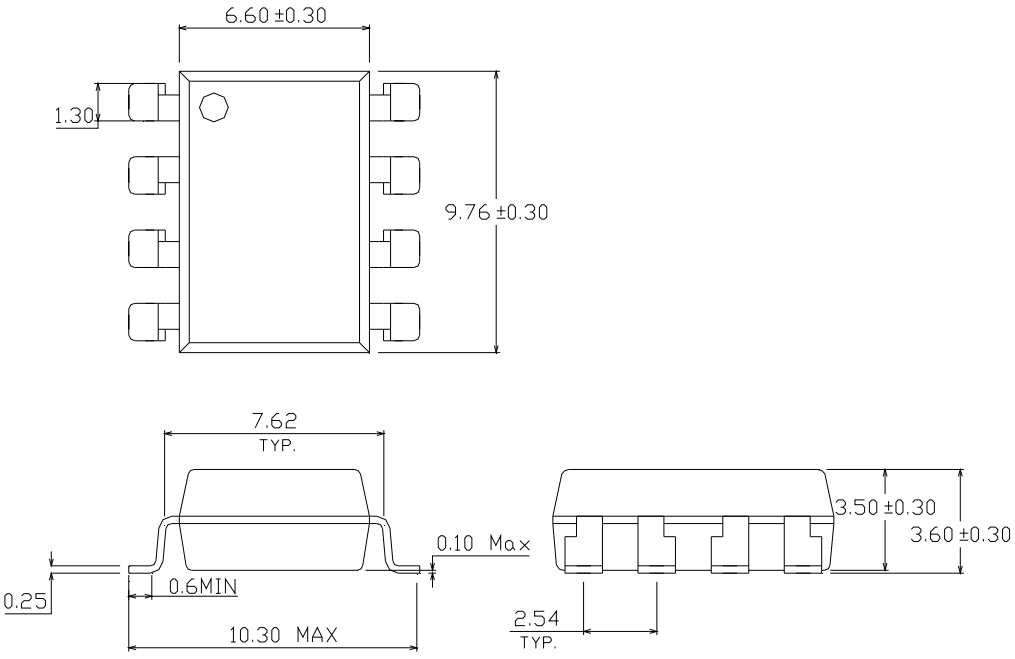
Option M Type



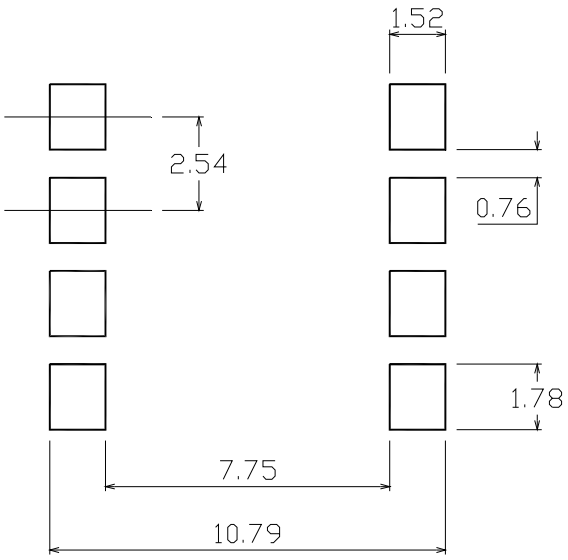
Option S Type



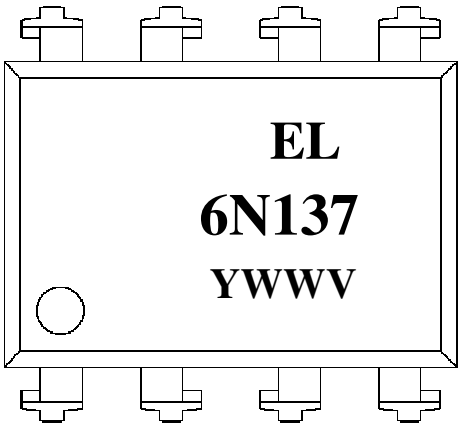
Option S1 Type



Recommended pad layout for surface mount leadform



Device Marking

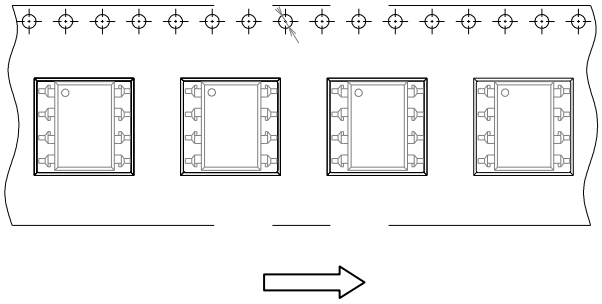


Notes

6N137	denotes Device Number
Y	denotes 1 digit Year code
WW	denotes 2 digit Week code
V	denotes VDE (optional)

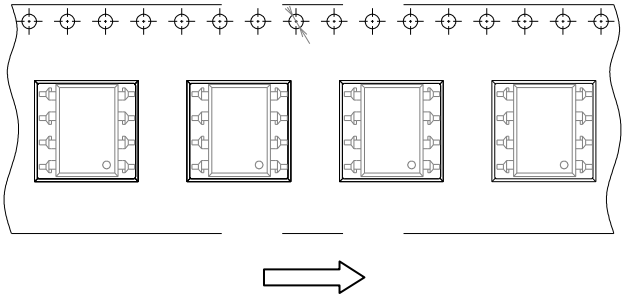
Tape & Reel Packing Specifications

Option TA



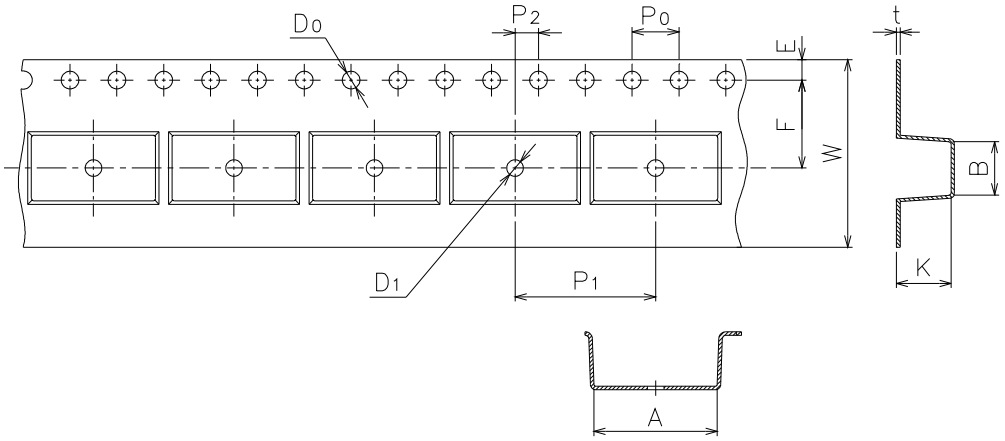
Direction of feed from reel

Option TB



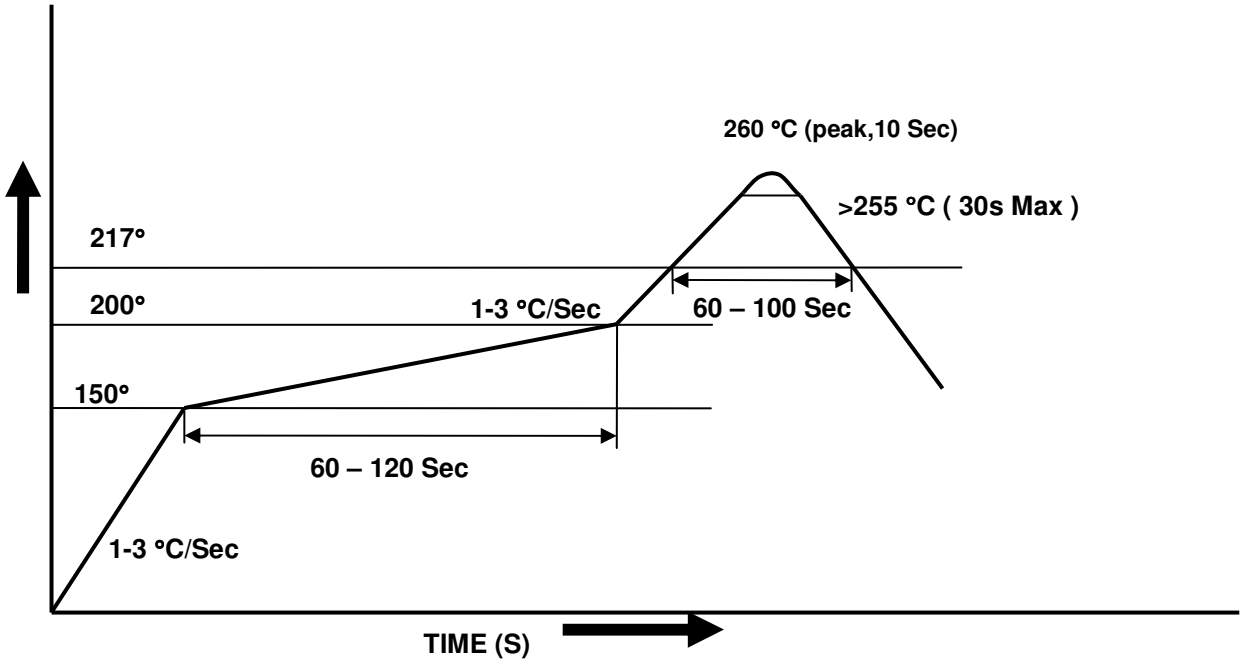
Direction of feed from reel

Tape dimensions



Dimension No.	A	B	Do	D1	E	F
Dimension(mm)	10.4±0.1	10.0±0.1	1.5±0.1	1.5±0.1	1.75±0.1	7.5±0.1
Dimension No.	Po	P1	P2	t	W	K
Dimension(mm)	4.0±0.1	12.0±0.1	2.0±0.1	0.4±0.1	16.0+0.3/ -0.1	4.5±0.1

Solder Reflow Temperature Profile



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