# EFM32 Happy Gecko Family
# EFM32HG Data Sheet

## The EFM32 Happy Gecko MCUs are the world's most energy-friendly microcontrollers.

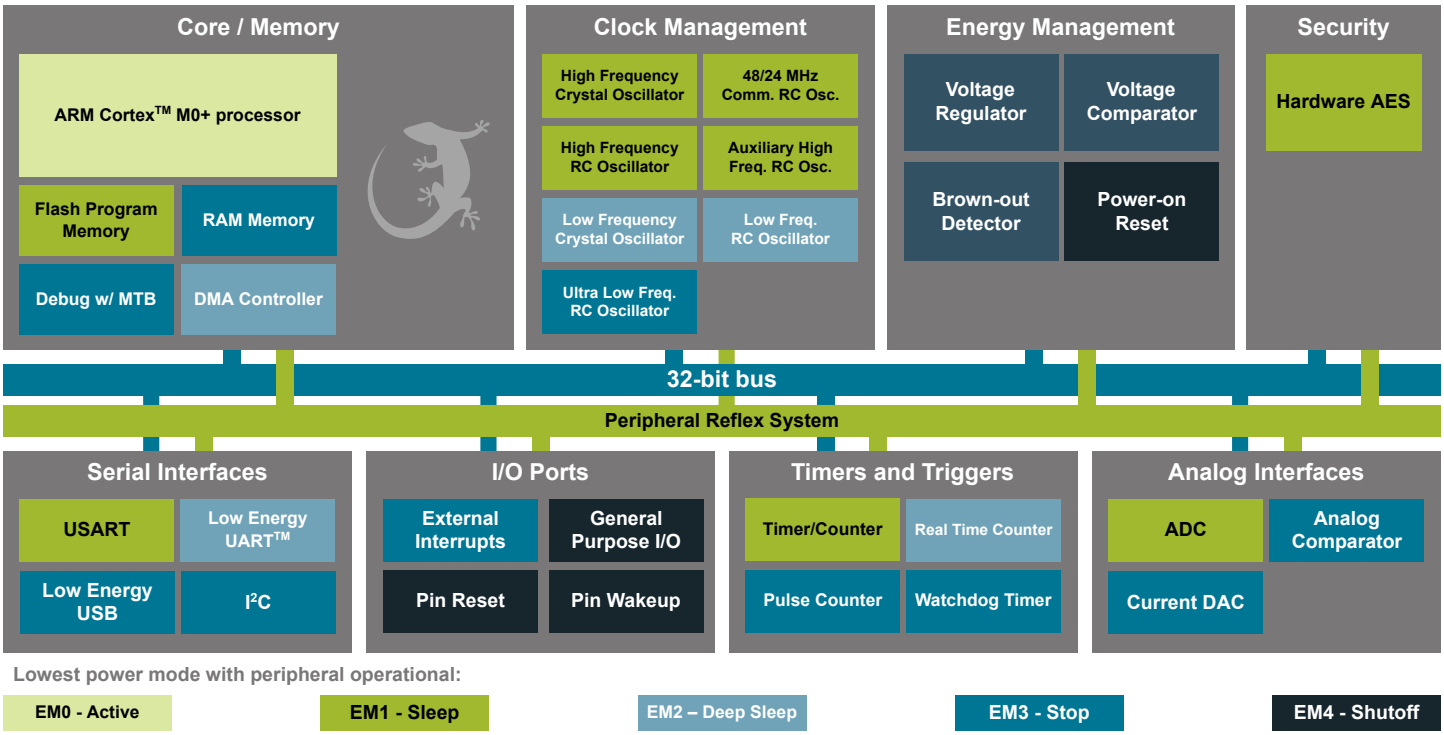
The EFM32HG offers unmatched performance and ultra low power consumption in both active and sleep modes. EFM32HG devices consume as little as 0.6 µA in Stop mode and 127 µA/MHz in Run mode. It also features autonomous peripherals, high overall chip and analog integration, and the performance of the industry standard 32-bit ARM Cortex-M0+ processor, making it perfect for battery-powered systems and systems with high-performance, low-energy requirements.

EFM32HG applications include the following:

- Energy, gas, water and smart metering
- Health and fitness applications
- Smart accessories
- Alarm and security systems
- Industrial and home automation

**KEY FEATURES**

- ARM Cortex-M0+ at 25 MHz
- Ultra low power operation
  - 0.6 µA current in Stop (EM3), with brown-out detection and RAM retention
  - 51 µA/MHz in EM1
  - 127 µA/MHz in Run mode (EM0)
- Fast wake-up time of 2 µs
- Hardware cryptography (AES)
- Up to 64 kB of Flash and 8 kB of RAM



# 1. Feature List

- ARM Cortex-M0+ CPU platform
  - High Performance 32-bit processor @ up to 25 MHz
  - Wake-up Interrupt Controller
  - SysTick System Timer
- Flexible Energy Management System
  - 20 nA @ 3 V Shutoff Mode
  - 0.6 µA @ 3 V Stop Mode, including Power-on Reset, Brown-out Detector, RAM and CPU retention
  - 0.9 µA @ 3 V Deep Sleep Mode, including RTC with 32.768 kHz oscillator, Power-on Reset, Brown-out Detector, RAM and CPU retention
  - 51 µA/MHz @ 3 V Sleep Mode
  - 127 µA/MHz @ 3 V Run Mode, with code executed from flash
- 64/32 kB Flash
- 8/4 kB RAM
- Up to 37 General Purpose I/O pins
  - Configurable push-pull, open-drain, pull-up/down, input filter, drive strength
  - Configurable peripheral I/O locations
  - Up to 16 asynchronous external interrupts
  - Output state retention and wake-up from Shutoff Mode
- 6 Channel DMA Controller
- 6 Channel Peripheral Reflex System (PRS) for autonomous inter-peripheral signaling
- Hardware AES with 128-bit keys in 54 cycles
- Timers/Counters
  - 3× 16-bit Timer/Counter
    - 3×3 Compare/Capture/PWM channels
    - Dead-Time Insertion on TIMER0
  - 1× 24-bit Real-Time Counter
  - 1× 16-bit Pulse Counter
  - Watchdog Timer with dedicated RC oscillator @ 50 nA
- Communication interfaces
  - Up to 2× Universal Synchronous/Asynchronous Receiver/Transmitter
    - UART/SPI/SmartCard (ISO 7816)/IrDA/I2S
    - Triple buffered full/half-duplex operation
  - Low Energy UART
    - Autonomous operation with DMA in Deep Sleep Mode
  - $I^2C$ Interface with SMBus support
    - Address recognition in Stop Mode
  - Low Energy Universal Serial Bus (USB) Device
    - Fully USB 2.0 compliant
    - On-chip PHY and embedded 5V to 3.3V regulator
    - Crystal-free operation
- Ultra low power precision analog peripherals
  - 12-bit 1 Msamples/s Analog-to-Digital Converter
    - 4 single-ended channels/2 differential channels
    - On-chip temperature sensor
  - Current Digital-to-Analog Converter
    - Selectable current range between 0.05 and 64 µA
  - 1× Analog Comparator
    - Capacitive sensing with up to 5 inputs
  - Supply Voltage Comparator
- Ultra efficient Power-on Reset and Brown-Out Detector

- Debug Interface
  - 2-pin Serial Wire Debug interface
  - Micro Trace Buffer (MTB)
- Pre-Programmed USB/UART Bootloader
- Temperature range -40 to 85 ºC (EFM32HGxxxFxx) or -40 to 105 ºC (EFM32HGxxxFxxN)
- Single power supply 1.98 to 3.8 V
- Packages:
  - CSP36 (3×3 mm)
  - QFN24 (5×5 mm)
  - QFN32 (6×6 mm)
  - TQFP48 (7×7 mm)

## 2. Ordering Information

The following table shows the available EFM32HG devices.

**Table 2.1. Ordering Information**

| Ordering Code | Flash (kB) | RAM (kB) | Max Speed (MHz) | Supply Voltage (V) | Temperature (ºC) | Package |
|---|---|---|---|---|---|---|
| EFM32HG108F32-C-QFN24 | 32 | 4 | 25 | 1.98 - 3.8 | -40 - 85 | QFN24 |
| EFM32HG108F64-C-QFN24 | 64 | 8 | 25 | 1.98 - 3.8 | -40 - 85 | QFN24 |
| EFM32HG110F32-C-QFN24 | 32 | 4 | 25 | 1.98 - 3.8 | -40 - 85 | QFN24 |
| EFM32HG110F64-C-QFN24 | 64 | 8 | 25 | 1.98 - 3.8 | -40 - 85 | QFN24 |
| EFM32HG210F32-C-QFN32 | 32 | 4 | 25 | 1.98 - 3.8 | -40 - 85 | QFN32 |
| EFM32HG210F64-C-QFN32 | 64 | 8 | 25 | 1.98 - 3.8 | -40 - 85 | QFN32 |
| EFM32HG222F32-C-QFP48 | 32 | 4 | 25 | 1.98 - 3.8 | -40 - 85 | TQFP48 |
| EFM32HG222F64-C-QFP48 | 64 | 8 | 25 | 1.98 - 3.8 | -40 - 85 | TQFP48 |
| EFM32HG308F32-C-QFN24 | 32 | 8 | 25 | 1.98 - 3.8 | -40 - 85 | QFN24 |
| EFM32HG308F64-C-QFN24 | 64 | 8 | 25 | 1.98 - 3.8 | -40 - 85 | QFN24 |
| EFM32HG309F32-C-QFN24 | 32 | 8 | 25 | 1.98 - 3.8 | -40 - 85 | QFN24 |
| EFM32HG309F64-C-QFN24 | 64 | 8 | 25 | 1.98 - 3.8 | -40 - 85 | QFN24 |
| EFM32HG310F32-C-QFN32 | 32 | 8 | 25 | 1.98 - 3.8 | -40 - 85 | QFN32 |
| EFM32HG310F64-C-QFN32 | 64 | 8 | 25 | 1.98 - 3.8 | -40 - 85 | QFN32 |
| EFM32HG321F32-C-QFP48 | 32 | 8 | 25 | 1.98 - 3.8 | -40 - 85 | TQFP48 |
| EFM32HG321F64-C-QFP48 | 64 | 8 | 25 | 1.98 - 3.8 | -40 - 85 | TQFP48 |
| EFM32HG322F32-C-QFP48 | 32 | 8 | 25 | 1.98 - 3.8 | -40 - 85 | TQFP48 |
| EFM32HG322F64-C-QFP48 | 64 | 8 | 25 | 1.98 - 3.8 | -40 - 85 | TQFP48 |
| EFM32HG350F32-C-CSP36 | 32 | 8 | 25 | 1.98 - 3.8 | -40 - 85 | CSP36 |
| EFM32HG350F64-C-CSP36 | 64 | 8 | 25 | 1.98 - 3.8 | -40 - 85 | CSP36 |
| EFM32HG108F32N-C-QFN24 | 32 | 4 | 25 | 1.98 - 3.8 | -40 - 105 | QFN24 |
| EFM32HG108F64N-C-QFN24 | 64 | 8 | 25 | 1.98 - 3.8 | -40 - 105 | QFN24 |
| EFM32HG110F32N-C-QFN24 | 32 | 4 | 25 | 1.98 - 3.8 | -40 - 105 | QFN24 |
| EFM32HG110F64N-C-QFN24 | 64 | 8 | 25 | 1.98 - 3.8 | -40 - 105 | QFN24 |
| EFM32HG210F32N-C-QFN32 | 32 | 4 | 25 | 1.98 - 3.8 | -40 - 105 | QFN32 |
| EFM32HG210F64N-C-QFN32 | 64 | 8 | 25 | 1.98 - 3.8 | -40 - 105 | QFN32 |
| EFM32HG222F32N-C-QFP48 | 32 | 4 | 25 | 1.98 - 3.8 | -40 - 105 | TQFP48 |
| EFM32HG222F64N-C-QFP48 | 64 | 8 | 25 | 1.98 - 3.8 | -40 - 105 | TQFP48 |
| EFM32HG308F32N-C-QFN24 | 32 | 8 | 25 | 1.98 - 3.8 | -40 - 105 | QFN24 |
| EFM32HG308F64N-C-QFN24 | 64 | 8 | 25 | 1.98 - 3.8 | -40 - 105 | QFN24 |
| EFM32HG309F32N-C-QFN24 | 32 | 8 | 25 | 1.98 - 3.8 | -40 - 105 | QFN24 |
| EFM32HG309F64N-C-QFN24 | 64 | 8 | 25 | 1.98 - 3.8 | -40 - 105 | QFN24 |

| Ordering Code | Flash (kB) | RAM (kB) | Max Speed (MHz) | Supply Voltage (V) | Temperature (ºC) | Package |
|---|---|---|---|---|---|---|
| EFM32HG310F32N-C-QFN32 | 32 | 8 | 25 | 1.98 - 3.8 | -40 - 105 | QFN32 |
| EFM32HG310F64N-C-QFN32 | 64 | 8 | 25 | 1.98 - 3.8 | -40 - 105 | QFN32 |
| EFM32HG321F32N-C-QFP48 | 32 | 8 | 25 | 1.98 - 3.8 | -40 - 105 | TQFP48 |
| EFM32HG321F64N-C-QFP48 | 64 | 8 | 25 | 1.98 - 3.8 | -40 - 105 | TQFP48 |
| EFM32HG322F32N-C-QFP48 | 32 | 8 | 25 | 1.98 - 3.8 | -40 - 105 | TQFP48 |
| EFM32HG322F64N-C-QFP48 | 64 | 8 | 25 | 1.98 - 3.8 | -40 - 105 | TQFP48 |

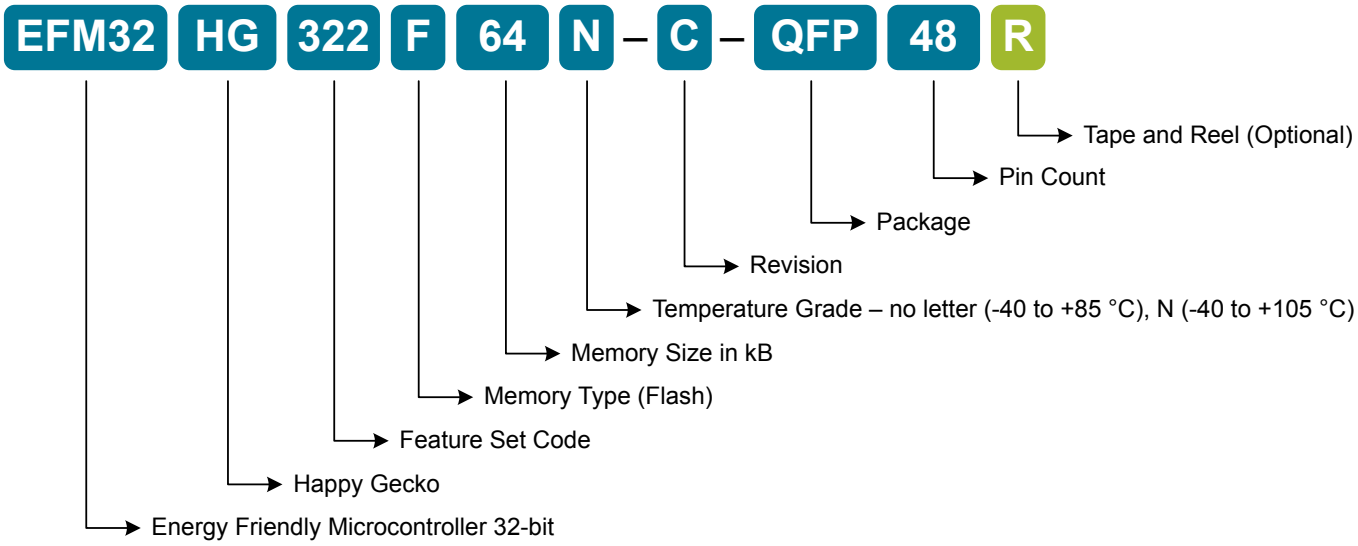



**Figure 2.1. Ordering Code Decoder**

Adding the suffix 'R' to the part number (e.g. EFM32HG322F64-C-QFP48R) denotes tape and reel.

Adding 'N' after the memory size (e.g. EFM32HG322F64N-C-QFP48) denotes -40 to +105 ºC temperature grade.

Visit http://www.silabs.com for information on global distributors and representatives.

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# 3. System Summary

## 3.1 System Introduction

The EFM32 MCUs are the world's most energy friendly microcontrollers. With a unique combination of the powerful 32-bit ARM Cortex-M0+, innovative low energy techniques, short wake-up time from energy saving modes, and a wide selection of peripherals, the EFM32HG microcontroller is well suited for any battery operated application as well as other systems requiring high performance and low-energy consumption. This section gives a short introduction to each of the modules in general terms and also shows a summary of the configuration for the EFM32HG devices. For a complete feature set and in-depth information on the modules, the reader is referred to the EFM32HG Reference Manual.

A block diagram of the EFM32HG is shown in the following figure.

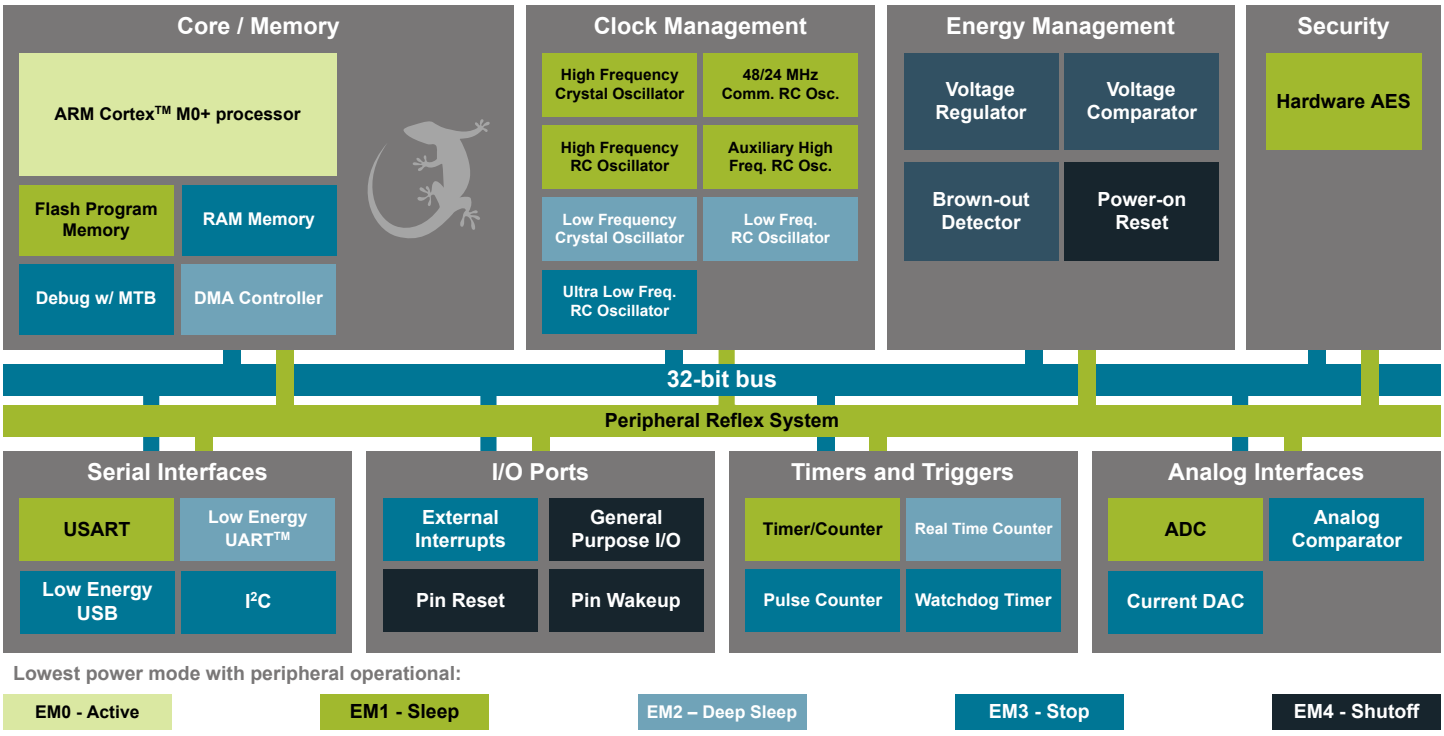



**Figure 3.1. Block Diagram**

### 3.1.1 ARM Cortex-M0+ Core

The ARM Cortex-M0+ includes a 32-bit RISC processor which can achieve as much as 0.9 Dhrystone MIPS/MHz. A wake-up Interrupt Controller handling interrupts triggered while the CPU is asleep is included as well. The EFM32 implementation of the Cortex-M0+ is described in detail in *ARM Cortex-M0+ Devices Generic User Guide*.

### 3.1.2 Debug Interface (DBG)

This device includes hardware debug support through a 2-pin serial-wire debug interface and a Micro Trace Buffer (MTB) for data/instruction tracing.

### 3.1.3 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the EFM32HG microcontroller. The flash memory is readable and writable from both the Cortex-M0+ and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block. Additionally, the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in the energy modes EM0 and EM1.

### 3.1.4 Direct Memory Access Controller (DMA)

The Direct Memory Access (DMA) controller performs memory operations independently of the CPU. This has the benefit of reducing the energy consumption and the workload of the CPU, and enables the system to stay in low energy modes when moving for instance data from the USART to RAM or from the External Bus Interface to a PWM-generating timer. The DMA controller uses the PL230 µDMA controller licensed from ARM.

### 3.1.5 Reset Management Unit (RMU)

The RMU is responsible for handling the reset functionality of the EFM32HG.

### 3.1.6 Energy Management Unit (EMU)

The Energy Management Unit (EMU) manage all the low energy modes (EM) in EFM32HG microcontrollers. Each energy mode manages if the CPU and the various peripherals are available. The EMU can also be used to turn off the power to unused SRAM blocks.

### 3.1.7 Clock Management Unit (CMU)

The Clock Management Unit (CMU) is responsible for controlling the oscillators and clocks on-board the EFM32HG. The CMU provides the capability to turn on and off the clock on an individual basis to all peripheral modules in addition to enable/disable and configure the available oscillators. The high degree of flexibility enables software to minimize energy consumption in any specific application by not wasting power on peripherals and oscillators that are inactive.

### 3.1.8 Watchdog (WDOG)

The purpose of the watchdog timer is to generate a reset in case of a system failure, to increase application reliability. The failure may e.g. be caused by an external event, such as an ESD pulse, or by a software failure.

### 3.1.9 Peripheral Reflex System (PRS)

The Peripheral Reflex System (PRS) system is a network which lets the different peripheral module communicate directly with each other without involving the CPU. Peripheral modules which send out Reflex signals are called producers. The PRS routes these reflex signals to consumer peripherals which apply actions depending on the data received. The format for the Reflex signals is not given, but edge triggers and other functionality can be applied by the PRS.

### 3.1.10 Low Energy USB

The unique Low Energy USB peripheral provides a full-speed USB 2.0 compliant device controller and PHY with ultra-low current consumption. The device supports both full-speed (12 MBit/s) and low speed (1.5 MBit/s) operation, and includes a dedicated USB oscillator with clock recovery mechanism for crystal-free operation. No external components are required. The Low Energy Mode ensures the current consumption is optimized and enables USB communication on a strict power budget. The USB device includes an internal dedicated descriptor-based Scatter/Gather DMA and supports up to 3 OUT endpoints and 3 IN endpoints, in addition to endpoint 0. The on-chip PHY includes software controllable pull-up and pull-down resistors.

### 3.1.11 Inter-Integrated Circuit Interface (I2C)

The $I^2C$ module provides an interface between the MCU and a serial $I^2C$-bus. It is capable of acting as both a master and a slave, and supports multi-master buses. Both standard-mode, fast-mode and fastmode plus speeds are supported, allowing transmission rates all the way from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also provided to allow implementation of an SMBus compliant system. The interface provided to software by the $I^2C$ module, allows both fine-grained control of the transmission process and close to automatic transfers. Automatic recognition of slave addresses is provided in all energy modes.

### 3.1.12 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous Asynchronous serial Receiver and Transmitter (USART) is a very flexible serial I/O module. It supports full duplex asynchronous UART communication as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with ISO7816 SmartCards, IrDA and I2S devices.

### 3.1.13 Pre-Programmed USB/UART Bootloader

The bootloader presented in application note AN0042 is pre-programmed in the device at factory. The bootloader enables users to program the EFM32 through a UART or a USB CDC class virtual UART without the need for a debugger. The autobaud feature, interface and commands are described further in the application note.

### 3.1.14 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART™, the Low Energy UART, is a UART that allows two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud/ s. The LEUART includes all necessary hardware support to make asynchronous serial communication possible with minimum of software intervention and energy consumption.

### 3.1.15 Timer/Counter (TIMER)

The 16-bit general purpose Timer has 3 compare/capture channels for input capture and compare/Pulse- Width Modulation (PWM) output. TIMER0 also includes a Dead-Time Insertion module suitable for motor control applications.

### 3.1.16 Real Time Counter (RTC)

The Real Time Counter (RTC) contains a 24-bit counter and is clocked either by a 32.768 kHz crystal oscillator, or a 32.768 kHz RC oscillator. In addition to energy modes EM0 and EM1, the RTC is also available in EM2. This makes it ideal for keeping track of time since the RTC is enabled in EM2 where most of the device is powered down.

### 3.1.17 Pulse Counter (PCNT)

The Pulse Counter (PCNT) can be used for counting pulses on a single input or to decode quadrature encoded inputs. It runs off either the internal LFACLK or the PCNTn_S0IN pin as external clock source. The module may operate in energy mode EM0 - EM3.

### 3.1.18 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs can either be one of the selectable internal references or from external pins. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

### 3.1.19 Voltage Comparator (VCMP)

The Voltage Supply Comparator is used to monitor the supply voltage from software. An interrupt can be generated when the supply falls below or rises above a programmable threshold. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

### 3.1.20 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to one million samples per second. The integrated input mux can select inputs from 4 external pins and 6 internal signals.

### 3.1.21 Current Digital to Analog Converter (IDAC)

The current digital to analog converter can source or sink a configurable constant current, which can be output on, or sinked from pin or ADC. The current is configurable with several ranges of various step sizes.

### 3.1.22 Advanced Encryption Standard Accelerator (AES)

The AES accelerator performs AES encryption and decryption with 128-bit. Encrypting or decrypting one 128-bit data block takes 52 HFCORECLK cycles with 128-bit keys. The AES module is an AHB slave which enables efficient access to the data and key registers. All write accesses to the AES module must be 32-bit operations, i.e. 8- or 16-bit operations are not supported.

### 3.1.23 General Purpose Input/Output (GPIO)

In the EFM32HG, there are up to 37 General Purpose Input/Output (GPIO) pins, which are divided into ports with up to 16 pins each. These pins can individually be configured as either an output or input. More advanced configurations like open-drain, filtering and drive strength can also be configured individually for the pins. The GPIO pins can also be overridden by peripheral pin connections, like Timer PWM outputs or USART communication, which can be routed to several locations on the device. The GPIO supports up to 16 asynchronous external pin interrupts, which enables interrupts from any pin on the device. Also, the input value of a pin can be routed through the Peripheral Reflex System to other peripherals.

## 3.2 Configuration Summary

### 3.2.1 EFM32HG108

The features of the EFM32HG108 is a subset of the feature set described in the EFM32HG Reference Manual. The following table describes device specific implementation of the features.

**Table 3.1. EFM32HG108 Configuration Summary**

| Module | Configuration | Pin Connections |
|---|---|---|
| Cortex-M0+ | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| USART0 | Full configuration with IrDA and I2S | US0_TX, US0_RX. US0_CLK, US0_CS |
| USART1 | Full configuration with IrDA and I2S | US1_TX, US1_RX, US1_CLK, US1_CS |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| TIMER2 | Full configuration | TIM2_CC[2:0] |
| RTC | Full configuration | NA |
| PCNT0 | Full configuration, 16-bit count register | PCNT0_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[1:0], ACMP0_O |
| VCMP | Full configuration | NA |
| GPIO | 17 pins | Available pins are shown in 5.1.3 GPIO Pinout Overview |

### 3.2.2 EFM32HG110

The features of the EFM32HG110 is a subset of the feature set described in the EFM32HG Reference Manual. The following table describes device specific implementation of the features.

**Table 3.2. EFM32HG110 Configuration Summary**

| Module | Configuration | Pin Connections |
|---|---|---|
| Cortex-M0+ | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| USART0 | Full configuration with IrDA and I2S | US0_TX, US0_RX. US0_CLK, US0_CS |
| USART1 | Full configuration with IrDA and I2S | US1_TX, US1_RX, US1_CLK, US1_CS |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| TIMER2 | Full configuration | TIM2_CC[2:0] |
| RTC | Full configuration | NA |
| PCNT0 | Full configuration, 16-bit count register | PCNT0_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[1:0], ACMP0_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:6], ADC0_CH[1:0] |
| IDAC0 | Full configuration | IDAC0_OUT |
| AES | Full configuration | NA |
| GPIO | 17 pins | Available pins are shown in 5.2.3 GPIO Pinout Overview |

### 3.2.3 EFM32HG210

The features of the EFM32HG210 is a subset of the feature set described in the EFM32HG Reference Manual. The following table describes device specific implementation of the features.

**Table 3.3. EFM32HG210 Configuration Summary**

| Module | Configuration | Pin Connections |
|---|---|---|
| Cortex-M0+ | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| USART0 | Full configuration with IrDA and I2S | US0_TX, US0_RX. US0_CLK, US0_CS |
| USART1 | Full configuration with IrDA and I2S | US1_TX, US1_RX, US1_CLK, US1_CS |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| TIMER2 | Full configuration | TIM2_CC[2:0] |
| RTC | Full configuration | NA |
| PCNT0 | Full configuration, 16-bit count register | PCNT0_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[1:0], ACMP0_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:4], ADC0_CH[1:0] |
| IDAC0 | Full configuration | IDAC0_OUT |
| AES | Full configuration | NA |
| GPIO | 24 pins | Available pins are shown in 5.3.3 GPIO Pinout Overview |

### 3.2.4 EFM32HG222

The features of the EFM32HG222 is a subset of the feature set described in the EFM32HG Reference Manual. The following table describes device specific implementation of the features.

**Table 3.4. EFM32HG222 Configuration Summary**

| Module | Configuration | Pin Connections |
|---|---|---|
| Cortex-M0+ | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| USART0 | Full configuration with IrDA and I2S | US0_TX, US0_RX. US0_CLK, US0_CS |
| USART1 | Full configuration with IrDA and I2S | US1_TX, US1_RX, US1_CLK, US1_CS |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| TIMER2 | Full configuration | TIM2_CC[2:0] |
| RTC | Full configuration | NA |
| PCNT0 | Full configuration, 16-bit count register | PCNT0_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[4:0], ACMP0_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:4], ADC0_CH[1:0] |
| IDAC0 | Full configuration | IDAC0_OUT |
| AES | Full configuration | NA |
| GPIO | 37 pins | Available pins are shown in 5.4.3 GPIO Pinout Overview |

### 3.2.5 EFM32HG308

The features of the EFM32HG308 is a subset of the feature set described in the EFM32HG Reference Manual. The following table describes device specific implementation of the features.

**Table 3.5. EFM32HG308 Configuration Summary**

| Module | Configuration | Pin Connections |
|---|---|---|
| Cortex-M0+ | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| USB | Full configuration | USB_VREGI, USB_VREGO, USB_DM, USB_DMPU, USB_DP |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| USART0 | Full configuration with IrDA and I2S | US0_TX, US0_RX. US0_CLK, US0_CS |
| USART1 | Full configuration with IrDA and I2S | US1_TX, US1_RX, US1_CLK, US1_CS |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| TIMER2 | Full configuration | TIM2_CC[2:0] |
| RTC | Full configuration | NA |
| PCNT0 | Full configuration, 16-bit count register | PCNT0_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[1:0], ACMP0_O |
| VCMP | Full configuration | NA |
| GPIO | 15 pins | Available pins are shown in 5.5.3 GPIO Pinout Overview |

### 3.2.6 EFM32HG309

The features of the EFM32HG309 is a subset of the feature set described in the EFM32HG Reference Manual. The following table describes device specific implementation of the features.

**Table 3.6. EFM32HG309 Configuration Summary**

| Module | Configuration | Pin Connections |
|---|---|---|
| Cortex-M0+ | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| USB | Full configuration | USB_VREGI, USB_VREGO, USB_DM, USB_DMPU, USB_DP |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| USART0 | Full configuration with IrDA and I2S | US0_TX, US0_RX. US0_CLK, US0_CS |
| USART1 | Full configuration with IrDA and I2S | US1_TX, US1_RX, US1_CLK, US1_CS |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| TIMER2 | Full configuration | TIM2_CC[2:0] |
| RTC | Full configuration | NA |
| PCNT0 | Full configuration, 16-bit count register | PCNT0_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[1:0], ACMP0_O |
| VCMP | Full configuration | ADC0_CH[1:0] |
| ADC0 | Full configuration | ADC0_CH[9:8] |
| IDAC0 | Full configuration | IDAC0_OUT |
| AES | Full configuration | NA |
| GPIO | 15 pins | Available pins are shown in 5.6.3 GPIO Pinout Overview |

### 3.2.7 EFM32HG310

The features of the EFM32HG310 is a subset of the feature set described in the EFM32HG Reference Manual. The following table describes device specific implementation of the features.

**Table 3.7. EFM32HG310 Configuration Summary**

| Module | Configuration | Pin Connections |
|---|---|---|
| Cortex-M0+ | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| USB | Full configuration | USB_VREGI, USB_VREGO, USB_DM, USB_DMPU, USB_DP |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| USART0 | Full configuration with IrDA and I2S | US0_TX, US0_RX. US0_CLK, US0_CS |
| USART1 | Full configuration with IrDA and I2S | US1_TX, US1_RX, US1_CLK, US1_CS |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| TIMER2 | Full configuration | TIM2_CC[2:0] |
| RTC | Full configuration | NA |
| PCNT0 | Full configuration, 16-bit count register | PCNT0_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[1:0], ACMP0_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:5], ADC0_CH[1:0] |
| IDAC0 | Full configuration | IDAC0_OUT |
| AES | Full configuration | NA |
| GPIO | 22 pins | Available pins are shown in 5.7.3 GPIO Pinout Overview |

### 3.2.8 EFM32HG321

The features of the EFM32HG321 is a subset of the feature set described in the EFM32HG Reference Manual. The following table describes device specific implementation of the features.

**Table 3.8. EFM32HG321 Configuration Summary**

| Module | Configuration | Pin Connections |
|---|---|---|
| Cortex-M0+ | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| USB | Full configuration | USB_VREGI, USB_VREGO, USB_DM, USB_DMPU, USB_DP |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| USART0 | Full configuration with IrDA and I2S | US0_TX, US0_RX. US0_CLK, US0_CS |
| USART1 | Full configuration with IrDA and I2S | US1_TX, US1_RX, US1_CLK, US1_CS |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| TIMER2 | Full configuration | TIM2_CC[2:0] |
| RTC | Full configuration | NA |
| PCNT0 | Full configuration, 16-bit count register | PCNT0_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[4:0], ACMP0_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:4], ADC0_CH[1:0] |
| IDAC0 | Full configuration | IDAC0_OUT |
| GPIO | 35 pins | Available pins are shown in 5.8.3 GPIO Pinout Overview |

### 3.2.9 EFM32HG322

The features of the EFM32HG322 is a subset of the feature set described in the EFM32HG Reference Manual. The following table describes device specific implementation of the features.

**Table 3.9. EFM32HG322 Configuration Summary**

| Module | Configuration | Pin Connections |
|---|---|---|
| Cortex-M0+ | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| USB | Full configuration | USB_VREGI, USB_VREGO, USB_DM, USB_DMPU, USB_DP |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| USART0 | Full configuration with IrDA and I2S | US0_TX, US0_RX. US0_CLK, US0_CS |
| USART1 | Full configuration with IrDA and I2S | US1_TX, US1_RX, US1_CLK, US1_CS |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| TIMER2 | Full configuration | TIM2_CC[2:0] |
| RTC | Full configuration | NA |
| PCNT0 | Full configuration, 16-bit count register | PCNT0_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[4:0], ACMP0_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:4], ADC0_CH[1:0] |
| IDAC0 | Full configuration | IDAC0_OUT |
| AES | Full configuration | NA |
| GPIO | 35 pins | Available pins are shown in 5.9.3 GPIO Pinout Overview |

### 3.2.10 EFM32HG350

The features of the EFM32HG350 is a subset of the feature set described in the EFM32HG Reference Manual. The following table describes device specific implementation of the features.

**Table 3.10. EFM32HG350 Configuration Summary**

| Module | Configuration | Pin Connections |
|---|---|---|
| Cortex-M0+ | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| USB | Full configuration | USB_VREGI, USB_VREGO, USB_DM, USB_DMPU, USB_DP |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| USART0 | Full configuration with IrDA and I2S | US0_TX, US0_RX. US0_CLK, US0_CS |
| USART1 | Full configuration with IrDA and I2S | US1_TX, US1_RX, US1_CLK, US1_CS |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| TIMER2 | Full configuration | TIM2_CC[2:0] |
| RTC | Full configuration | NA |
| PCNT0 | Full configuration, 16-bit count register | PCNT0_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[1:0], ACMP0_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:5], ADC0_CH[1:0] |
| IDAC0 | Full configuration | IDAC0_OUT |
| AES | Full configuration | NA |
| GPIO | 22 pins | Available pins are shown in 5.10.3 GPIO Pinout Overview |

### 3.3 Memory Map

The EFM32HG memory map is shown in the following figure, with RAM and Flash sizes for the largest memory configuration.

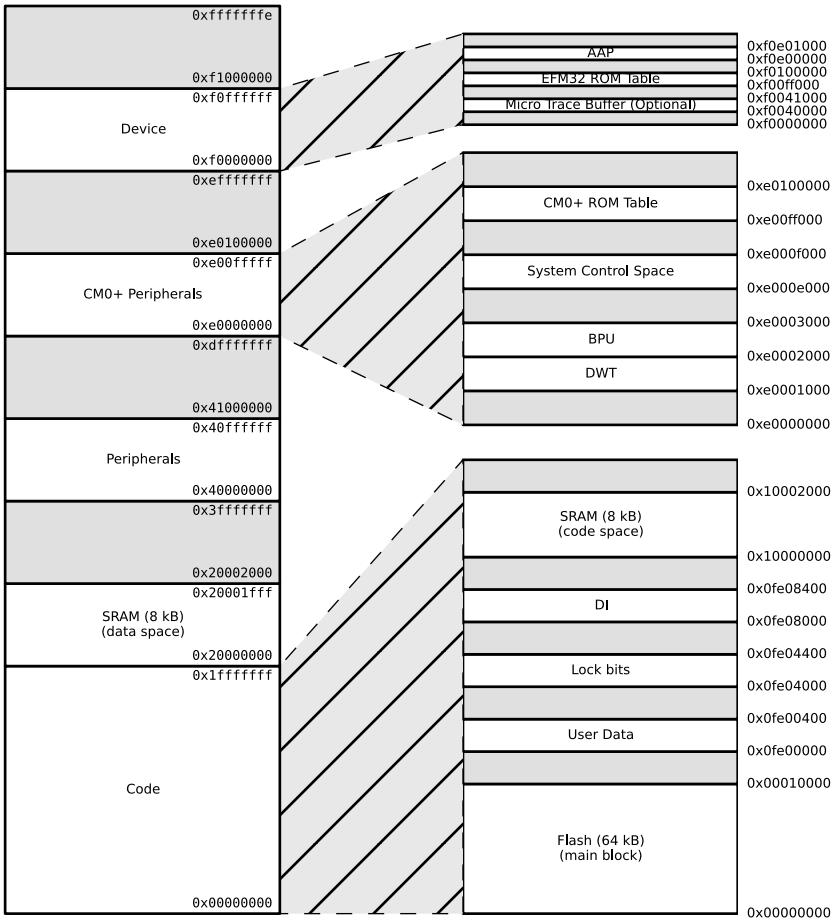



**Figure 3.2. System Address Space with Core and Code Space Listing**

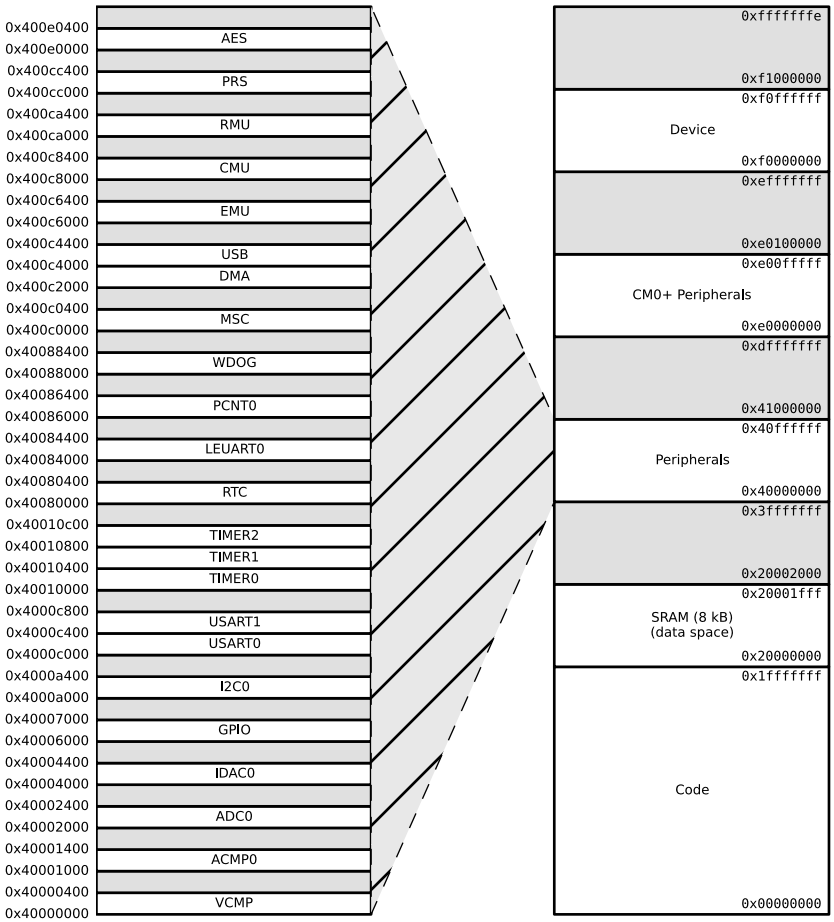



**Figure 3.3. System Address Space with Peripheral Listing**

# 4. Electrical Characteristics

## 4.1 Test Conditions

### 4.1.1 Typical Values

The typical data are based on $T_{AMB}$=25°C and $V_{DD}$=3.0 V, as defined in 4.3 General Operating Conditions, unless otherwise specified.

### 4.1.2 Minimum and Maximum Values

The minimum and maximum values represent the worst conditions of ambient temperature, supply voltage and frequencies, as defined in 4.3 General Operating Conditions, unless otherwise specified.

## 4.2 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings, and functional operation under such conditions are not guaranteed. Stress beyond the limits specified in the following table may affect the device reliability or cause permanent damage to the device. Functional operating conditions are given in 4.3 General Operating Conditions.

**Table 4.1. Absolute Maximum Ratings**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Storage temperature range | $T_{STG}$ | | -40 | — | 150 | °C |
| Maximum soldering temperature | $T_S$ | Latest IPC/JEDEC J-STD-020 Standard | — | — | 260 | °C |
| External main supply voltage | $V_{DDMAX}$ | | 0 | — | 3.8 | V |
| Voltage on any I/O pin | $V_{IOPIN}$ | | -0.3 | — | $V_{DD}$+0.3 | V |
| Current per I/O pin (sink) | $I_{IOMAX_SINK}$ | | — | — | 100 | mA |
| Current per I/O pin (source) | $I_{IOMAX_SOURCE}$ | | — | — | -100 | mA |

## 4.3 General Operating Conditions

**Table 4.2. General Operating Conditions**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Ambient temperature range (EFM32HGxxxFxx only) | $T_{AMB}$ | -40 | — | 85 | °C |
| Ambient temperature range (EFM32HGxxxFxxN only) | $T_{AMB}$ | -40 | — | 105 | °C |
| Operating supply voltage | $V_{DDOP}$ | 1.98 | — | 3.8 | V |
| Internal APB clock frequency | $f_{APB}$ | — | — | 25 | MHz |
| Internal AHB clock frequency | $f_{AHB}$ | — | — | 25 | MHz |

### 4.4 Thermal Characteristics

**Table 4.3. Thermal Characteristics**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Thermal resistance, Junction to Ambient | $\theta_{JA}$ | QFN24 Package, 4-Layer PCB, Air velocity = 0 m/s | — | 25.8 | — | °C/W |
| | | QFN32 Package, 4-Layer PCB, Air velocity = 0 m/s | — | 24.1 | — | °C/W |
| | | TQFP48 Package, 4-Layer PCB, Air velocity = 0 m/s | — | 60.0 | — | °C/W |
| Thermal resistance, Junction to Case | $\theta_{JC}$ | QFN24 Package, 4-Layer PCB, Air velocity = 0 m/s | — | 20.7 | — | °C/W |
| | | QFN32 Package, 4-Layer PCB, Air velocity = 0 m/s | — | 16.0 | — | °C/W |
| | | TQFP48 Package, 4-Layer PCB, Air velocity = 0 m/s | — | 15.0 | — | °C/W |

## 4.5 Current Consumption

**Table 4.4. Current Consumption**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| EM0 current. No prescaling. Running prime number calculation code from Flash. | $I_{EM0}$ | 24 MHz HFXO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | — | 148 | 158 | µA/MHz |
| | | 24 MHz HFXO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=105°C | — | 153 | 163 | µA/MHz |
| | | 24 MHz USHFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | — | 161 | 172 | µA/MHz |
| | | 24 MHz USHFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=105°C | — | 163 | 174 | µA/MHz |
| | | 24 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | — | 127 | 137 | µA/MHz |
| | | 24 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=105°C | — | 129 | 139 | µA/MHz |
| | | 21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | — | 131 | 140 | µA/MHz |
| | | 21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=105°C | — | 134 | 143 | µA/MHz |
| | | 14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | — | 134 | 143 | µA/MHz |
| | | 14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=105°C | — | 137 | 145 | µA/MHz |
| | | 11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | — | 136 | 144 | µA/MHz |
| | | 11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=105°C | — | 139 | 148 | µA/MHz |
| | | 6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | — | 142 | 150 | µA/MHz |
| | | 6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=105°C | — | 146 | 154 | µA/MHz |
| | | 1.2 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | — | 184 | 196 | µA/MHz |
| | | 1.2 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=105°C | — | 194 | 208 | µA/MHz |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| EM1 current | $I_{EM1}$ | 24 MHz HFXO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | — | 64 | 68 | µA/MHz |
| | | 24 MHz HFXO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=105°C | — | 67 | 71 | µA/MHz |
| | | 24 MHz USHFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | — | 85 | 91 | µA/MHz |
| | | 24 MHz USHFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=105°C | — | 86 | 92 | µA/MHz |
| | | 24 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | — | 51 | 55 | µA/MHz |
| | | 24 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=105°C | — | 52 | 56 | µA/MHz |
| | | 21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | — | 53 | 57 | µA/MHz |
| | | 21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=105°C | — | 54 | 58 | µA/MHz |
| | | 14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | — | 56 | 59 | µA/MHz |
| | | 14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=105°C | — | 57 | 61 | µA/MHz |
| | | 11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | — | 58 | 61 | µA/MHz |
| | | 11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=105°C | — | 59 | 63 | µA/MHz |
| | | 6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | — | 64 | 68 | µA/MHz |
| | | 6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=105°C | — | 67 | 71 | µA/MHz |
| | | 1.2 MHz HFRCO. all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | — | 106 | 114 | µA/MHz |
| | | 1.2 MHz HFRCO. all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=105°C | — | 114 | 126 | µA/MHz |
| EM2 current | $I_{EM2}$ | EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | — | 0.9 | 1.35 | µA |
| | | EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | — | 1.6 | 3.50 | µA |
| | | EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, $V_{DD}$= 3.0 V, $T_{AMB}$=105°C, EFM32HGxxxFxxN only | — | 1.6 | 8.00 | µA |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| EM3 current | $I_{EM3}$ | EM3 current (ULFRCO enabled, LFRCO/LFXO disabled), $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | — | 0.6 | 0.90 | µA |
| | | EM3 current (ULFRCO enabled, LFRCO/LFXO disabled), $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | — | 1.2 | 2.65 | µA |
| | | EM3 current (ULFRCO enabled, LFRCO/LFXO disabled), $V_{DD}$= 3.0 V, $T_{AMB}$=105°C, EFM32HGxxxFxxN only | — | 1.2 | 7.00 | µA |
| EM4 current | $I_{EM4}$ | $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | — | 0.02 | 0.035 | µA |
| | | $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | — | 0.18 | 0.480 | µA |
| | | $V_{DD}$= 3.0 V, $T_{AMB}$=105°C, EFM32HGxxxFxxN only | — | 0.18 | 1.500 | µA |

### 4.5.1 EM0 Current Consumption

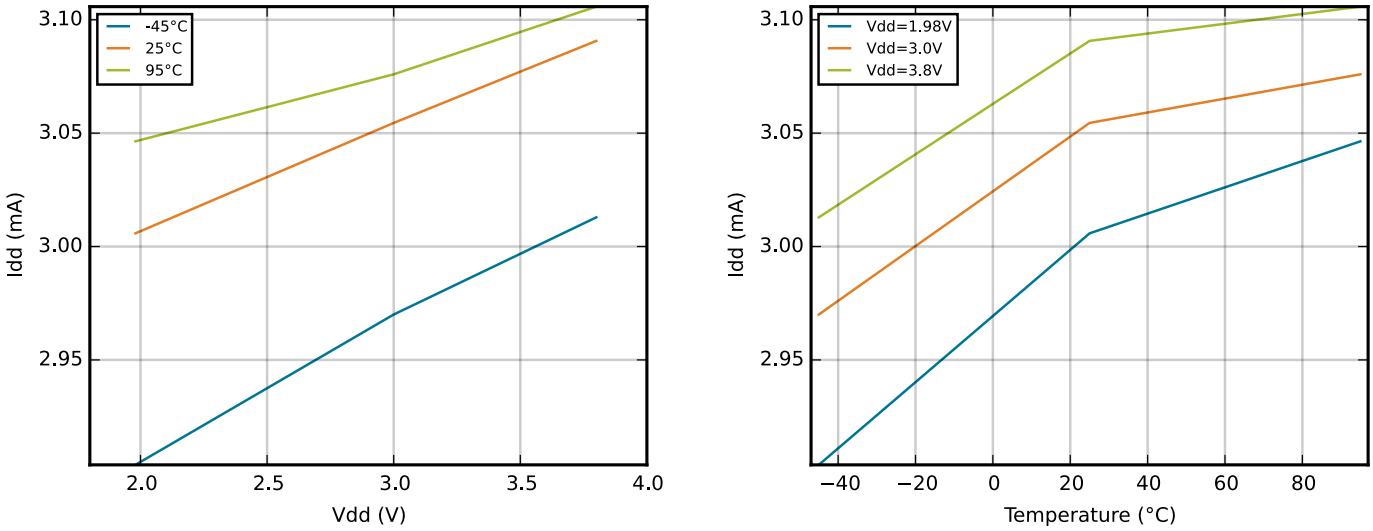



**Figure 4.1. EM0 Current Consumption while Executing Prime Number Calculation Code from Flash with all Peripheral Clocks Disabled and HFRCO Running at 24 MHz**

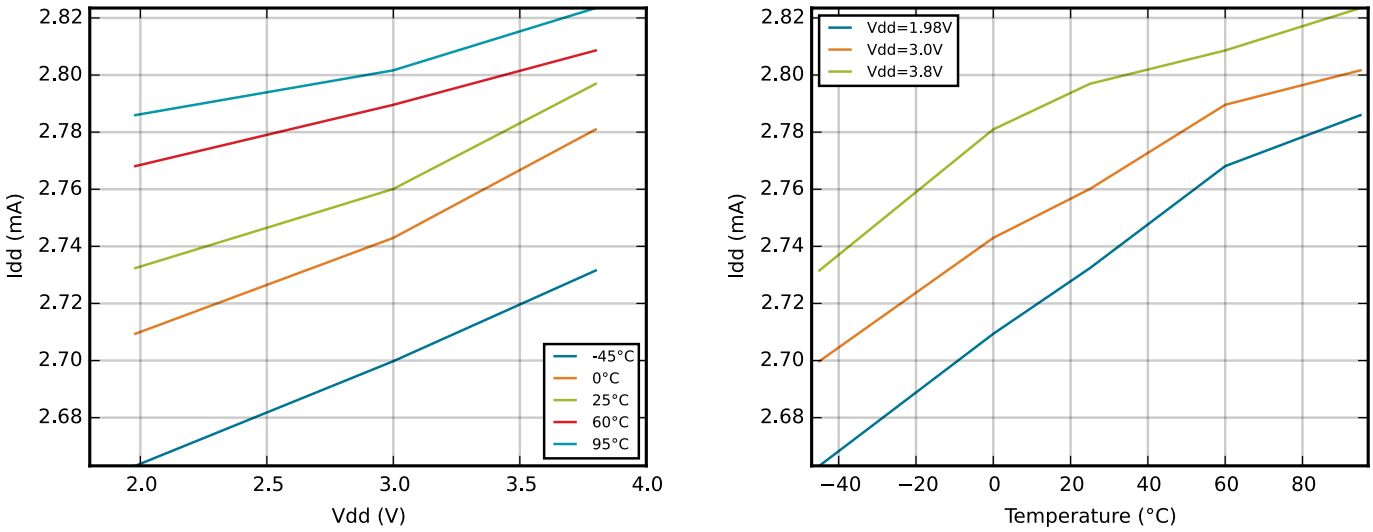



**Figure 4.2. EM0 Current Consumption while Executing Prime Number Calculation Code from Flash with all Peripheral Clocks Disabled and HFRCO Running at 21 MHz**

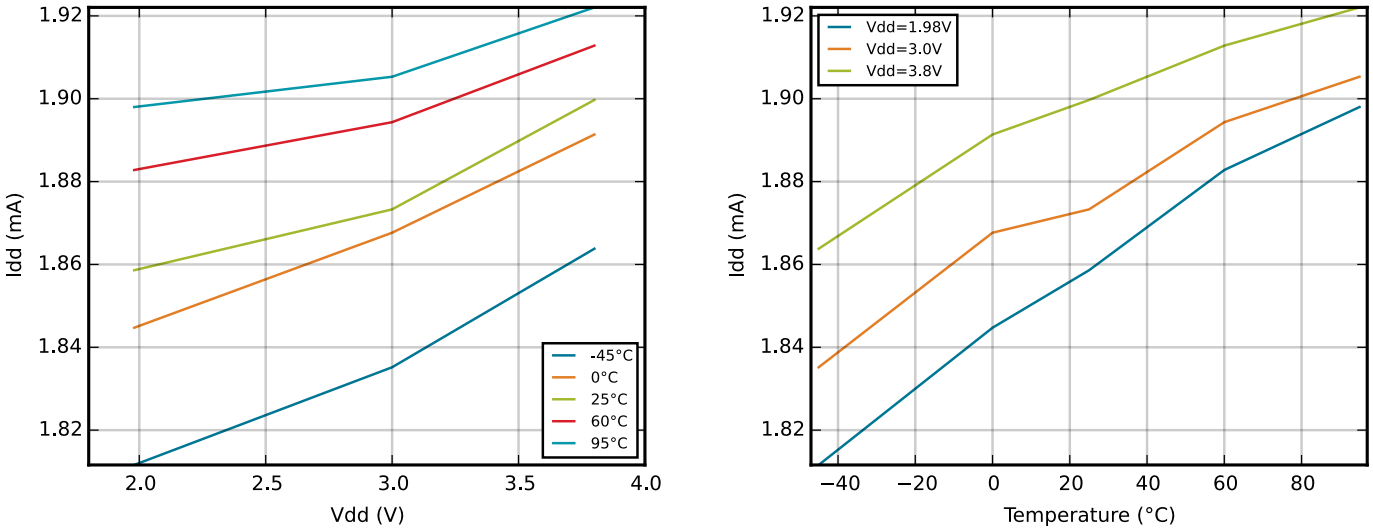



**Figure 4.3. EM0 Current Consumption while Executing Prime Number Calculation Code from Flash with all Peripheral Clocks Disabled and HFRCO Running at 14 MHz**

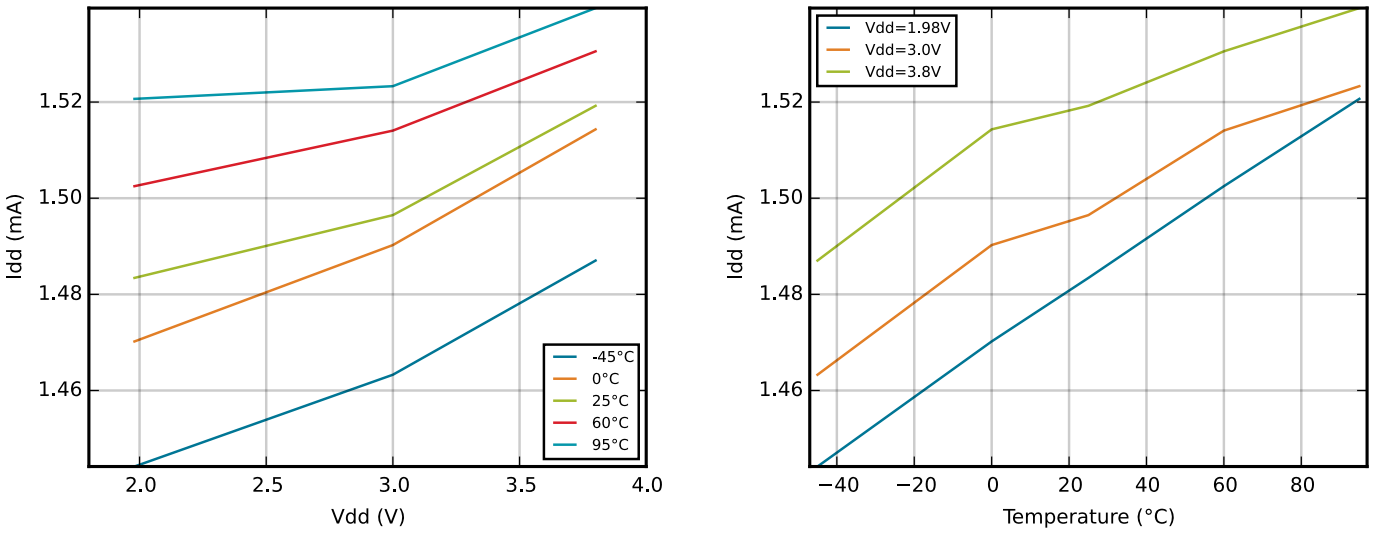



**Figure 4.4. EM0 Current Consumption while Executing Prime Number Calculation Code from Flash with all Peripheral Clocks Disabled and HFRCO Running at 11 MHz**

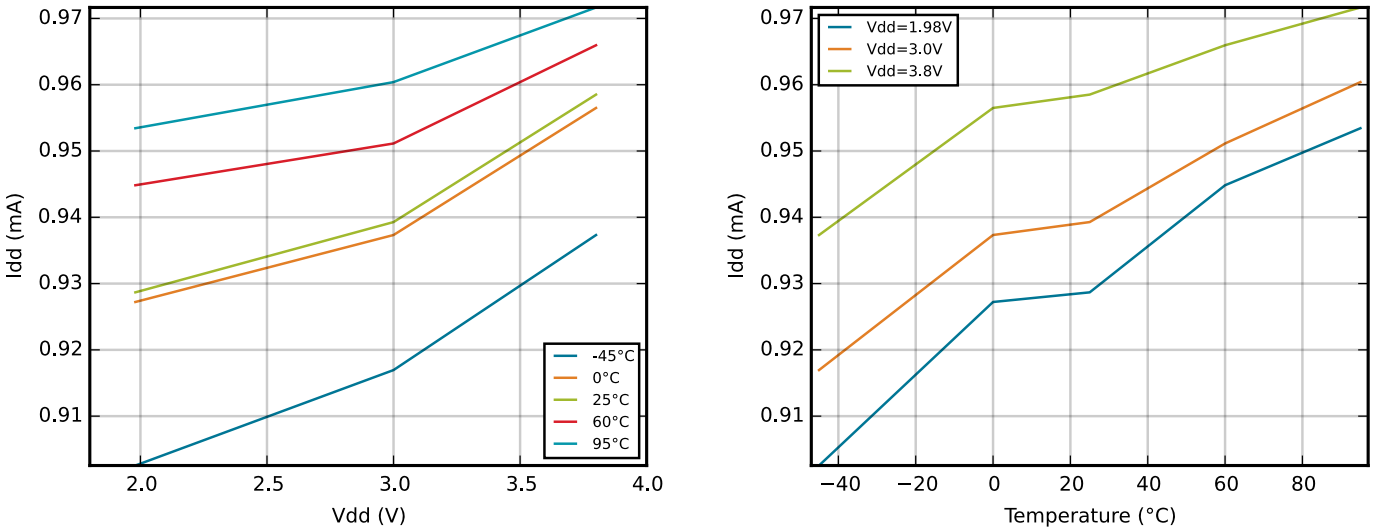



**Figure 4.5. EM0 Current Consumption with all Peripheral Clocks Disabled and HFRCO Running at 6.6 MHz**

### 4.5.2 EM1 Current Consumption

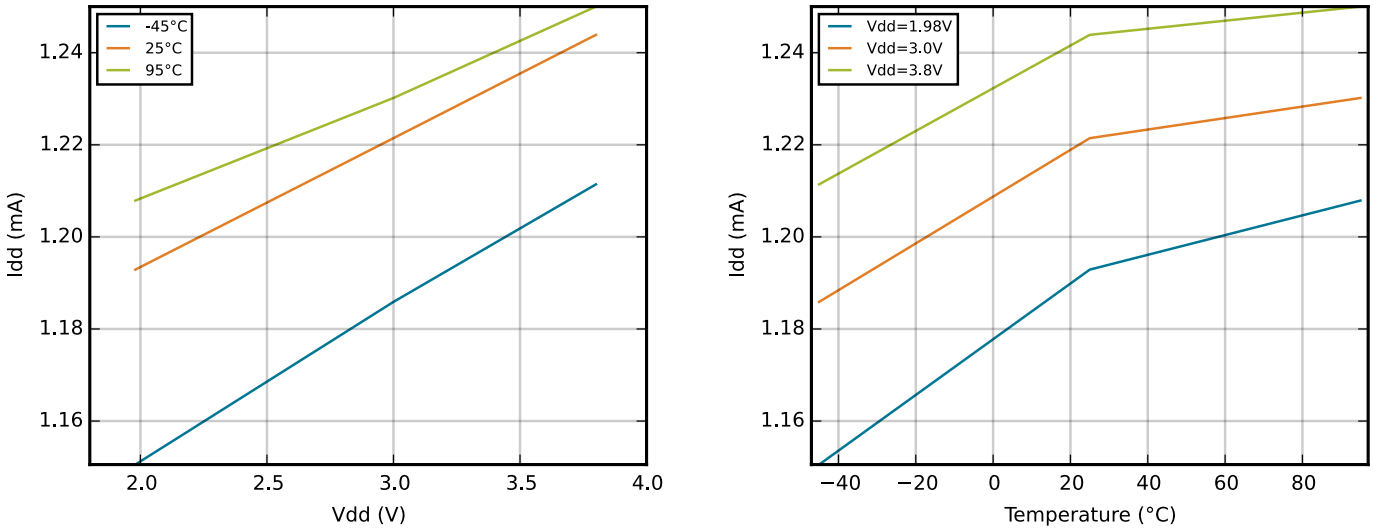



**Figure 4.6. EM1 Current Consumption with all Peripheral Clocks Disabled and HFRCO Running at 24 MHz**

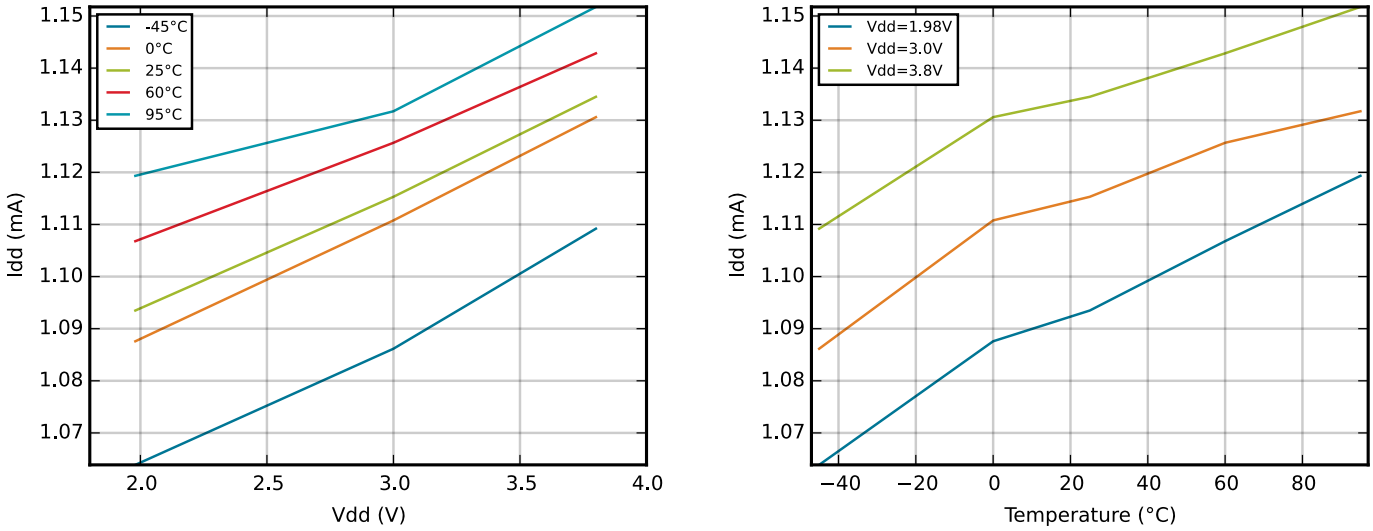



**Figure 4.7. EM1 Current Consumption with all Peripheral Clocks Disabled and HFRCO Running at 21 MHz**

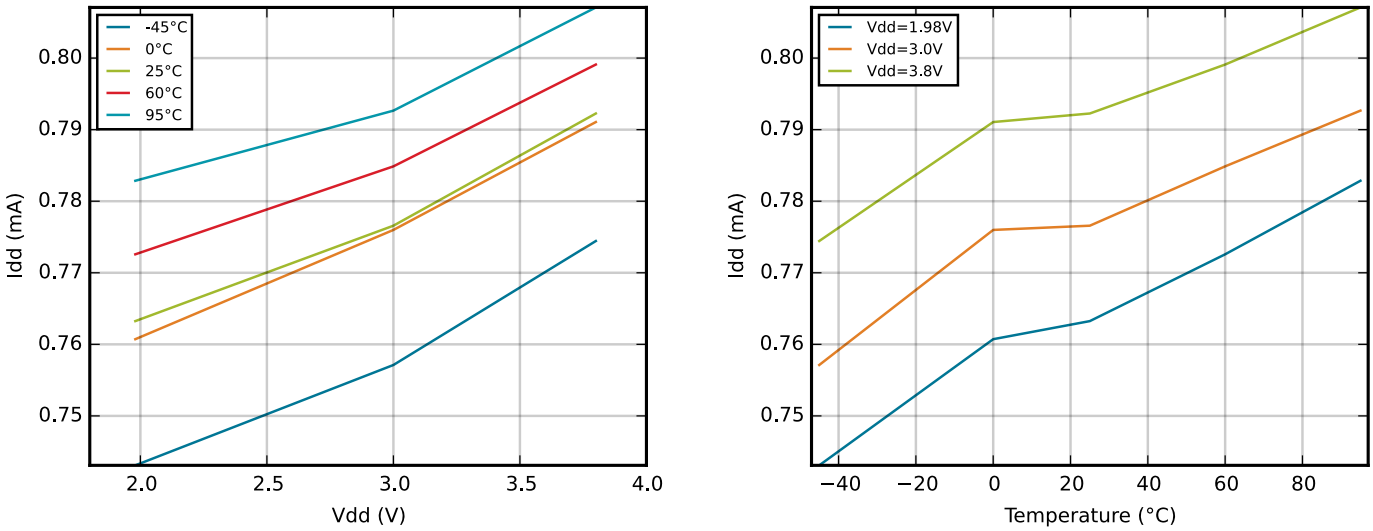



**Figure 4.8. EM1 Current Consumption with all Peripheral Clocks Disabled and HFRCO Running at 14 MHz**

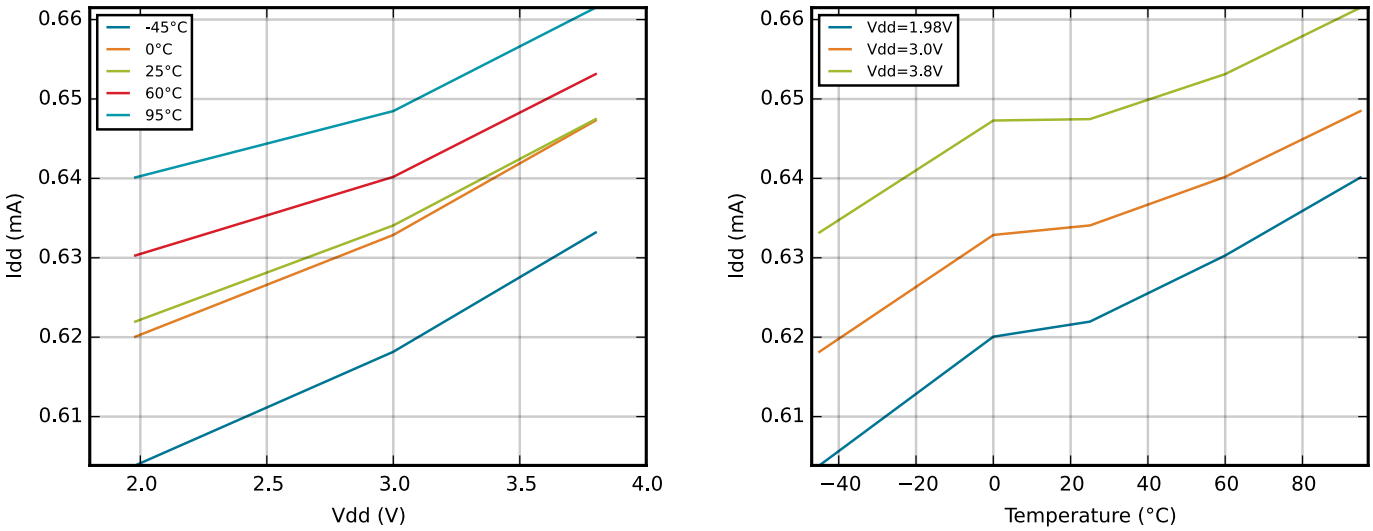



**Figure 4.9. EM1 Current Consumption with all Peripheral Clocks Disabled and HFRCO Running at 11 MHz**

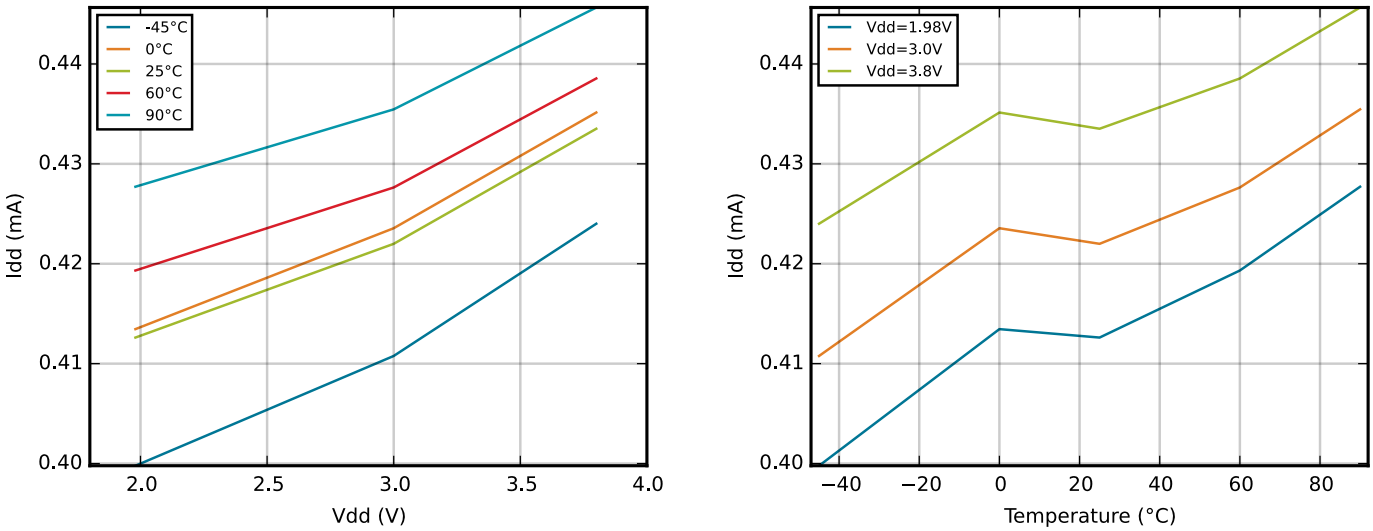



**Figure 4.10. EM1 Current Consumption with all Peripheral Clocks Disabled and HFRCO Running at 6.6 MHz**

### 4.5.3 EM2 Current Consumption

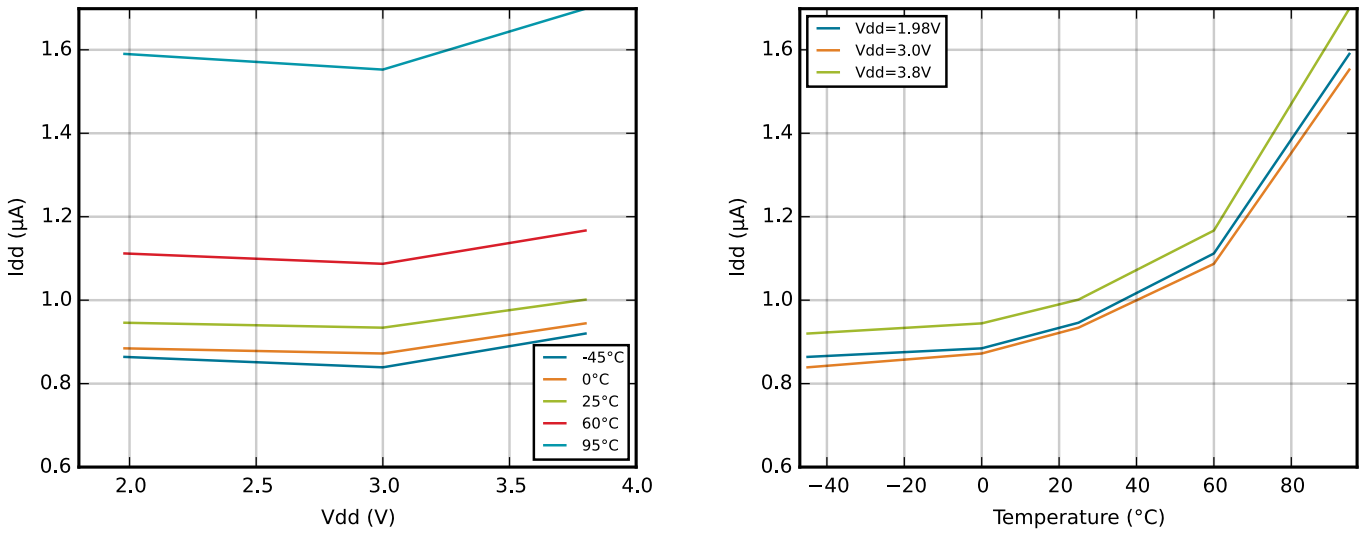



**Figure 4.11. EM2 Current Consumption, RTC prescaled to 1 kHz, 32.768 kHz LFRCO**

### 4.5.4 EM3 Current Consumption

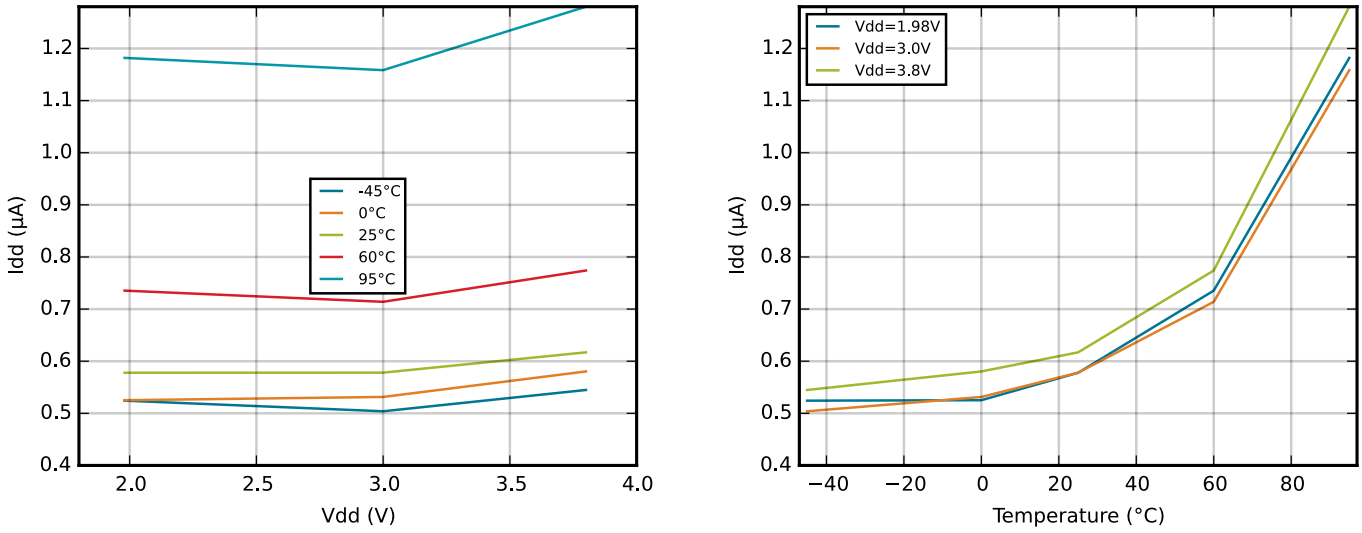



**Figure 4.12. EM3 Current Consumption**

### 4.5.5 EM4 Current Consumption

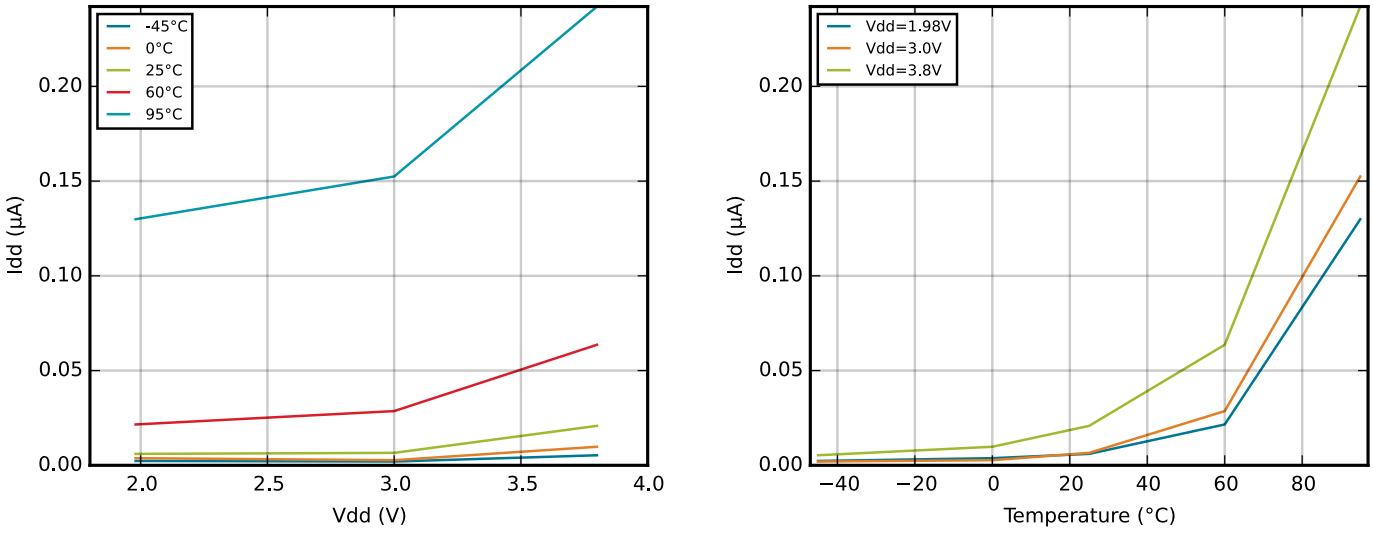



**Figure 4.13. EM4 Current Consumption**

### 4.6 Transition between Energy Modes

The transition times are measured from the trigger to the first clock edge in the CPU.

**Table 4.5. Energy Modes Transitions**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Transition time from EM1 to EM0 | $t_{EM10}$ | — | 0 | — | HFCORECLK cycles |
| Transition time from EM2 to EM0 | $t_{EM20}$ | — | 2 | — | µs |
| Transition time from EM3 to EM0 | $t_{EM30}$ | — | 2 | — | µs |
| Transition time from EM4 to EM0 | $t_{EM40}$ | — | 163 | — | µs |

### 4.7 Power Management

The EFM32HG requires the AVDD_x, VDD_DREG and IOVDD_x pins to be connected together (with optional filter) at the PCB level. For practical schematic recommendations, please see the application note, *AN0002 EFM32 Hardware Design Considerations*.

**Table 4.6. Power Management**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| BOD threshold on falling external supply voltage | $V_{BODextthr-}$ | EM0 | 1.74 | — | 1.96 | V |
| | | EM2 | 1.71 | 1.86 | 1.98 | V |
| BOD threshold on rising external supply voltage | $V_{BODextthr+}$ | | — | 1.85 | — | V |
| Delay from reset is released until program execution starts | $t_{RESET}$ | Applies to Power-on Reset, Brown-out Reset and pin reset. | — | 163 | — | µs |
| Voltage regulator decoupling capacitor. | $C_{DECOUPLE}$ | X5R capacitor recommended. Apply between DECOUPLE pin and GROUND | — | 1 | — | µF |
| USB voltage regulator out decoupling capacitor. | $C_{USB_VREGO}$ | X5R capacitor recommended. Apply between USB_VREGO pin and GROUND | — | 1 | — | µF |
| USB voltage regulator in decoupling capacitor. | $C_{USB_VREGI}$ | X5R capacitor recommended. Apply between USB_VREGI pin and GROUND | — | 4.7 | — | µF |

## 4.8 Flash

**Table 4.7. Flash**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Flash erase cycles before failure | $EC_{FLASH}$ | | 20000 | — | — | cycles |
| Flash word write cycles between erase | $WWC_{FLASH}$ | | — | — | 2[1] | cycles |
| Flash data retention | $RET_{FLASH}$ | $T_{AMB}$<150 °C | 10000 | — | — | h |
| | | $T_{AMB}$<85 °C | 10 | — | — | years |
| | | $T_{AMB}$<70 °C | 20 | — | — | years |
| Word (32-bit) programming time | $t_{W_PROG}$ | | 20 | — | — | µs |
| Page erase time[2] | $t_{PERASE}$ | | 20.7 | 22.0 | 24.8 | ms |
| Device erase time[3] | $t_{DERASE}$ | | 41.8 | 45.0 | 49.2 | ms |
| Erase current | $I_{ERASE}$ | | — | — | 7[4] | mA |
| Write current | $I_{WRITE}$ | | — | — | 7[4] | mA |
| Supply voltage during flash erase and write | $V_{FLASH}$ | | 1.98 | — | 3.8 | V |

**Note:**

1. There is a maximum of two writes to the same word between each erase due to a physical limitation of the flash. No bit should be written to ‘0’ more than once between erases. To write a word twice between erases, any bit written to ‘0’ by the first write should be written to ‘1’ by the second write. This preserves the specified flash write/erase endurance and does not change the ‘0’ written by the first write.
2. From setting ERASEPAGE bit in MSC_WRITECMD to 1 to reading 1 in ERASE bit in MSC_IF. Internal setup and hold times for flash control signals are included.
3. From setting DEVICEERASE bit in AAP_CMD to 1 to reading 0 in ERASEBUSY bit in AAP_STATUS. Internal setup and hold times for flash control signals are included.
4. Measured at 25 °C.

## 4.9 General Purpose Input Output

**Table 4.8. GPIO**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input low voltage | $V_{IOIL}$ | | — | — | 0.30×$V_{DD}$ | V |
| Input high voltage | $V_{IOIH}$ | | 0.70×$V_{DD}$ | — | — | V |
| Output high voltage (Production test condition = 3.0V, DRIVEMODE = STANDARD) | $V_{IOOH}$ | Sourcing 0.1 mA, $V_{DD}$=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST | — | 0.80×$V_{DD}$ | — | V |
| | | Sourcing 0.1 mA, $V_{DD}$=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST | — | 0.90×$V_{DD}$ | — | V |
| | | Sourcing 1 mA, $V_{DD}$=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOW | — | 0.85×$V_{DD}$ | — | V |
| | | Sourcing 1 mA, $V_{DD}$=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOW | — | 0.90×$V_{DD}$ | — | V |
| | | Sourcing 6 mA, $V_{DD}$=1.98 V, GPIO_Px_CTRL DRIVEMODE = STANDARD | 0.75×$V_{DD}$ | — | — | V |
| | | Sourcing 6 mA, $V_{DD}$=3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD | 0.85×$V_{DD}$ | — | — | V |
| | | Sourcing 20 mA, $V_{DD}$=1.98 V, GPIO_Px_CTRL DRIVEMODE = HIGH | 0.60×$V_{DD}$ | — | — | V |
| | | Sourcing 20 mA, $V_{DD}$=3.0 V, GPIO_Px_CTRL DRIVEMODE = HIGH | 0.80×$V_{DD}$ | — | — | V |
| Output low voltage (Production test condition = 3.0V, DRIVEMODE = STANDARD) | $V_{IOOL}$ | Sinking 0.1 mA, $V_{DD}$=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST | — | 0.20×$V_{DD}$ | — | V |
| | | Sinking 0.1 mA, $V_{DD}$=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST | — | 0.10×$V_{DD}$ | — | V |
| | | Sinking 1 mA, $V_{DD}$=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOW | — | 0.10×$V_{DD}$ | — | V |
| | | Sinking 1 mA, $V_{DD}$=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOW | — | 0.05×$V_{DD}$ | — | V |
| | | Sinking 6 mA, $V_{DD}$=1.98 V, GPIO_Px_CTRL DRIVEMODE = STANDARD | — | — | 0.30×$V_{DD}$ | V |
| | | Sinking 6 mA, $V_{DD}$=3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD | — | — | 0.20×$V_{DD}$ | V |
| | | Sinking 20 mA, $V_{DD}$=1.98 V, GPIO_Px_CTRL DRIVEMODE = HIGH | — | — | 0.35×$V_{DD}$ | V |
| | | Sinking 20 mA, $V_{DD}$=3.0 V, GPIO_Px_CTRL DRIVEMODE = HIGH | — | — | 0.25×$V_{DD}$ | V |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input leakage current | $I_{IOLEAK}$ | High Impedance IO connected to GROUND or VDD, EFM32HGxxxFxx only | — | ±0.1 | ±40 | nA |
| | | High Impedance IO connected to GROUND or VDD, EFM32HGxxxFxxN only | — | ±0.1 | ±70 | nA |
| I/O pin pull-up resistor | $R_{PU}$ | | — | 40 | — | kΩ |
| I/O pin pull-down resistor | $R_{PD}$ | | — | 40 | — | kΩ |
| Internal ESD series resistor | $R_{IOESD}$ | | — | 200 | — | Ω |
| Pulse width of pulses to be removed by the glitch suppression filter | $t_{IO-GLITCH}$ | | 10 | — | 50 | ns |
| Output fall time | $t_{IOOF}$ | GPIO_Px_CTRL DRIVEMODE = LOWEST and load capacitance $C_L$=12.5-25pF. | 20+0.1×$C_L$ | — | 250 | ns |
| | | GPIO_Px_CTRL DRIVEMODE = LOW and load capacitance $C_L$=350-600pF | 20+0.1×$C_L$ | — | 250 | ns |
| I/O pin hysteresis ($V_{IOTHR+}$ - $V_{IOTHR-}$) | $V_{IOHYST}$ | $V_{DD}$ = 1.98 - 3.8 V | 0.10×$V_{DD}$ | — | — | V |

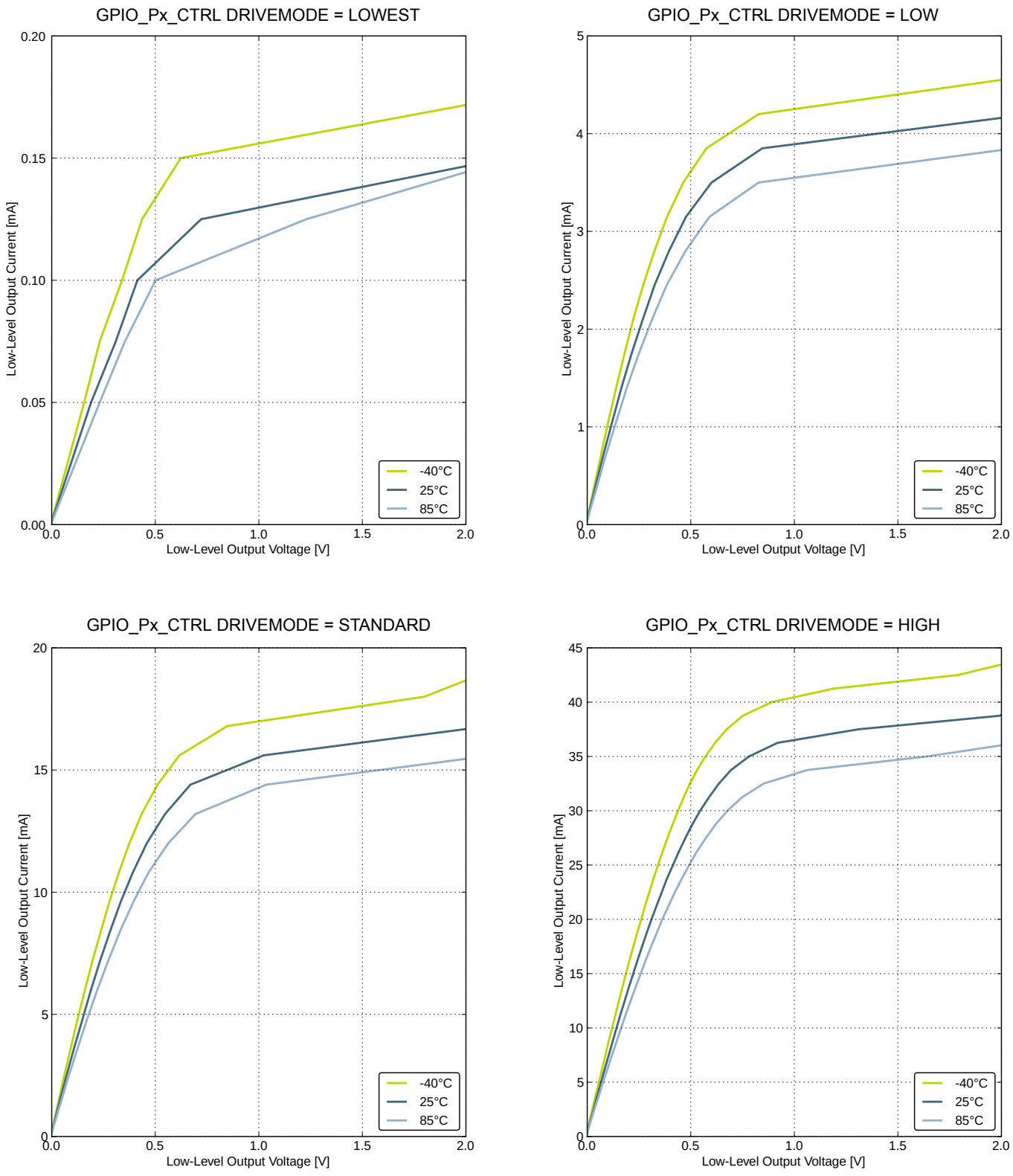



**Figure 4.14. Typical Low-Level Output Current, 2V Supply Voltage**

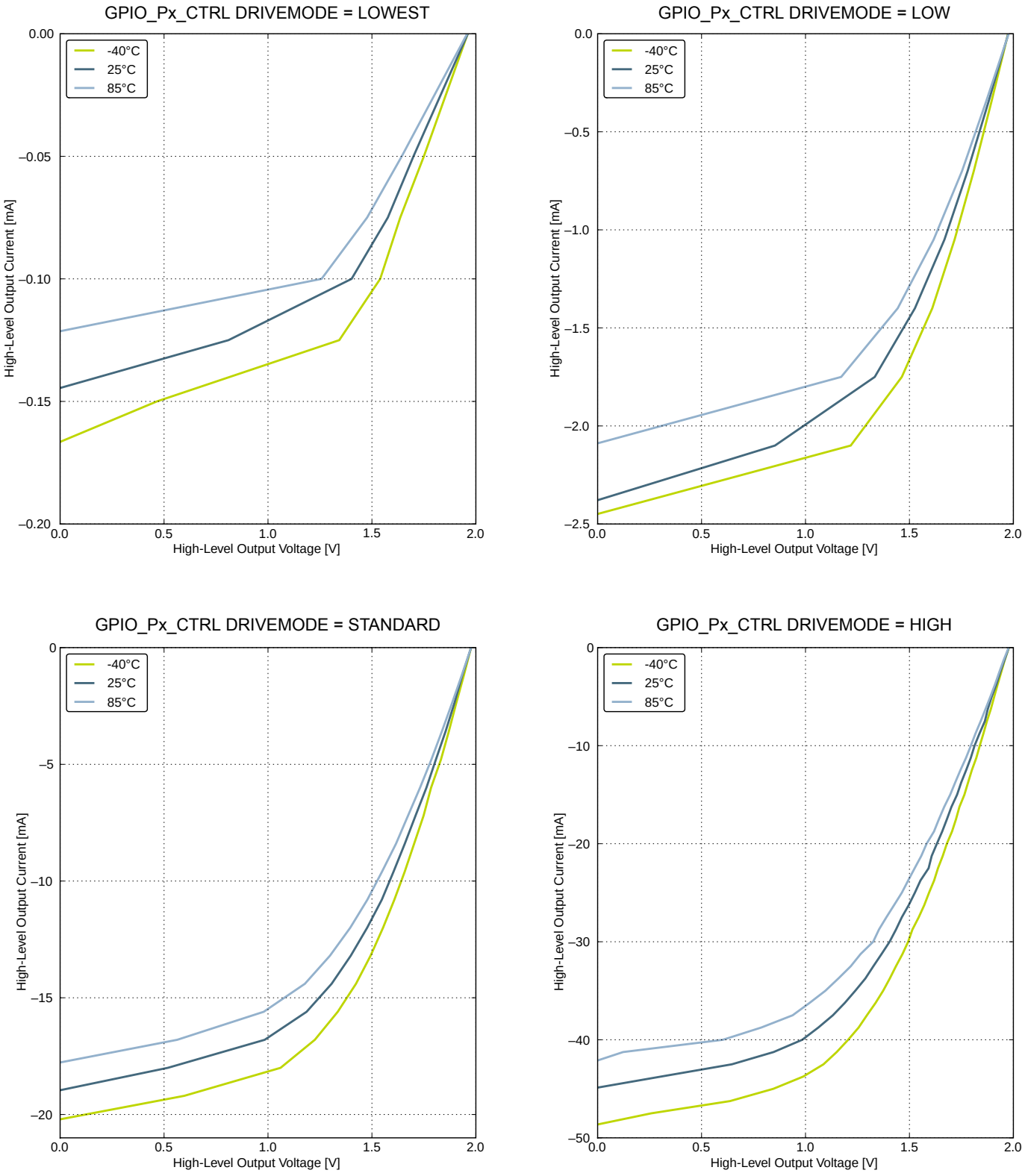



**Figure 4.15. Typical High-Level Output Current, 2 V Supply Voltage**

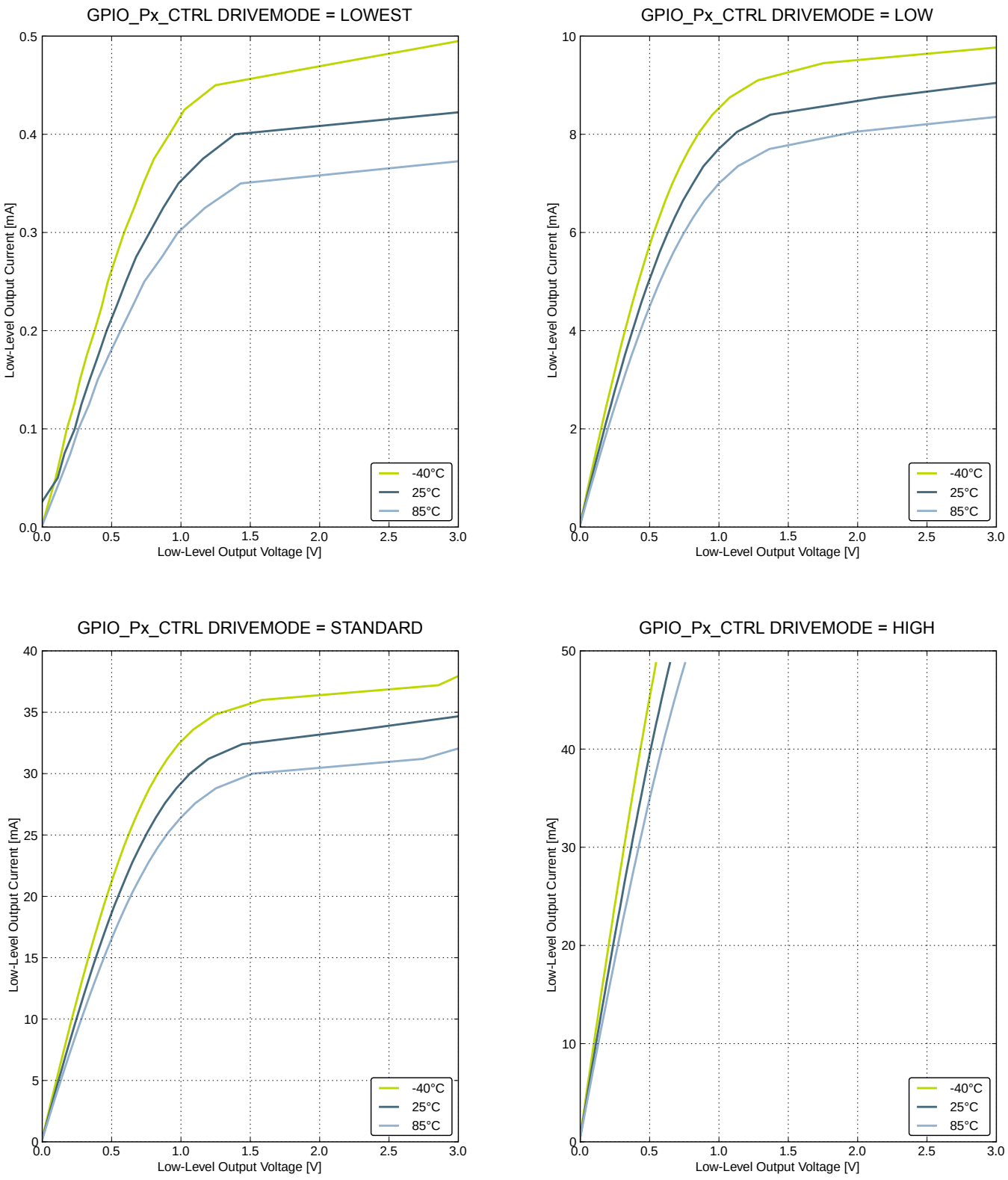



**Figure 4.16. Typical Low-Level Output Current, 3 V Supply Voltage**

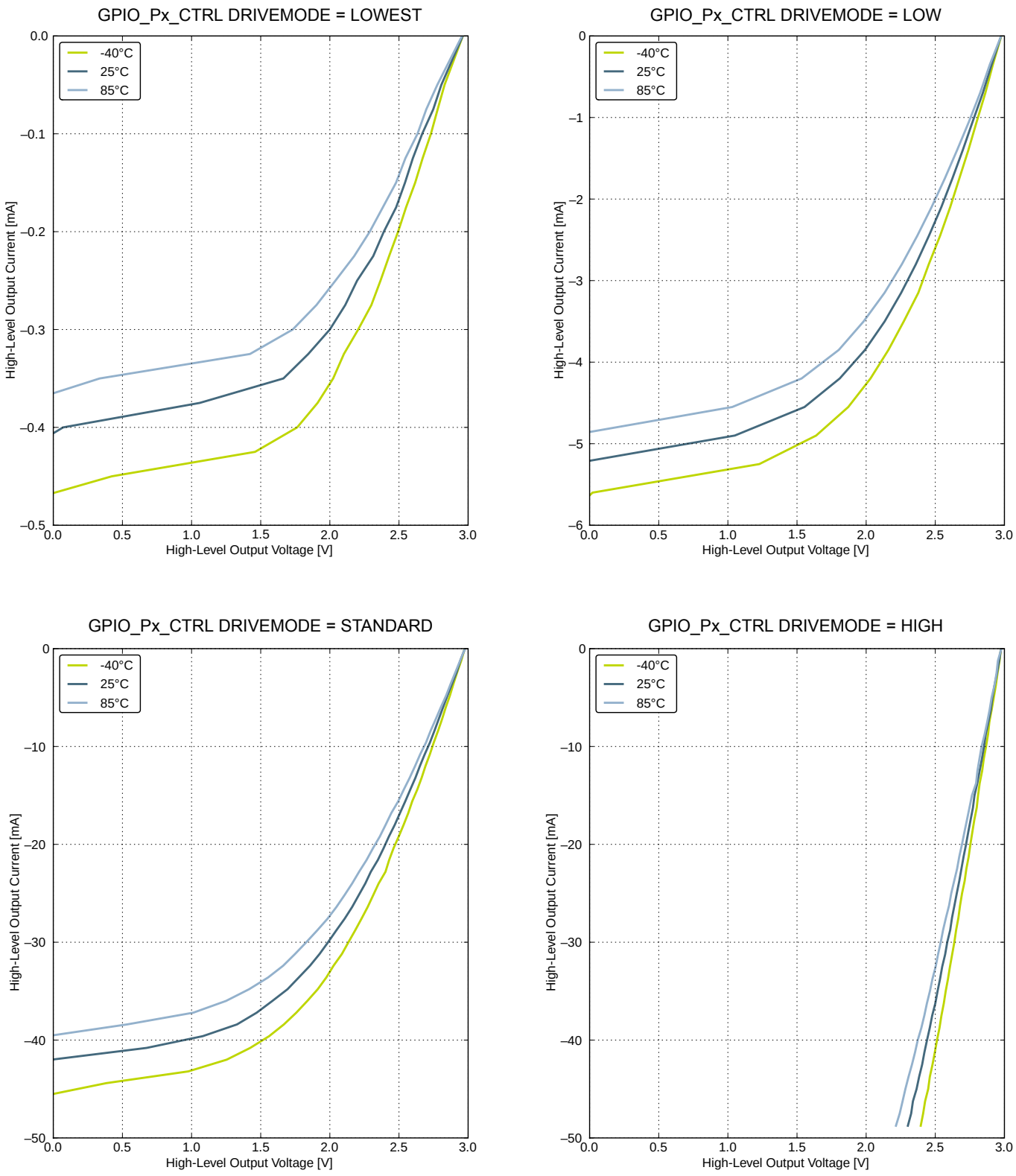



**Figure 4.17. Typical High-Level Output Current, 3 V Supply Voltage**

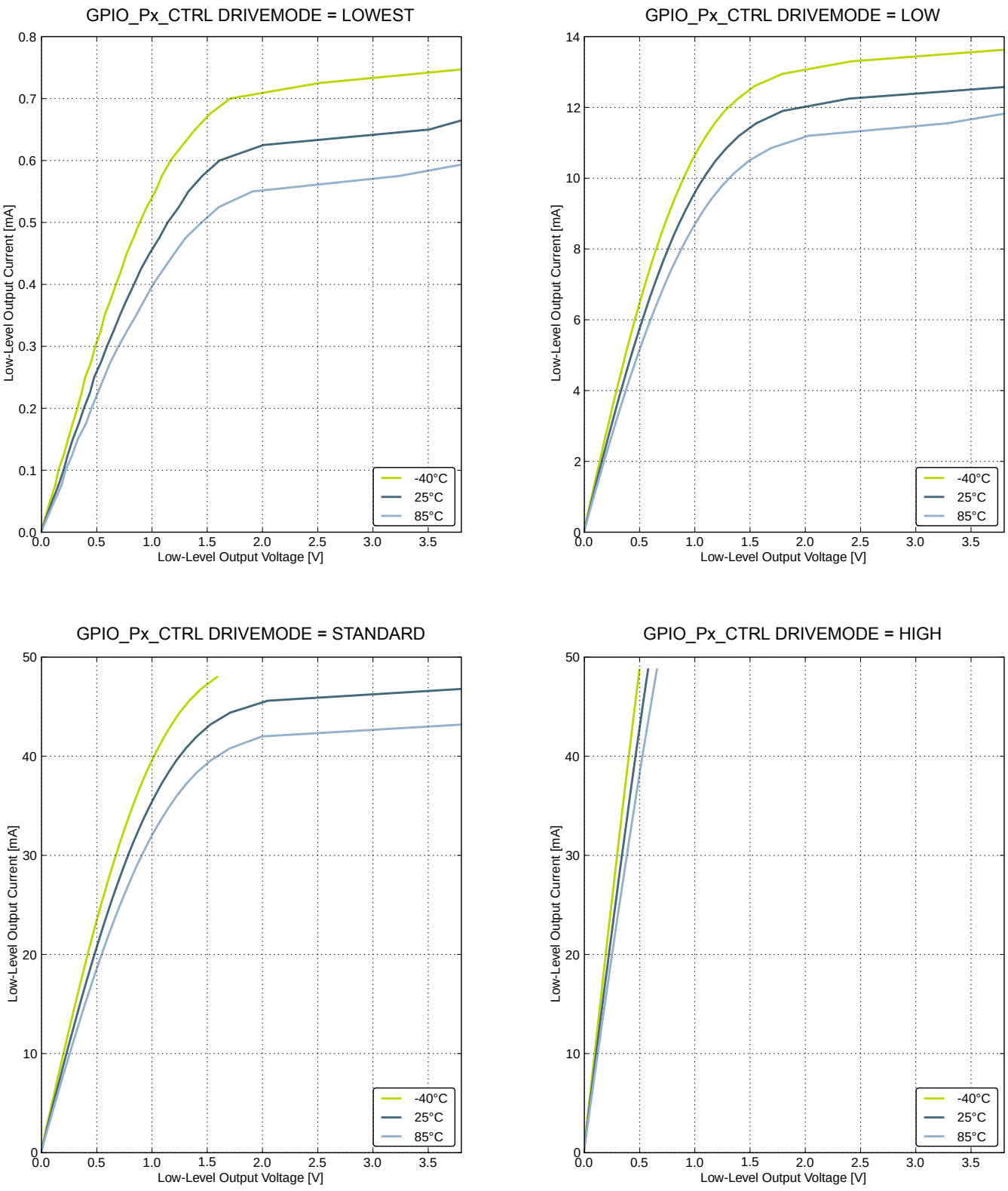



**Figure 4.18. Typical Low-Level Output Current, 3.8 V Supply Voltage**

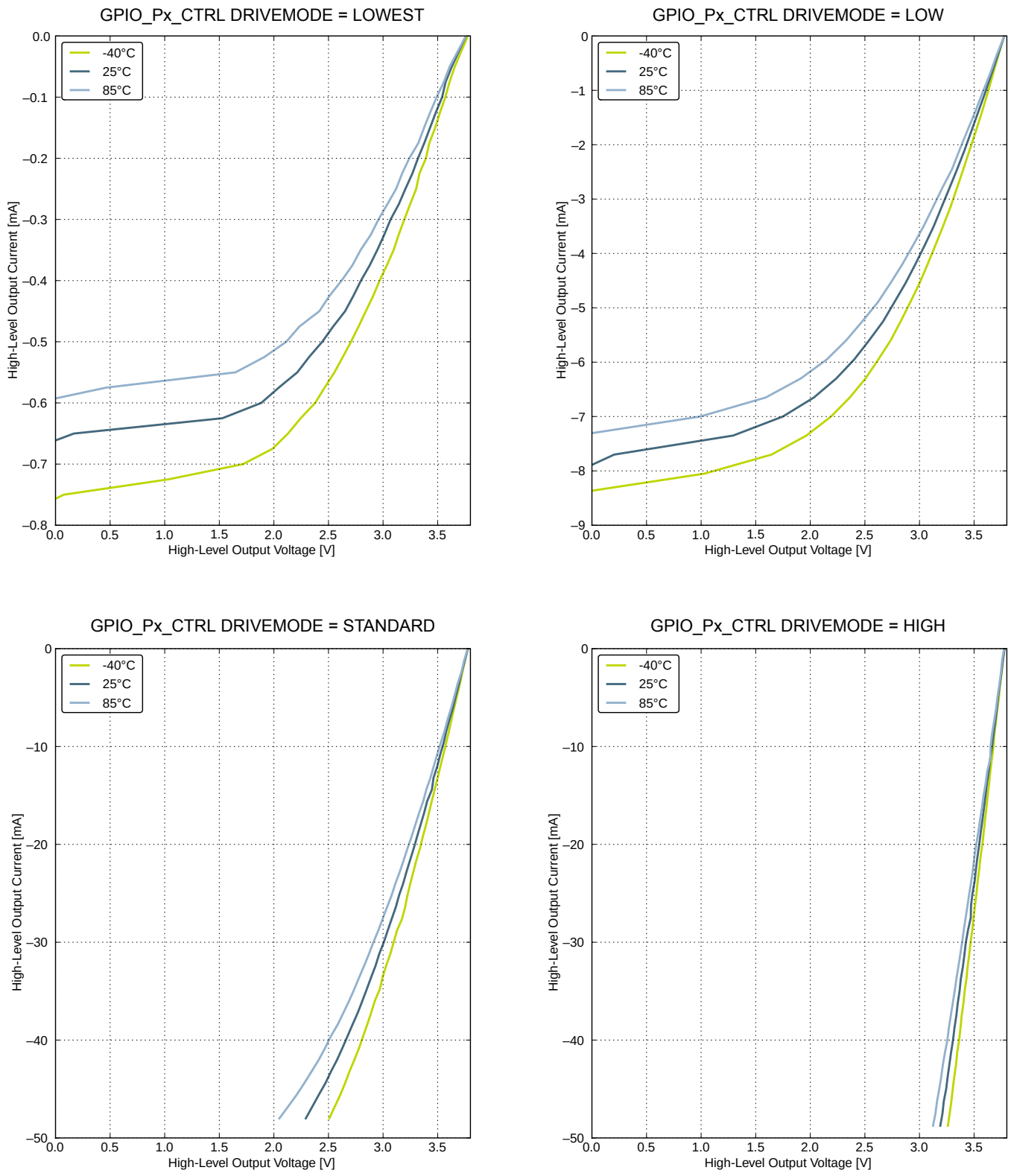



**Figure 4.19. Typical High-Level Output Current, 3.8 V Supply Voltage**

## 4.10 Oscillators

### 4.10.1 LFXO

**Table 4.9. LFXO**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supported nominal crystal frequency | $f_{LFXO}$ | | — | 32.768 | — | kHz |
| Supported crystal equivalent series resistance (ESR) | $ESR_{LFXO}$ | | — | 30 | 120 | kΩ |
| Supported crystal external load range | $C_{LFXOL}$ | | 5 | — | 25 | pF |
| Current consumption for core and buffer after startup. | $I_{LFXO}$ | ESR=30 kΩ, $C_L$=10 pF, LFXOBOOST in CMU_CTRL is 1 | — | 190 | — | nA |
| Start- up time. | $t_{LFXO}$ | ESR=30 kΩ, CL=10 pF, 40% - 60% duty cycle has been reached, LFXOBOOST in CMU_CTRL is 1 | — | 1100 | — | ms |

For safe startup of a given crystal, the Configurator tool in Simplicity Studio contains a tool to help users configure both load capacitance and software settings for using the LFXO. For details regarding the crystal configuration, the reader is referred to application note *AN0016 EFM32 Oscillator Design Consideration*.

### 4.10.2 HFXO

**Table 4.10. HFXO**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supported nominal crystal Frequency | $f_{HFXO}$ | | 4 | — | 25 | MHz |
| Supported crystal equivalent series resistance (ESR) | $ESR_{HFXO}$ | Crystal frequency 25 MHz | — | 30 | 100 | Ω |
| | | Crystal frequency 4 MHz | — | 400 | 1500 | Ω |
| The transconductance of the HFXO input transistor at crystal startup | $g_{mHFXO}$ | HFXOBOOST in CMU_CTRL equals 0b11 | 20 | — | — | mS |
| Supported crystal external load range | $C_{HFXOL}$ | | 5 | — | 25 | pF |
| Current consumption for HFXO after startup | $I_{HFXO}$ | 4 MHz: ESR=400 Ω, $C_L$=20 pF, HFXOBOOST in CMU_CTRL equals 0b11 | — | 85 | — | µA |
| | | 25 MHz: ESR=30 Ω, $C_L$=10 pF, HFXOBOOST in CMU_CTRL equals 0b11 | — | 165 | — | µA |
| Startup time | $t_{HFXO}$ | 25 MHz: ESR=30 Ω, $C_L$=10 pF, HFXOBOOST in CMU_CTRL equals 0b11 | — | 785 | — | µs |

### 4.10.3 LFRCO

**Table 4.11. LFRCO**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Oscillation frequency, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | $f_{LFRCO}$ | | 31.3 | 32.768 | 34.3 | kHz |
| Startup time not including software calibration | $t_{LFRCO}$ | | — | 150 | — | µs |
| Current consumption | $I_{LFRCO}$ | | — | 361 | 492 | nA |
| Frequency step for LSB change in TUNING value | $TUNESTEP_{LFRCO}$ | | — | 202 | — | Hz |

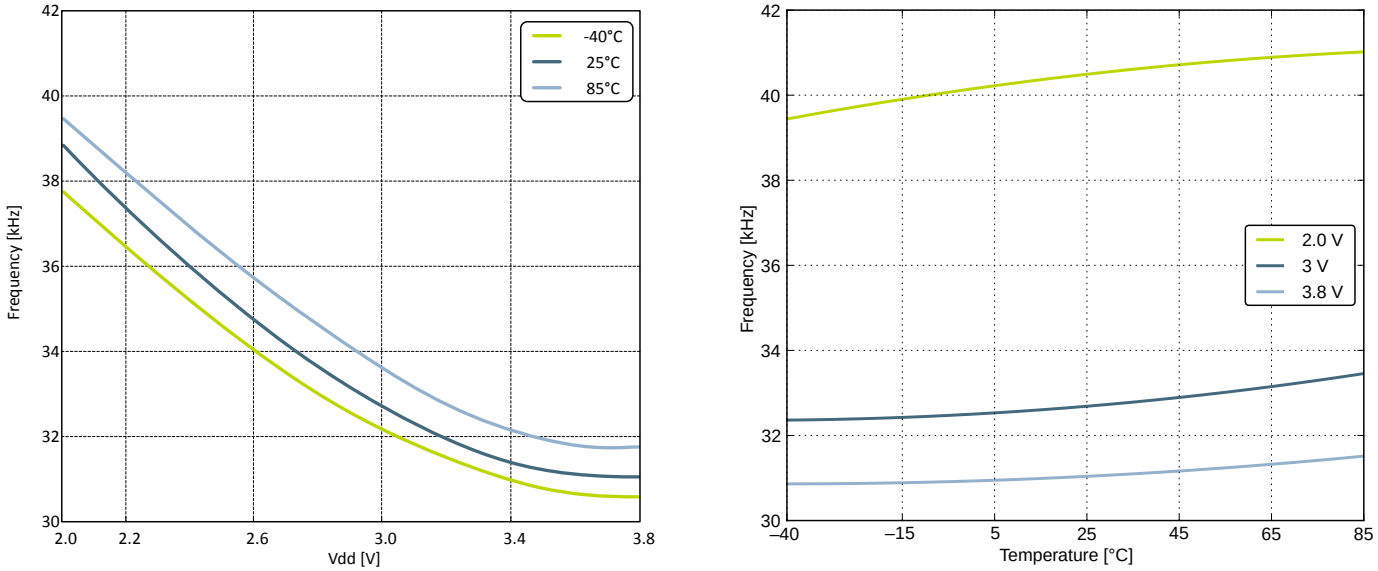



**Figure 4.20. Calibrated LFRCO Frequency vs Temperature and Supply Voltage**

### 4.10.4 HFRCO

**Table 4.12. HFRCO**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Oscillation frequency, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | $f_{HFRCO}$ | 21 MHz frequency band | 20.37 | 21.0 | 21.63 | MHz |
| | | 14 MHz frequency band | 13.58 | 14.0 | 14.42 | MHz |
| | | 11 MHz frequency band | 10.67 | 11.0 | 11.33 | MHz |
| | | 7 MHz frequency band | 6.40 | 6.60 | 6.80 | MHz |
| | | 1 MHz frequency band | 1.15 | 1.20 | 1.25 | MHz |
| Settling time after start-up | $t_{HFRCO_settling}$ | $f_{HFRCO}$ = 14 MHz | — | 0.6 | — | Cycles |
| Current consumption | $I_{HFRCO}$ | $f_{HFRCO}$ = 21 MHz | — | 143 | 175 | µA |
| | | $f_{HFRCO}$ = 14 MHz | — | 113 | 140 | µA |
| | | $f_{HFRCO}$ = 11 MHz | — | 101 | 125 | µA |
| | | $f_{HFRCO}$ = 6.6 MHz | — | 84 | 105 | µA |
| | | $f_{HFRCO}$ = 1.2 MHz | — | 27 | 40 | µA |
| Frequency step for LSB change in TUNING value | $TUNESTEP_{HFRCO}$ | 21 MHz frequency band | — | 52.8[1] | — | kHz |
| | | 14 MHz frequency band | — | 36.9[1] | — | kHz |
| | | 11 MHz frequency band | — | 30.1[1] | — | kHz |
| | | 7 MHz frequency band | — | 18.0[1] | — | kHz |
| | | 1 MHz frequency band | — | 3.4 | — | kHz |

**Note:**

1. The TUNING field in the CMU_HFRCOCTRL register may be used to adjust the HFRCO frequency. There is enough adjustment range to ensure that the frequency bands above 7 MHz will always have some overlap across supply voltage and temperature. By using a stable frequency reference such as the LFXO or HFXO, a firmware calibration routine can vary the TUNING bits and the frequency band to maintain the HFRCO frequency at any arbitrary value between 7 MHz and 21 MHz across operating conditions.

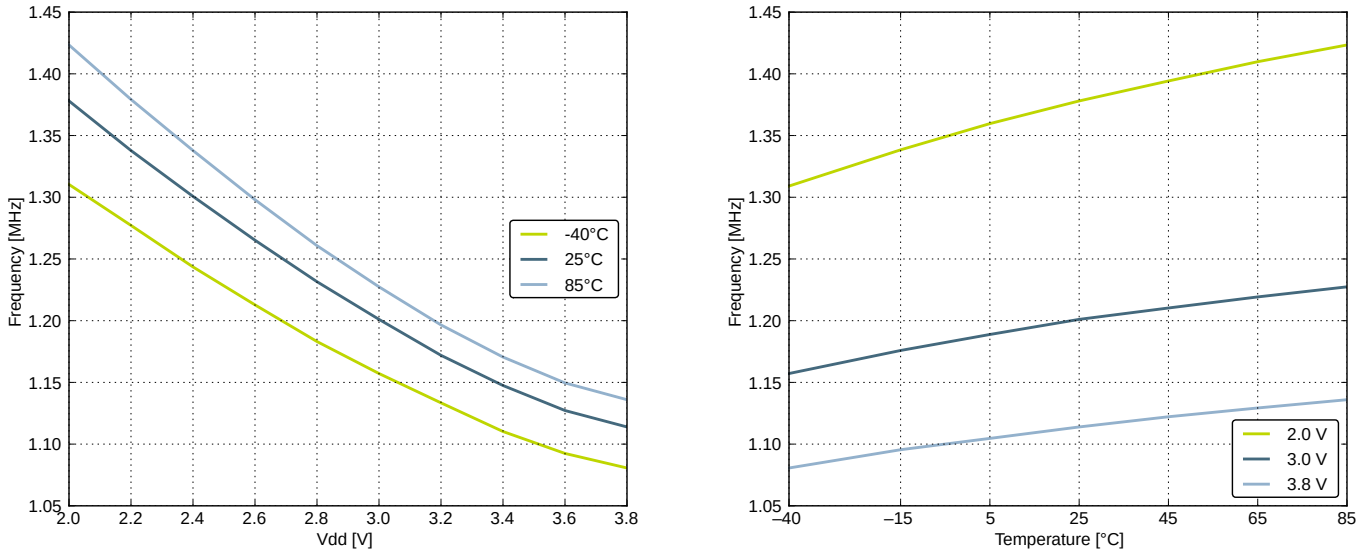



**Figure 4.21. Calibrated HFRCO 1 MHz Band Frequency vs Supply Voltage and Temperature**

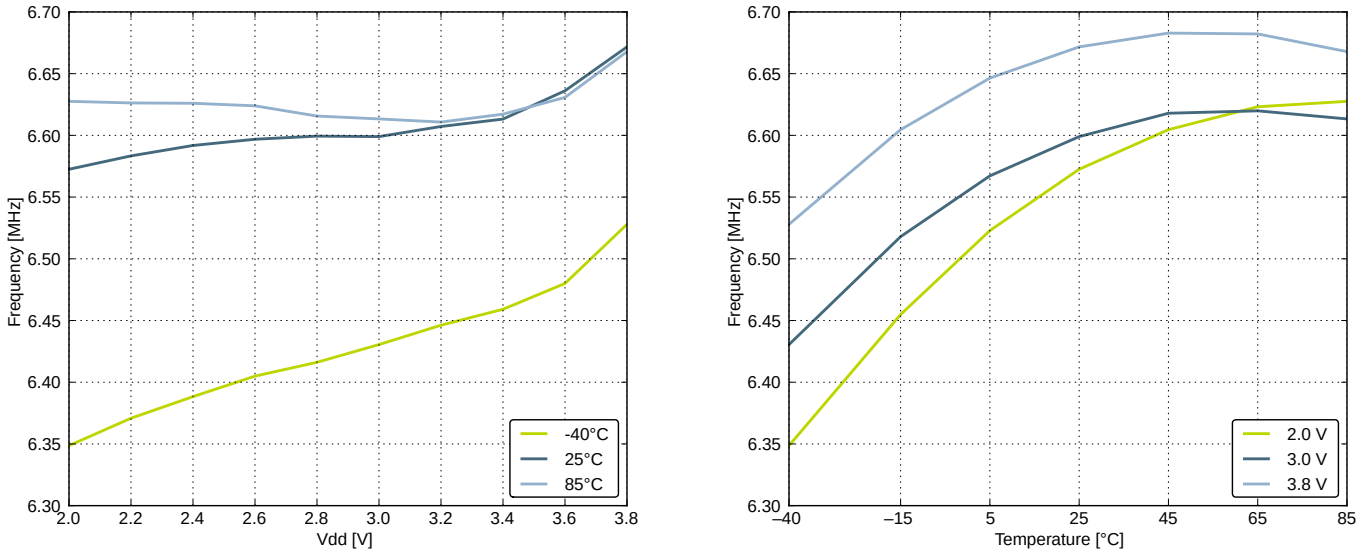



**Figure 4.22. Calibrated HFRCO 7 MHz Band Frequency vs Supply Voltage and Temperature**

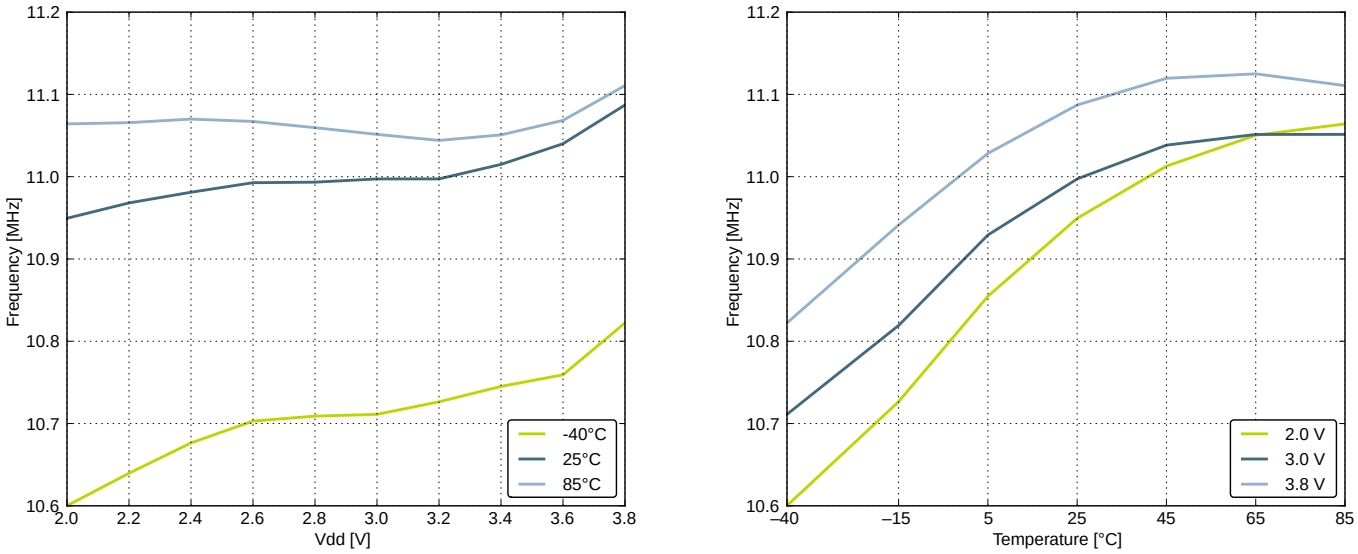



**Figure 4.23. Calibrated HFRCO 11 MHz Band Frequency vs Supply Voltage and Temperature**

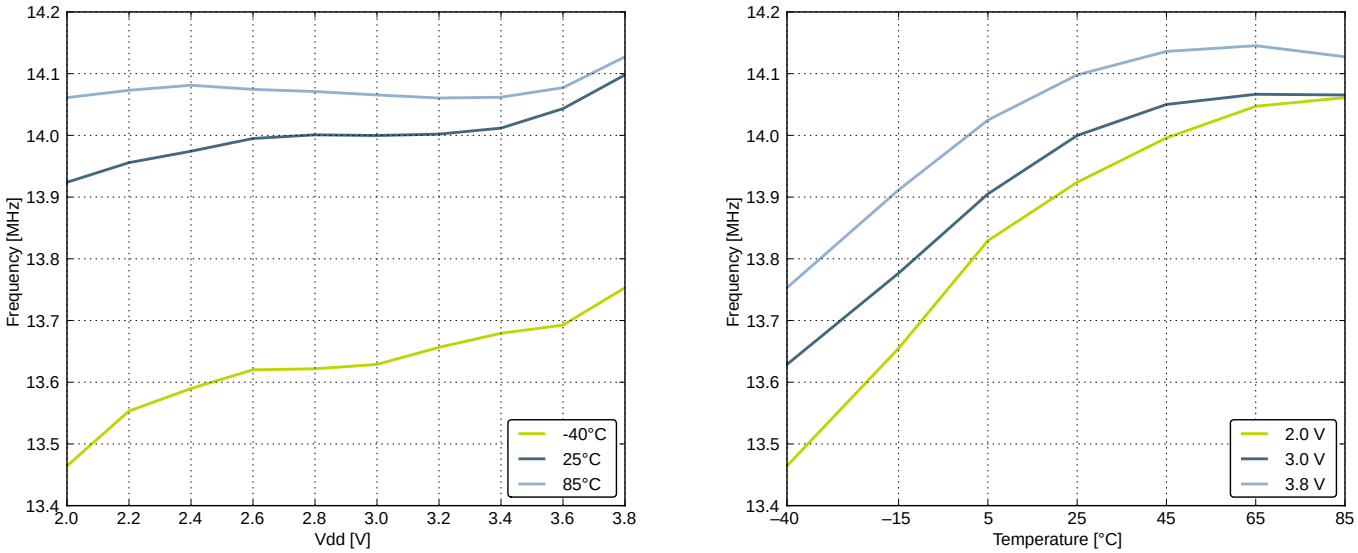



**Figure 4.24. Calibrated HFRCO 14 MHz Band Frequency vs Supply Voltage and Temperature**

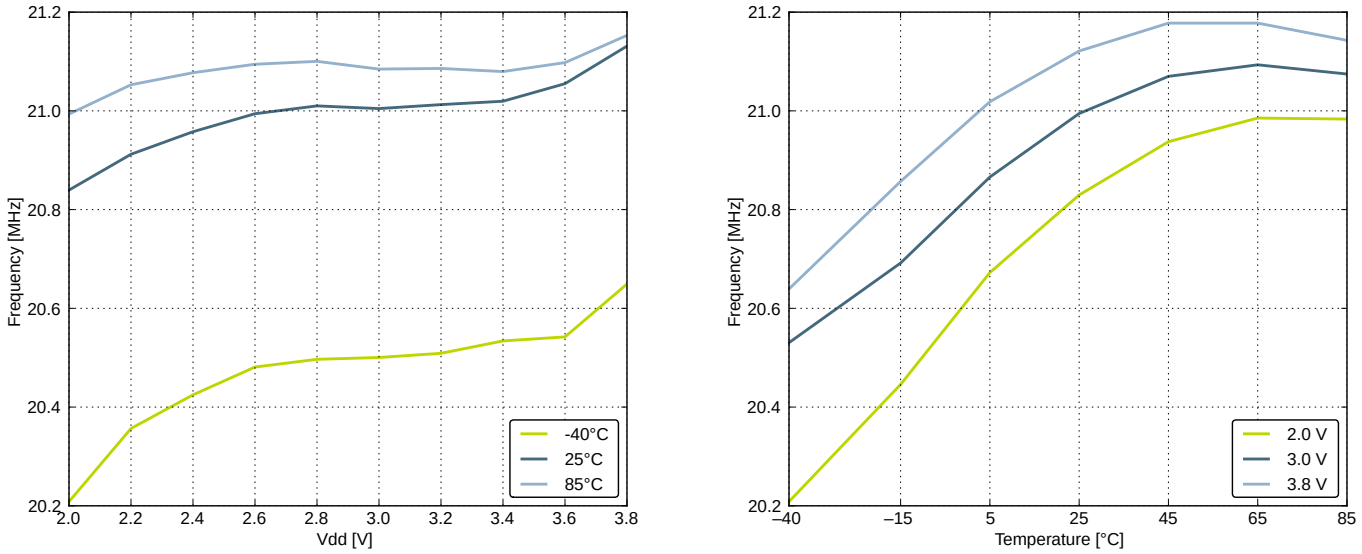



**Figure 4.25. Calibrated HFRCO 21 MHz Band Frequency vs Supply Voltage and Temperature**

### 4.10.5 AUXHFRCO

**Table 4.13. AUXHFRCO**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Oscillation frequency, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | $f_{AUXHFRCO}$ | 21 MHz frequency band | 20.37 | 21.0 | 21.63 | MHz |
| | | 14 MHz frequency band | 13.58 | 14.0 | 14.42 | MHz |
| | | 11 MHz frequency band | 10.67 | 11.0 | 11.33 | MHz |
| | | 7 MHz frequency band | 6.40 | 6.60 | 6.80 | MHz |
| | | 1 MHz frequency band | 1.15 | 1.20 | 1.25 | MHz |
| Settling time after start-up | $t_{AUXHFRCO_settling}$ | $f_{AUXHFRCO}$ = 14 MHz | — | 0.6 | — | Cycles |
| Frequency step for LSB change in TUNING value | $TUNESTEP_{AUXHFRCO}$ | 21 MHz frequency band | — | 52.8 | — | kHz |
| | | 14 MHz frequency band | — | 36.9 | — | kHz |
| | | 11 MHz frequency band | — | 30.1 | — | kHz |
| | | 7 MHz frequency band | — | 18.0 | — | kHz |
| | | 1 MHz frequency band | — | 3.4 | — | kHz |

### 4.10.6 USHFRCO

**Table 4.14. USHFRCO**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Oscillation frequency | $f_{USHFRCO}$ | No Clock Recovery, Full Temperature and Supply Range, 48 MHz band | 47.10 | 48.00 | 48.90 | MHz |
| | | No Clock Recovery, Full Temperature and Supply Range, 24 MHz band | 23.73 | 24.00 | 24.32 | MHz |
| | | No Clock Recovery, 25°C, 3.3V, 48 MHz band | 47.50 | 48.00 | 48.50 | MHz |
| | | No Clock Recovery, 25°C, 3.3V, 24 MHz band | 23.86 | 24.00 | 24.16 | MHz |
| | | USB Active with Clock Recovery, Full Temperature and Supply Range | 47.88 | 48.00 | 48.12 | MHz |
| Temperature coefficient | $T_{CUSHFRCO}$ | 3.3 V | — | 0.0175 | — | %/°C |
| Supply voltage coefficient | $VC_{USHFRCO}$ | 25°C | — | 0.0045 | — | %/V |
| Current consumption | $I_{USHFRCO}$ | $f_{USHFRCO}$ = 48 MHz | 1.21 | 1.36 | 1.48 | mA |
| | | $f_{USHFRCO}$ = 24 MHz | 0.81 | 0.92 | 1.02 | mA |

### 4.10.7 ULFRCO

**Table 4.15. ULFRCO**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Oscillation frequency | $f_{ULFRCO}$ | 25°C, 3V | 0.70 | — | 1.75 | kHz |
| Temperature coefficient | $TC_{ULFRCO}$ | | — | 0.05 | — | %/°C |
| Supply voltage coefficient | $VC_{ULFRCO}$ | | — | -18.2 | — | %/V |

## 4.11 Analog Digital Converter (ADC)

**Table 4.16. ADC**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input voltage range | $V_{ADCIN}$ | Single-ended | 0 | — | $V_{REF}$ | V |
| | | Differential | $-V_{REF}/2$ | — | $V_{REF}/2$ | V |
| Input range of external reference voltage, single-ended and differential | $V_{ADCREFIN}$ | | 1.25 | — | $V_{DD}$ | V |
| Input range of external negative reference voltage on channel 7 | $V_{ADCREFIN_CH7}$ | See $V_{ADCREFIN}$ | 0 | — | $V_{DD}$ - 1.1 | V |
| Input range of external positive reference voltage on channel 6 | $V_{ADCREFIN_CH6}$ | See $V_{ADCREFIN}$ | 0.625 | — | $V_{DD}$ | V |
| Common mode input range | $V_{ADCCMIN}$ | | 0 | — | $V_{DD}$ | V |
| Input current | $I_{ADCIN}$ | 2 pF sampling capacitors | — | <100 | — | nA |
| Analog input common mode rejection ratio | $CMRR_{ADC}$ | | — | 65 | — | dB |
| Average active current | $I_{ADC}$ | 1 Msamples/s, 12 bit, external reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B | — | 735[1] | — | µA |
| | | 1 Msamples/s, 12 bit, internal 1.25V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B | — | 760[1] | — | µA |
| | | 500 Ksamples/s, 12 bit, external reference, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 346[1] | — | µA |
| | | 500 Ksamples/s, 12 bit, internal 1.25V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 354[1] | — | µA |
| | | 10 kSamples/s, 12 bit, internal 1.25 V reference, WARMUP = 00b, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 52[1] | — | µA |
| | | 10 kSamples/s, 12 bit, internal 1.25 V reference, WARMUP = 01b, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 50[1] | — | µA |
| | | 10 kSamples/s, 12 bit, internal 1.25 V reference, WARMUP = 10b, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 54[1] | — | µA |
| Current Consumption of internal voltage referene | $I_{ADCREF}$ | Internal voltage reference | — | 65 | — | µA |
| Input capacitance | $C_{ADCIN}$ | | — | 2 | — | pF |
| Input ON resistance | $R_{ADCIN}$ | | 1 | — | — | MΩ |
| Input RC filter resistance | $R_{ADCFILT}$ | | — | 10 | — | kΩ |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input RC filter/decoupling capacitance | $C_{ADCFILT}$ | | — | 250 | — | fF |
| Input bias current | $I_{ADCBIASIN}$ | VSS < VIN < VDD | -40 | — | 40 | nA |
| Input offset current | $I_{ADCOFFSETIN}$ | VSS < VIN < VDD | -40 | — | 40 | nA |
| ADC Clock Frequency | $f_{ADCCLK}$ | BIASPROG=0x747 | — | — | 7 | MHz |
| | | BIASPROG=0xF4B | — | — | 13 | MHz |
| Conversion time | $t_{ADCCONV}$ | 6-bit | 7 | — | — | ADCCLK Cycles |
| | | 8-bit | 11 | — | — | ADCCLK Cycles |
| | | 12-bit | 13 | — | — | ADCCLK Cycles |
| Acquisition time | $t_{ADCACQ}$ | Programmable | 1 | — | 256 | ADCCLK Cycles |
| Required acquisition time for VDD/3 reference | $t_{ADCACQVDD3}$ | | 2 | — | — | µs |
| Startup time of reference generator and ADC core | $t_{ADCSTART}$ | NORMAL mode | — | 5 | — | µs |
| | | KEEPADCWARM mode | — | 1 | — | µs |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Signal-to-Noise Ratio (SNR) | $SNR_{ADC}$ | 1 MSamples/s, 12 bit, single-ended, internal 1.25 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B | — | 59 | — | dB |
| | | 1 MSamples/s, 12 bit, single-ended, internal 2.5 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B | — | 63 | — | dB |
| | | 1 MSamples/s, 12 bit, single-ended, $V_{DD}$ reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B | — | 67 | — | dB |
| | | 1 MSamples/s, 12 bit, differential, internal 1.25 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B | — | 63 | — | dB |
| | | 1 MSamples/s, 12 bit, differential, internal 2.5 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B | — | 66 | — | dB |
| | | 1 MSamples/s, 12 bit, differential, 5 V reference, ADC_CLK =13 MHz, BIASPROG = 0xF4B | — | 66 | — | dB |
| | | 1 MSamples/s, 12 bit, differential, $V_{DD}$ reference, ADC_CLK= 13 MHz, BIASPROG =0xF4B | 63 | 69 | — | dB |
| | | 1 MSamples/s, 12 bit, differential, $2xV_{DD}$ reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B | — | 70 | — | dB |
| | | 200 kSamples/s, 12 bit, single-ended, internal 1.25 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 62 | — | dB |
| | | 200 kSamples/s, 12 bit, single-ended, internal 2.5 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 63 | — | dB |
| | | 200 kSamples/s, 12 bit, single-ended, $V_{DD}$ reference, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 67 | — | dB |
| | | 200 kSamples/s, 12 bit, differential, internal 1.25 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 63 | — | dB |
| | | 200 kSamples/s, 12 bit, differential, internal 2.5 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 66 | — | dB |
| | | 200 kSamples/s, 12 bit, differential, 5 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 66 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Signal-to-Noise Ratio (SNR) | $SNR_{ADC}$ | 200 kSamples/s, 12 bit, differential, $V_{DD}$ reference,ADC_CLK = 7 MHz, BIASPROG = 0x747 | 63 | 69 | — | dB |
| | | 200 kSamples/s, 12 bit, differential, 2x$V_{DD}$ reference,ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 70 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Signal-to-Noise And Distortion Ratio (SINAD) | $SINAD_{ADC}$ | 1 MSamples/s, 12 bit, single-ended, internal 1.25 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B | — | 58 | — | dB |
| | | 1 MSamples/s, 12 bit, single-ended, internal 2.5 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B | — | 62 | — | dB |
| | | 1 MSamples/s, 12 bit, single-ended, $V_{DD}$ reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B | — | 66 | — | dB |
| | | 1 MSamples/s, 12 bit, differential, internal 1.25 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B | — | 63 | — | dB |
| | | 1 MSamples/s, 12 bit, differential, internal 2.5 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B | — | 66 | — | dB |
| | | 1 MSamples/s, 12 bit, differential, 5 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B | — | 66 | — | dB |
| | | 1 MSamples/s, 12 bit, differential, $V_{DD}$ reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B | 62 | 68 | — | dB |
| | | 1 MSamples/s, 12 bit, differential, $2xV_{DD}$ reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B | — | 68 | — | dB |
| | | 200 kSamples/s, 12 bit, single-ended, internal 1.25 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 61 | — | dB |
| | | 200 kSamples/s, 12 bit, single-ended, internal 2.5 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 62 | — | dB |
| | | 200 kSamples/s, 12 bit, single-ended, VDD reference, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 66 | — | dB |
| | | 200 kSamples/s, 12 bit, differential, internal 1.25 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 63 | — | dB |
| | | 200 kSamples/s, 12 bit, differential, internal 2.5 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 66 | — | dB |
| | | 200 kSamples/s, 12 bit, differential, 5V reference, ADC_CLK= 7 MHz, BIASPROG = 0x747 | — | 66 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Signal-to-Noise And Distortion Ratio (SINAD) | $SINAD_{ADC}$ | 200 kSamples/s, 12 bit, differential, $V_{DD}$ reference, ADC_CLK = 7 MHz, BIASPROG = 0x747 | 62 | 68 | — | dB |
| | | 200 kSamples/s, 12 bit, differential, $2xV_{DD}$ reference, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 69 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Spurious-Free Dynamic Range (SFDR) | $SFDR_{ADC}$ | 1 MSamples/s, 12 bit, single-ended, internal 1.25 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B | — | 75 | — | dBc |
| | | 1 MSamples/s, 12 bit, single-ended, internal 2.5 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B | — | 76 | — | dBc |
| | | 1 MSamples/s, 12 bit, single-ended, $V_{DD}$ reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B | — | 76 | — | dBc |
| | | 1 MSamples/s, 12 bit, differential, internal 1.25 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B | — | 78 | — | dBc |
| | | 1 MSamples/s, 12 bit, differential, internal 2.5 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B | — | 77 | — | dBc |
| | | 1 MSamples/s, 12 bit, differential, $V_{DD}$ reference, ADC_CLK= 13 MHz, BIASPROG = 0xF4B | — | 76 | — | dBc |
| | | 1 MSamples/s, 12 bit, differential, $2xV_{DD}$ reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B | 68 | 79 | — | dBc |
| | | 1 MSamples/s, 12 bit, differential, 5 V reference, ADC_CLK =13 MHz, BIASPROG = 0xF4B | — | 79 | — | dBc |
| | | 200 kSamples/s, 12 bit, single-ended, internal 1.25 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 75 | — | dBc |
| | | 200 kSamples/s, 12 bit, single-ended, internal 2.5 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 75 | — | dBc |
| | | 200 kSamples/s, 12 bit, single-ended, $V_{DD}$ reference, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 76 | — | dBc |
| | | 200 kSamples/s, 12 bit, differential, internal 1.25 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 79 | — | dBc |
| | | 200 kSamples/s, 12 bit, differential, internal 2.5 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 79 | — | dBc |
| | | 200 kSamples/s, 12 bit, differential, 5 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 78 | — | dBc |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Spurious-Free Dynamic Range (SFDR) | $SFDR_{ADC}$ | 200 kSamples/s, 12 bit, differential, $V_{DD}$ reference, ADC_CLK = 7 MHz, BIASPROG = 0x747 | 68 | 79 | — | dBc |
| | | 200 kSamples/s, 12 bit, differential, 2x$V_{DD}$ reference,ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 79 | — | dBc |
| Offset voltage | $V_{ADCOFFSET}$ | After calibration, single-ended | — | 0.3 | — | mV |
| | | After calibration, differential | -4 | 0.3 | 4 | mV |
| Thermometer output gradient | $TGRAD_{ADCTH}$ | | — | -1.92 | — | mV/°C |
| | | | — | -6.3 | — | ADC Codes/°C |
| Differential non-linearity (DNL) | $DNL_{ADC}$ | $V_{DD}$= 3.0 V, external 2.5V reference | -1 | ±0.7 | 4 | LSB |
| Integral non-linearity (INL), End point method | $INL_{ADC}$ | $V_{DD}$= 3.0 V, external 2.5V reference | — | ±1.6 | ±3 | LSB |
| Missing codes | $MC_{ADC}$ | | — | — | 3 | LSB |
| Gain error drift | $GAIN_{ED}$ | 1.25 V reference | — | 0.01[2] | 0.033[3] | %/°C |
| | | 2.5 V reference | — | 0.01[2] | 0.03[3] | %/°C |
| Offset error drift | $OFFSET_{ED}$ | 1.25 V reference | — | 0.00[2] | 0.06[3] | LSB/°C |
| | | 2.5 V reference | — | 0.00[2] | 0.04[3] | LSB/°C |
| VREF voltage | $V_{REF}$ | 1.25 V reference | 1.2 | 1.25 | 1.3 | V |
| | | 2.5 V reference | 2.4 | 2.5 | 2.6 | V |
| VREF voltage drift | $V_{REF_VDRIFT}$ | 1.25 V reference | -12.4 | 2.9 | 18.2 | mV/V |
| | | 2.5 V reference, VDD > 2.5 V | -24.6 | 5.7 | 35.2 | mV/V |
| VREF temperature drift | $V_{REF_TDRIFT}$ | 1.25 V reference | -132 | 272 | 677 | µV/°C |
| | | 2.5 V reference | -231 | 545 | 1271 | µV/°C |
| VREF current consumption | $I_{VREF}$ | 1.25 V reference | — | 67 | 114 | µA |
| | | 2.5 V reference | — | 55 | 82 | µA |
| ADC and DAC VREF matching | $V_{REF_MATCH}$ | 1.25 V reference | — | 99.85 | — | % |
| | | 2.5 V reference | — | 100.01 | — | % |

**Note:**

1. Includes required contribution from the voltage reference.
2. Typical numbers given by abs(Mean) / (85 - 25).
3. Max number given by (abs(Mean) + 3x stddev) / (85 - 25).

The integral non-linearity (INL) and differential non-linearity parameters are explained in the following two figures.

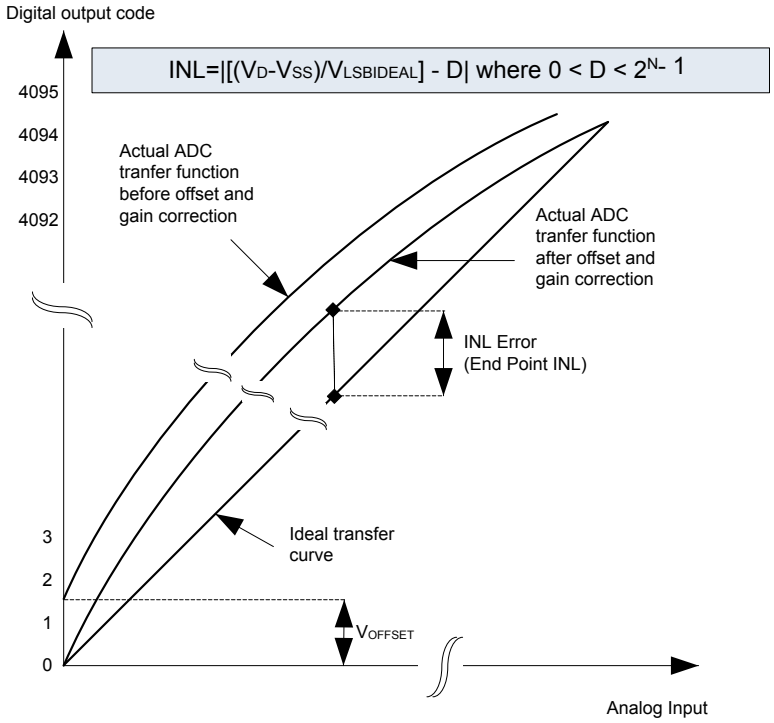



**Figure 4.26. Integral Non-Linearity (INL)**

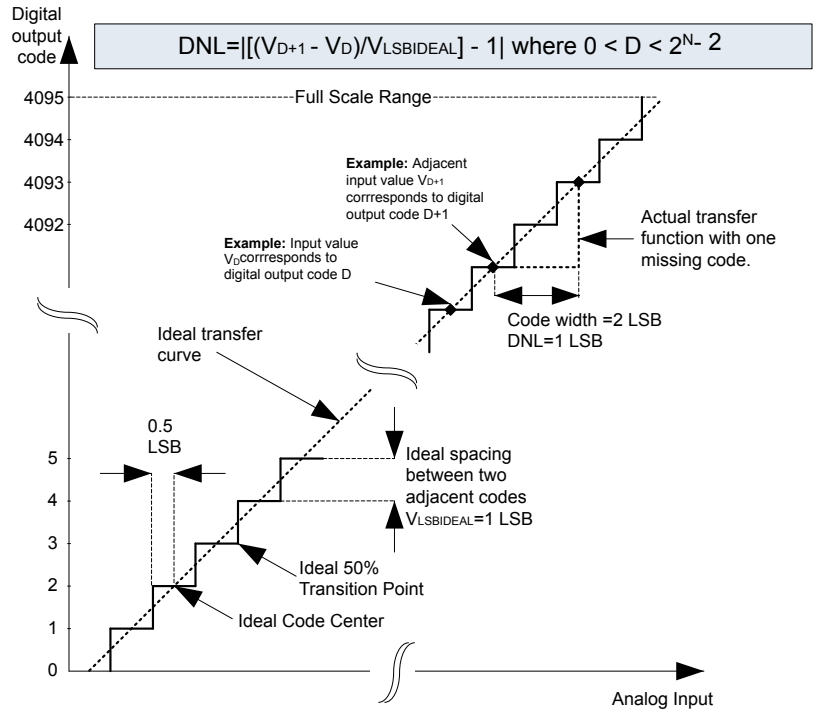



**Figure 4.27. Differential Non-Linearity (DNL)**

### 4.11.1 Typical Performance

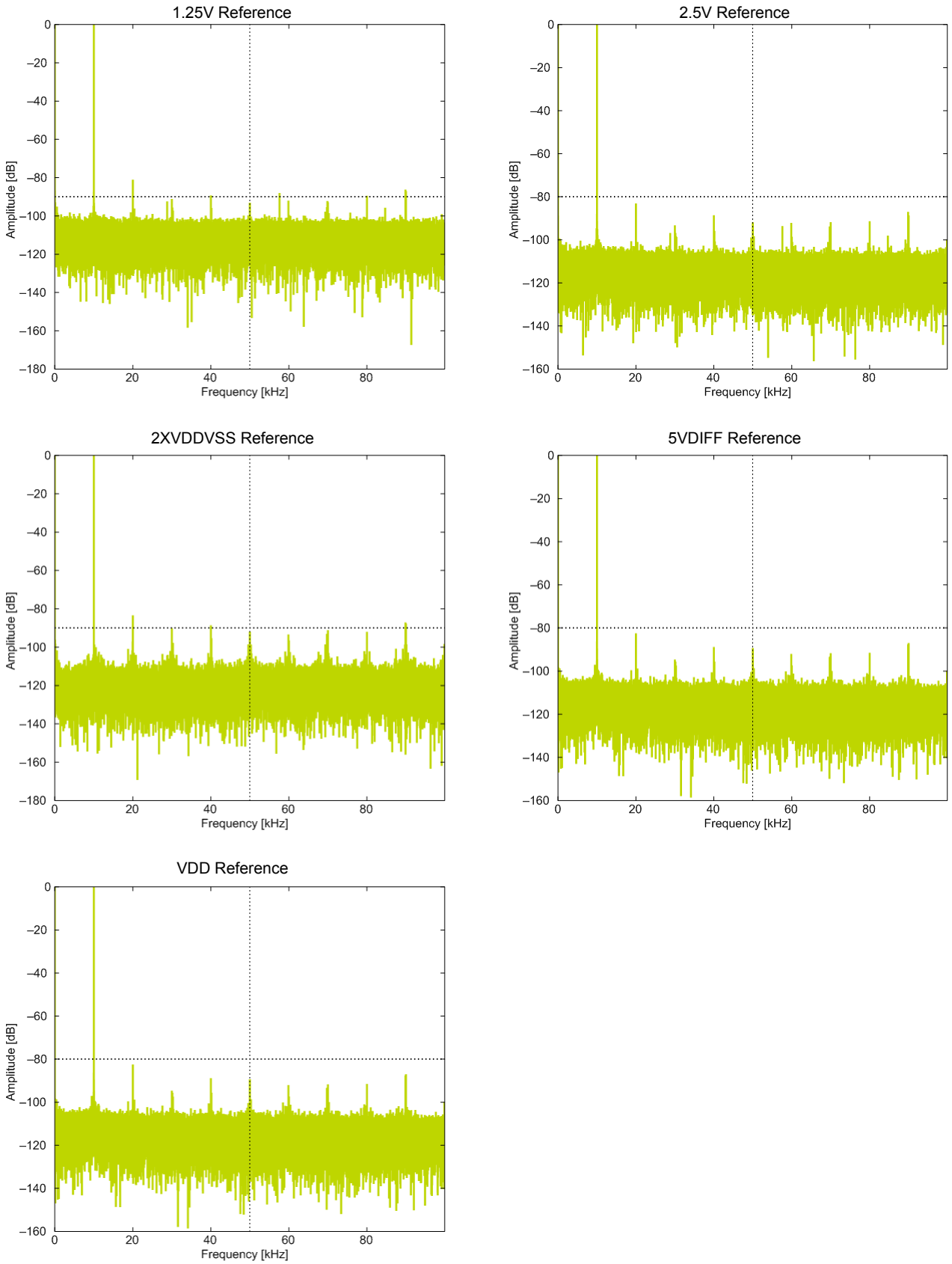



**Figure 4.28. ADC Frequency Spectrum, VDD = 3 V, Temp = 25 °C**

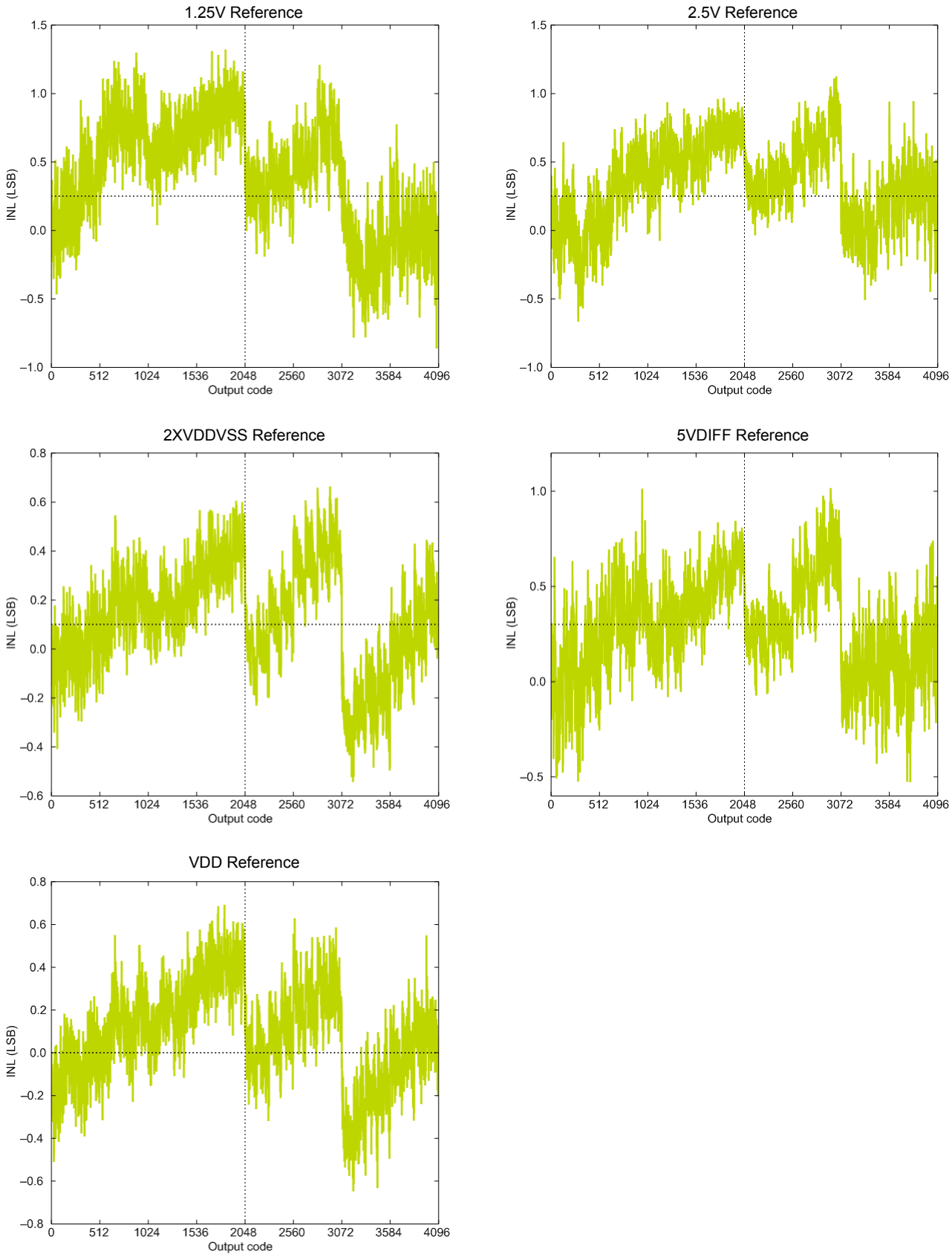



**Figure 4.29. ADC Integral Linearity Error vs Code, VDD = 3 V, Temp = 25 °C**

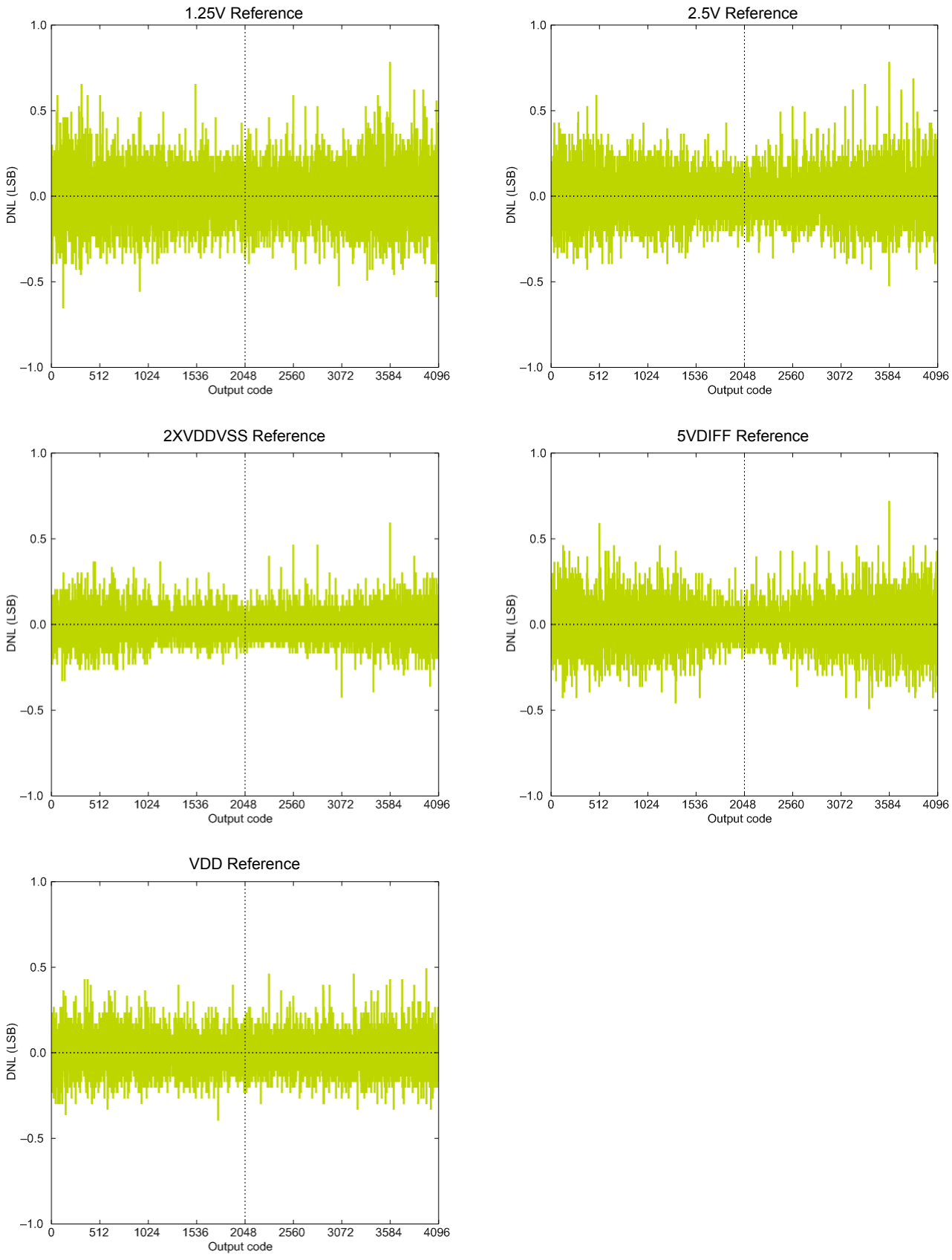



**Figure 4.30. ADC Differential Linearity Error vs Code, VDD = 3 V, Temp = 25 °C**

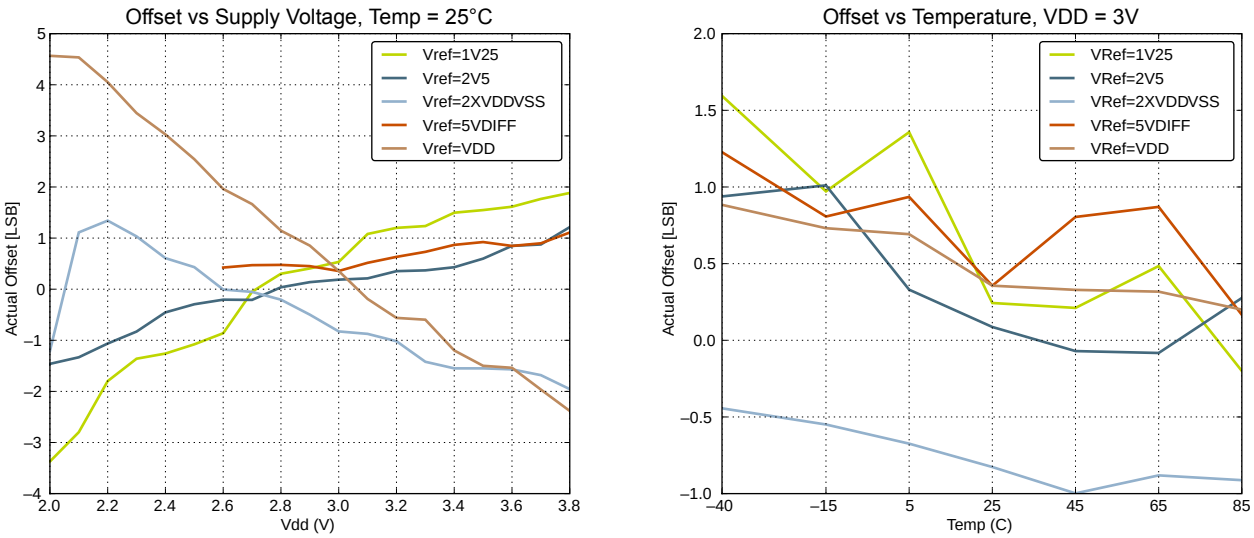



**Figure 4.31. ADC Absolute Offset, Common Mode = VDD/2**

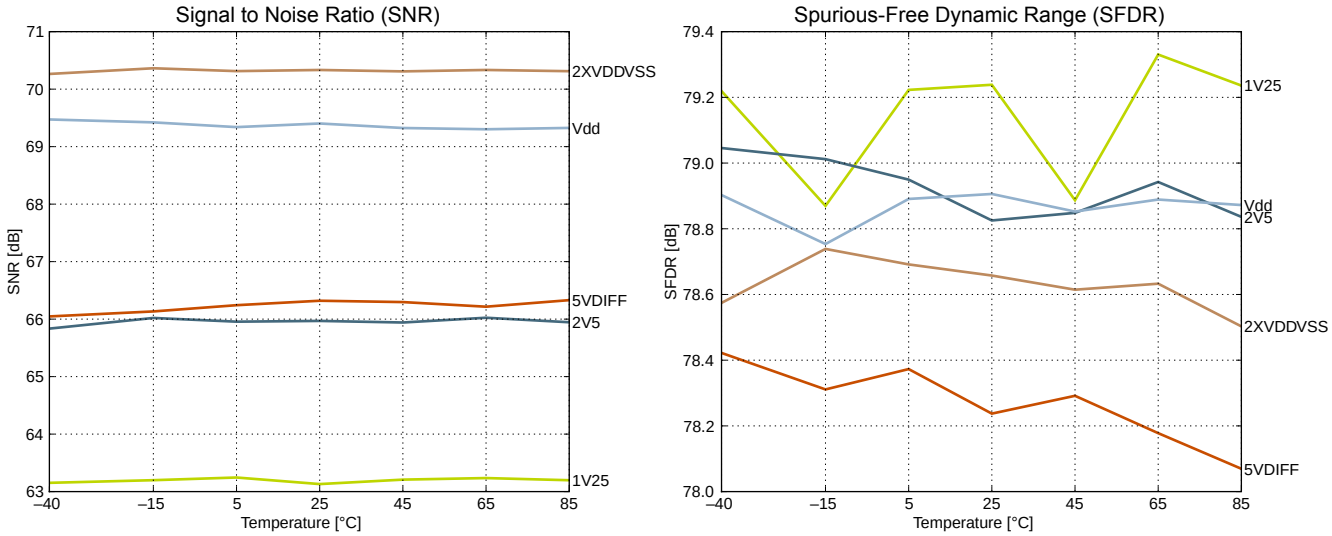



**Figure 4.32. ADC Dynamic Performance vs Temperature for all ADC References, VDD = 3 V**

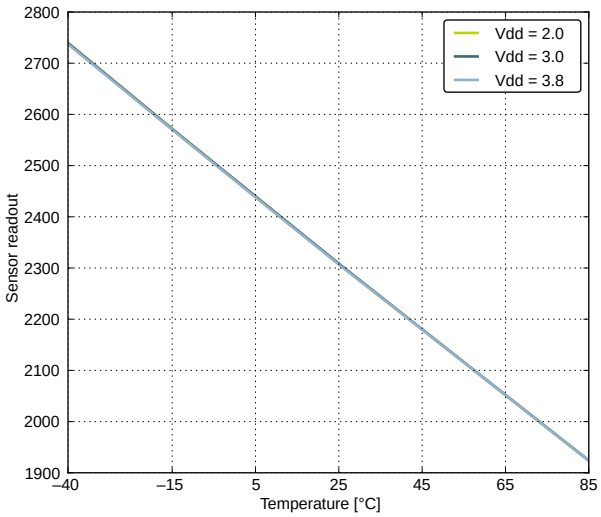



**Figure 4.33. ADC Temperature Sensor Readout**

## 4.12 Current Digital Analog Converter (IDAC)

**Table 4.17. IDAC Range 0 Source**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Active current with STEP-SEL=0x10 | $I_{IDAC}$ | EM0, default settings | — | 13.0 | — | µA |
| | | Duty-cycled | — | 10 | — | nA |
| Nominal IDAC output current with STEPSEL=0x10 | $I_{0x10}$ | | — | 0.85 | — | µA |
| Step size | $I_{STEP}$ | | — | 0.05 | — | µA |
| Current drop at high impedance load | $I_D$ | $V_{IDAC_OUT}$ = VDD - 100mV | — | 0.79 | — | % |
| Temperature coefficient | $TC_{IDAC}$ | VDD = 3.0V, STEPSEL=0x10 | — | 0.3 | — | nA/°C |
| Voltage coefficient | $VC_{IDAC}$ | T = 25°C, STEPSEL=0x10 | — | 11.7 | — | nA/V |

**Table 4.18. IDAC Range 0 Sink**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Active current with STEP-SEL=0x10 | $I_{IDAC}$ | EM0, default settings | — | 15.1 | — | µA |
| Nominal IDAC output current with STEPSEL=0x10 | $I_{0x10}$ | | — | 0.85 | — | µA |
| Step size | $I_{STEP}$ | | — | 0.05 | — | µA |
| Current drop at high impedance load | $I_D$ | $V_{IDAC_OUT}$ = 200mV | — | 0.30 | — | % |
| Temperature coefficient | $TC_{IDAC}$ | VDD = 3.0V, STEPSEL=0x10 | — | 0.2 | — | nA/°C |
| Voltage coefficient | $VC_{IDAC}$ | T = 25°C, STEPSEL=0x10 | — | 12.5 | — | nA/V |

**Table 4.19. IDAC Range 1 Source**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Active current with STEP-SEL=0x10 | $I_{IDAC}$ | EM0, default settings | — | 14.4 | — | µA |
| | | Duty-cycled | — | 10 | — | nA |
| Nominal IDAC output current with STEPSEL=0x10 | $I_{0x10}$ | | — | 3.2 | — | µA |
| Step size | $I_{STEP}$ | | — | 0.1 | — | µA |
| Current drop at high impedance load | $I_D$ | $V_{IDAC_OUT}$ = VDD - 100mV | — | 0.75 | — | % |
| Temperature coefficient | $TC_{IDAC}$ | VDD = 3.0V, STEPSEL=0x10 | — | 0.7 | — | nA/°C |
| Voltage coefficient | $VC_{IDAC}$ | T = 25°C, STEPSEL=0x10 | — | 38.4 | — | nA/V |

**Table 4.20. IDAC Range 1 Sink**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Active current with STEP-SEL=0x10 | $I_{IDAC}$ | EM0, default settings | — | 19.4 | — | µA |
| Nominal IDAC output current with STEPSEL=0x10 | $I_{0x10}$ | | — | 3.2 | — | µA |
| Step size | $I_{STEP}$ | | — | 0.1 | — | µA |
| Current drop at high impedance load | $I_D$ | $V_{IDAC_OUT}$ = 200mV | — | 0.32 | — | % |
| Temperature coefficient | $TC_{IDAC}$ | VDD = 3.0V, STEPSEL=0x10 | — | 0.7 | — | nA/°C |
| Voltage coefficient | $VC_{IDAC}$ | T = 25°C, STEPSEL=0x10 | — | 40.9 | — | nA/V |

**Table 4.21. IDAC Range 2 Source**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Active current with STEP-SEL=0x10 | $I_{IDAC}$ | EM0, default settings | — | 17.3 | — | µA |
| | | Duty-cycled | — | 10 | — | nA |
| Nominal IDAC output current with STEPSEL=0x10 | $I_{0x10}$ | | — | 8.5 | — | µA |
| Step size | $I_{STEP}$ | | — | 0.5 | — | µA |
| Current drop at high impedance load | $I_D$ | $V_{IDAC_OUT}$ = VDD - 100mV | — | 1.22 | — | % |
| Temperature coefficient | $TC_{IDAC}$ | VDD = 3.0V, STEPSEL=0x10 | — | 2.8 | — | nA/°C |
| Voltage coefficient | $VC_{IDAC}$ | T = 25°C, STEPSEL=0x10 | — | 96.6 | — | nA/V |

**Table 4.22. IDAC Range 2 Sink**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Active current with STEP-SEL=0x10 | $I_{IDAC}$ | EM0, default settings | — | 29.3 | — | µA |
| Nominal IDAC output current with STEPSEL=0x10 | $I_{0x10}$ | | — | 8.5 | — | µA |
| Step size | $I_{STEP}$ | | — | 0.5 | — | µA |
| Current drop at high impedance load | $I_D$ | $V_{IDAC_OUT}$ = 200mV | — | 0.62 | — | % |
| Temperature coefficient | $TC_{IDAC}$ | VDD = 3.0V, STEPSEL=0x10 | — | 2.8 | — | nA/°C |
| Voltage coefficient | $VC_{IDAC}$ | T = 25°C, STEPSEL=0x10 | — | 94.4 | — | nA/V |

**Table 4.23. IDAC Range 3 Source**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Active current with STEP-SEL=0x10 | $I_{IDAC}$ | EM0, default settings | — | 18.7 | — | µA |
| | | Duty-cycled | — | 10 | — | nA |
| Nominal IDAC output current with STEPSEL=0x10 | $I_{0x10}$ | | — | 33.9 | — | µA |
| Step size | $I_{STEP}$ | | — | 2.0 | — | µA |
| Current drop at high impedance load | $I_D$ | $V_{IDAC_OUT}$ = VDD - 100mV | — | 3.54 | — | % |
| Temperature coefficient | $TC_{IDAC}$ | VDD = 3.0V, STEPSEL=0x10 | — | 10.9 | — | nA/°C |
| Voltage coefficient | $VC_{IDAC}$ | T = 25°C, STEPSEL=0x10 | — | 159.5 | — | nA/V |

**Table 4.24. IDAC Range 3 Sink**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Active current with STEP-SEL=0x10 | $I_{IDAC}$ | EM0, default settings | — | 62.5 | — | µA |
| Nominal IDAC output current with STEPSEL=0x10 | $I_{0x10}$ | | — | 34.1 | — | µA |
| Step size | $I_{STEP}$ | | — | 2.0 | — | µA |
| Current drop at high impedance load | $I_D$ | $V_{IDAC_OUT}$ = 200mV | — | 1.75 | — | % |
| Temperature coefficient | $TC_{IDAC}$ | VDD = 3.0V, STEPSEL=0x10 | — | 10.9 | — | nA/°C |
| Voltage coefficient | $VC_{IDAC}$ | T = 25°C, STEPSEL=0x10 | — | 148.6 | — | nA/V |

**Table 4.25. IDAC**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Start-up time, from enabled to output settled | $t_{IDAC-START}$ | | — | 40 | — | µs |

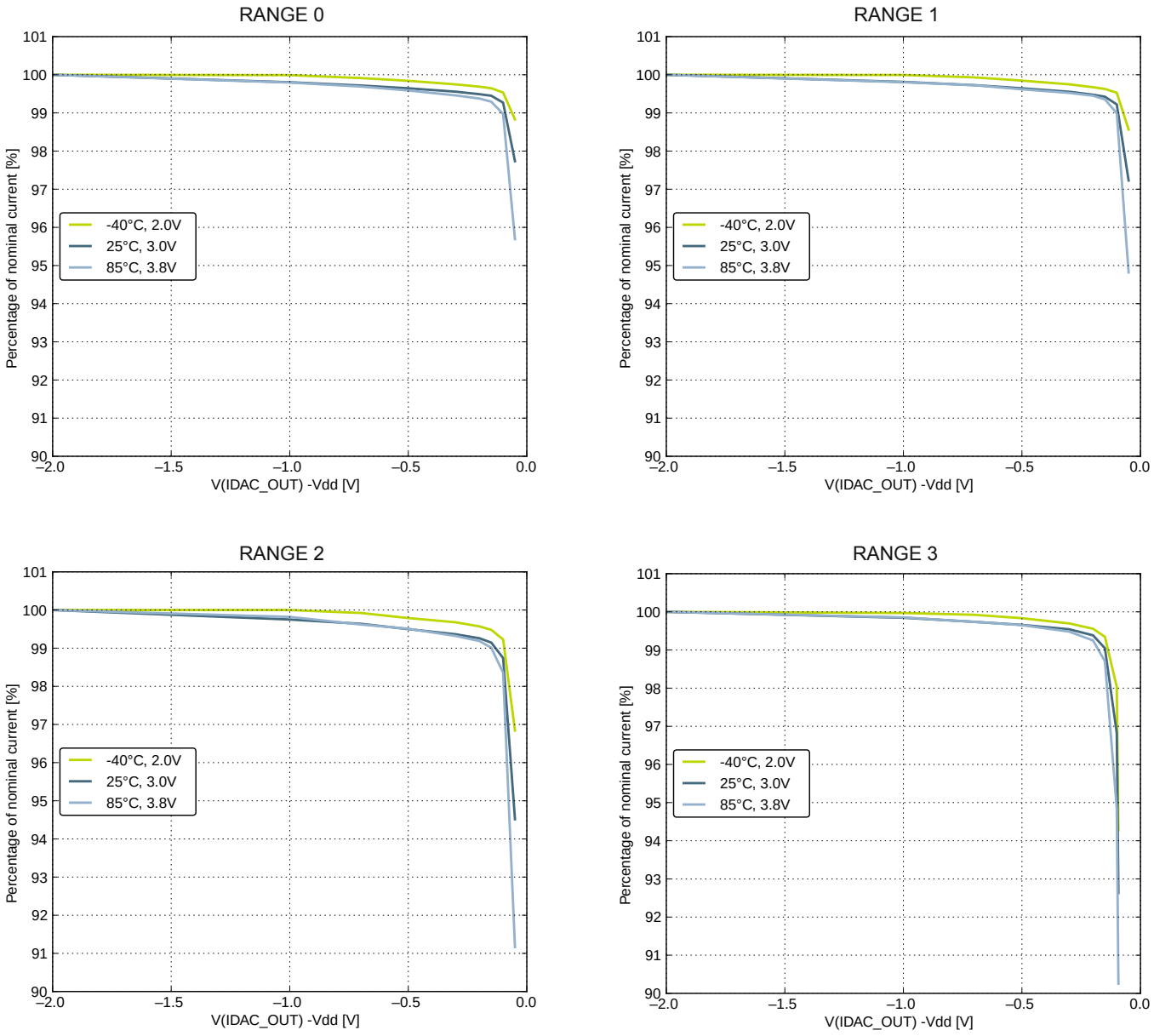



**Figure 4.34. IDAC Source Current as a function of voltage on IDAC_OUT**

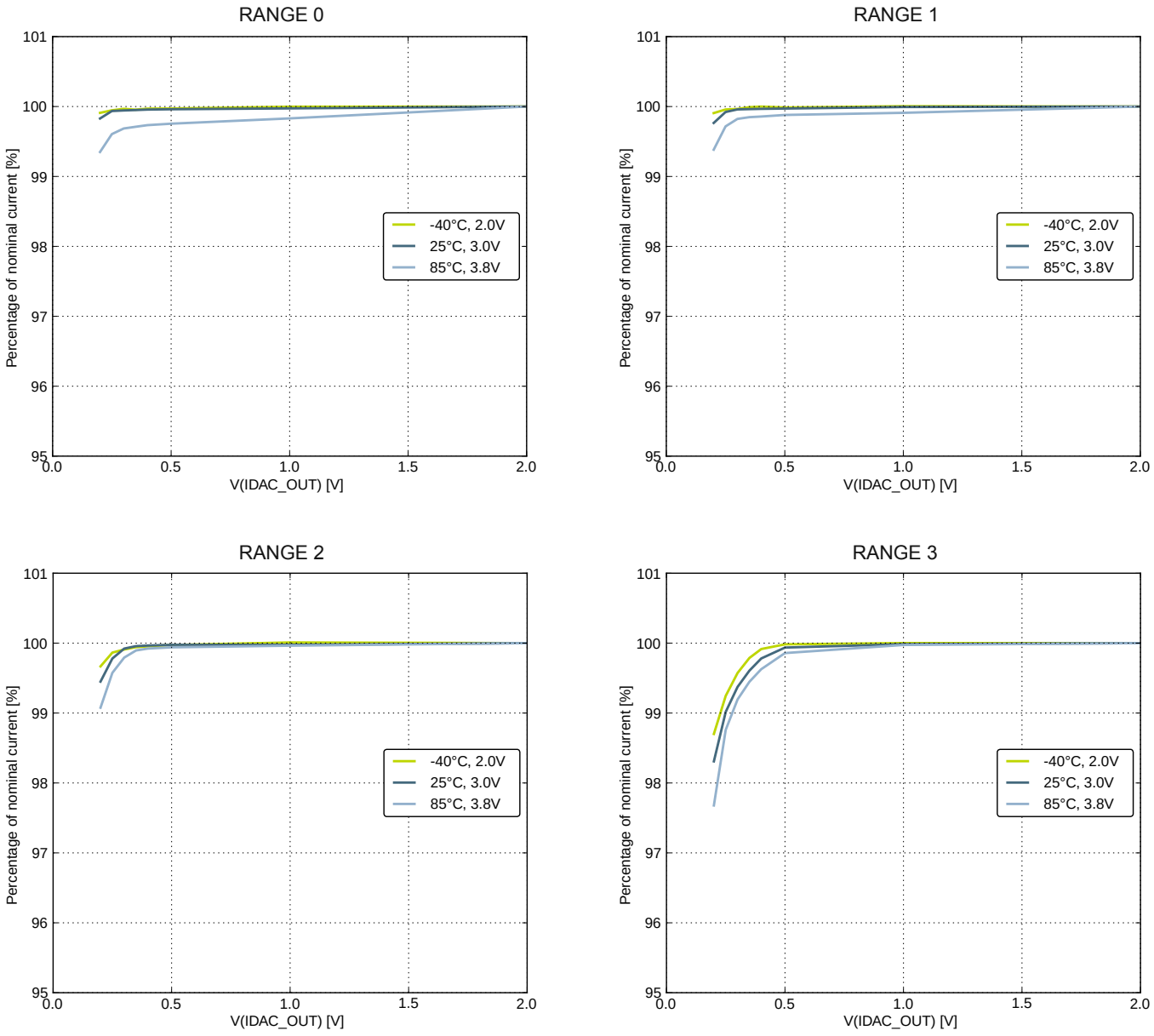



**Figure 4.35. IDAC Sink Current as a function of voltage on IDAC_OUT**

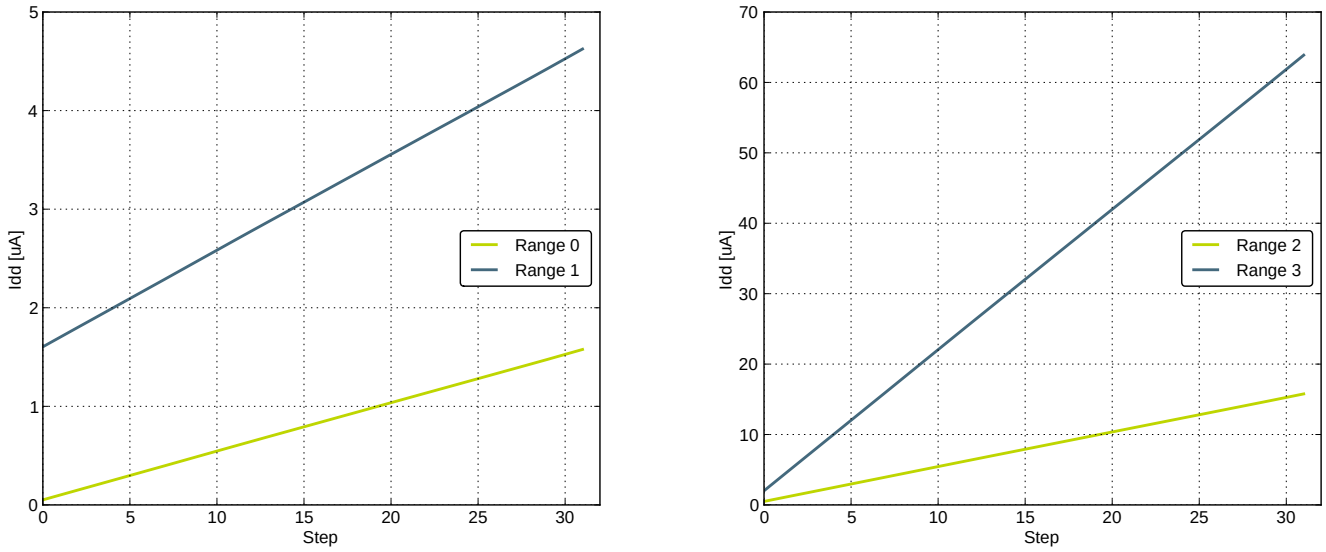



**Figure 4.36. IDAC Linearity**

### 4.13 Analog Comparator (ACMP)

**Table 4.26. ACMP**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input voltage range | $V_{ACMPIN}$ | | 0 | — | $V_{DD}$ | V |
| ACMP Common Mode voltage range | $V_{ACMPCM}$ | | 0 | — | $V_{DD}$ | V |
| Active current | $I_{ACMP}$ | BIASPROG=0b0000, FULLBIAS=0 and HALFBIAS=1 in ACMPn_CTRL register | — | 0.1 | 0.4 | µA |
| | | BIASPROG=0b1111, FULLBIAS= 0 and HALFBIAS=0 in ACMPn_CTRL register | — | 2.87 | 15 | µA |
| | | BIASPROG=0b1111, FULLBIAS= 1 and HALFBIAS=0 in ACMPn_CTRL register | — | 195 | 520 | µA |
| Current consumption of internal voltage reference | $I_{ACMPREF}$ | Internal voltage reference off. Using external voltage reference | — | 0 | — | µA |
| | | Internal voltage reference | — | 5 | — | µA |
| Offset voltage | $V_{ACMPOFFSET}$ | BIASPROG= 0b1010, FULLBIAS=0 and HALFBIAS=0 in ACMPn_CTRL register | -12 | 0 | 12 | mV |
| ACMP hysteresis | $V_{ACMPHYST}$ | Programmable | — | 17 | — | mV |
| Capacitive Sense Internal Resistance | $R_{CSRES}$ | CSRESSEL=0b00 in ACMPn_INPUTSEL | — | 40 | — | kΩ |
| | | CSRESSEL=0b01 in ACMPn_INPUTSEL | — | 70 | — | kΩ |
| | | CSRESSEL=0b10 in ACMPn_INPUTSEL | — | 101 | — | kΩ |
| | | CSRESSEL=0b11 in ACMPn_INPUTSEL | — | 132 | — | kΩ |
| Startup time | $t_{ACMPSTART}$ | | — | — | 10 | µs |

The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference as given in in the following equation. $I_{ACMPREF}$ is zero if an external voltage reference is used.

$$I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF}$$

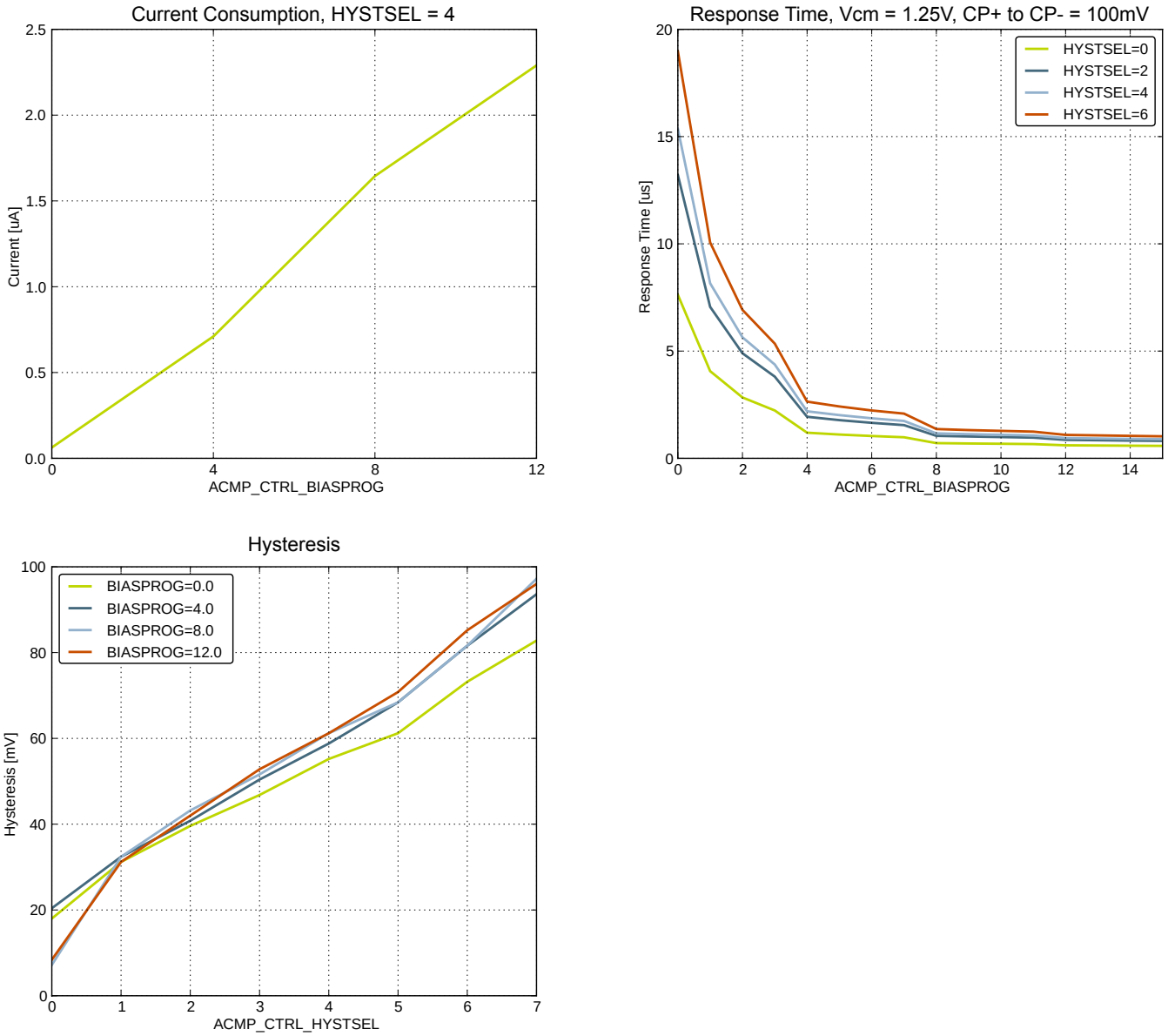



**Figure 4.37. ACMP Characteristics, Vdd = 3 V, Temp = 25 °C, FULLBIAS = 0, HALFBIAS = 1**

### 4.14 Voltage Comparator (VCMP)

**Table 4.27. VCMP**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input voltage range | $V_{VCMPIN}$ | | — | $V_{DD}$ | — | V |
| VCMP Common Mode voltage range | $V_{VCMPCM}$ | | — | $V_{DD}$ | — | V |
| Active current | $I_{VCMP}$ | BIASPROG=0b0000 and HALFBIAS=1 in VCMPn_CTRL register | — | 0.2 | 0.8 | µA |
| | | BIASPROG=0b1111 and HALFBIAS=0 in VCMPn_CTRL register. LPREF=0. | — | 22 | 35 | µA |
| Startup time reference generator | $t_{VCMPREF}$ | NORMAL | — | 10 | — | µs |
| Offset voltage | $V_{VCMPOFFSET}$ | Single-ended | — | 10 | — | mV |
| | | Differential | — | 10 | — | mV |
| VCMP hysteresis | $V_{VCMPHYST}$ | | — | 17 | — | mV |
| Startup time | $t_{VCMPSTART}$ | | — | — | 10 | µs |

The $V_{DD}$ trigger level can be configured by setting the TRIGLEVEL field of the VCMP_CTRL register in accordance with the following equation:

$$V_{\text{DD Trigger Level}} = 1.667V + 0.034 \times \text{TRIGLEVEL}$$

### 4.15 I2C

**Table 4.28. I2C Standard-mode (Sm)**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| SCL clock frequency | $f_{SCL}$ | 0 | — | 100[1] | kHz |
| SCL clock low time | $t_{LOW}$ | 4.7 | — | — | µs |
| SCL clock high time | $t_{HIGH}$ | 4.0 | — | — | µs |
| SDA set-up time | $t_{SU,DAT}$ | 250 | — | — | ns |
| SDA hold time | $t_{HD,DAT}$ | 8 | — | 3450[2,3] | ns |
| Repeated START condition set-up time | $t_{SU,STA}$ | 4.7 | — | — | µs |
| (Repeated) START condition hold time | $t_{HD,STA}$ | 4.0 | — | — | µs |
| STOP condition set-up time | $t_{SU,STO}$ | 4.0 | — | — | µs |
| Bus free time between a STOP and a START condition | $t_{BUF}$ | 4.7 | — | — | µs |

**Note:**
1. For the minimum HFPERCLK frequency required in Standard-mode, see the I2C chapter in the EFM32HG Reference Manual.
2. The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL ($t_{LOW}$).
3. When transmitting data, this number is guaranteed only when I2Cn_CLKDIV < ((3450*$10^{-9}$ [s] * $f_{HFPERCLK}$ [Hz]) - 5).

**Table 4.29. I2C Fast-mode (Fm)**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| SCL clock frequency | $f_{SCL}$ | 0 | — | 400[1] | kHz |
| SCL clock low time | $t_{LOW}$ | 1.3 | — | — | µs |
| SCL clock high time | $t_{HIGH}$ | 0.6 | — | — | µs |
| SDA set-up time | $t_{SU,DAT}$ | 100 | — | — | ns |
| SDA hold time | $t_{HD,DAT}$ | 8 | — | 900[2,3] | ns |
| Repeated START condition set-up time | $t_{SU,STA}$ | 0.6 | — | — | µs |
| (Repeated) START condition hold time | $t_{HD,STA}$ | 0.6 | — | — | µs |
| STOP condition set-up time | $t_{SU,STO}$ | 0.6 | — | — | µs |
| Bus free time between a STOP and a START condition | $t_{BUF}$ | 1.3 | — | — | µs |

**Note:**
1. For the minimum HFPERCLK frequency required in Fast-mode, see the I2C chapter in the EFM32HG Reference Manual.
2. The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL ($t_{LOW}$).
3. When transmitting data, this number is guaranteed only when I2Cn_CLKDIV < ((900*$10^{-9}$ [s] * $f_{HFPERCLK}$ [Hz]) - 5).

**Table 4.30. I2C Fast-mode Plus (Fm+)**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| SCL clock frequency | $f_{SCL}$ | 0 | — | 1000[1] | kHz |
| SCL clock low time | $t_{LOW}$ | 0.5 | — | — | µs |
| SCL clock high time | $t_{HIGH}$ | 0.26 | — | — | µs |
| SDA set-up time | $t_{SU,DAT}$ | 50 | — | — | ns |
| SDA hold time | $t_{HD,DAT}$ | 8 | — | — | ns |
| Repeated START condition set-up time | $t_{SU,STA}$ | 0.26 | — | — | µs |
| (Repeated) START condition hold time | $t_{HD,STA}$ | 0.26 | — | — | µs |
| STOP condition set-up time | $t_{SU,STO}$ | 0.26 | — | — | µs |
| Bus free time between a STOP and a START condition | $t_{BUF}$ | 0.5 | — | — | µs |

**Note:**
1. For the minimum HFPERCLK frequency required in Fast-mode Plus, see the I2C chapter in the EFM32HG Reference Manual.

### 4.16 USB

The USB hardware in the EFM32HG passes all tests for USB 2.0 Full Speed certification. The test report will be distributed with application note *AN0046 - USB Hardware Design Guide* when ready.

**Table 4.31. USB**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| USB regulator output voltage | $V_{USBOUT}$ | | 3.1 | 3.4 | 3.7 | V |
| USB regulator output current | $I_{USBOUT}$ | BIASPROG=0, $T_{AMB}$=25°C | 55.7 | 79.4 | 104.1 | mA |
| | | BIASPROG=1, $T_{AMB}$=25°C | 66.0 | 95.9 | 126.4 | mA |
| | | BIASPROG=2, $T_{AMB}$=25°C | 94.6 | 146.5 | 188.1 | mA |
| | | BIASPROG=3, $T_{AMB}$=25°C | 80.4 | 128.3 | 176.0 | mA |

### 4.17 Digital Peripherals

**Table 4.32. Digital Peripherals**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| USART current | $I_{USART}$ | USART idle current, clock enabled | — | 7.5 | — | µA/MHz |
| LEUART current | $I_{LEUART}$ | LEUART idle current, clock enabled | — | 150 | — | nA |
| I2C current | $I_{I2C}$ | I2C idle current, clock enabled | — | 6.25 | — | µA/MHz |
| TIMER current | $I_{TIMER}$ | TIMER_0 idle current, clock enabled | — | 8.75 | — | µA/MHz |
| PCNT current | $I_{PCNT}$ | PCNT idle current, clock enabled | — | 100 | — | nA |
| RTC current | $I_{RTC}$ | RTC idle current, clock enabled | — | 100 | — | nA |
| AES current | $I_{AES}$ | AES idle current, clock enabled | — | 2.5 | — | µA/MHz |
| GPIO current | $I_{GPIO}$ | GPIO idle current, clock enabled | — | 5.31 | — | µA/MHz |
| PRS current | $I_{PRS}$ | PRS idle current | — | 2.81 | — | µA/MHz |
| DMA current | $I_{DMA}$ | Clock enable | — | 8.12 | — | µA/MHz |

# 5. Pin Definitions

**Note:** Please refer to the application note *AN0002 EFM32 Hardware Design Considerations* for guidelines on designing Printed Circuit Boards (PCBs) for the EFM32HG.

## 5.1 EFM32HG108 (QFN24)

### 5.1.1 Pinout

The EFM32HG108 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

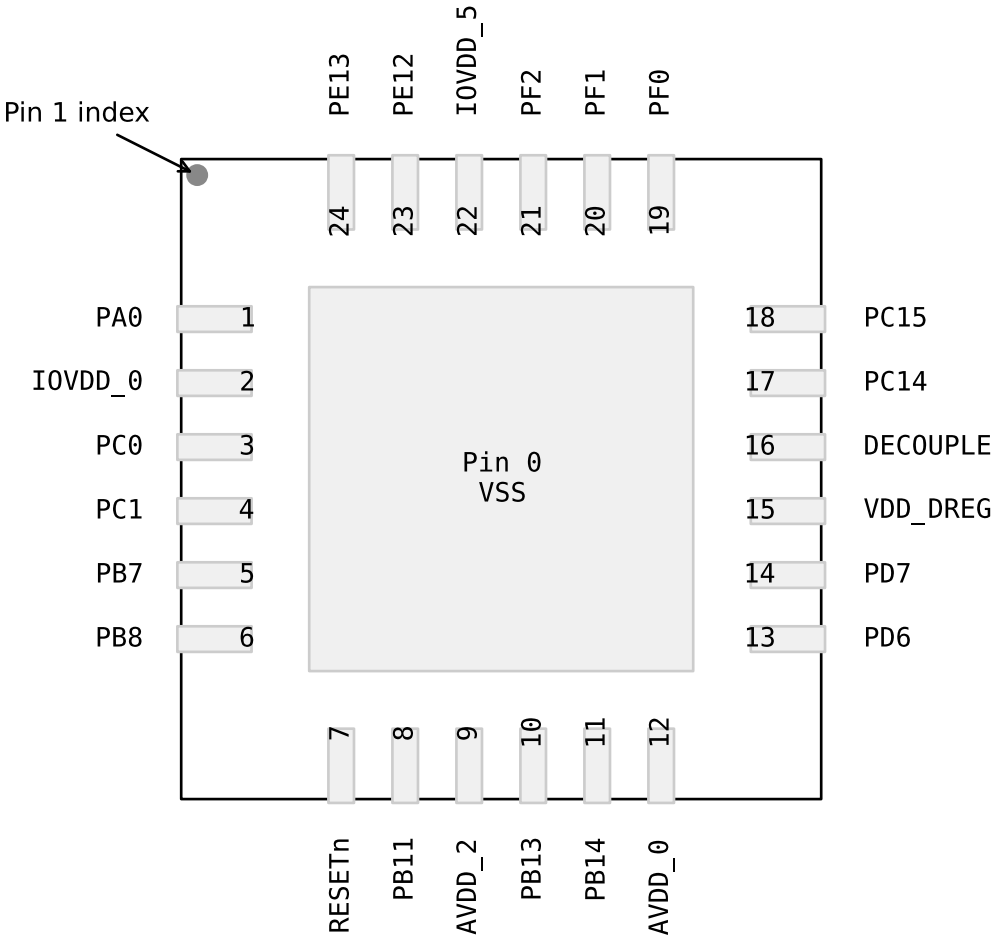



**Figure 5.1. EFM32HG108 Pinout (top view, not to scale)**

**Table 5.1. Device Pinout**

| QFN24 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 0 | VSS | Ground. | | | |
| 1 | PA0 | | TIM0_CC1 #6<br>TIM0_CC0 #0/1/4<br>PCNT0_S0IN #4 | US1_RX #4<br>LEU0_RX #4<br>I2C0_SDA #0 | PRS_CH0 #0<br>PRS_CH3 #3<br>GPIO_EM4WU0 |
| 2 | IOVDD_0 | Digital IO power supply 0. | | | |

| QFN24 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 3 | PC0 | ACMP0_CH0 | TIM0_CC1 #4<br>PCNT0_S0IN #2 | US0_TX #5/6<br>US1_TX #0<br>US1_CS #5<br>I2C0_SDA #4 | PRS_CH2 #0 |
| 4 | PC1 | ACMP0_CH1 | TIM0_CC2 #4<br>PCNT0_S1IN #2 | US0_RX #5/6<br>US1_TX #5<br>US1_RX #0<br>I2C0_SCL #4 | PRS_CH3 #0 |
| 5 | PB7 | LFXTAL_P | TIM1_CC0 #3 | US0_TX #4<br>US1_CLK #0 | |
| 6 | PB8 | LFXTAL_N | TIM1_CC1 #3 | US0_RX #4<br>US1_CS #0 | |
| 7 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | |
| 8 | PB11 | | TIM1_CC2 #3<br>PCNT0_S1IN #4 | US1_CLK #4 | CMU_CLK1 #3<br>ACMP0_O #3 |
| 9 | AVDD_2 | Analog power supply 2. | | | |
| 10 | PB13 | HFXTAL_P | | US0_CLK #4/5<br>LEU0_TX #1 | |
| 11 | PB14 | HFXTAL_N | | US0_CS #4/5<br>LEU0_RX #1 | |
| 12 | AVDD_0 | Analog power supply 0. | | | |
| 13 | PD6 | | TIM1_CC0 #4<br>PCNT0_S0IN #3 | US1_RX #2/3<br>I2C0_SDA #1 | ACMP_O #2 |
| 14 | PD7 | | TIM1_CC1 #4<br>PCNT0_S1IN #3 | US1_TX #2/3<br>I2C0_SCL #1 | CMU_CLK0 #2 |
| 15 | VDD_DREG | Power supply for on-chip voltage regulator. | | | |
| 16 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin. | | | |
| 17 | PC14 | | TIM0_CDTI1 #1/6<br>TIM1_CC1 #0<br>PCNT0_S1IN #0 | US0_CS #3<br>US1_CS #3/4<br>LEU0_TX #5 | PRS_CH0 #2 |
| 18 | PC15 | | TIM0_CDTI2 #1/6<br>TIM1_CC2 #0 | US0_CLK #3<br>US1_CLK #3<br>LEU0_RX #5 | PRS_CH1 #2 |

| QFN24 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 19 | PF0 | | TIM0_CC0 #5 | US1_CLK #2<br>LEU0_TX #3<br>I2C0_SDA #5 | DBG_SWCLK #0<br>BOOT_TX |
| 20 | PF1 | | TIM0_CC1 #5 | US1_CS #2<br>LEU0_RX #3<br>I2C0_SCL #5 | DBG_SWDIO #0<br>GPIO_EM4WU3<br>BOOT_RX |
| 21 | PF2 | | TIM0_CC2 #5/6<br>TIM2_CC0 #3 | US1_TX #4<br>LEU0_TX #4 | CMU_CLK0 #3<br>PRS_CH0 #3<br>GPIO_EM4WU4 |
| 22 | IOVDD_5 | Digital IO power supply 5. | | | |
| 23 | PE12 | | TIM1_CC2 #1<br>TIM2_CC1 #3 | US0_RX #3<br>US0_CLK #0/6<br>I2C0_SDA #6 | CMU_CLK1 #2<br>PRS_CH1 #3 |
| 24 | PE13 | | TIM2_CC2 #3 | US0_TX #3<br>US0_CS #0/6<br>I2C0_SCL #6 | ACMP0_O #0<br>PRS_CH2 #3<br>GPIO_EM4WU5 |

### 5.1.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

**Note:** Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

**Table 5.2. Alternate functionality overview**

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ACMP0_CH0 | PC0 | | | | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH1 | PC1 | | | | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_O | PE13 | | PD6 | PB11 | | | | Analog comparator ACMP0, digital output. |
| BOOT_RX | PF1 | | | | | | | Bootloader RX. |
| BOOT_TX | PF0 | | | | | | | Bootloader TX. |
| CMU_CLK0 | | | PD7 | PF2 | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | | | PE12 | PB11 | | | | Clock Management Unit, clock output number 1. |
| DBG_SWCLK | PF0 | | | | | | | Debug-interface Serial Wire clock input.<br>Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | | | | | | | Debug-interface Serial Wire data input / output.<br>Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| GPIO_EM4WU0 | PA0 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU3 | PF1 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | PF2 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU5 | PE13 | | | | | | | Pin can be used to wake the system up from EM4 |
| HFXTAL_N | PB14 | | | | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | | PD7 | | | PC1 | PF1 | PE13 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | | | PC0 | PF0 | PE12 | I2C0 Serial Data input / output. |
| LEU0_RX | | PB14 | | PF1 | PA0 | PC15 | | LEUART0 Receive input. |
| LEU0_TX | | PB13 | | PF0 | PF2 | PC14 | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | | | PC0 | PD6 | PA0 | | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | PC14 | | PC1 | PD7 | PB11 | | | Pulse Counter PCNT0 input number 1. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| PRS_CH0 | PA0 | | PC14 | PF2 | | | | Peripheral Reflex System PRS, channel 0. |
| PRS_CH1 | | | PC15 | PE12 | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | PC0 | | | PE13 | | | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | PC1 | | | PA0 | | | | Peripheral Reflex System PRS, channel 3. |
| TIM0_CC0 | PA0 | PA0 | | | PA0 | PF0 | | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | | | | | PC0 | PF1 | PA0 | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | | | | | PC1 | PF2 | PF2 | Timer 0 Capture Compare input / output channel 2. |
| TIM0_CDTI1 | | PC14 | | | | | PC14 | Timer 0 Complimentary Dead Time Insertion channel 1. |
| TIM0_CDTI2 | | PC15 | | | | | PC15 | Timer 0 Complimentary Dead Time Insertion channel 2. |
| TIM1_CC0 | | | | PB7 | PD6 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | | | PB8 | PD7 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | | PB11 | | | | Timer 1 Capture Compare input / output channel 2. |
| TIM2_CC0 | | | | PF2 | | | | Timer 2 Capture Compare input / output channel 0. |
| TIM2_CC1 | | | | PE12 | | | | Timer 2 Capture Compare input / output channel 1. |
| TIM2_CC2 | | | | PE13 | | | | Timer 2 Capture Compare input / output channel 2. |
| US0_CLK | PE12 | | | PC15 | PB13 | PB13 | PE12 | USART0 clock input / output. |
| US0_CS | PE13 | | | PC14 | PB14 | PB14 | PE13 | USART0 chip select input / output. |
| US0_RX | | | | PE12 | PB8 | PC1 | PC1 | USART0 Asynchronous Receive.<br>USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | | | | PE13 | PB7 | PC0 | PC0 | USART0 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | | PF0 | PC15 | PB11 | | | USART1 clock input / output. |
| US1_CS | PB8 | | PF1 | PC14 | PC14 | PC0 | | USART1 chip select input / output. |
| US1_RX | PC1 | | PD6 | PD6 | PA0 | | | USART1 Asynchronous Receive.<br>USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | PC0 | | PD7 | PD7 | PF2 | PC1 | | USART1 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART1 Synchronous mode Master Output / Slave Input (MOSI). |

### 5.1.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32HG108 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

**Table 5.3. GPIO Pinout**

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Port A | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | PA0 |
| Port B | - | PB14 | PB13 | - | PB11 | - | - | PB8 | PB7 | - | - | - | - | - | - | - |
| Port C | PC15 | PC14 | - | - | - | - | - | - | - | - | - | - | - | - | PC1 | PC0 |
| Port D | - | - | - | - | - | - | - | - | PD7 | PD6 | - | - | - | - | - | - |
| Port E | - | - | PE13 | PE12 | - | - | - | - | - | - | - | - | - | - | - | - |
| Port F | - | - | - | - | - | - | - | - | - | - | - | - | - | PF2 | PF1 | PF0 |

## 5.2 EFM32HG110 (QFN24)

### 5.2.1 Pinout

The EFM32HG110 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

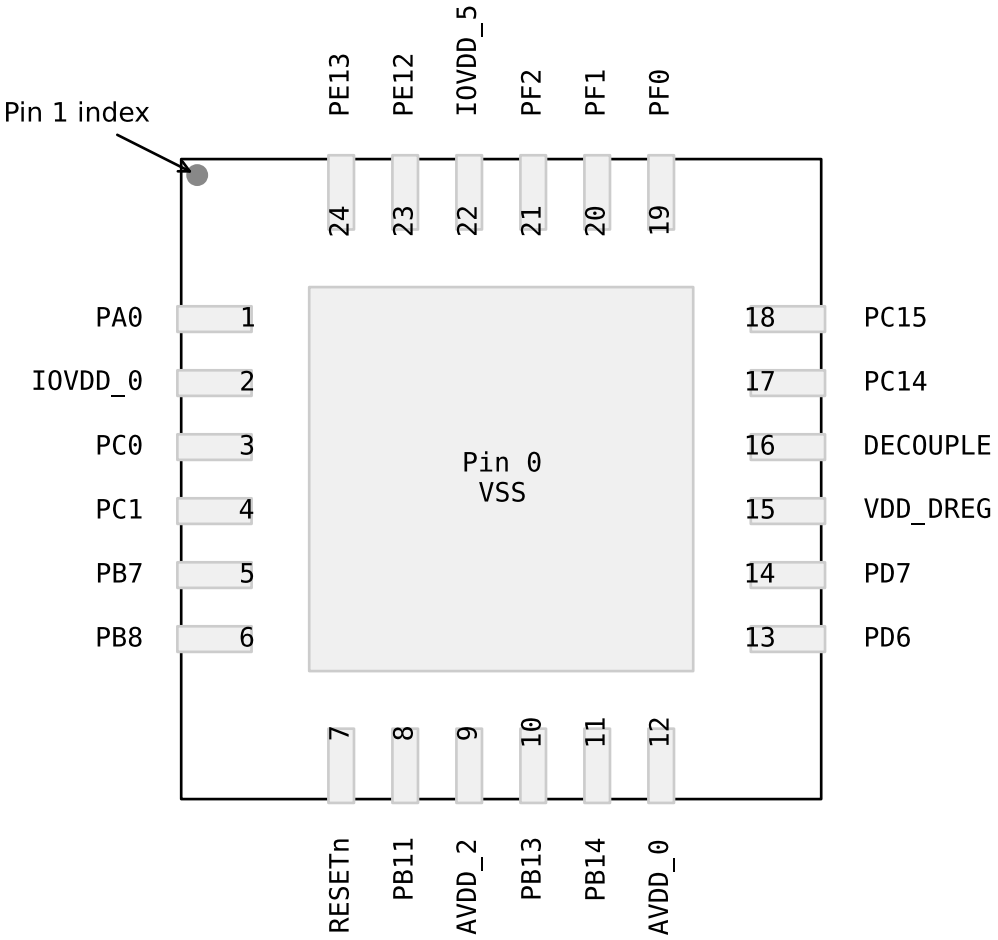



**Figure 5.2. EFM32HG110 Pinout (top view, not to scale)**

**Table 5.4. Device Pinout**

| QFN24 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 0 | VSS | Ground. | | | |
| 1 | PA0 | | TIM0_CC1 #6<br>TIM0_CC0 #0/1/4<br>PCNT0_S0IN #4 | US1_RX #4<br>LEU0_RX #4<br>I2C0_SDA #0 | PRS_CH0 #0<br>PRS_CH3 #3<br>GPIO_EM4WU0 |
| 2 | IOVDD_0 | Digital IO power supply 0. | | | |

| QFN24 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 3 | PC0 | ACMP0_CH0 | TIM0_CC1 #4<br>PCNT0_S0IN #2 | US0_TX #5/6<br>US1_TX #0<br>US1_CS #5<br>I2C0_SDA #4 | PRS_CH2 #0 |
| 4 | PC1 | ACMP0_CH1 | TIM0_CC2 #4<br>PCNT0_S1IN #2 | US0_RX #5/6<br>US1_TX #5<br>US1_RX #0<br>I2C0_SCL #4 | PRS_CH3 #0 |
| 5 | PB7 | LFXTAL_P | TIM1_CC0 #3 | US0_TX #4<br>US1_CLK #0 | |
| 6 | PB8 | LFXTAL_N | TIM1_CC1 #3 | US0_RX #4<br>US1_CS #0 | |
| 7 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | |
| 8 | PB11 | IDAC0_OUT | TIM1_CC2 #3<br>PCNT0_S1IN #4 | US1_CLK #4 | CMU_CLK1 #3<br>ACMP0_O #3 |
| 9 | AVDD_2 | Analog power supply 2. | | | |
| 10 | PB13 | HFXTAL_P | | US0_CLK #4/5<br>LEU0_TX #1 | |
| 11 | PB14 | HFXTAL_N | | US0_CS #4/5<br>LEU0_RX #1 | |
| 12 | AVDD_0 | Analog power supply 0. | | | |
| 13 | PD6 | ADC_CH6 | TIM1_CC0 #4<br>PCNT0_S0IN #3 | US1_RX #2/3<br>I2C0_SDA #1 | ACMP_O #2 |
| 14 | PD7 | ADC_CH7 | TIM1_CC1 #4<br>PCNT0_S1IN #3 | US1_TX #2/3<br>I2C0_SCL #1 | CMU_CLK0 #2 |
| 15 | VDD_DREG | Power supply for on-chip voltage regulator. | | | |
| 16 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin. | | | |
| 17 | PC14 | | TIM0_CDTI1 #1/6<br>TIM1_CC1 #0<br>PCNT0_S1IN #0 | US0_CS #3<br>US1_CS #3/4<br>LEU0_TX #5 | PRS_CH0 #2 |
| 18 | PC15 | | TIM0_CDTI2 #1/6<br>TIM1_CC2 #0 | US0_CLK #3<br>US1_CLK #3<br>LEU0_RX #5 | PRS_CH1 #2 |

| QFN24 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 19 | PF0 | | TIM0_CC0 #5 | US1_CLK #2<br>LEU0_TX #3<br>I2C0_SDA #5 | DBG_SWCLK #0<br>BOOT_TX |
| 20 | PF1 | | TIM0_CC1 #5 | US1_CS #2<br>LEU0_RX #3<br>I2C0_SCL #5 | DBG_SWDIO #0<br>GPIO_EM4WU3<br>BOOT_RX |
| 21 | PF2 | | TIM0_CC2 #5/6<br>TIM2_CC0 #3 | US1_TX #4<br>LEU0_TX #4 | CMU_CLK0 #3<br>PRS_CH0 #3<br>GPIO_EM4WU4 |
| 22 | IOVDD_5 | Digital IO power supply 5. | | | |
| 23 | PE12 | ADC0_CH0 | TIM1_CC2 #1<br>TIM2_CC1 #3 | US0_RX #3<br>US0_CLK #0/6<br>I2C0_SDA #6 | CMU_CLK1 #2<br>PRS_CH1 #3 |
| 24 | PE13 | ADC0_CH1 | TIM2_CC2 #3 | US0_TX #3<br>US0_CS #0/6<br>I2C0_SCL #6 | ACMP0_O #0<br>PRS_CH2 #3<br>GPIO_EM4WU5 |

### 5.2.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

**Note:** Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

**Table 5.5. Alternate functionality overview**

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ACMP0_CH0 | PC0 | | | | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH1 | PC1 | | | | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_O | PE13 | | PD6 | PB11 | | | | Analog comparator ACMP0, digital output. |
| ADC0_CH0 | PE12 | | | | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PE13 | | | | | | | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH6 | PD6 | | | | | | | Analog to digital converter ADC0, input channel number 6. |
| ADC0_CH7 | P7 | | | | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PF1 | | | | | | | Bootloader RX. |
| BOOT_TX | PF0 | | | | | | | Bootloader TX. |
| CMU_CLK0 | | | PD7 | PF2 | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | | | PE12 | PB11 | | | | Clock Management Unit, clock output number 1. |
| DBG_SWCLK | PF0 | | | | | | | Debug-interface Serial Wire clock input.<br>Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | | | | | | | Debug-interface Serial Wire data input / output.<br>Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| GPIO_EM4WU0 | PA0 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU3 | PF1 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | PF2 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU5 | PE13 | | | | | | | Pin can be used to wake the system up from EM4 |
| HFXTAL_N | PB14 | | | | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | | PD7 | | | PC1 | PF1 | PE13 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | | | PC0 | PF0 | PE12 | I2C0 Serial Data input / output. |
| IDAC0_OUT | PB11 | | | | | | | IDAC0 output. |
| LEU0_RX | | PB14 | | PF1 | PA0 | PC15 | | LEUART0 Receive input. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LEU0_TX | | PB13 | | PF0 | PF2 | PC14 | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | | | PC0 | PD6 | PA0 | | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | PC14 | | PC1 | PD7 | PB11 | | | Pulse Counter PCNT0 input number 1. |
| PRS_CH0 | PA0 | | PC14 | PF2 | | | | Peripheral Reflex System PRS, channel 0. |
| PRS_CH1 | | | PC15 | PE12 | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | PC0 | | | PE13 | | | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | PC1 | | | PA0 | | | | Peripheral Reflex System PRS, channel 3. |
| TIM0_CC0 | PA0 | PA0 | | | PA0 | PF0 | | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | | | | | PC0 | PF1 | PA0 | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | | | | | PC1 | PF2 | PF2 | Timer 0 Capture Compare input / output channel 2. |
| TIM0_CDTI1 | | PC14 | | | | | PC14 | Timer 0 Complimentary Deat Time Insertion channel 1. |
| TIM0_CDTI2 | | PC15 | | | | | PC15 | Timer 0 Complimentary Deat Time Insertion channel 2. |
| TIM1_CC0 | | | | PB7 | PD6 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | | | PB8 | PD7 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | | PB11 | | | | Timer 1 Capture Compare input / output channel 2. |
| TIM2_CC0 | | | | PF2 | | | | Timer 2 Capture Compare input / output channel 0. |
| TIM2_CC1 | | | | PE12 | | | | Timer 2 Capture Compare input / output channel 1. |
| TIM2_CC2 | | | | PE13 | | | | Timer 2 Capture Compare input / output channel 2. |
| US0_CLK | PE12 | | | PC15 | PB13 | PB13 | PE12 | USART0 clock input / output. |
| US0_CS | PE13 | | | PC14 | PB14 | PB14 | PE13 | USART0 chip select input / output. |
| US0_RX | | | | PE12 | PB8 | PC1 | PC1 | USART0 Asynchronous Receive.<br>USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | | | | PE13 | PB7 | PC0 | PC0 | USART0 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | | PF0 | PC15 | PB11 | | | USART1 clock input / output. |
| US1_CS | PB8 | | PF1 | PC14 | PC14 | PC0 | | USART1 chip select input / output. |
| US1_RX | PC1 | | PD6 | PD6 | PA0 | | | USART1 Asynchronous Receive.<br>USART1 Synchronous mode Master Input / Slave Output (MISO). |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| US1_TX | PC0 | | PD7 | PD7 | PF2 | PC1 | | USART1 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART1 Synchronous mode Master Output / Slave Input (MOSI). |

### 5.2.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32HG110 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

**Table 5.6. GPIO Pinout**

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Port A | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | PA0 |
| Port B | - | PB14 | PB13 | - | PB11 | - | - | PB8 | PB7 | - | - | - | - | - | - | - |
| Port C | PC15 | PC14 | - | - | - | - | - | - | - | - | - | - | - | - | PC1 | PC0 |
| Port D | - | - | - | - | - | - | - | - | PD7 | PD6 | - | - | - | - | - | - |
| Port E | - | - | PE13 | PE12 | - | - | - | - | - | - | - | - | - | - | - | - |
| Port F | - | - | - | - | - | - | - | - | - | - | - | - | - | PF2 | PF1 | PF0 |

### 5.3 EFM32HG210 (QFN32)

#### 5.3.1 Pinout

The EFM32HG210 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

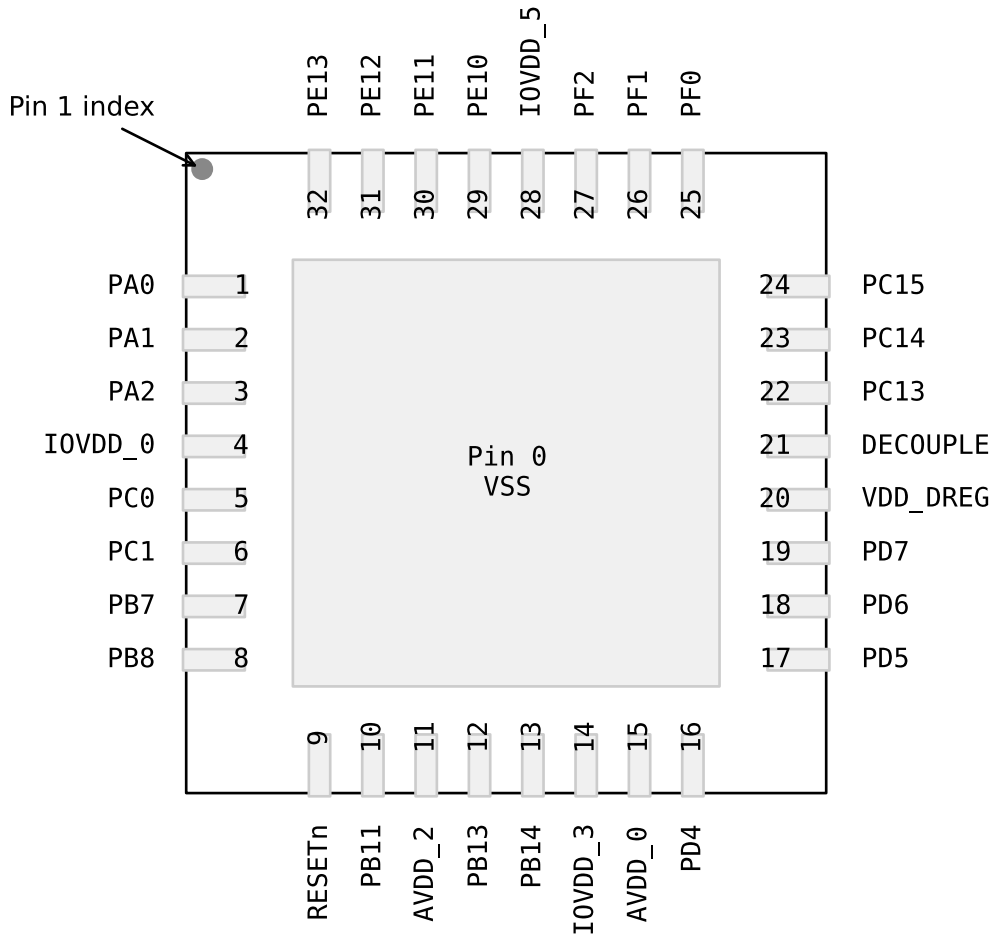



**Figure 5.3. EFM32HG210 Pinout (top view, not to scale)**

**Table 5.7. Device Pinout**

| QFN32 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 0 | VSS | Ground. | | | |
| 1 | PA0 | | TIM0_CC1 #6<br>TIM0_CC0 #0/1/4<br>PCNT0_S0IN #4 | US1_RX #4<br>LEU0_RX #4<br>I2C0_SDA #0 | PRS_CH0 #0<br>PRS_CH3 #3<br>GPIO_EM4WU0 |

| QFN32 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 2 | PA1 | | TIM0_CC0 #6<br>TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0<br>PRS_CH1 #0 |
| 3 | PA2 | | TIM0_CC2 #0/1 | | CMU_CLK0 #0 |
| 4 | IOVDD_0 | Digital IO power supply 0. | | | |
| 5 | PC0 | ACMP0_CH0 | TIM0_CC1 #4<br>PCNT0_S0IN #2 | US0_TX #5/6<br>US1_TX #0<br>US1_CS #5<br>I2C0_SDA #4 | PRS_CH2 #0 |
| 6 | PC1 | ACMP0_CH1 | TIM0_CC2 #4<br>PCNT0_S1IN #2 | US0_RX #5/6<br>US1_TX #5<br>US1_RX #0<br>I2C0_SCL #4 | PRS_CH3 #0 |
| 7 | PB7 | LFXTAL_P | TIM1_CC0 #3 | US0_TX #4<br>US1_CLK #0 | |
| 8 | PB8 | LFXTAL_N | TIM1_CC1 #3 | US0_RX #4<br>US1_CS #0 | |
| 9 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | |
| 10 | PB11 | IDAC0_OUT | TIM1_CC2 #3<br>PCNT0_S1IN #4 | US1_CLK #4 | CMU_CLK1 #3<br>ACMP0_O #3 |
| 11 | AVDD_2 | Analog power supply 2. | | | |
| 12 | PB13 | HFXTAL_P | | US0_CLK #4/5<br>LEU0_TX #1 | |
| 13 | PB14 | HFXTAL_N | | US0_CS #4/5<br>LEU0_RX #1 | |
| 14 | IOVDD_3 | Digital IO power supply 3. | | | |
| 15 | AVDD_0 | Analog power supply 0. | | | |
| 16 | PD4 | ADC0_CH4 | | LEU0_TX #0 | |
| 17 | PD5 | ADC0_CH5 | | LEU0_RX #0 | |
| 18 | PD6 | ADC0_CH6 | TIM1_CC0 #4<br>PCNT0_S0IN #3 | US1_RX #2/3<br>I2C0_SDA #1 | ACMP0_O #2 |
| 19 | PD7 | ADC0_CH7 | TIM1_CC1 #4<br>PCNT0_S1IN #3 | US1_TX #2/3<br>I2C0_SCL #1 | CMU_CLK0 #2 |
| 20 | VDD_DREG | Power supply for on-chip voltage regulator. | | | |
| 21 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin. | | | |

| QFN32 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 22 | PC13 | | TIM0_CDTI0 #1/6<br>TIM1_CC0 #0<br>TIM1_CC2 #4<br>PCNT0_S0IN #0 | | |
| 23 | PC14 | | TIM0_CDTI1 #1/6<br>TIM1_CC1 #0<br>PCNT0_S1IN #0 | US0_CS #3<br>US1_CS #3/4<br>LEU0_TX #5 | PRS_CH0 #2 |
| 24 | PC15 | | TIM0_CDTI2 #1/6<br>TIM1_CC2 #0 | US0_CLK #3<br>US1_CLK #3<br>LEU0_RX #5 | PRS_CH1 #2 |
| 25 | PF0 | | TIM0_CC0 #5 | US1_CLK #2<br>LEU0_TX #3<br>I2C0_SDA #5 | DBG_SWCLK #0<br>BOOT_TX |
| 26 | PF1 | | TIM0_CC1 #5 | US1_CS #2<br>LEU0_RX #3<br>I2C0_SCL #5 | DBG_SWDIO #0<br>GPIO_EM4WU3<br>BOOT_RX |
| 27 | PF2 | | TIM0_CC2 #5/6<br>TIM2_CC0 #3 | US1_TX #4<br>LEU0_TX #4 | CMU_CLK0 #3<br>PRS_CH0 #3<br>GPIO_EM4WU4 |
| 28 | IOVDD_5 | Digital IO power supply 5. | | | |
| 29 | PE10 | | TIM1_CC0 #1 | US0_TX #0 | PRS_CH2 #2 |
| 30 | PE11 | | TIM1_CC1 #1 | US0_RX #0 | PRS_CH3 #2 |
| 31 | PE12 | ADC0_CH0 | TIM1_CC2 #1<br>TIM2_CC1 #3 | US0_RX #3<br>US0_CLK #0/6<br>I2C0_SDA #6 | CMU_CLK1 #2<br>PRS_CH1 #3 |
| 32 | PE13 | ADC0_CH1 | TIM2_CC2 #3 | US0_TX #3<br>US0_CS #0/6<br>I2C0_SCL #6 | ACMP0_O #0<br>PRS_CH2 #3<br>GPIO_EM4WU5 |

### 5.3.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

**Note:** Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

**Table 5.8. Alternate functionality overview**

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ACMP0_CH0 | PC0 | | | | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH1 | PC1 | | | | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_O | PE13 | | PD6 | PB11 | | | | Analog comparator ACMP0, digital output. |
| ADC0_CH0 | PE12 | | | | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PE13 | | | | | | | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH4 | PD4 | | | | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | | | | Analog to digital converter ADC0, input channel number 6. |
| ADC0_CH7 | PD7 | | | | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PF1 | | | | | | | Bootloader RX. |
| BOOT_TX | PF0 | | | | | | | Bootloader TX. |
| CMU_CLK0 | PA2 | | PD7 | PF2 | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | | PE12 | PB11 | | | | Clock Management Unit, clock output number 1. |
| DBG_SWCLK | PF0 | | | | | | | Debug-interface Serial Wire clock input.<br>Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | | | | | | | Debug-interface Serial Wire data input / output.<br>Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| GPIO_EM4WU0 | PA0 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU3 | PF1 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | PF2 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU5 | PE13 | | | | | | | Pin can be used to wake the system up from EM4 |
| HFXTAL_N | PB14 | | | | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | | | PC1 | PF1 | PE13 | I2C0 Serial Clock Line input / output. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| I2C0_SDA | PA0 | PD6 | | | PC0 | PF0 | PE12 | I2C0 Serial Data input / output. |
| IDAC0_OUT | PB11 | | | | | | | IDAC0 output. |
| LEU0_RX | PD5 | PB14 | | PF1 | PA0 | PC15 | | LEUART0 Receive input. |
| LEU0_TX | PD4 | PB13 | | PF0 | PF2 | PC14 | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | PC13 | | PC0 | PD6 | PA0 | | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | PC14 | | PC1 | PD7 | PB11 | | | Pulse Counter PCNT0 input number 1. |
| PRS_CH0 | PA0 | | PC14 | PF2 | | | | Peripheral Reflex System PRS, channel 0. |
| PRS_CH1 | PA1 | | PC15 | PE12 | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | PC0 | | PE10 | PE13 | | | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | PC1 | | PE11 | PA0 | | | | Peripheral Reflex System PRS, channel 3. |
| TIM0_CC0 | PA0 | PA0 | | | PA0 | PF0 | PA1 | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | | | PC0 | PF1 | PA0 | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | | | PC1 | PF2 | PF2 | Timer 0 Capture Compare input / output channel 2. |
| TIM0_CDTI0 | | PC13 | | | | | PC13 | Timer 0 Complimentary Dead Time Insertion channel 0. |
| TIM0_CDTI1 | | PC14 | | | | | PC14 | Timer 0 Complimentary Dead Time Insertion channel 1. |
| TIM0_CDTI2 | | PC15 | | | | | PC15 | Timer 0 Complimentary Dead Time Insertion channel 2. |
| TIM1_CC0 | PC13 | PE10 | | PB7 | PD6 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | PE11 | | PB8 | PD7 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | | PB11 | PC13 | | | Timer 1 Capture Compare input / output channel 2. |
| TIM2_CC0 | | | | PF2 | | | | Timer 2 Capture Compare input / output channel 0. |
| TIM2_CC1 | | | | PE12 | | | | Timer 2 Capture Compare input / output channel 1. |
| TIM2_CC2 | | | | PE13 | | | | Timer 2 Capture Compare input / output channel 2. |
| US0_CLK | PE12 | | | PC15 | PB13 | PB13 | PE12 | USART0 clock input / output. |
| US0_CS | PE13 | | | PC14 | PB14 | PB14 | PE13 | USART0 chip select input / output. |
| US0_RX | PE11 | | | PE12 | PB8 | PC1 | PC1 | USART0 Asynchronous Receive.<br>USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | PE10 | | | PE13 | PB7 | PC0 | PC0 | USART0 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART0 Synchronous mode Master Output / Slave Input (MOSI). |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| US1_CLK | PB7 | | PF0 | PC15 | PB11 | | | USART1 clock input / output. |
| US1_CS | PB8 | | PF1 | PC14 | PC14 | PC0 | | USART1 chip select input / output. |
| US1_RX | PC1 | | PD6 | PD6 | PA0 | | | USART1 Asynchronous Receive.<br>USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | PC0 | | PD7 | PD7 | PF2 | PC1 | | USART1 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART1 Synchronous mode Master Output / Slave Input (MOSI). |

### 5.3.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32HG210 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

**Table 5.9. GPIO Pinout**

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Port A | - | - | - | - | - | - | - | - | - | - | - | - | - | PA2 | PA1 | PA0 |
| Port B | - | PB14 | PB13 | - | PB11 | - | - | PB8 | PB7 | - | - | - | - | - | - | - |
| Port C | PC15 | PC14 | PC13 | - | - | - | - | - | - | - | - | - | - | - | PC1 | PC0 |
| Port D | - | - | - | - | - | - | - | - | PD7 | PD6 | PD5 | PD4 | - | - | - | - |
| Port E | - | - | PE13 | PE12 | PE11 | PE10 | - | - | - | - | - | - | - | - | - | - |
| Port F | - | - | - | - | - | - | - | - | - | - | - | - | - | PF2 | PF1 | PF0 |

## 5.4 EFM32HG222 (TQFP48)

### 5.4.1 Pinout

The EFM32HG222 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

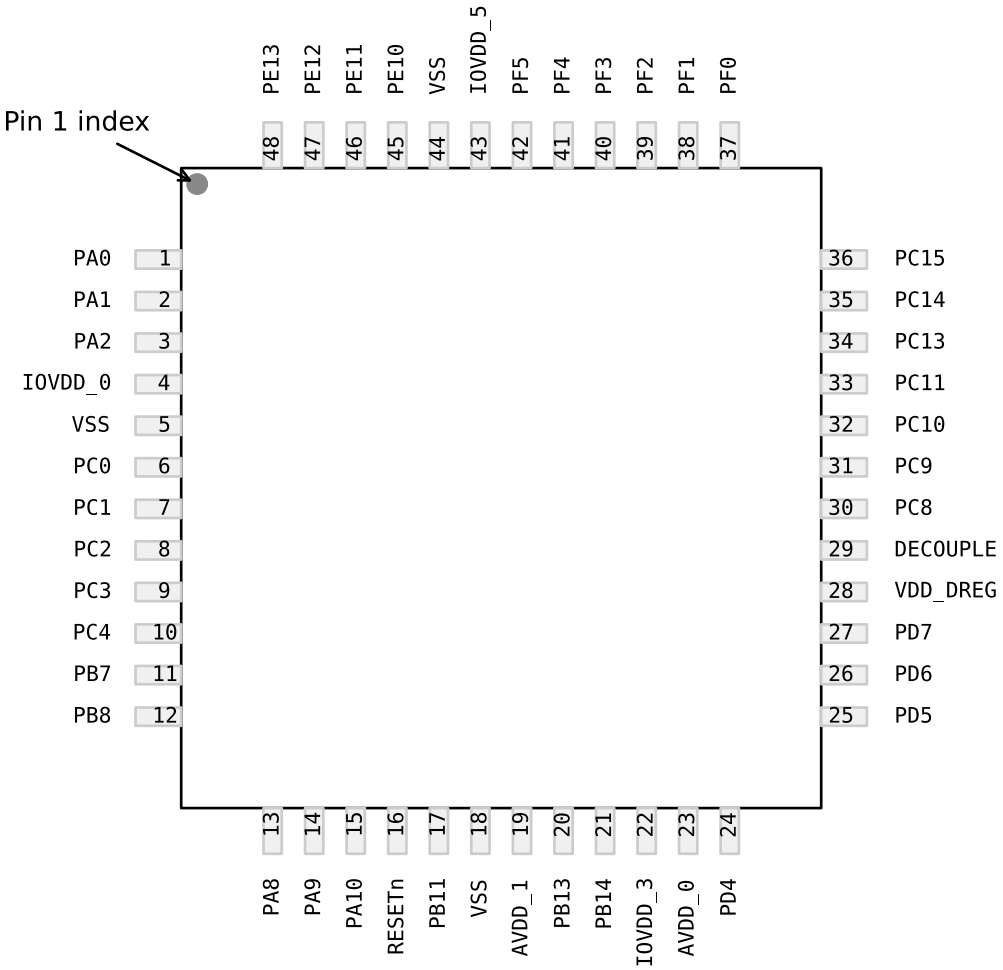



**Figure 5.4. EFM32HG222 Pinout (top view, not to scale)**

**Table 5.10. Device Pinout**

| QFP48 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 1 | PA0 | | TIM0_CC1 #6<br>TIM0_CC0 #0/1/4<br>PCNT0_S0IN #4 | US1_RX #4<br>LEU0_RX #4<br>I2C0_SDA #0 | PRS_CH0 #0<br>PRS_CH3 #3<br>GPIO_EM4WU0 |
| 2 | PA1 | | TIM0_CC0 #6<br>TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0<br>PRS_CH1 #0 |

| QFP48 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 3 | PA2 | | TIM0_CC2 #0/1 | | CMU_CLK0 #0 |
| 4 | IOVDD_0 | Digital IO power supply 0. | | | |
| 5 | VSS | Ground. | | | |
| 6 | PC0 | ACMP0_CH0 | TIM0_CC1 #4<br>PCNT0_S0IN #2 | US0_TX #5/6<br>US1_TX #0<br>US1_CS #5<br>I2C0_SDA #4 | PRS_CH2 #0 |
| 7 | PC1 | ACMP0_CH1 | TIM0_CC2 #4<br>PCNT0_S1IN #2 | US0_RX #5/6<br>US1_TX #5<br>US1_RX #0<br>I2C0_SCL #4 | PRS_CH3 #0 |
| 8 | PC2 | ACMP0_CH2 | TIM0_CDTI0 #4 | US1_RX #5 | |
| 9 | PC3 | ACMP0_CH3 | TIM0_CDTI1 #4 | US1_CLK #5 | |
| 10 | PC4 | ACMP0_CH4 | TIM0_CDTI2 #4 | | GPIO_EM4WU6 |
| 11 | PB7 | LFXTAL_P | TIM1_CC0 #3 | US0_TX #4<br>US1_CLK #0 | |
| 12 | PB8 | LFXTAL_N | TIM1_CC1 #3 | US0_RX #4<br>US1_CS #0 | |
| 13 | PA8 | | TIM2_CC0 #0 | | |
| 14 | PA9 | | TIM2_CC1 #0 | | |
| 15 | PA10 | | TIM2_CC2 #0 | | |
| 16 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | |
| 17 | PB11 | IDAC0_OUT | TIM1_CC2 #3<br>PCNT0_S1IN #4 | US1_CLK #4 | CMU_CLK1 #3<br>ACMP0_O #3 |
| 18 | VSS | Ground. | | | |
| 19 | AVDD_1 | Analog power supply 1. | | | |
| 20 | PB13 | HFXTAL_P | | US0_CLK #4/5<br>LEU0_TX #1 | |
| 21 | PB14 | HFXTAL_N | | US0_CS #4/5<br>LEU0_RX #1 | |
| 22 | IOVDD_3 | Digital IO power supply 3. | | | |
| 23 | AVDD_0 | Analog power supply 0. | | | |
| 24 | PD4 | ADC0_CH4 | | LEU0_TX #0 | |
| 25 | PD5 | ADC0_CH5 | | LEU0_RX #0 | |

| QFP48 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 26 | PD6 | ADC0_CH6 | TIM1_CC0 #4<br>PCNT0_S0IN #3 | US1_RX #2/3<br>I2C0_SDA #1 | ACMP0_O #2 |
| 27 | PD7 | ADC0_CH7 | TIM1_CC1 #4<br>PCNT0_S1IN #3 | US1_TX #2/3<br>I2C0_SCL #1 | CMU_CLK0 #2 |
| 28 | VDD_DREG | Power supply for on-chip voltage regulator. | | | |
| 29 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin. | | | |
| 30 | PC8 | | TIM2_CC0 #2 | US0_CS #2 | |
| 31 | PC9 | | TIM2_CC1 #2 | US0_CLK #2 | GPIO_EM4WU2 |
| 32 | PC10 | | TIM2_CC2 #2 | US0_RX #2 | |
| 33 | PC11 | | | US0_TX #2 | |
| 34 | PC13 | | TIM0_CDTI0 #1/6<br>TIM1_CC0 #0<br>TIM1_CC2 #4<br>PCNT0_S0IN #0 | | |
| 35 | PC14 | | TIM0_CDTI1 #1/6<br>TIM1_CC1 #0<br>PCNT0_S1IN #0 | US0_CS #3<br>US1_CS #3/4<br>LEU0_TX #5 | PRS_CH0 #2 |
| 36 | PC15 | | TIM0_CDTI2 #1/6<br>TIM1_CC2 #0 | US0_CLK #3<br>US1_CLK #3<br>LEU0_RX #5 | PRS_CH1 #2 |
| 37 | PF0 | | TIM0_CC0 #5 | US1_CLK #2<br>LEU0_TX #3<br>I2C0_SDA #5 | DBG_SWCLK #0<br>BOOT_TX |
| 38 | PF1 | | TIM0_CC1 #5 | US1_CS #2<br>LEU0_RX #3<br>I2C0_SCL #5 | DBG_SWDIO #0<br>GPIO_EM4WU3<br>BOOT_RX |
| 39 | PF2 | | TIM0_CC2 #5/6<br>TIM2_CC0 #3 | US1_TX #4<br>LEU0_TX #4 | CMU_CLK0 #3<br>PRS_CH0 #3<br>GPIO_EM4WU4 |
| 40 | PF3 | | TIM0_CDTI0 #5 | | PRS_CH0 #1 |
| 41 | PF4 | | TIM0_CDTI1 #5 | | PRS_CH1 #1 |
| 42 | PF5 | | TIM0_CDTI2 #5 | | PRS_CH2 #1 |
| 43 | IOVDD_5 | Digital IO power supply 5. | | | |
| 44 | VSS | Ground. | | | |
| 45 | PE10 | | TIM1_CC0 #1 | US0_TX #0 | PRS_CH2 #2 |

| QFP48 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 46 | PE11 | | TIM1_CC1 #1 | US0_RX #0 | PRS_CH3 #2 |
| 47 | PE12 | ADC0_CH0 | TIM1_CC2 #1<br>TIM2_CC1 #3 | US0_RX #3<br>US0_CLK #0/6<br>I2C0_SDA #6 | CMU_CLK1 #2<br>PRS_CH1 #3 |
| 48 | PE13 | ADC0_CH1 | TIM2_CC2 #3 | US0_TX #3<br>US0_CS #0/6<br>I2C0_SCL #6 | ACMP0_O #0<br>PRS_CH2 #3<br>GPIO_EM4WU5 |

### 5.4.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

**Note:** Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

**Table 5.11. Alternate functionality overview**

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ACMP0_CH0 | PC0 | | | | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH1 | PC1 | | | | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_CH2 | PC2 | | | | | | | Analog comparator ACMP0, channel 2. |
| ACMP0_CH3 | PC3 | | | | | | | Analog comparator ACMP0, channel 3. |
| ACMP0_CH4 | PC4 | | | | | | | Analog comparator ACMP0, channel 4. |
| ACMP0_O | PE13 | | PD6 | PB11 | | | | Analog comparator ACMP0, digital output. |
| ADC0_CH0 | PE12 | | | | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PE13 | | | | | | | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH4 | PD4 | | | | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | | | | Analog to digital converter ADC0, input channel number 6. |
| ADC0_CH7 | PD7 | | | | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PF1 | | | | | | | Bootloader RX. |
| BOOT_TX | PF0 | | | | | | | Bootloader TX. |
| CMU_CLK0 | PA2 | | PD7 | PF2 | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | | PE12 | PB11 | | | | Clock Management Unit, clock output number 1. |
| DBG_SWCLK | PF0 | | | | | | | Debug-interface Serial Wire clock input.<br>Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | | | | | | | Debug-interface Serial Wire data input / output.<br>Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| GPIO_EM4WU0 | PA0 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU2 | PC9 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU3 | PF1 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | PF2 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU5 | PE13 | | | | | | | Pin can be used to wake the system up from EM4 |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| GPIO_EM4WU6 | PC4 | | | | | | | Pin can be used to wake the system up from EM4 |
| HFXTAL_N | PB14 | | | | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | | | PC1 | PF1 | PE13 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | | | PC0 | PF0 | PE12 | I2C0 Serial Data input / output. |
| IDAC0_OUT | PB11 | | | | | | | IDAC0 output. |
| LEU0_RX | PD5 | PB14 | | PF1 | PA0 | PC15 | | LEUART0 Receive input. |
| LEU0_TX | PD4 | PB13 | | PF0 | PF2 | PC14 | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | PC13 | | PC0 | PD6 | PA0 | | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | PC14 | | PC1 | PD7 | PB11 | | | Pulse Counter PCNT0 input number 1. |
| PRS_CH0 | PA0 | PF3 | PC14 | PF2 | | | | Peripheral Reflex System PRS, channel 0. |
| PRS_CH1 | PA1 | PF4 | PC15 | PE12 | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | PC0 | PF5 | PE10 | PE13 | | | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | PC1 | | PE11 | PA0 | | | | Peripheral Reflex System PRS, channel 3. |
| TIM0_CC0 | PA0 | PA0 | | | PA0 | PF0 | PA1 | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | | | PC0 | PF1 | PA0 | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | | | PC1 | PF2 | PF2 | Timer 0 Capture Compare input / output channel 2. |
| TIM0_CDTI0 | | PC13 | | | PC2 | PF3 | PC13 | Timer 0 Complimentary Dead Time Insertion channel 0. |
| TIM0_CDTI1 | | PC14 | | | PC3 | PF4 | PC14 | Timer 0 Complimentary Dead Time Insertion channel 1. |
| TIM0_CDTI2 | | PC15 | | | PC4 | PF5 | PC15 | Timer 0 Complimentary Dead Time Insertion channel 2. |
| TIM1_CC0 | PC13 | PE10 | | PB7 | PD6 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | PE11 | | PB8 | PD7 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | | PB11 | PC13 | | | Timer 1 Capture Compare input / output channel 2. |
| TIM2_CC0 | PA8 | | PC8 | PF2 | | | | Timer 2 Capture Compare input / output channel 0. |
| TIM2_CC1 | PA9 | | PC9 | PE12 | | | | Timer 2 Capture Compare input / output channel 1. |
| TIM2_CC2 | PA10 | | PC10 | PE13 | | | | Timer 2 Capture Compare input / output channel 2. |
| US0_CLK | PE12 | | PC9 | PC15 | PB13 | PB13 | PE12 | USART0 clock input / output. |
| US0_CS | PE13 | | PC8 | PC14 | PB14 | PB14 | PE13 | USART0 chip select input / output. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| US0_RX | PE11 | | PC10 | PE12 | PB8 | PC1 | PC1 | USART0 Asynchronous Receive.<br>USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | PE10 | | PC11 | PE13 | PB7 | PC0 | PC0 | USART0 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | | PF0 | PC15 | PB11 | PC3 | | USART1 clock input / output. |
| US1_CS | PB8 | | PF1 | PC14 | PC14 | PC0 | | USART1 chip select input / output. |
| US1_RX | PC1 | | PD6 | PD6 | PA0 | PC2 | | USART1 Asynchronous Receive.<br>USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | PC0 | | PD7 | PD7 | PF2 | PC1 | | USART1 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART1 Synchronous mode Master Output / Slave Input (MOSI). |

### 5.4.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32HG222 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

**Table 5.12. GPIO Pinout**

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Port A | - | - | - | - | - | PA10 | PA9 | PA8 | - | - | - | - | - | PA2 | PA1 | PA0 |
| Port B | - | PB14 | PB13 | - | PB11 | - | - | PB8 | PB7 | - | - | - | - | - | - | - |
| Port C | PC15 | PC14 | PC13 | - | PC11 | PC10 | PC9 | PC8 | - | - | - | PC4 | PC3 | PC2 | PC1 | PC0 |
| Port D | - | - | - | - | - | - | - | - | PD7 | PD6 | PD5 | PD4 | - | - | - | - |
| Port E | - | - | PE13 | PE12 | PE11 | PE10 | - | - | - | - | - | - | - | - | - | - |
| Port F | - | - | - | - | - | - | - | - | - | - | PF5 | PF4 | PF3 | PF2 | PF1 | PF0 |

### 5.5 EFM32HG308 (QFN24)

#### 5.5.1 Pinout

The EFM32HG308 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

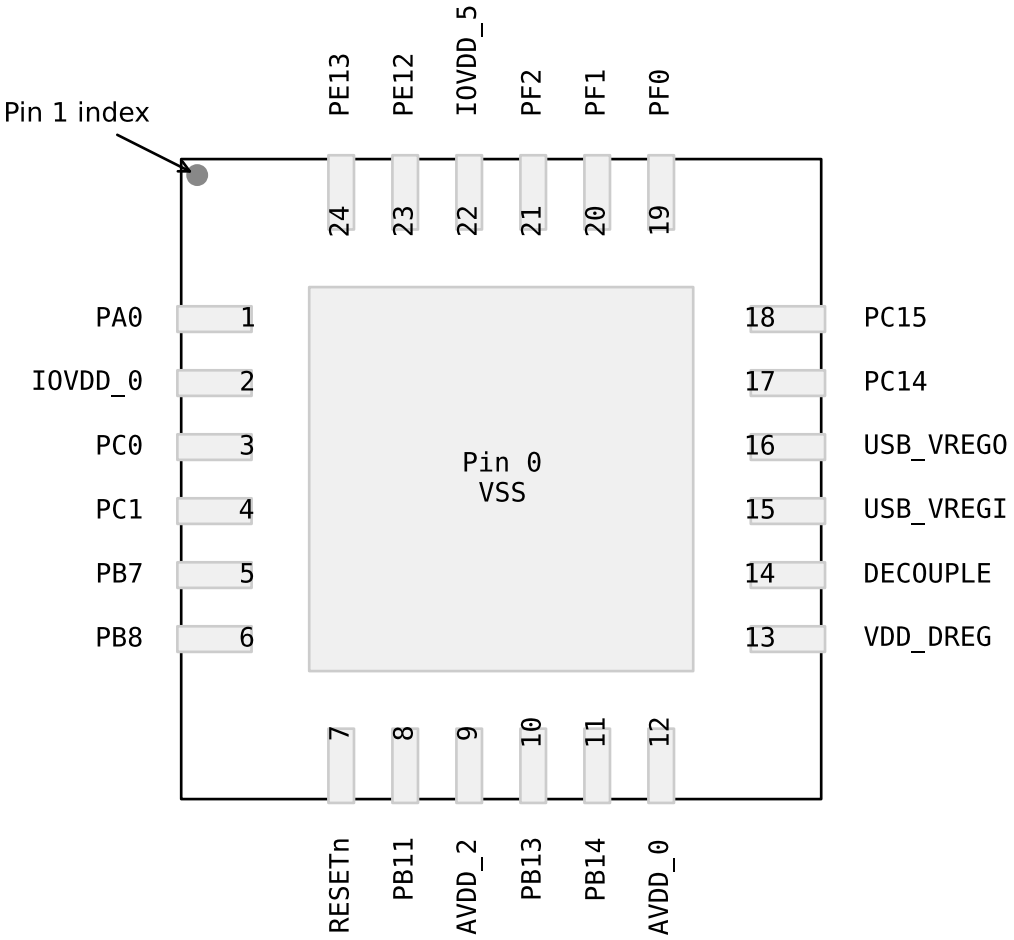



**Figure 5.5. EFM32HG308 Pinout (top view, not to scale)**

**Table 5.13. Device Pinout**

| QFN24 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 0 | VSS | Ground. | | | |
| 1 | PA0 | | TIM0_CC1 #6<br>TIM0_CC0 #0/1/4<br>PCNT0_S0IN #4 | USB_DMPU #0<br>US1_RX #4<br>LEU0_RX #4<br>I2C0_SDA #0 | PRS_CH0 #0<br>PRS_CH3 #3<br>GPIO_EM4WU0 |

| QFN24 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 2 | IOVDD_0 | Digital IO power supply 0. | | | |
| 3 | PC0 | ACMP0_CH0 | TIM0_CC1 #4<br>PCNT0_S0IN #2 | US0_TX #5/6<br>US1_TX #0<br>US1_CS #5<br>I2C0_SDA #4 | PRS_CH2 #0 |
| 4 | PC1 | ACMP0_CH1 | TIM0_CC2 #4<br>PCNT0_S1IN #2 | US0_RX #5/6<br>US1_TX #5<br>US1_RX #0<br>I2C0_SCL #4 | PRS_CH3 #0 |
| 5 | PB7 | LFXTAL_P | TIM1_CC0 #3 | US0_TX #4<br>US1_CLK #0 | |
| 6 | PB8 | LFXTAL_N | TIM1_CC1 #3 | US0_RX #4<br>US1_CS #0 | |
| 7 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | |
| 8 | PB11 | | TIM1_CC2 #3<br>PCNT0_S1IN #4 | US1_CLK #4 | CMU_CLK1 #3<br>ACMP0_O #3 |
| 9 | AVDD_2 | Analog power supply 2. | | | |
| 10 | PB13 | HFXTAL_P | | US0_CLK #4/5<br>LEU0_TX #1 | |
| 11 | PB14 | HFXTAL_N | | US0_CS #4/5<br>LEU0_RX #1 | |
| 12 | AVDD_0 | Analog power supply 0. | | | |
| 13 | VDD_DREG | Power supply for on-chip voltage regulator. | | | |
| 14 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin. | | | |
| 15 | USB_VREGI | | | | |
| 16 | USB_VREGO | | | | |
| 17 | PC14 | | TIM0_CDTI1 #1/6<br>TIM1_CC1 #0<br>PCNT0_S1IN #0 | US0_CS #3<br>US1_CS #3/4<br>LEU0_TX #5<br>USB_DM | PRS_CH0 #2 |
| 18 | PC15 | | TIM0_CDTI2 #1/6<br>TIM1_CC2 #0 | US0_CLK #3<br>US1_CLK #3<br>LEU0_RX #5<br>USB_DP | PRS_CH1 #2 |

| QFN24 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 19 | PF0 | | TIM0_CC0 #5 | US1_CLK #2<br>LEU0_TX #3<br>I2C0_SDA #5 | DBG_SWCLK #0<br>BOOT_TX |
| 20 | PF1 | | TIM0_CC1 #5 | US1_CS #2<br>LEU0_RX #3<br>I2C0_SCL #5 | DBG_SWDIO #0<br>GPIO_EM4WU3<br>BOOT_RX |
| 21 | PF2 | | TIM0_CC2 #5/6<br>TIM2_CC0 #3 | US1_TX #4<br>LEU0_TX #4 | CMU_CLK0 #3<br>PRS_CH0 #3<br>GPIO_EM4WU4 |
| 22 | IOVDD_5 | Digital IO power supply 5. | | | |
| 23 | PE12 | | TIM1_CC2 #1<br>TIM2_CC1 #3 | US0_RX #3<br>US0_CLK #0/6<br>I2C0_SDA #6 | CMU_CLK1 #2<br>PRS_CH1 #3 |
| 24 | PE13 | | TIM2_CC2 #3 | US0_TX #3<br>US0_CS #0/6<br>I2C0_SCL #6 | ACMP0_O #0<br>PRS_CH2 #3<br>GPIO_EM4WU5 |

### 5.5.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

**Note:** Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

**Table 5.14. Alternate functionality overview**

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ACMP0_CH0 | PC0 | | | | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH1 | PC1 | | | | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_O | PE13 | | | PB11 | | | | Analog comparator ACMP0, digital output. |
| BOOT_RX | PF1 | | | | | | | Bootloader RX. |
| BOOT_TX | PF0 | | | | | | | Bootloader TX. |
| CMU_CLK0 | | | | PF2 | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | | | PE12 | PB11 | | | | Clock Management Unit, clock output number 1. |
| DBG_SWCLK | PF0 | | | | | | | Debug-interface Serial Wire clock input.<br>Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | | | | | | | Debug-interface Serial Wire data input / output.<br>Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| GPIO_EM4WU0 | PA0 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU3 | PF1 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | PF2 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU5 | PE13 | | | | | | | Pin can be used to wake the system up from EM4 |
| HFXTAL_N | PB14 | | | | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | | | | | PC1 | PF1 | PE13 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | | | | PC0 | PF0 | PE12 | I2C0 Serial Data input / output. |
| LEU0_RX | | PB14 | | PF1 | PA0 | PC15 | | LEUART0 Receive input. |
| LEU0_TX | | PB13 | | PF0 | PF2 | PC14 | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | | | PC0 | | PA0 | | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | PC14 | | PC1 | | PB11 | | | Pulse Counter PCNT0 input number 1. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| PRS_CH0 | PA0 | | PC14 | PF2 | | | | Peripheral Reflex System PRS, channel 0. |
| PRS_CH1 | | | PC15 | PE12 | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | PC0 | | | PE13 | | | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | PC1 | | | PA0 | | | | Peripheral Reflex System PRS, channel 3. |
| TIM0_CC0 | PA0 | PA0 | | | PA0 | PF0 | | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | | | | | PC0 | PF1 | PA0 | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | | | | | PC1 | PF2 | PF2 | Timer 0 Capture Compare input / output channel 2. |
| TIM0_CDTI1 | | PC14 | | | | | PC14 | Timer 0 Complimentary Dead Time Insertion channel 1. |
| TIM0_CDTI2 | | PC15 | | | | | PC15 | Timer 0 Complimentary Dead Time Insertion channel 2. |
| TIM1_CC0 | | | | PB7 | | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | | | PB8 | | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | | PB11 | | | | Timer 1 Capture Compare input / output channel 2. |
| TIM2_CC0 | | | | PF2 | | | | Timer 2 Capture Compare input / output channel 0. |
| TIM2_CC1 | | | | PE12 | | | | Timer 2 Capture Compare input / output channel 1. |
| TIM2_CC2 | | | | PE13 | | | | Timer 2 Capture Compare input / output channel 2. |
| US0_CLK | PE12 | | | PC15 | PB13 | PB13 | PE12 | USART0 clock input / output. |
| US0_CS | PE13 | | | PC14 | PB14 | PB14 | PE13 | USART0 chip select input / output. |
| US0_RX | | | | PE12 | PB8 | PC1 | PC1 | USART0 Asynchronous Receive.<br>USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | | | | PE13 | PB7 | PC0 | PC0 | USART0 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | | PF0 | PC15 | PB11 | | | USART1 clock input / output. |
| US1_CS | PB8 | | PF1 | PC14 | PC14 | PC0 | | USART1 chip select input / output. |
| US1_RX | PC1 | | | | PA0 | | | USART1 Asynchronous Receive.<br>USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | PC0 | | | | PF2 | PC1 | | USART1 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART1 Synchronous mode Master Output / Slave Input (MOSI). |
| USB_DM | PC14 | | | | | | | USB D- pin. |
| USB_DMPU | PA0 | | | | | | | USB D- Pullup control. |
| USB_DP | PC15 | | | | | | | USB D+ pin. |
| USB_VREGI | USB_VREGI | | | | | | | USB Input to internal 3.3 V regulator |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| USB_VREGO | USB_VREGO | | | | | | | USB Decoupling for internal 3.3 V USB regulator and regulator output |

### 5.5.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32HG309 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

**Table 5.15. GPIO Pinout**

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Port A | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | PA0 |
| Port B | - | PB14 | PB13 | - | PB11 | - | - | PB8 | PB7 | - | - | - | - | - | - | - |
| Port C | PC15 | PC14 | - | - | - | - | - | - | - | - | - | - | - | - | PC1 | PC0 |
| Port D | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| Port E | - | - | PE13 | PE12 | - | - | - | - | - | - | - | - | - | - | - | - |
| Port F | - | - | - | - | - | - | - | - | - | - | - | - | - | PF2 | PF1 | PF0 |

### 5.6 EFM32HG309 (QFN24)

#### 5.6.1 Pinout

The EFM32HG309 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

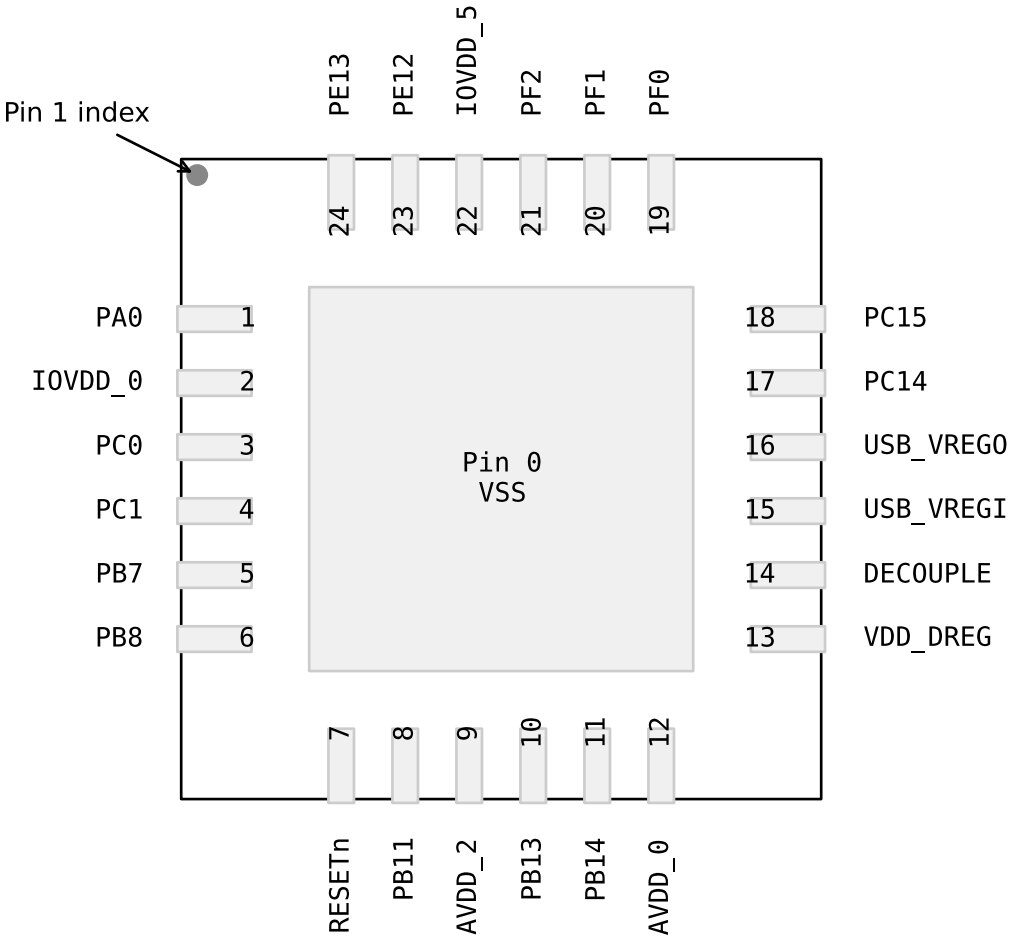



**Figure 5.6. EFM32HG309 Pinout (top view, not to scale)**

**Table 5.16. Device Pinout**

| QFN24 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 0 | VSS | Ground. | | | |
| 1 | PA0 | | TIM0_CC1 #6<br>TIM0_CC0 #0/1/4<br>PCNT0_S0IN #4 | USB_DMPU #0<br>US1_RX #4<br>LEU0_RX #4<br>I2C0_SDA #0 | PRS_CH0 #0<br>PRS_CH3 #3<br>GPIO_EM4WU0 |

| QFN24 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 2 | IOVDD_0 | Digital IO power supply 0. | | | |
| 3 | PC0 | ACMP0_CH0 | TIM0_CC1 #4<br>PCNT0_S0IN #2 | US0_TX #5/6<br>US1_TX #0<br>US1_CS #5<br>I2C0_SDA #4 | PRS_CH2 #0 |
| 4 | PC1 | ACMP0_CH1 | TIM0_CC2 #4<br>PCNT0_S1IN #2 | US0_RX #5/6<br>US1_TX #5<br>US1_RX #0<br>I2C0_SCL #4 | PRS_CH3 #0 |
| 5 | PB7 | LFXTAL_P | TIM1_CC0 #3 | US0_TX #4<br>US1_CLK #0 | |
| 6 | PB8 | LFXTAL_N | TIM1_CC1 #3 | US0_RX #4<br>US1_CS #0 | |
| 7 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | |
| 8 | PB11 | IDAC0_OUT | TIM1_CC2 #3<br>PCNT0_S1IN #4 | US1_CLK #4 | CMU_CLK1 #3<br>ACMP0_O #3 |
| 9 | AVDD_2 | Analog power supply 2. | | | |
| 10 | PB13 | HFXTAL_P | | US0_CLK #4/5<br>LEU0_TX #1 | |
| 11 | PB14 | HFXTAL_N | | US0_CS #4/5<br>LEU0_RX #1 | |
| 12 | AVDD_0 | Analog power supply 0. | | | |
| 13 | VDD_DREG | Power supply for on-chip voltage regulator. | | | |
| 14 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin. | | | |
| 15 | USB_VREGI | | | | |
| 16 | USB_VREGO | | | | |
| 17 | PC14 | | TIM0_CDTI1 #1/6<br>TIM1_CC1 #0<br>PCNT0_S1IN #0 | US0_CS #3<br>US1_CS #3/4<br>LEU0_TX #5<br>USB_DM | PRS_CH0 #2 |
| 18 | PC15 | | TIM0_CDTI2 #1/6<br>TIM1_CC2 #0 | US0_CLK #3<br>US1_CLK #3<br>LEU0_RX #5<br>USB_DP | PRS_CH1 #2 |

| QFN24 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 19 | PF0 | | TIM0_CC0 #5 | US1_CLK #2<br>LEU0_TX #3<br>I2C0_SDA #5 | DBG_SWCLK #0<br>BOOT_TX |
| 20 | PF1 | | TIM0_CC1 #5 | US1_CS #2<br>LEU0_RX #3<br>I2C0_SCL #5 | DBG_SWDIO #0<br>GPIO_EM4WU3<br>BOOT_RX |
| 21 | PF2 | | TIM0_CC2 #5/6<br>TIM2_CC0 #3 | US1_TX #4<br>LEU0_TX #4 | CMU_CLK0 #3<br>PRS_CH0 #3<br>GPIO_EM4WU4 |
| 22 | IOVDD_5 | Digital IO power supply 5. | | | |
| 23 | PE12 | ADC0_CH0 | TIM1_CC2 #1<br>TIM2_CC1 #3 | US0_RX #3<br>US0_CLK #0/6<br>I2C0_SDA #6 | CMU_CLK1 #2<br>PRS_CH1 #3 |
| 24 | PE13 | ADC0_CH1 | TIM2_CC2 #3 | US0_TX #3<br>US0_CS #0/6<br>I2C0_SCL #6 | ACMP0_O #0<br>PRS_CH2 #3<br>GPIO_EM4WU5 |

### 5.6.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

**Note:** Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

**Table 5.17. Alternate functionality overview**

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ACMP0_CH0 | PC0 | | | | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH1 | PC1 | | | | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_O | PE13 | | | PB11 | | | | Analog comparator ACMP0, digital output. |
| ADC0_CH0 | PE12 | | | | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PE13 | | | | | | | Analog to digital converter ADC0, input channel number 1. |
| BOOT_RX | PF1 | | | | | | | Bootloader RX. |
| BOOT_TX | PF0 | | | | | | | Bootloader TX. |
| CMU_CLK0 | | | | PF2 | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | | | PE12 | PB11 | | | | Clock Management Unit, clock output number 1. |
| DBG_SWCLK | PF0 | | | | | | | Debug-interface Serial Wire clock input.<br>Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | | | | | | | Debug-interface Serial Wire data input / output.<br>Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| GPIO_EM4WU0 | PA0 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU3 | PF1 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | PF2 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU5 | PE13 | | | | | | | Pin can be used to wake the system up from EM4 |
| HFXTAL_N | PB14 | | | | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | | | | | PC1 | PF1 | PE13 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | | | | PC0 | PF0 | PE12 | I2C0 Serial Data input / output. |
| IDAC0_OUT | PB11 | | | | | | | IDAC0 output. |
| LEU0_RX | | PB14 | | PF1 | PA0 | PC15 | | LEUART0 Receive input. |
| LEU0_TX | | PB13 | | PF0 | PF2 | PC14 | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LFXTAL_P | PB7 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | | | PC0 | | PA0 | | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | PC14 | | PC1 | | PB11 | | | Pulse Counter PCNT0 input number 1. |
| PRS_CH0 | PA0 | | PC14 | PF2 | | | | Peripheral Reflex System PRS, channel 0. |
| PRS_CH1 | | | PC15 | PE12 | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | PC0 | | | PE13 | | | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | PC1 | | | PA0 | | | | Peripheral Reflex System PRS, channel 3. |
| TIM0_CC0 | PA0 | PA0 | | | PA0 | PF0 | | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | | | | | PC0 | PF1 | PA0 | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | | | | | PC1 | PF2 | PF2 | Timer 0 Capture Compare input / output channel 2. |
| TIM0_CDTI1 | | PC14 | | | | | PC14 | Timer 0 Complimentary Dead Time Insertion channel 1. |
| TIM0_CDTI2 | | PC15 | | | | | PC15 | Timer 0 Complimentary Dead Time Insertion channel 2. |
| TIM1_CC0 | | | | PB7 | | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | | | PB8 | | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | | PB11 | | | | Timer 1 Capture Compare input / output channel 2. |
| TIM2_CC0 | | | | PF2 | | | | Timer 2 Capture Compare input / output channel 0. |
| TIM2_CC1 | | | | PE12 | | | | Timer 2 Capture Compare input / output channel 1. |
| TIM2_CC2 | | | | PE13 | | | | Timer 2 Capture Compare input / output channel 2. |
| US0_CLK | PE12 | | | PC15 | PB13 | PB13 | PE12 | USART0 clock input / output. |
| US0_CS | PE13 | | | PC14 | PB14 | PB14 | PE13 | USART0 chip select input / output. |
| US0_RX | | | | PE12 | PB8 | PC1 | PC1 | USART0 Asynchronous Receive.<br>USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | | | | PE13 | PB7 | PC0 | PC0 | USART0 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | | PF0 | PC15 | PB11 | | | USART1 clock input / output. |
| US1_CS | PB8 | | PF1 | PC14 | PC14 | PC0 | | USART1 chip select input / output. |
| US1_RX | PC1 | | | | PA0 | | | USART1 Asynchronous Receive.<br>USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | PC0 | | | | PF2 | PC1 | | USART1 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART1 Synchronous mode Master Output / Slave Input (MOSI). |
| USB_DM | PC14 | | | | | | | USB D- pin. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| USB_DMPU | PA0 | | | | | | | USB D- Pullup control. |
| USB_DP | PC15 | | | | | | | USB D+ pin. |
| USB_VREGI | USB_VREGI | | | | | | | USB Input to internal 3.3 V regulator |
| USB_VREGO | USB_VREGO | | | | | | | USB Decoupling for internal 3.3 V USB regulator and regulator output |

### 5.6.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32HG309 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

**Table 5.18. GPIO Pinout**

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Port A | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | PA0 |
| Port B | - | PB14 | PB13 | - | PB11 | - | - | PB8 | PB7 | - | - | - | - | - | - | - |
| Port C | PC15 | PC14 | - | - | - | - | - | - | - | - | - | - | - | - | PC1 | PC0 |
| Port D | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| Port E | - | - | PE13 | PE12 | - | - | - | - | - | - | - | - | - | - | - | - |
| Port F | - | - | - | - | - | - | - | - | - | - | - | - | - | PF2 | PF1 | PF0 |

## 5.7 EFM32HG310 (QFN32)

### 5.7.1 Pinout

The EFM32HG310 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

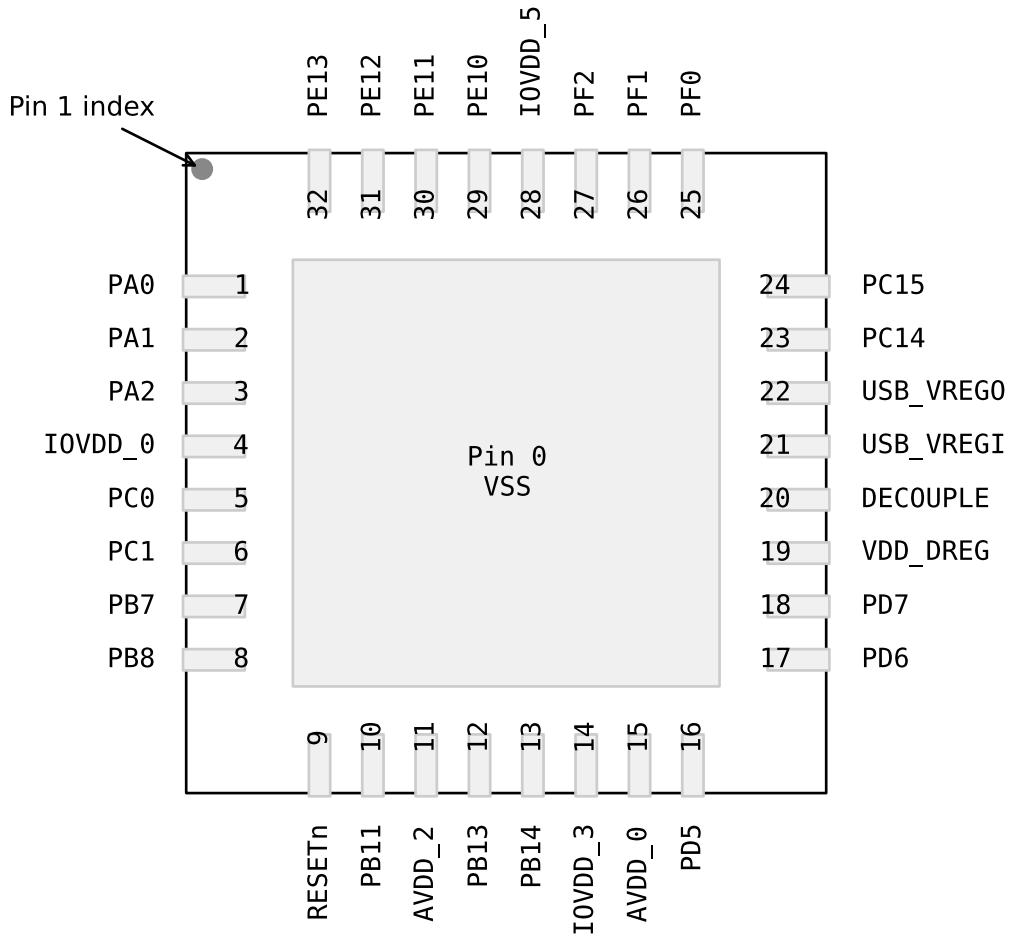



**Figure 5.7. EFM32HG310 Pinout (top view, not to scale)**

**Table 5.19. Device Pinout**

| QFN32 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 0 | VSS | Ground. | | | |
| 1 | PA0 | | TIM0_CC1 #6<br>TIM0_CC0 #0/1/4<br>PCNT0_S0IN #4 | USB_DMPU #0<br>US1_RX #4<br>LEU0_RX #4<br>I2C0_SDA #0 | PRS_CH0 #0<br>PRS_CH3 #3<br>GPIO_EM4WU0 |

| QFN32 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 2 | PA1 | | TIM0_CC0 #6<br>TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0<br>PRS_CH1 #0 |
| 3 | PA2 | | TIM0_CC2 #0/1 | | CMU_CLK0 #0 |
| 4 | IOVDD_0 | Digital IO power supply 0. | | | |
| 5 | PC0 | ACMP0_CH0 | TIM0_CC1 #4<br>PCNT0_S0IN #2 | US0_TX #5/6<br>US1_TX #0<br>US1_CS #5<br>I2C0_SDA #4 | PRS_CH2 #0 |
| 6 | PC1 | ACMP0_CH1 | TIM0_CC2 #4<br>PCNT0_S1IN #2 | US0_RX #5/6<br>US1_TX #5<br>US1_RX #0<br>I2C0_SCL #4 | PRS_CH3 #0 |
| 7 | PB7 | LFXTAL_P | TIM1_CC0 #3 | US0_TX #4<br>US1_CLK #0 | |
| 8 | PB8 | LFXTAL_N | TIM1_CC1 #3 | US0_RX #4<br>US1_CS #0 | |
| 9 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | |
| 10 | PB11 | IDAC0_OUT | TIM1_CC2 #3<br>PCNT0_S1IN #4 | US1_CLK #4 | CMU_CLK1 #3<br>ACMP0_O #3 |
| 11 | AVDD_2 | Analog power supply 2. | | | |
| 12 | PB13 | HFXTAL_P | | US0_CLK #4/5<br>LEU0_TX #1 | |
| 13 | PB14 | HFXTAL_N | | US0_CS #4/5<br>LEU0_RX #1 | |
| 14 | IOVDD_3 | Digital IO power supply 3. | | | |
| 15 | AVDD_0 | Analog power supply 0. | | | |
| 16 | PD5 | ADC0_CH5 | | LEU0_RX #0 | |
| 17 | PD6 | ADC0_CH6 | TIM1_CC0 #4<br>PCNT0_S0IN #3 | US1_RX #2/3<br>I2C0_SDA #1 | ACMP0_O #2 |
| 18 | PD7 | ADC0_CH7 | TIM1_CC1 #4<br>PCNT0_S1IN #3 | US1_TX #2/3<br>I2C0_SCL #1 | CMU_CLK0 #2 |
| 19 | VDD_DREG | Power supply for on-chip voltage regulator. | | | |
| 20 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin. | | | |
| 21 | USB_VREGI | | | | |
| 22 | USB_VREGO | | | | |

| QFN32 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 23 | PC14 | | TIM0_CDTI1 #1/6<br>TIM1_CC1 #0<br>PCNT0_S1IN #0 | US0_CS #3<br>US1_CS #3/4<br>LEU0_TX #5<br>USB_DM | PRS_CH0 #2 |
| 24 | PC15 | | TIM0_CDTI2 #1/6<br>TIM1_CC2 #0 | US0_CLK #3<br>US1_CLK #3<br>LEU0_RX #5<br>USB_DP | PRS_CH1 #2 |
| 25 | PF0 | | TIM0_CC0 #5 | US1_CLK #2<br>LEU0_TX #3<br>I2C0_SDA #5 | DBG_SWCLK #0<br>BOOT_TX |
| 26 | PF1 | | TIM0_CC1 #5 | US1_CS #2<br>LEU0_RX #3<br>I2C0_SCL #5 | DBG_SWDIO #0<br>GPIO_EM4WU3<br>BOOT_RX |
| 27 | PF2 | | TIM0_CC2 #5/6<br>TIM2_CC0 #3 | US1_TX #4<br>LEU0_TX #4 | CMU_CLK0 #3<br>PRS_CH0 #3<br>GPIO_EM4WU4 |
| 28 | IOVDD_5 | Digital IO power supply 5. | | | |
| 29 | PE10 | | TIM1_CC0 #1 | US0_TX #0 | PRS_CH2 #2 |
| 30 | PE11 | | TIM1_CC1 #1 | US0_RX #0 | PRS_CH3 #2 |
| 31 | PE12 | ADC0_CH0 | TIM1_CC2 #1<br>TIM2_CC1 #3 | US0_RX #3<br>US0_CLK #0/6<br>I2C0_SDA #6 | CMU_CLK1 #2<br>PRS_CH1 #3 |
| 32 | PE13 | ADC0_CH1 | TIM2_CC2 #3 | US0_TX #3<br>US0_CS #0/6<br>I2C0_SCL #6 | ACMP0_O #0<br>PRS_CH2 #3<br>GPIO_EM4WU5 |

### 5.7.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

**Note:** Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

**Table 5.20. Alternate functionality overview**

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ACMP0_CH0 | PC0 | | | | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH1 | PC1 | | | | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_O | PE13 | | PD6 | PB11 | | | | Analog comparator ACMP0, digital output. |
| ADC0_CH0 | PE12 | | | | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PE13 | | | | | | | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH5 | PD5 | | | | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | | | | Analog to digital converter ADC0, input channel number 6. |
| ADC0_CH7 | PD7 | | | | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PF1 | | | | | | | Bootloader RX. |
| BOOT_TX | PF0 | | | | | | | Bootloader TX. |
| CMU_CLK0 | PA2 | | PD7 | PF2 | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | | PE12 | PB11 | | | | Clock Management Unit, clock output number 1. |
| DBG_SWCLK | PF0 | | | | | | | Debug-interface Serial Wire clock input.<br>Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | | | | | | | Debug-interface Serial Wire data input / output.<br>Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| GPIO_EM4WU0 | PA0 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU3 | PF1 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | PF2 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU5 | PE13 | | | | | | | Pin can be used to wake the system up from EM4 |
| HFXTAL_N | PB14 | | | | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | | | PC1 | PF1 | PE13 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | | | PC0 | PF0 | PE12 | I2C0 Serial Data input / output. |
| IDAC0_OUT | PB11 | | | | | | | IDAC0 output. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LEU0_RX | PD5 | PB14 | | PF1 | PA0 | PC15 | | LEUART0 Receive input. |
| LEU0_TX | | PB13 | | PF0 | PF2 | PC14 | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | | | PC0 | PD6 | PA0 | | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | PC14 | | PC1 | PD7 | PB11 | | | Pulse Counter PCNT0 input number 1. |
| PRS_CH0 | PA0 | | PC14 | PF2 | | | | Peripheral Reflex System PRS, channel 0. |
| PRS_CH1 | PA1 | | PC15 | PE12 | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | PC0 | | PE10 | PE13 | | | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | PC1 | | PE11 | PA0 | | | | Peripheral Reflex System PRS, channel 3. |
| TIM0_CC0 | PA0 | PA0 | | | PA0 | PF0 | PA1 | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | | | PC0 | PF1 | PA0 | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | | | PC1 | PF2 | PF2 | Timer 0 Capture Compare input / output channel 2. |
| TIM0_CDTI1 | | PC14 | | | | | PC14 | Timer 0 Complimentary Dead Time Insertion channel 1. |
| TIM0_CDTI2 | | PC15 | | | | | PC15 | Timer 0 Complimentary Dead Time Insertion channel 2. |
| TIM1_CC0 | | PE10 | | PB7 | PD6 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | PE11 | | PB8 | PD7 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | | PB11 | | | | Timer 1 Capture Compare input / output channel 2. |
| TIM2_CC0 | | | | PF2 | | | | Timer 2 Capture Compare input / output channel 0. |
| TIM2_CC1 | | | | PE12 | | | | Timer 2 Capture Compare input / output channel 1. |
| TIM2_CC2 | | | | PE13 | | | | Timer 2 Capture Compare input / output channel 2. |
| US0_CLK | PE12 | | | PC15 | PB13 | PB13 | PE12 | USART0 clock input / output. |
| US0_CS | PE13 | | | PC14 | PB14 | PB14 | PE13 | USART0 chip select input / output. |
| US0_RX | PE11 | | | PE12 | PB8 | PC1 | PC1 | USART0 Asynchronous Receive.<br>USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | PE10 | | | PE13 | PB7 | PC0 | PC0 | USART0 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | | PF0 | PC15 | PB11 | | | USART1 clock input / output. |
| US1_CS | PB8 | | PF1 | PC14 | PC14 | PC0 | | USART1 chip select input / output. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| US1_RX | PC1 | | PD6 | PD6 | PA0 | | | USART1 Asynchronous Receive.<br>USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | PC0 | | PD7 | PD7 | PF2 | PC1 | | USART1 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART1 Synchronous mode Master Output / Slave Input (MOSI). |
| USB_DM | PC14 | | | | | | | USB D- pin. |
| USB_DMPU | PA0 | | | | | | | USB D- Pullup control. |
| USB_DP | PC15 | | | | | | | USB D+ pin. |
| USB_VREGI | USB_VREGI | | | | | | | USB Input to internal 3.3 V regulator |
| USB_VREGO | USB_VREGO | | | | | | | USB Decoupling for internal 3.3 V USB regulator and regulator output |

### 5.7.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32HG310 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

**Table 5.21. GPIO Pinout**

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Port A | - | - | - | - | - | - | - | - | - | - | - | - | - | PA2 | PA1 | PA0 |
| Port B | - | PB14 | PB13 | - | PB11 | - | - | PB8 | PB7 | - | - | - | - | - | - | - |
| Port C | PC15 | PC14 | - | - | - | - | - | - | - | - | - | - | - | - | PC1 | PC0 |
| Port D | - | - | - | - | - | - | - | - | PD7 | PD6 | PD5 | - | - | - | - | - |
| Port E | - | - | PE13 | PE12 | PE11 | PE10 | - | - | - | - | - | - | - | - | - | - |
| Port F | - | - | - | - | - | - | - | - | - | - | - | - | - | PF2 | PF1 | PF0 |

## 5.8 EFM32HG321 (TQFP48)

### 5.8.1 Pinout

The EFM32HG321 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

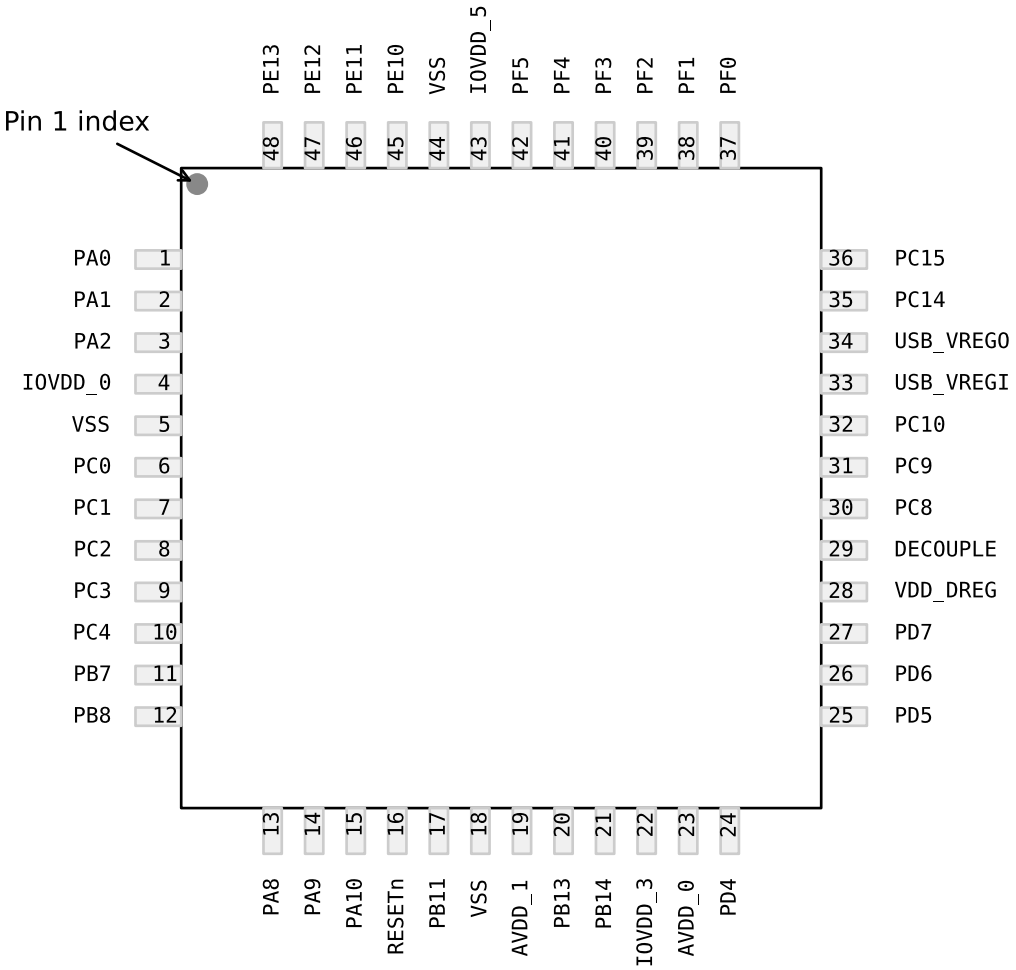



**Figure 5.8. EFM32HG321 Pinout (top view, not to scale)**

**Table 5.22. Device Pinout**

| QFP48 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| **Pin #** | **Pin Name** | **Analog** | **Timers** | **Communication** | **Other** |
| 1 | PA0 | | TIM0_CC1 #6<br>TIM0_CC0 #0/1/4<br>PCNT0_S0IN #4 | USB_DMPU #0<br>US1_RX #4<br>LEU0_RX #4<br>I2C0_SDA #0 | PRS_CH0 #0<br>PRS_CH3 #3<br>GPIO_EM4WU0 |

| QFP48 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 2 | PA1 | | TIM0_CC0 #6<br>TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0<br>PRS_CH1 #0 |
| 3 | PA2 | | TIM0_CC2 #0/1 | | CMU_CLK0 #0 |
| 4 | IOVDD_0 | Digital IO power supply 0. | | | |
| 5 | VSS | Ground. | | | |
| 6 | PC0 | ACMP0_CH0 | TIM0_CC1 #4<br>PCNT0_S0IN #2 | US0_TX #5/6<br>US1_TX #0<br>US1_CS #5<br>I2C0_SDA #4 | PRS_CH2 #0 |
| 7 | PC1 | ACMP0_CH1 | TIM0_CC2 #4<br>PCNT0_S1IN #2 | US0_RX #5/6<br>US1_TX #5<br>US1_RX #0<br>I2C0_SCL #4 | PRS_CH3 #0 |
| 8 | PC2 | ACMP0_CH2 | TIM0_CDTI0 #4 | US1_RX #5 | |
| 9 | PC3 | ACMP0_CH3 | TIM0_CDTI1 #4 | US1_CLK #5 | |
| 10 | PC4 | ACMP0_CH4 | TIM0_CDTI2 #4 | | GPIO_EM4WU6 |
| 11 | PB7 | LFXTAL_P | TIM1_CC0 #3 | US0_TX #4<br>US1_CLK #0 | |
| 12 | PB8 | LFXTAL_N | TIM1_CC1 #3 | US0_RX #4<br>US1_CS #0 | |
| 13 | PA8 | | TIM2_CC0 #0 | | |
| 14 | PA9 | | TIM2_CC1 #0 | | |
| 15 | PA10 | | TIM2_CC2 #0 | | |
| 16 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | |
| 17 | PB11 | IDAC0_OUT | TIM1_CC2 #3<br>PCNT0_S1IN #4 | US1_CLK #4 | CMU_CLK1 #3<br>ACMP0_O #3 |
| 18 | VSS | Ground. | | | |
| 19 | AVDD_1 | Analog power supply 1. | | | |
| 20 | PB13 | HFXTAL_P | | US0_CLK #4/5<br>LEU0_TX #1 | |
| 21 | PB14 | HFXTAL_N | | US0_CS #4/5<br>LEU0_RX #1 | |
| 22 | IOVDD_3 | Digital IO power supply 3. | | | |
| 23 | AVDD_0 | Analog power supply 0. | | | |
| 24 | PD4 | ADC0_CH4 | | LEU0_TX #0 | |

| QFP48 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 25 | PD5 | ADC0_CH5 | | LEU0_RX #0 | |
| 26 | PD6 | ADC0_CH6 | TIM1_CC0 #4<br>PCNT0_S0IN #3 | US1_RX #2/3<br>I2C0_SDA #1 | ACMP0_O #2 |
| 27 | PD7 | ADC0_CH7 | TIM1_CC1 #4<br>PCNT0_S1IN #3 | US1_TX #2/3<br>I2C0_SCL #1 | CMU_CLK0 #2 |
| 28 | VDD_DREG | Power supply for on-chip voltage regulator. | | | |
| 29 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin. | | | |
| 30 | PC8 | | TIM2_CC0 #2 | US0_CS #2 | |
| 31 | PC9 | | TIM2_CC1 #2 | US0_CLK #2 | GPIO_EM4WU2 |
| 32 | PC10 | | TIM2_CC2 #2 | US0_RX #2 | |
| 33 | USB_VREGI | | | | |
| 34 | USB_VREGO | | | | |
| 35 | PC14 | | TIM0_CDTI1 #1/6<br>TIM1_CC1 #0<br>PCNT0_S1IN #0 | US0_CS #3<br>US1_CS #3/4<br>LEU0_TX #5<br>USB_DM | PRS_CH0 #2 |
| 36 | PC15 | | TIM0_CDTI2 #1/6<br>TIM1_CC2 #0 | US0_CLK #3<br>US1_CLK #3<br>LEU0_RX #5<br>USB_DP | PRS_CH1 #2 |
| 37 | PF0 | | TIM0_CC0 #5 | US1_CLK #2<br>LEU0_TX #3<br>I2C0_SDA #5 | DBG_SWCLK #0<br>BOOT_TX |
| 38 | PF1 | | TIM0_CC1 #5 | US1_CS #2<br>LEU0_RX #3<br>I2C0_SCL #5 | DBG_SWDIO #0<br>GPIO_EM4WU3<br>BOOT_RX |
| 39 | PF2 | | TIM0_CC2 #5/6<br>TIM2_CC0 #3 | US1_TX #4<br>LEU0_TX #4 | CMU_CLK0 #3<br>PRS_CH0 #3<br>GPIO_EM4WU4 |
| 40 | PF3 | | TIM0_CDTI0 #5 | | PRS_CH0 #1 |
| 41 | PF4 | | TIM0_CDTI1 #5 | | PRS_CH1 #1 |
| 42 | PF5 | | TIM0_CDTI2 #5 | | PRS_CH2 #1 |
| 43 | IOVDD_5 | Digital IO power supply 5. | | | |
| 44 | VSS | Ground. | | | |
| 45 | PE10 | | TIM1_CC0 #1 | US0_TX #0 | PRS_CH2 #2 |

| QFP48 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 46 | PE11 | | TIM1_CC1 #1 | US0_RX #0 | PRS_CH3 #2 |
| 47 | PE12 | ADC0_CH0 | TIM1_CC2 #1<br>TIM2_CC1 #3 | US0_RX #3<br>US0_CLK #0/6<br>I2C0_SDA #6 | CMU_CLK1 #2<br>PRS_CH1 #3 |
| 48 | PE13 | ADC0_CH1 | TIM2_CC2 #3 | US0_TX #3<br>US0_CS #0/6<br>I2C0_SCL #6 | ACMP0_O #0<br>PRS_CH2 #3<br>GPIO_EM4WU5 |

### 5.8.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

**Note:** Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

**Table 5.23. Alternate functionality overview**

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ACMP0_CH0 | PC0 | | | | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH1 | PC1 | | | | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_CH2 | PC2 | | | | | | | Analog comparator ACMP0, channel 2. |
| ACMP0_CH3 | PC3 | | | | | | | Analog comparator ACMP0, channel 3. |
| ACMP0_CH4 | PC4 | | | | | | | Analog comparator ACMP0, channel 4. |
| ACMP0_O | PE13 | | PD6 | PB11 | | | | Analog comparator ACMP0, digital output. |
| ADC0_CH0 | PE12 | | | | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PE13 | | | | | | | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH4 | PD4 | | | | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | | | | Analog to digital converter ADC0, input channel number 6. |
| ADC0_CH7 | PD7 | | | | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PF1 | | | | | | | Bootloader RX. |
| BOOT_TX | PF0 | | | | | | | Bootloader TX. |
| CMU_CLK0 | PA2 | | PD7 | PF2 | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | | PE12 | PB11 | | | | Clock Management Unit, clock output number 1. |
| DBG_SWCLK | PF0 | | | | | | | Debug-interface Serial Wire clock input.<br>Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | | | | | | | Debug-interface Serial Wire data input / output.<br>Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| GPIO_EM4WU0 | PA0 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU2 | PC9 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU3 | PF1 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | PF2 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU5 | PE13 | | | | | | | Pin can be used to wake the system up from EM4 |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| GPIO_EM4WU6 | PC4 | | | | | | | Pin can be used to wake the system up from EM4 |
| HFXTAL_N | PB14 | | | | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | | | PC1 | PF1 | PE13 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | | | PC0 | PF0 | PE12 | I2C0 Serial Data input / output. |
| IDAC0_OUT | PB11 | | | | | | | IDAC0 output. |
| LEU0_RX | PD5 | PB14 | | PF1 | PA0 | PC15 | | LEUART0 Receive input. |
| LEU0_TX | PD4 | PB13 | | PF0 | PF2 | PC14 | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | | | PC0 | PD6 | PA0 | | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | PC14 | | PC1 | PD7 | PB11 | | | Pulse Counter PCNT0 input number 1. |
| PRS_CH0 | PA0 | PF3 | PC14 | PF2 | | | | Peripheral Reflex System PRS, channel 0. |
| PRS_CH1 | PA1 | PF4 | PC15 | PE12 | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | PC0 | PF5 | PE10 | PE13 | | | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | PC1 | | PE11 | PA0 | | | | Peripheral Reflex System PRS, channel 3. |
| TIM0_CC0 | PA0 | PA0 | | | PA0 | PF0 | PA1 | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | | | PC0 | PF1 | PA0 | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | | | PC1 | PF2 | PF2 | Timer 0 Capture Compare input / output channel 2. |
| TIM0_CDTI0 | | | | | PC2 | PF3 | | Timer 0 Complimentary Dead Time Insertion channel 0. |
| TIM0_CDTI1 | | PC14 | | | PC3 | PF4 | PC14 | Timer 0 Complimentary Dead Time Insertion channel 1. |
| TIM0_CDTI2 | | PC15 | | | PC4 | PF5 | PC15 | Timer 0 Complimentary Dead Time Insertion channel 2. |
| TIM1_CC0 | | PE10 | | PB7 | PD6 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | PE11 | | PB8 | PD7 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | | PB11 | | | | Timer 1 Capture Compare input / output channel 2. |
| TIM2_CC0 | PA8 | | PC8 | PF2 | | | | Timer 2 Capture Compare input / output channel 0. |
| TIM2_CC1 | PA9 | | PC9 | PE12 | | | | Timer 2 Capture Compare input / output channel 1. |
| TIM2_CC2 | PA10 | | PC10 | PE13 | | | | Timer 2 Capture Compare input / output channel 2. |
| US0_CLK | PE12 | | PC9 | PC15 | PB13 | PB13 | PE12 | USART0 clock input / output. |
| US0_CS | PE13 | | PC8 | PC14 | PB14 | PB14 | PE13 | USART0 chip select input / output. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| US0_RX | PE11 | | PC10 | PE12 | PB8 | PC1 | PC1 | USART0 Asynchronous Receive.<br>USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | PE10 | | | PE13 | PB7 | PC0 | PC0 | USART0 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | | PF0 | PC15 | PB11 | PC3 | | USART1 clock input / output. |
| US1_CS | PB8 | | PF1 | PC14 | PC14 | PC0 | | USART1 chip select input / output. |
| US1_RX | PC1 | | PD6 | PD6 | PA0 | PC2 | | USART1 Asynchronous Receive.<br>USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | PC0 | | PD7 | PD7 | PF2 | PC1 | | USART1 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART1 Synchronous mode Master Output / Slave Input (MOSI). |
| USB_DM | PC14 | | | | | | | USB D- pin. |
| USB_DMPU | PA0 | | | | | | | USB D- Pullup control. |
| USB_DP | PC15 | | | | | | | USB D+ pin. |
| USB_VREGI | USB_VREGI | | | | | | | USB Input to internal 3.3 V regulator |
| USB_VREGO | USB_VREGO | | | | | | | USB Decoupling for internal 3.3 V USB regulator and regulator output |

### 5.8.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32HG321 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

**Table 5.24. GPIO Pinout**

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Port A | - | - | - | - | - | PA10 | PA9 | PA8 | - | - | - | - | - | PA2 | PA1 | PA0 |
| Port B | - | PB14 | PB13 | - | PB11 | - | - | PB8 | PB7 | - | - | - | - | - | - | - |
| Port C | PC15 | PC14 | - | - | - | PC10 | PC9 | PC8 | - | - | - | PC4 | PC3 | PC2 | PC1 | PC0 |
| Port D | - | - | - | - | - | - | - | - | PD7 | PD6 | PD5 | PD4 | - | - | - | - |
| Port E | - | - | PE13 | PE12 | PE11 | PE10 | - | - | - | - | - | - | - | - | - | - |
| Port F | - | - | - | - | - | - | - | - | - | - | PF5 | PF4 | PF3 | PF2 | PF1 | PF0 |

### 5.9 EFM32HG322 (TQFP48)

#### 5.9.1 Pinout

The EFM32HG322 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

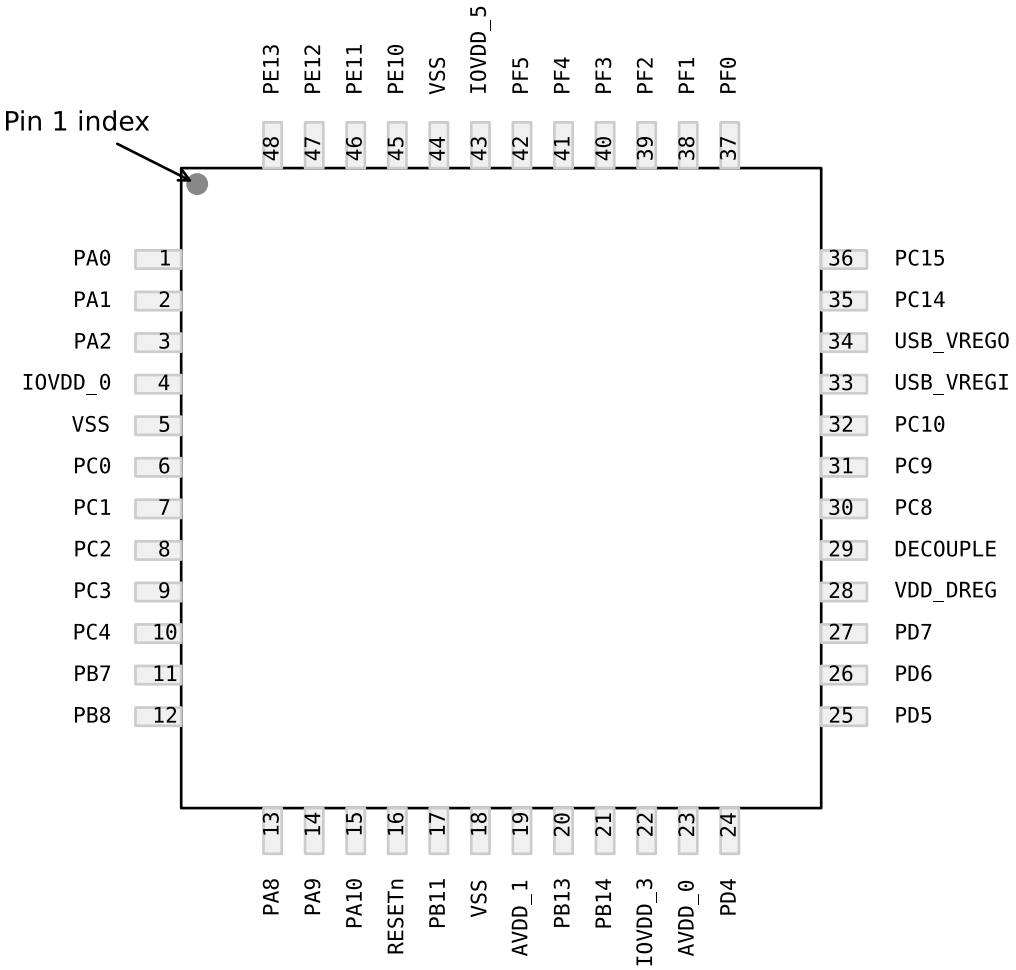



**Figure 5.9. EFM32HG322Pinout (top view, not to scale)**

**Table 5.25. Device Pinout**

| QFP48 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| **Pin #** | **Pin Name** | **Analog** | **Timers** | **Communication** | **Other** |
| 1 | PA0 | | TIM0_CC1 #6<br>TIM0_CC0 #0/1/4<br>PCNT0_S0IN #4 | USB_DMPU #0<br>US1_RX #4<br>LEU0_RX #4<br>I2C0_SDA #0 | PRS_CH0 #0<br>PRS_CH3 #3<br>GPIO_EM4WU0 |

| QFP48 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 2 | PA1 | | TIM0_CC0 #6<br>TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0<br>PRS_CH1 #0 |
| 3 | PA2 | | TIM0_CC2 #0/1 | | CMU_CLK0 #0 |
| 4 | IOVDD_0 | Digital IO power supply 0. | | | |
| 5 | VSS | Ground. | | | |
| 6 | PC0 | ACMP0_CH0 | TIM0_CC1 #4<br>PCNT0_S0IN #2 | US0_TX #5/6<br>US1_TX #0<br>US1_CS #5<br>I2C0_SDA #4 | PRS_CH2 #0 |
| 7 | PC1 | ACMP0_CH1 | TIM0_CC2 #4<br>PCNT0_S1IN #2 | US0_RX #5/6<br>US1_TX #5<br>US1_RX #0<br>I2C0_SCL #4 | PRS_CH3 #0 |
| 8 | PC2 | ACMP0_CH2 | TIM0_CDTI0 #4 | US1_RX #5 | |
| 9 | PC3 | ACMP0_CH3 | TIM0_CDTI1 #4 | US1_CLK #5 | |
| 10 | PC4 | ACMP0_CH4 | TIM0_CDTI2 #4 | | GPIO_EM4WU6 |
| 11 | PB7 | LFXTAL_P | TIM1_CC0 #3 | US0_TX #4<br>US1_CLK #0 | |
| 12 | PB8 | LFXTAL_N | TIM1_CC1 #3 | US0_RX #4<br>US1_CS #0 | |
| 13 | PA8 | | TIM2_CC0 #0 | | |
| 14 | PA9 | | TIM2_CC1 #0 | | |
| 15 | PA10 | | TIM2_CC2 #0 | | |
| 16 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | |
| 17 | PB11 | IDAC0_OUT | TIM1_CC2 #3<br>PCNT0_S1IN #4 | US1_CLK #4 | CMU_CLK1 #3<br>ACMP0_O #3 |
| 18 | VSS | Ground. | | | |
| 19 | AVDD_1 | Analog power supply 1. | | | |
| 20 | PB13 | HFXTAL_P | | US0_CLK #4/5<br>LEU0_TX #1 | |
| 21 | PB14 | HFXTAL_N | | US0_CS #4/5<br>LEU0_RX #1 | |
| 22 | IOVDD_3 | Digital IO power supply 3. | | | |
| 23 | AVDD_0 | Analog power supply 0. | | | |
| 24 | PD4 | ADC0_CH4 | | LEU0_TX #0 | |

| QFP48 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 25 | PD5 | ADC0_CH5 | | LEU0_RX #0 | |
| 26 | PD6 | ADC0_CH6 | TIM1_CC0 #4<br>PCNT0_S0IN #3 | US1_RX #2/3<br>I2C0_SDA #1 | ACMP0_O #2 |
| 27 | PD7 | ADC0_CH7 | TIM1_CC1 #4<br>PCNT0_S1IN #3 | US1_TX #2/3<br>I2C0_SCL #1 | CMU_CLK0 #2 |
| 28 | VDD_DREG | Power supply for on-chip voltage regulator. | | | |
| 29 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin. | | | |
| 30 | PC8 | | TIM2_CC0 #2 | US0_CS #2 | |
| 31 | PC9 | | TIM2_CC1 #2 | US0_CLK #2 | GPIO_EM4WU2 |
| 32 | PC10 | | TIM2_CC2 #2 | US0_RX #2 | |
| 33 | USB_VREGI | | | | |
| 34 | USB_VREGO | | | | |
| 35 | PC14 | | TIM0_CDTI1 #1/6<br>TIM1_CC1 #0<br>PCNT0_S1IN #0 | US0_CS #3<br>US1_CS #3/4<br>LEU0_TX #5<br>USB_DM | PRS_CH0 #2 |
| 36 | PC15 | | TIM0_CDTI2 #1/6<br>TIM1_CC2 #0 | US0_CLK #3<br>US1_CLK #3<br>LEU0_RX #5<br>USB_DP | PRS_CH1 #2 |
| 37 | PF0 | | TIM0_CC0 #5 | US1_CLK #2<br>LEU0_TX #3<br>I2C0_SDA #5 | DBG_SWCLK #0<br>BOOT_TX |
| 38 | PF1 | | TIM0_CC1 #5 | US1_CS #2<br>LEU0_RX #3<br>I2C0_SCL #5 | DBG_SWDIO #0<br>GPIO_EM4WU3<br>BOOT_RX |
| 39 | PF2 | | TIM0_CC2 #5/6<br>TIM2_CC0 #3 | US1_TX #4<br>LEU0_TX #4 | CMU_CLK0 #3<br>PRS_CH0 #3<br>GPIO_EM4WU4 |
| 40 | PF3 | | TIM0_CDTI0 #5 | | PRS_CH0 #1 |
| 41 | PF4 | | TIM0_CDTI1 #5 | | PRS_CH1 #1 |
| 42 | PF5 | | TIM0_CDTI2 #5 | | PRS_CH2 #1 |
| 43 | IOVDD_5 | Digital IO power supply 5. | | | |
| 44 | VSS | Ground. | | | |
| 45 | PE10 | | TIM1_CC0 #1 | US0_TX #0 | PRS_CH2 #2 |

| QFP48 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 46 | PE11 | | TIM1_CC1 #1 | US0_RX #0 | PRS_CH3 #2 |
| 47 | PE12 | ADC0_CH0 | TIM1_CC2 #1<br>TIM2_CC1 #3 | US0_RX #3<br>US0_CLK #0/6<br>I2C0_SDA #6 | CMU_CLK1 #2<br>PRS_CH1 #3 |
| 48 | PE13 | ADC0_CH1 | TIM2_CC2 #3 | US0_TX #3<br>US0_CS #0/6<br>I2C0_SCL #6 | ACMP0_O #0<br>PRS_CH2 #3<br>GPIO_EM4WU5 |

### 5.9.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

**Note:** Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

**Table 5.26. Alternate functionality overview**

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ACMP0_CH0 | PC0 | | | | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH1 | PC1 | | | | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_CH2 | PC2 | | | | | | | Analog comparator ACMP0, channel 2. |
| ACMP0_CH3 | PC3 | | | | | | | Analog comparator ACMP0, channel 3. |
| ACMP0_CH4 | PC4 | | | | | | | Analog comparator ACMP0, channel 4. |
| ACMP0_O | PE13 | | PD6 | PB11 | | | | Analog comparator ACMP0, digital output. |
| ADC0_CH0 | PE12 | | | | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PE13 | | | | | | | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH4 | PD4 | | | | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | | | | Analog to digital converter ADC0, input channel number 6. |
| ADC0_CH7 | PD7 | | | | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PF1 | | | | | | | Bootloader RX. |
| BOOT_TX | PF0 | | | | | | | Bootloader TX. |
| CMU_CLK0 | PA2 | | PD7 | PF2 | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | | PE12 | PB11 | | | | Clock Management Unit, clock output number 1. |
| DBG_SWCLK | PF0 | | | | | | | Debug-interface Serial Wire clock input.<br>Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | | | | | | | Debug-interface Serial Wire data input / output.<br>Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| GPIO_EM4WU0 | PA0 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU2 | PC9 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU3 | PF1 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | PF2 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU5 | PE13 | | | | | | | Pin can be used to wake the system up from EM4 |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| GPIO_EM4WU6 | PC4 | | | | | | | Pin can be used to wake the system up from EM4 |
| HFXTAL_N | PB14 | | | | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | | | PC1 | PF1 | PE13 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | | | PC0 | PF0 | PE12 | I2C0 Serial Data input / output. |
| IDAC0_OUT | PB11 | | | | | | | IDAC0 output. |
| LEU0_RX | PD5 | PB14 | | PF1 | PA0 | PC15 | | LEUART0 Receive input. |
| LEU0_TX | PD4 | PB13 | | PF0 | PF2 | PC14 | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | | | PC0 | PD6 | PA0 | | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | PC14 | | PC1 | PD7 | PB11 | | | Pulse Counter PCNT0 input number 1. |
| PRS_CH0 | PA0 | PF3 | PC14 | PF2 | | | | Peripheral Reflex System PRS, channel 0. |
| PRS_CH1 | PA1 | PF4 | PC15 | PE12 | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | PC0 | PF5 | PE10 | PE13 | | | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | PC1 | | PE11 | PA0 | | | | Peripheral Reflex System PRS, channel 3. |
| TIM0_CC0 | PA0 | PA0 | | | PA0 | PF0 | PA1 | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | | | PC0 | PF1 | PA0 | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | | | PC1 | PF2 | PF2 | Timer 0 Capture Compare input / output channel 2. |
| TIM0_CDTI0 | | | | | PC2 | PF3 | | Timer 0 Complimentary Dead Time Insertion channel 0. |
| TIM0_CDTI1 | | PC14 | | | PC3 | PF4 | PC14 | Timer 0 Complimentary Dead Time Insertion channel 1. |
| TIM0_CDTI2 | | PC15 | | | PC4 | PF5 | PC15 | Timer 0 Complimentary Dead Time Insertion channel 2. |
| TIM1_CC0 | | PE10 | | PB7 | PD6 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | PE11 | | PB8 | PD7 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | | PB11 | | | | Timer 1 Capture Compare input / output channel 2. |
| TIM2_CC0 | PA8 | | PC8 | PF2 | | | | Timer 2 Capture Compare input / output channel 0. |
| TIM2_CC1 | PA9 | | PC9 | PE12 | | | | Timer 2 Capture Compare input / output channel 1. |
| TIM2_CC2 | PA10 | | PC10 | PE13 | | | | Timer 2 Capture Compare input / output channel 2. |
| US0_CLK | PE12 | | PC9 | PC15 | PB13 | PB13 | PE12 | USART0 clock input / output. |
| US0_CS | PE13 | | PC8 | PC14 | PB14 | PB14 | PE13 | USART0 chip select input / output. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| US0_RX | PE11 | | PC10 | PE12 | PB8 | PC1 | PC1 | USART0 Asynchronous Receive.<br>USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | PE10 | | | PE13 | PB7 | PC0 | PC0 | USART0 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | | PF0 | PC15 | PB11 | PC3 | | USART1 clock input / output. |
| US1_CS | PB8 | | PF1 | PC14 | PC14 | PC0 | | USART1 chip select input / output. |
| US1_RX | PC1 | | PD6 | PD6 | PA0 | PC2 | | USART1 Asynchronous Receive.<br>USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | PC0 | | PD7 | PD7 | PF2 | PC1 | | USART1 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART1 Synchronous mode Master Output / Slave Input (MOSI). |
| USB_DM | PC14 | | | | | | | USB D- pin. |
| USB_DMPU | PA0 | | | | | | | USB D- Pullup control. |
| USB_DP | PC15 | | | | | | | USB D+ pin. |
| USB_VREGI | USB_VREGI | | | | | | | USB Input to internal 3.3 V regulator |
| USB_VREGO | USB_VREGO | | | | | | | USB Decoupling for internal 3.3 V USB regulator and regulator output |

### 5.9.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32HG322 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

**Table 5.27. GPIO Pinout**

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Port A | - | - | - | - | - | PA10 | PA9 | PA8 | - | - | - | - | - | PA2 | PA1 | PA0 |
| Port B | - | PB14 | PB13 | - | PB11 | - | - | PB8 | PB7 | - | - | - | - | - | - | - |
| Port C | PC15 | PC14 | - | - | - | PC10 | PC9 | PC8 | - | - | - | PC4 | PC3 | PC2 | PC1 | PC0 |
| Port D | - | - | - | - | - | - | - | - | PD7 | PD6 | PD5 | PD4 | - | - | - | - |
| Port E | - | - | PE13 | PE12 | PE11 | PE10 | - | - | - | - | - | - | - | - | - | - |
| Port F | - | - | - | - | - | - | - | - | - | - | PF5 | PF4 | PF3 | PF2 | PF1 | PF0 |

## 5.10 EFM32HG350 (CSP36)

### 5.10.1 Pinout

The EFM32HG350 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

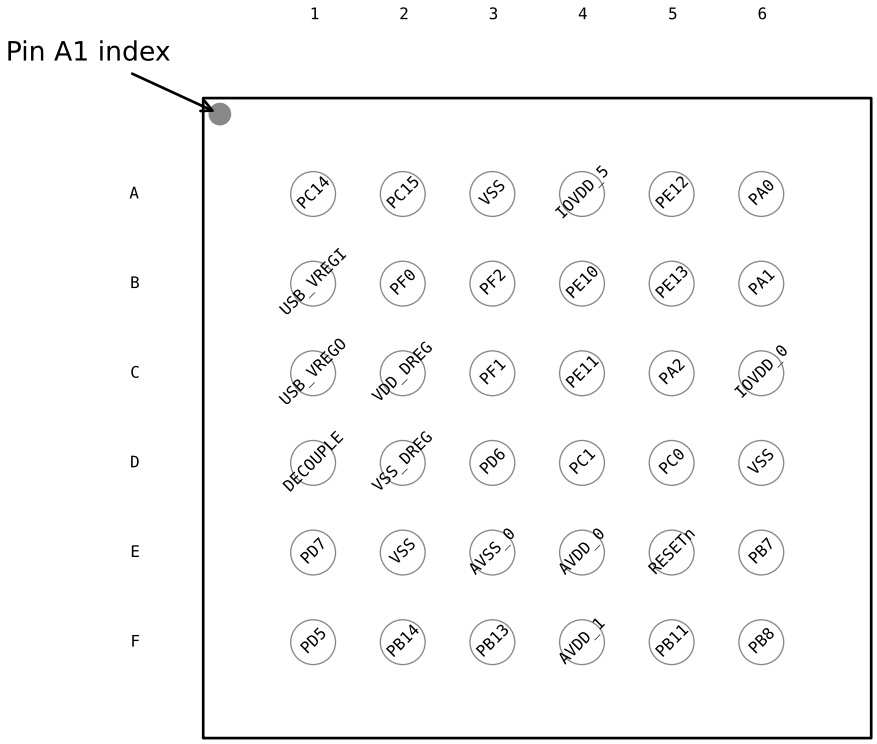



**Figure 5.10. EFM32HG350 Pinout (top view, not to scale)**

**Table 5.28. Device Pinout**

| CSP36 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| **Pin #** | **Pin Name** | **Analog** | **Timers** | **Communication** | **Other** |
| A1 | PC14 | | TIM0_CDTI1 #1/6<br>TIM1_CC1 #0<br>PCNT0_S1IN #0 | US0_CS #3<br>US1_CS #3/4<br>LEU0_TX #5<br>USB_DM | PRS_CH0 #2 |

| CSP36 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| A2 | PC15 | | TIM0_CDTI2 #1/6<br>TIM1_CC2 #0 | US0_CLK #3<br>US1_CLK #3<br>LEU0_RX #5<br>USB_DP | PRS_CH1 #2 |
| A3 | VSS | Ground. | | | |
| A4 | IOVDD_5 | Digital IO power supply 5. | | | |
| A5 | PE12 | ADC0_CH0 | TIM1_CC2 #1<br>TIM2_CC1 #3 | US0_RX #3<br>US0_CLK #0/6<br>I2C0_SDA #6 | CMU_CLK1 #2<br>PRS_CH1 #3 |
| A6 | PA0 | | TIM0_CC1 #6<br>TIM0_CC0 #0/1/4<br>PCNT0_S0IN #4 | USB_DMPU #0<br>US1_RX #4<br>LEU0_RX #4<br>I2C0_SDA #0 | PRS_CH0 #0<br>PRS_CH3 #3<br>GPIO_EM4WU0 |
| B1 | USB_VREGI | | | | |
| B2 | PF0 | | TIM0_CC0 #5 | US1_CLK #2<br>LEU0_TX #3<br>I2C0_SDA #5 | DBG_SWCLK #0<br>BOOT_TX |
| B3 | PF2 | | TIM0_CC2 #5/6<br>TIM2_CC0 #3 | US1_TX #4<br>LEU0_TX #4 | CMU_CLK0 #3<br>PRS_CH0 #3<br>GPIO_EM4WU4 |
| B4 | PE10 | | TIM1_CC0 #1 | US0_TX #0 | PRS_CH2 #2 |
| B5 | PE13 | ADC0_CH1 | TIM2_CC2 #3 | US0_TX #3<br>US0_CS #0/6<br>I2C0_SCL #6 | ACMP0_O #0<br>PRS_CH2 #3<br>GPIO_EM4WU5 |
| B6 | PA1 | | TIM0_CC0 #6<br>TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0<br>PRS_CH1 #0 |
| C1 | USB_VREGO | | | | |
| C2 | VDD_DREG | Power supply for on-chip voltage regulator. | | | |
| C3 | PF1 | | TIM0_CC1 #5 | US1_CS #2<br>LEU0_RX #3<br>I2C0_SCL #5 | DBG_SWDIO #0<br>GPIO_EM4WU3<br>BOOT_RX |
| C4 | PE11 | | TIM1_CC1 #1 | US0_RX #0 | PRS_CH3 #2 |
| C5 | PA2 | | TIM0_CC2 #0/1 | | CMU_CLK0 #0 |
| C6 | IOVDD_0 | Digital IO power supply 0. | | | |
| D1 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin. | | | |

| CSP36 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| D2 | VSS_DREG | Ground for on-chip voltage regulator. | | | |
| D3 | PD6 | ADC0_CH6 | TIM1_CC0 #4<br>PCNT0_S0IN #3 | US1_RX #2/3<br>I2C0_SDA #1 | ACMP0_O #2 |
| D4 | PC1 | ACMP0_CH1 | TIM0_CC2 #4<br>PCNT0_S1IN #2 | US0_RX #5/6<br>US1_TX #5<br>US1_RX #0<br>I2C0_SCL #4 | PRS_CH3 #0 |
| D5 | PC0 | ACMP0_CH0 | TIM0_CC1 #4<br>PCNT0_S0IN #2 | US0_TX #5/6<br>US1_TX #0<br>US1_CS #5<br>I2C0_SDA #4 | PRS_CH2 #0 |
| D6 | VSS | Ground. | | | |
| E1 | PD7 | ADC0_CH7 | TIM1_CC1 #4<br>PCNT0_S1IN #3 | US1_TX #2/3<br>I2C0_SCL #1 | CMU_CLK0 #2 |
| E2 | VSS | Ground. | | | |
| E3 | AVSS_0 | Analog ground 0. | | | |
| E4 | AVDD_0 | Analog power supply 0. | | | |
| E5 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | |
| E6 | PB7 | LFXTAL_P | TIM1_CC0 #3 | US0_TX #4<br>US1_CLK #0 | |
| F1 | PD5 | ADC0_CH5 | | LEU0_RX #0 | |
| F2 | PB14 | HFXTAL_N | | US0_CS #4/5<br>LEU0_RX #1 | |
| F3 | PB13 | HFXTAL_P | | US0_CLK #4/5<br>LEU0_TX #1 | |
| F4 | AVDD_1 | Analog power supply 1. | | | |
| F5 | PB11 | IDAC0_OUT | TIM1_CC2 #3<br>PCNT0_S1IN #4 | US1_CLK #4 | CMU_CLK1 #3<br>ACMP0_O #3 |
| F6 | PB8 | LFXTAL_N | TIM1_CC1 #3 | US0_RX #4<br>US1_CS #0 | |

### 5.10.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

**Note:** Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

**Table 5.29. Alternate functionality overview**

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ACMP0_CH0 | PC0 | | | | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH1 | PC1 | | | | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_O | PE13 | | PD6 | PB11 | | | | Analog comparator ACMP0, digital output. |
| ADC0_CH0 | PE12 | | | | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PE13 | | | | | | | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH5 | PD5 | | | | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | | | | Analog to digital converter ADC0, input channel number 6. |
| ADC0_CH7 | PD7 | | | | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PF1 | | | | | | | Bootloader RX. |
| BOOT_TX | PF0 | | | | | | | Bootloader TX. |
| CMU_CLK0 | PA2 | | PD7 | PF2 | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | | PE12 | PB11 | | | | Clock Management Unit, clock output number 1. |
| DBG_SWCLK | PF0 | | | | | | | Debug-interface Serial Wire clock input.<br>Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | | | | | | | Debug-interface Serial Wire data input / output.<br>Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| GPIO_EM4WU0 | PA0 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU3 | PF1 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | PF2 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU5 | PE13 | | | | | | | Pin can be used to wake the system up from EM4 |
| HFXTAL_N | PB14 | | | | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | | | PC1 | PF1 | PE13 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | | | PC0 | PF0 | PE12 | I2C0 Serial Data input / output. |
| IDAC0_OUT | PB11 | | | | | | | IDAC0 output. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LEU0_RX | PD5 | PB14 | | PF1 | PA0 | PC15 | | LEUART0 Receive input. |
| LEU0_TX | | PB13 | | PF0 | PF2 | PC14 | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | | | PC0 | PD6 | PA0 | | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | PC14 | | PC1 | PD7 | PB11 | | | Pulse Counter PCNT0 input number 1. |
| PRS_CH0 | PA0 | | PC14 | PF2 | | | | Peripheral Reflex System PRS, channel 0. |
| PRS_CH1 | PA1 | | PC15 | PE12 | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | PC0 | | PE10 | PE13 | | | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | PC1 | | PE11 | PA0 | | | | Peripheral Reflex System PRS, channel 3. |
| TIM0_CC0 | PA0 | PA0 | | | PA0 | PF0 | PA1 | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | | | PC0 | PF1 | PA0 | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | | | PC1 | PF2 | PF2 | Timer 0 Capture Compare input / output channel 2. |
| TIM0_CDTI1 | | PC14 | | | | | PC14 | Timer 0 Complimentary Dead Time Insertion channel 1. |
| TIM0_CDTI2 | | PC15 | | | | | PC15 | Timer 0 Complimentary Dead Time Insertion channel 2. |
| TIM1_CC0 | | PE10 | | PB7 | PD6 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | PE11 | | PB8 | PD7 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | | PB11 | | | | Timer 1 Capture Compare input / output channel 2. |
| TIM2_CC0 | | | | PF2 | | | | Timer 2 Capture Compare input / output channel 0. |
| TIM2_CC1 | | | | PE12 | | | | Timer 2 Capture Compare input / output channel 1. |
| TIM2_CC2 | | | | PE13 | | | | Timer 2 Capture Compare input / output channel 2. |
| US0_CLK | PE12 | | | PC15 | PB13 | PB13 | PE12 | USART0 clock input / output. |
| US0_CS | PE13 | | | PC14 | PB14 | PB14 | PE13 | USART0 chip select input / output. |
| US0_RX | PE11 | | | PE12 | PB8 | PC1 | PC1 | USART0 Asynchronous Receive.<br>USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | PE10 | | | PE13 | PB7 | PC0 | PC0 | USART0 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | | PF0 | PC15 | PB11 | | | USART1 clock input / output. |
| US1_CS | PB8 | | PF1 | PC14 | PC14 | PC0 | | USART1 chip select input / output. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| US1_RX | PC1 | | PD6 | PD6 | PA0 | | | USART1 Asynchronous Receive.<br>USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | PC0 | | PD7 | PD7 | PF2 | PC1 | | USART1 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART1 Synchronous mode Master Output / Slave Input (MOSI). |
| USB_DM | PC14 | | | | | | | USB D- pin. |
| USB_DMPU | PA0 | | | | | | | USB D- Pullup control. |
| USB_DP | PC15 | | | | | | | USB D+ pin. |
| USB_VREGI | USB_VREGI | | | | | | | USB Input to internal 3.3 V regulator |
| USB_VREGO | USB_VREGO | | | | | | | USB Decoupling for internal 3.3 V USB regulator and regulator output |

### 5.10.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32HG350 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

**Table 5.30. GPIO Pinout**

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Port A | - | - | - | - | - | - | - | - | - | - | - | - | - | PA2 | PA1 | PA0 |
| Port B | - | PB14 | PB13 | - | PB11 | - | - | PB8 | PB7 | - | - | - | - | - | - | - |
| Port C | PC15 | PC14 | - | - | - | - | - | - | - | - | - | - | - | - | PC1 | PC0 |
| Port D | - | - | - | - | - | - | - | - | PD7 | PD6 | PD5 | - | - | - | - | - |
| Port E | - | - | PE13 | PE12 | PE11 | PE10 | - | - | - | - | - | - | - | - | - | - |
| Port F | - | - | - | - | - | - | - | - | - | - | - | - | - | PF2 | PF1 | PF0 |

# 6. CSP36 Package Specifications

## 6.1 CSP36 Package Dimensions

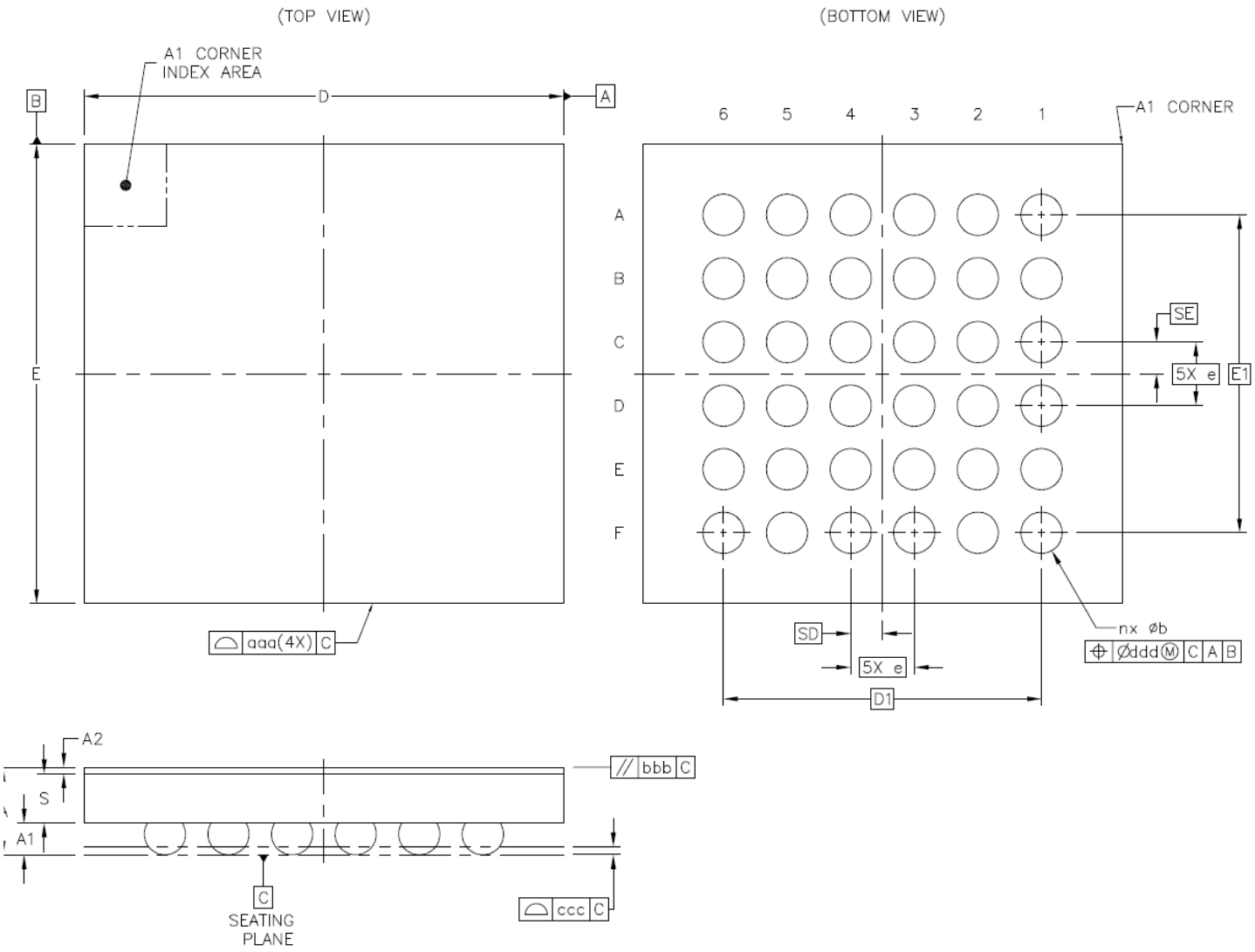



**Figure 6.1. CSP81**

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Primary datum “C” and seating plane are defined by the spherical crowns of the solder balls.
4. Dimension “b” is measured at the maximum solder bump diameter, parallel to primary datum “C”.
5. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

**Table 6.1. CSP36 (Dimensions in mm)**

| Symbol | A | A1 | A2 | b | S | D | E | e | D1 | E1 | SD | SE | n | aaa | bbb | ccc | ddd |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Min | 0.491 | 0.17 | 0.036 | 0.23 | 0.3075 | 3.016 BSC. | 2.891 BSC. | 0.40 BSC. | 2.00 BSC. | 2.00 BSC. | 0.2 | 0.2 | 36 | 0.03 | 0.06 | 0.05 | 0.015 |
| Nom | 0.55 | - | 0.040 | - | 0.31 | | | | | | | | | | | | |
| Max | 0.609 | 0.23 | 0.044 | 0.29 | 0.3125 | | | | | | | | | | | | |

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see: http://www.silabs.com/support/quality/pages/default.aspx.

### 6.2 CSP36 PCB Layout

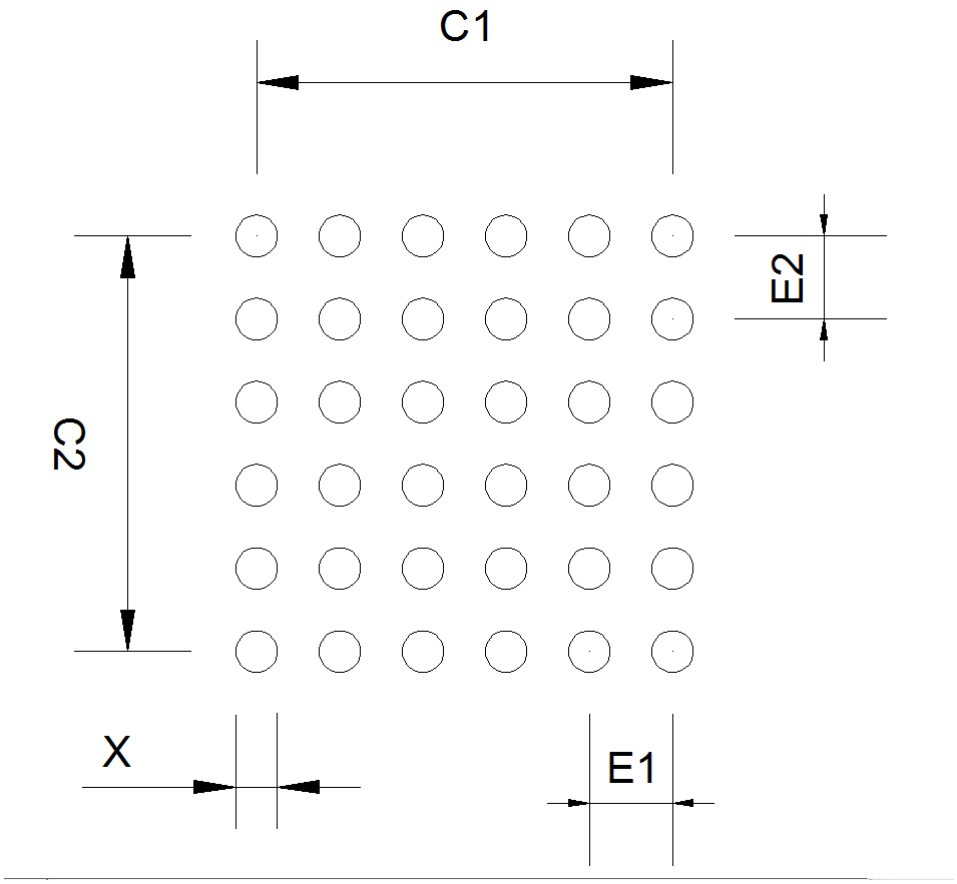



**Figure 6.2. CSP36 PCB Land Pattern**

**Table 6.2. CSP36 PCB Land Pattern Dimensions (Dimensions in mm)**

| Symbol | Dim. (mm) |
|---|---|
| X | 0.20 |
| C1 | 2.00 |
| C2 | 2.00 |
| E1 | 0.40 |
| E2 | 0.40 |

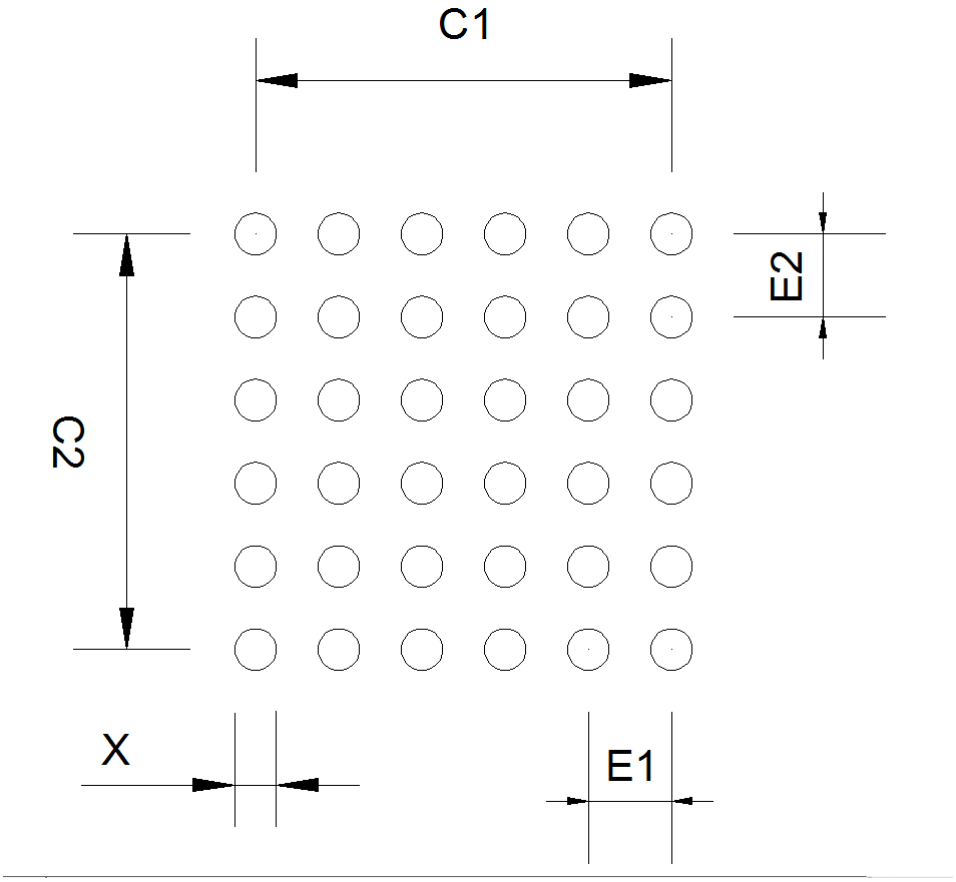



**Figure 6.3. CSP36 PCB Solder Mask**

**Table 6.3. CSP36 PCB Solder Mask Dimensions (Dimensions in mm)**

| Symbol | Dim. (mm) |
|---|---|
| X | 0.26 |
| C1 | 2.00 |
| C2 | 2.00 |
| E1 | 0.40 |
| E2 | 0.40 |

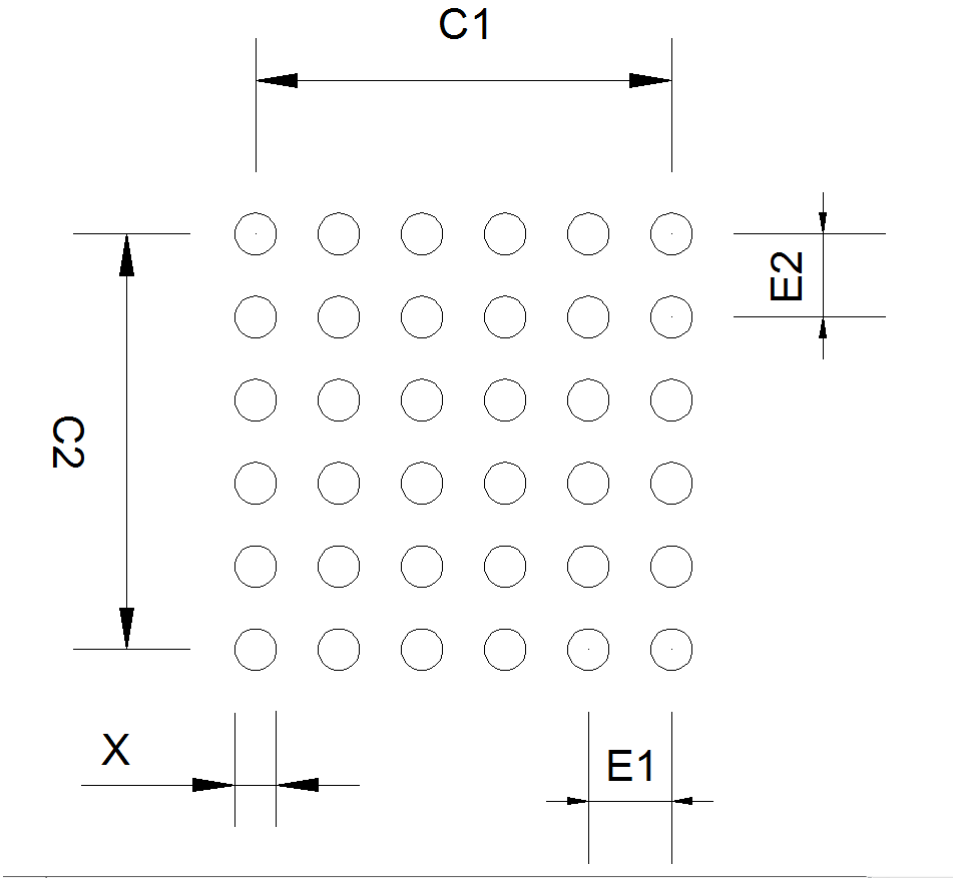



**Figure 6.4. CSP36 PCB Stencil Design**

**Table 6.4. CSP36 PCB Stencil Design Dimensions (Dimensions in mm)**

| Symbol | Dim. (mm) |
|---|---|
| X | 0.20 |
| C1 | 2.00 |
| C2 | 2.00 |
| E1 | 0.40 |
| E2 | 0.40 |

**Note:**

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.075 mm (3 mils).
6. For detailed pin-positioning, see Pin Definitions.

### 6.3 CSP36 Chip Marking

In the illustration below package fields and position are shown.

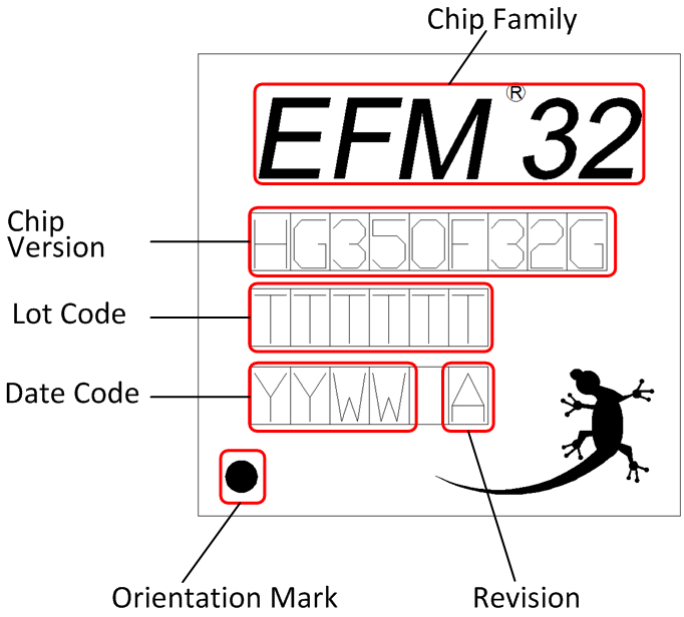



**Figure 6.5. Example Chip Marking (Top View)**

### 6.4 CSP36 Environmental

WLCSP devices can be handled and soldered using industry standard surface mount assembly techniques. However, because WLCSP devices are essentially a piece of silicon and are not encapsulated in plastic, they are susceptible to mechanical damage and may be sensitive to light. When WLCSPs must be used in an environment exposed to light, it may be necessary to cover the top and sides with an opaque material.

# 7. QFN24 Package Specifications

## 7.1 QFN24 Package Dimensions

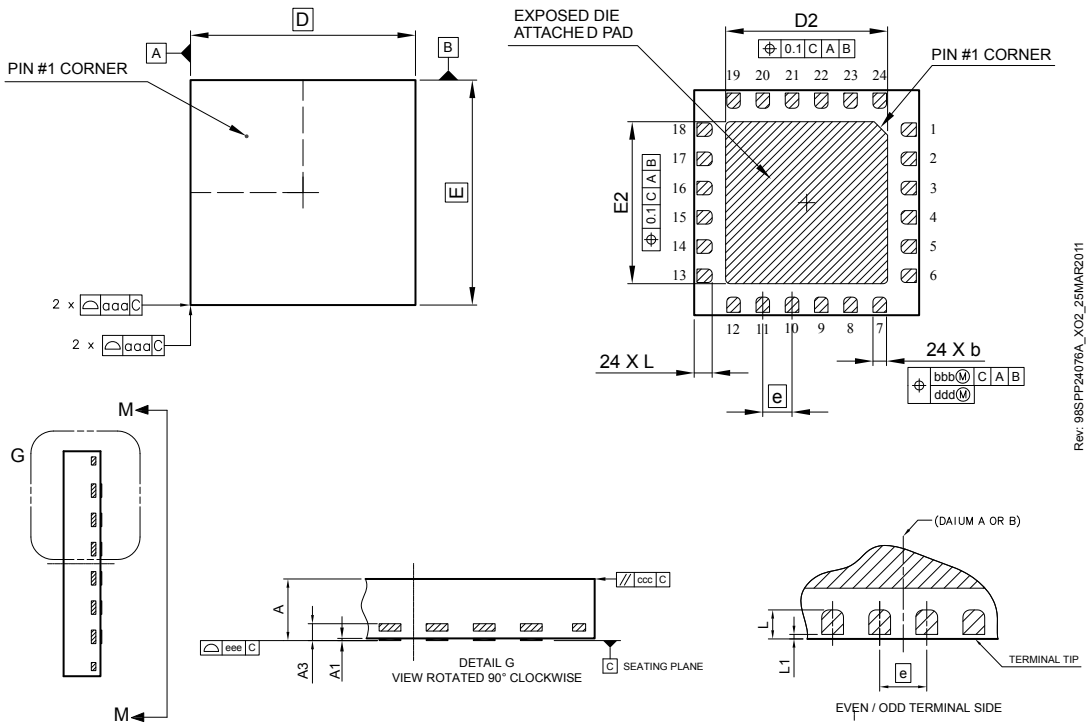



**Figure 7.1. QFN24**

**Note:**

1. Dimensioning & tolerancing confirm to ASME Y14.5M-1994.
2. All dimensions are in millimeters. Angles are in degrees.
3. Dimension 'b' applies to metallized terminal and is measured between 0.25 mm and 0.30 mm from the terminal tip. Dimension L1 represents terminal full back from package edge up to 0.1 mm is acceptable.
4. Coplanarity applies to the exposed heat slug as well as the terminal.
5. Radius on terminal is optional.

**Table 7.1. QFN (Dimensions in mm)**

| Symbol | A | A1 | A3 | b | D | E | D2 | E2 | e | L | L1 | aaa | bbb | ccc | ddd | eee |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Min | 0.80 | 0.00 | 0.203 REF | 0.25 | 5.00 BSC | 5.00 BSC | 3.50 | 3.50 | 0.65 BSC | 0.35 | 0.00 | 0.10 | 0.10 | 0.10 | 0.05 | 0.08 |
| Nom | 0.85 | — | | 0.30 | | | 3.60 | 3.60 | | 0.40 | | | | | | |
| Max | 0.90 | 0.05 | | 0.35 | | | 3.70 | 3.70 | | 0.45 | 0.10 | | | | | |

The QFN24 package uses matte-Sn post plated leadframe.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see: http://www.silabs.com/support/quality/pages/default.aspx.

### 7.2 QFN24 PCB Layout

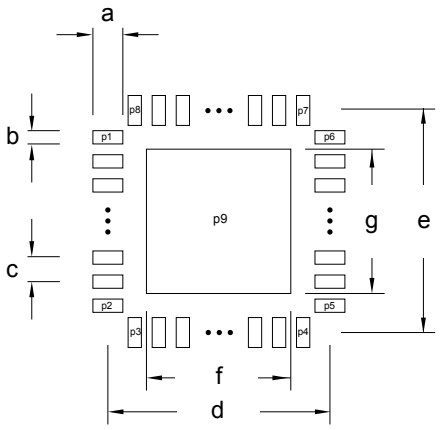



**Figure 7.2. QFN24 PCB Land Pattern**

**Table 7.2. QFN24 PCB Land Pattern Dimensions (Dimensions in mm)**

| Symbol | Dim. (mm) | Symbol | Pin Number | Symbol | Pin Number |
|---|---|---|---|---|---|
| a | 0.80 | P1 | 1 | P8 | 24 |
| b | 0.30 | P2 | 6 | P9 | 0 |
| c | 0.65 | P3 | 7 | - | - |
| d | 5.00 | P4 | 12 | - | - |
| e | 5.00 | P5 | 13 | - | - |
| f | 3.60 | P6 | 18 | - | - |
| g | 3.60 | P7 | 19 | - | - |

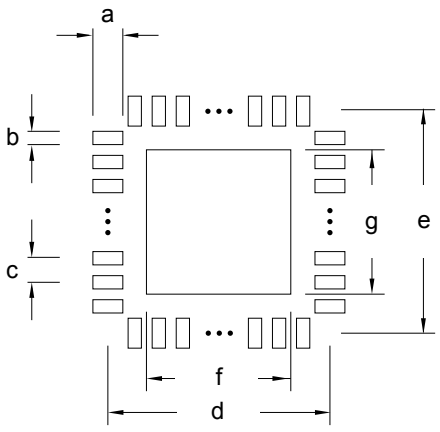



**Figure 7.3. QFN24 PCB Solder Mask**

**Table 7.3. QFN24 PCB Solder Mask Dimensions (Dimensions in mm)**

| Symbol | Dim. (mm) |
|---|---|
| a | 0.92 |
| b | 0.42 |
| c | 0.65 |

| Symbol | Dim. (mm) |
|---|---|
| d | 5.00 |
| e | 5.00 |
| f | 3.72 |
| g | 3.72 |

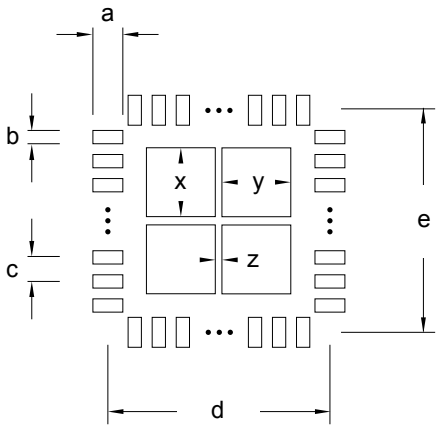



**Figure 7.4. QFN24 PCB Stencil Design**

**Table 7.4. QFN24 PCB Stencil Design Dimensions (Dimensions in mm)**

| Symbol | Dim. (mm) |
|---|---|
| a | 0.60 |
| b | 0.25 |
| c | 0.65 |
| d | 5.00 |
| e | 5.00 |
| x | 1.00 |
| y | 1.00 |
| z | 0.50 |

**Note:**

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Pin Definitions.

### 7.3 QFN24 Package Marking

In the illustration below package fields and position are shown.

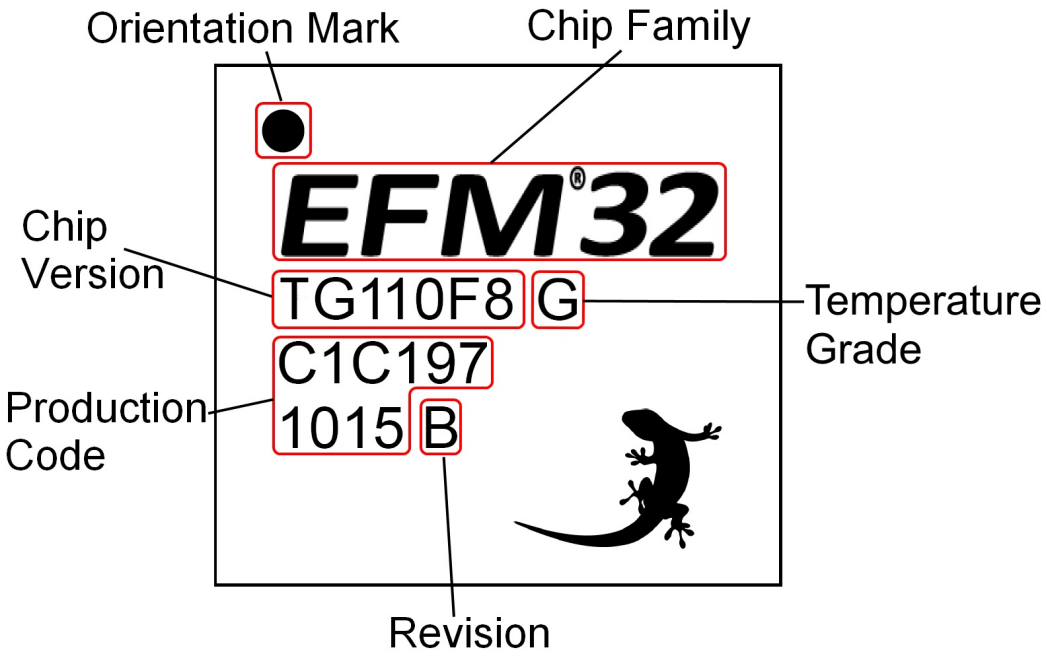



**Figure 7.5. Example Chip Marking (Top View)**

# 8. QFN32 Package Specifications

## 8.1 QFN32 Package Dimensions

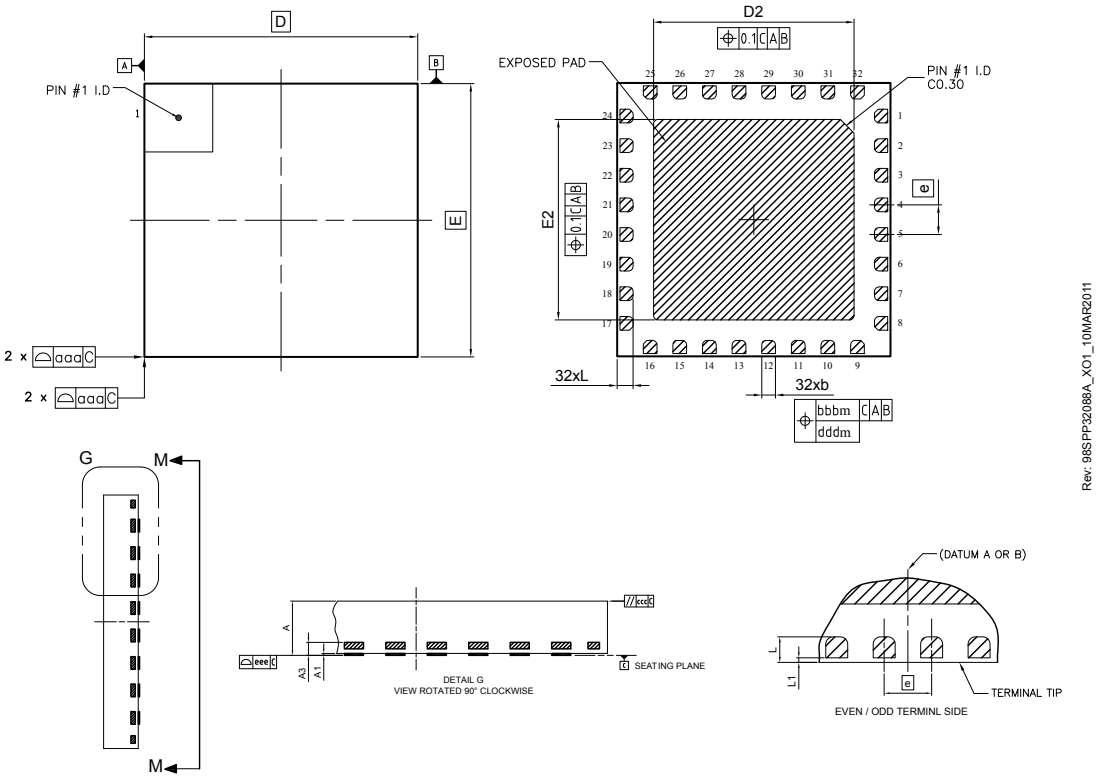



**Figure 8.1. QFN32**

**Note:**

1. Dimensioning & tolerancing confirm to ASME Y14.5M-1994.
2. All dimensions are in millimeters. Angles are in degrees.
3. Dimension 'b' applies to metallized terminal and is measured between 0.25 mm and 0.30 mm from the terminal tip. Dimension L1 represents terminal full back from package edge up to 0.1 mm is acceptable.
4. Coplanarity applies to the exposed heat slug as well as the terminal.
5. Radius on terminal is optional.

**Table 8.1. QFN32 (Dimensions in mm)**

| Symbol | A | A1 | A3 | b | D | E | D2 | E2 | e | L | L1 | aaa | bbb | ccc | ddd | eee |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Min | 0.80 | 0.00 | 0.203 REF | 0.25 | 6.00 BSC | 6.00 BSC | 4.30 | 4.30 | 0.65 BSC | 0.30 | 0.00 | 0.10 | 0.10 | 0.10 | 0.05 | 0.08 |
| Nom | 0.85 | — | | 0.30 | | | 4.40 | 4.40 | | 0.35 | | | | | | |
| Max | 0.90 | 0.05 | | 0.35 | | | 4.50 | 4.50 | | 0.40 | 0.10 | | | | | |

The QFN32 package uses matte-Sn post plated leadframe.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see: http://www.silabs.com/support/quality/pages/default.aspx.

### 8.2 QFN32 PCB Layout

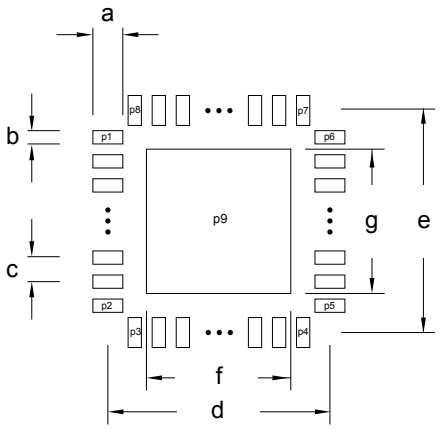



**Figure 8.2. QFN32 PCB Land Pattern**

**Table 8.2. QFN32 PCB Land Pattern Dimensions (Dimensions in mm)**

| Symbol | Dim. (mm) | Symbol | Pin Number | Symbol | Pin Number |
|---|---|---|---|---|---|
| a | 0.80 | P1 | 1 | P6 | 24 |
| b | 0.35 | P2 | 8 | P7 | 25 |
| c | 0.65 | P3 | 26 | P8 | 32 |
| d | 6.00 | P4 | 16 | P9 | 0 |
| e | 6.00 | P5 | 17 | | |
| f | 4.40 | | | | |
| g | 4.40 | | | | |

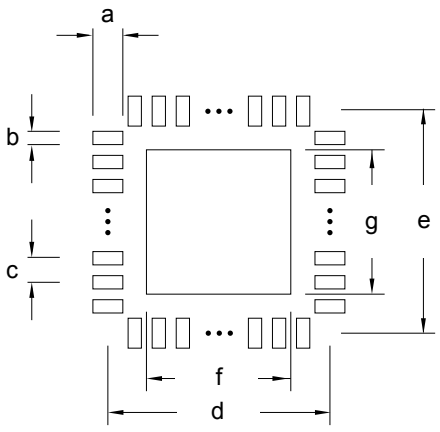



**Figure 8.3. QFN32 PCB Solder Mask**

**Table 8.3. QFN32 PCB Solder Mask Dimensions (Dimensions in mm)**

| Symbol | Dim. (mm) |
|---|---|
| a | 0.92 |
| b | 0.47 |
| c | 0.65 |

| Symbol | Dim. (mm) |
|---|---|
| d | 6.00 |
| e | 6.00 |
| f | 4.52 |
| g | 4.52 |

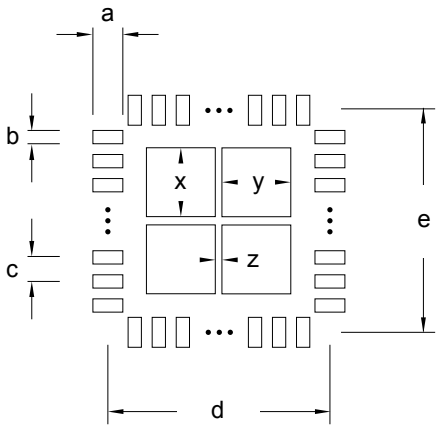



**Figure 8.4. QFN32 PCB Stencil Design**

**Table 8.4. QFN32 PCB Stencil Design Dimensions (Dimensions in mm)**

| Symbol | Dim. (mm) |
|---|---|
| a | 0.70 |
| b | 0.25 |
| c | 0.65 |
| d | 6.00 |
| e | 6.00 |
| x | 1.30 |
| y | 1.30 |
| z | 0.50 |

**Note:**

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Pin Definitions.

### 8.3 QFN32 Package Marking

In the illustration below package fields and position are shown.

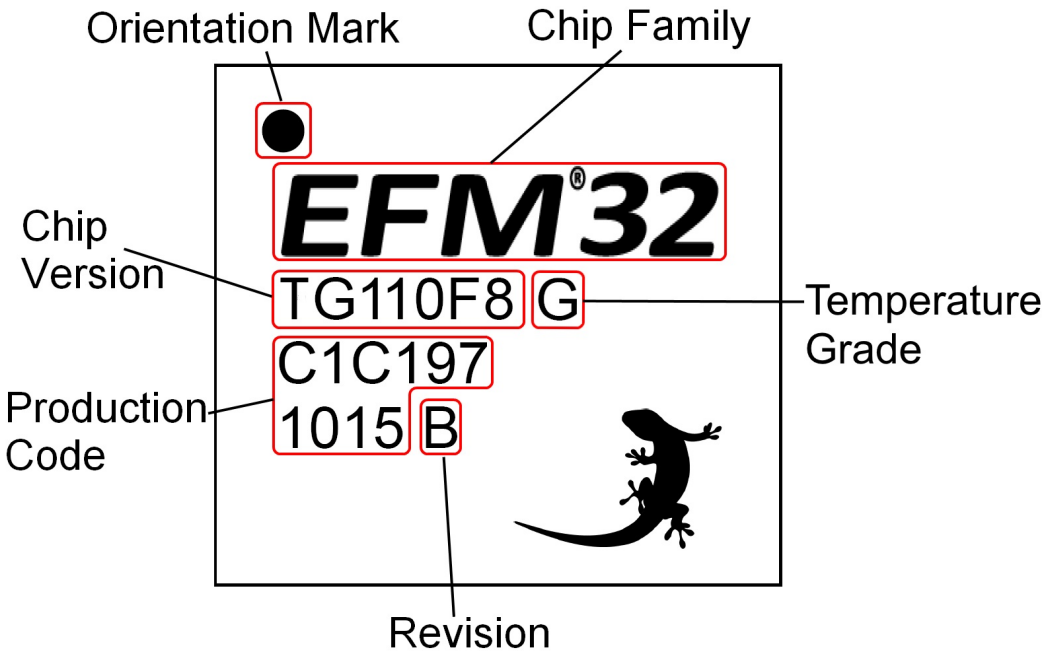



**Figure 8.5. Example Chip Marking (Top View)**

# 9. TQFP48 Package Specifications

## 9.1 TQFP48 Package Dimensions

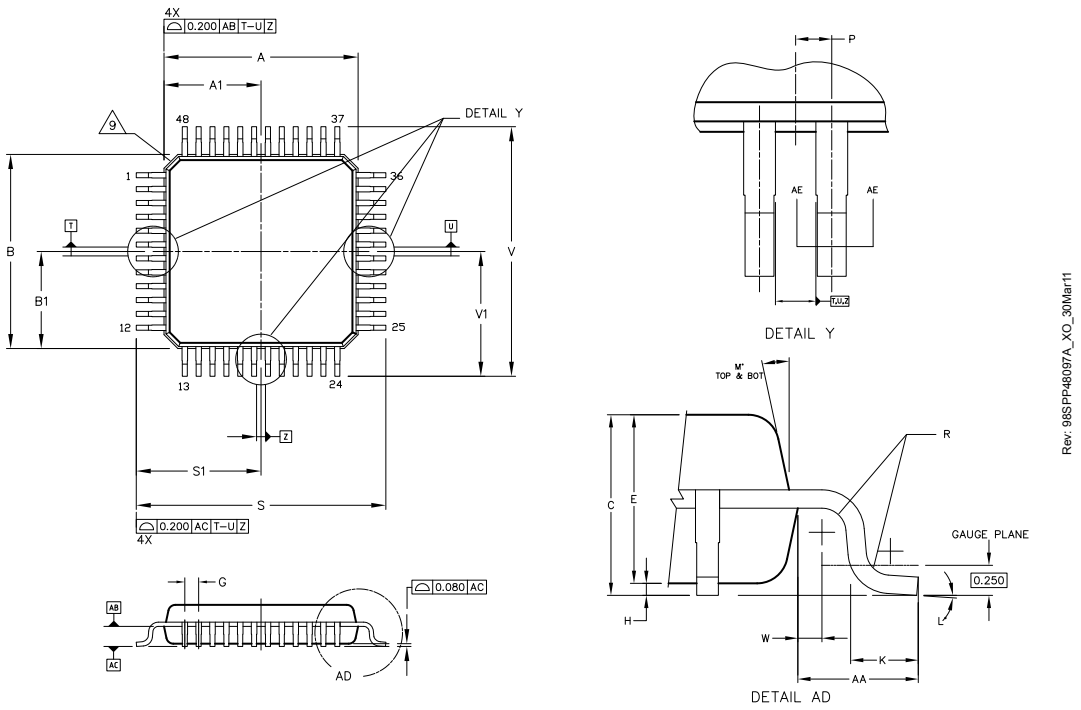



**Figure 9.1. TQFP48**

**Note:**

1. Dimensions and tolerance per ASME Y14.5M-1994.
2. Control dimension: Millimeter.
3. Datum plane AB is located at bottom of lead and is coincident with the lead where the lead exists from the plastic body at the bottom of the parting line.
4. Datums T, U and Z to be determined at datum plane AB.
5. Dimensions S and V to be determined at seating plane AC.
6. Dimensions A and B do not include mold protrusion. Allowable protrusion is 0.250 per side. Dimensions A and B do include mold mismatch and are determined at datum AB.
7. Dimension D does not include dambar protrusion. Dambar protrusion shall not cause the D dimension to exceed 0.350.
8. Minimum solder plate thickness shall be 0.0076.
9. Exact shape of each corner is optional.

**Table 9.1. QFP48 (Dimensions in mm)**

| DIM | MIN | NOM | MAX | DIM | MIN | NOM | MAX |
|---|---|---|---|---|---|---|---|
| A | — | 7.000 BSC | — | M | — | 12DEG REF | |
| A1 | — | 3.500 BSC | — | N | 0.090 | — | 0.160 |
| B | — | 7.000 BSC | — | P | — | 0.250 BSC | — |
| B1 | — | 3.500 BSC | — | R | 0.150 | — | 0.250 |
| C | 1.000 | — | 1.200 | S | — | 9.000 BSC | — |

| DIM | MIN | NOM | MAX | DIM | MIN | NOM | MAX |
|---|---|---|---|---|---|---|---|
| D | 0.170 | — | 0.270 | S1 | — | 4.500 BSC | — |
| E | 0.950 | — | 1.050 | V | — | 9.000 BSC | — |
| F | 0.170 | — | 0.230 | V1 | — | 4.5000 BSC | — |
| G | — | 0.500 BSC | — | W | — | 0.200 BSC | — |
| H | 0.050 | — | 0.150 | AA | — | 1.000BSC | — |
| J | 0.090 | — | 0.200 | | | | |
| K | 0.500 | — | 0.700 | | | | |
| L | 0DEG | — | 7DEG | | | | |

The TQFP48 package is 7 by 7 mm in size and has a 0.5 mm pin pitch.

The TQFP48 package uses matte-Sn post plated leadframe.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see: http://www.silabs.com/support/quality/pages/default.aspx.

### 9.2 TQFP48 PCB Layout

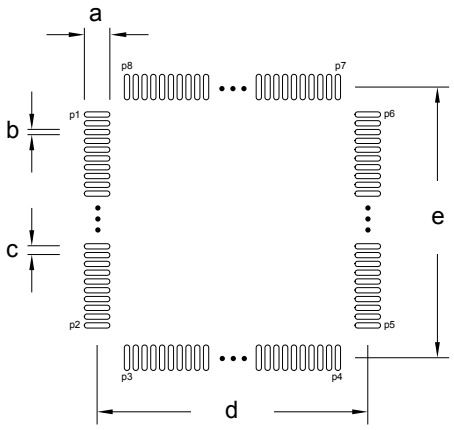



**Figure 9.2. TQFP48 PCB Land Pattern**

**Table 9.2. TQFP48 PCB Land Pattern Dimensions (Dimensions in mm)**

| Symbol | Dim. (mm) | Symbol | Pin Number | Symbol | Pin Number |
|---|---|---|---|---|---|
| a | 1.60 | P1 | 1 | P6 | 36 |
| b | 0.30 | P2 | 12 | P7 | 37 |
| c | 0.50 | P3 | 13 | P8 | 48 |
| d | 8.50 | P4 | 24 | | |
| e | 8.50 | P5 | 25 | | |

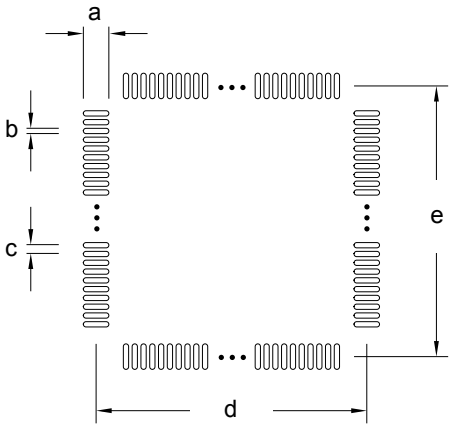



**Figure 9.3. TQFP48 PCB Solder Mask**

**Table 9.3. TQFP48 PCB Solder Mask Dimensions (Dimensions in mm)**

| Symbol | Dim. (mm) |
|---|---|
| a | 1.72 |
| b | 0.42 |
| c | 0.50 |
| d | 8.50 |
| e | 8.50 |

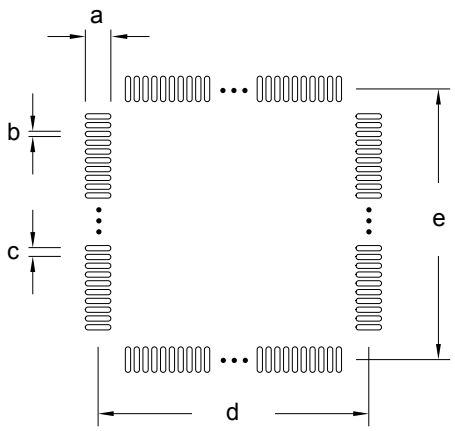



**Figure 9.4. TQFP48 PCB Stencil Design**

**Table 9.4. TQFP48 PCB Stencil Design Dimensions (Dimensions in mm)**

| Symbol | Dim. (mm) |
|---|---|
| a | 1.50 |
| b | 0.20 |
| c | 0.50 |
| d | 8.50 |
| e | 8.50 |

**Note:**

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Pin Definitions.

### 9.3 TQFP48 Package Marking

In the illustration below package fields and position are shown.

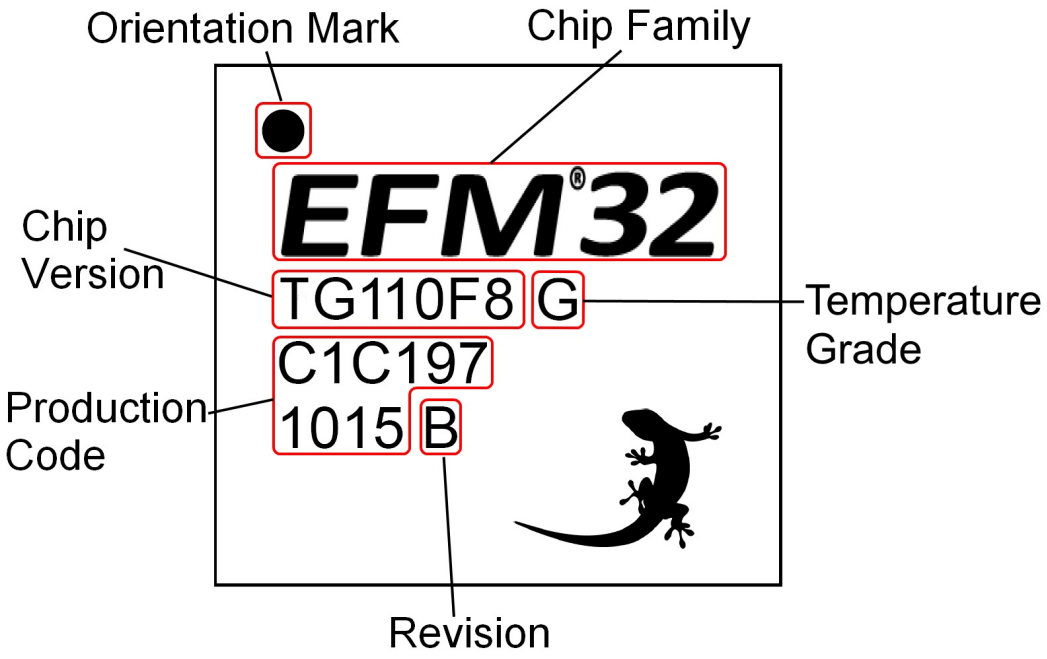



**Figure 9.5. Example Chip Marking (Top View)**

# 10. Chip Revision, Solder Information, Errata

## 10.1 Chip Revision

The revision of a chip can be determined from the "Revision" field in the package marking.

## 10.2 Soldering Information

The latest IPC/JEDEC J-STD-020 recommendations for Pb-Free reflow soldering should be followed.

## 10.3 Errata

Please see the errata document for description and resolution of device errata. This document is available in Simplicity Studio and online at: http://www.silabs.com/support/pages/document-library.aspx?p=MCUs--32-bit

# 11. Revision History

### Revision 2.20

August, 2019

- Updated 2. Ordering Information for release of revision C devices.
- 4.8 Flash – Added word write cycles between erase ($WWC_{FLASH}$) specification.

### Revision 2.10

October, 2018

- 1. Feature List – Added temperature range for EFM32HGxxxFxxN part numbers.
- 2. Ordering Information – Added EFM32HGxxxFxxN part numbers and updated ordering code decoder.
- Added ADC0_CH[1:0] to Configuration Summary sections:
  - 3.2.2 EFM32HG110
  - 3.2.3 EFM32HG210
  - 3.2.4 EFM32HG222
  - 3.2.6 EFM32HG309
  - 3.2.7 EFM32HG310
  - 3.2.8 EFM32HG321
  - 3.2.9 EFM32HG322
  - 3.2.10 EFM32HG350
- 4.2 Absolute Maximum Ratings - Removed footnote about storage temperature and added max sink/source current per I/O pin.
- 4.3 General Operating Conditions – Added ambient temperature range specification for EFM32HGxxxFxxN part numbers.
- 4.4 Thermal Characteristics – Added thermal characteristics for QFN24, QFN32 and TQFP48 packages.
- 4.5 Current Consumption – Updated EM0 current and EM1 current test conditions. Added EM2 current, EM3 current, and EM4 current specifications for EFM32HGxxxFxxN part numbers.
- 4.8 Flash – Updated flash page erase time and device erase time and added footnotes.
- 4.9 General Purpose Input Output – Added input leakage current specification for EFM32HGxxxFxxN part numbers.
- 4.10.4 HFRCO - Removed 24 MHz band.
- In 4.11 Analog Digital Converter (ADC):
  - Updated test conditions, updated specifications, and added footnote for average active current.
  - Added input bias current.
  - Added input offset current.
  - Updated ADC clock frequency.
  - Updated SNR, SINAD and SFDR.
  - Updated offset voltage.
  - Updated missing codes.
  - Added gain error drift and offset error drift.
  - Removed ADC internal voltage reference.
  - Added VREF output voltage, VREF voltage drift, VREF temperature drift, VREF current consumption, and ADC and DAC VREF matching.
- 7.2 QFN24 PCB Layout - Corrected pin number for symbol P9.
- 8.2 QFN32 PCB Layout - Corrected pin number for symbol P9.

**Rev 2.00**

March, 2018

- Consolidated all EFM32HG data sheets:
  - EFM32HG108
  - EFM32HG110
  - EFM32HG210
  - EFM32HG222
  - EFM32HG308
  - EFM32HG309
  - EFM32HG310
  - EFM32HG321
  - EFM32HG322
  - EFM32HG350
- Added a Feature List section.
- 2. Ordering Information – Added ordering code decoder.
- 3.3 Memory Map – Separated the Memory Map into two figures – one for core and code space listing and one for peripheral listing.
- New formatting throughout.

**Revision 1.00**

December 4th, 2015

- This revision applies the following devices:
  - EFM32HG108
  - EFM32HG110
  - EFM32HG210
  - EFM32HG222
  - EFM32HG308
  - EFM32HG309
  - EFM32HG310
  - EFM32HG321
  - EFM32HG322
  - EFM32HG350
- Updated all specs with results of full characterization.
- Updated part number to revision B.
- For devices with USB, added the USB electrical specifications table.

**Revision 0.91**

May 6th, 2015

- This revision applies the following devices:
  - EFM32HG290
  - EFM32HG295
  - EFM32HG390
  - EFM32HG395
  - EFM32HG890
  - EFM32HG895
  - EFM32HG990
  - EFM32HG995
- Updated current consumption table for energy modes.
- Updated GPIO max leakage current.
- Updated startup time for HFXO and LFXO.
- Updated current consumption for HFRCO and LFRCO.
- Updated ADC current consumption.
- Updated IDAC characteristics tables.
- Updated ACMP internal resistance.
- Updated VCMP current consumption.

**Revision 0.90**

March 16th, 2015

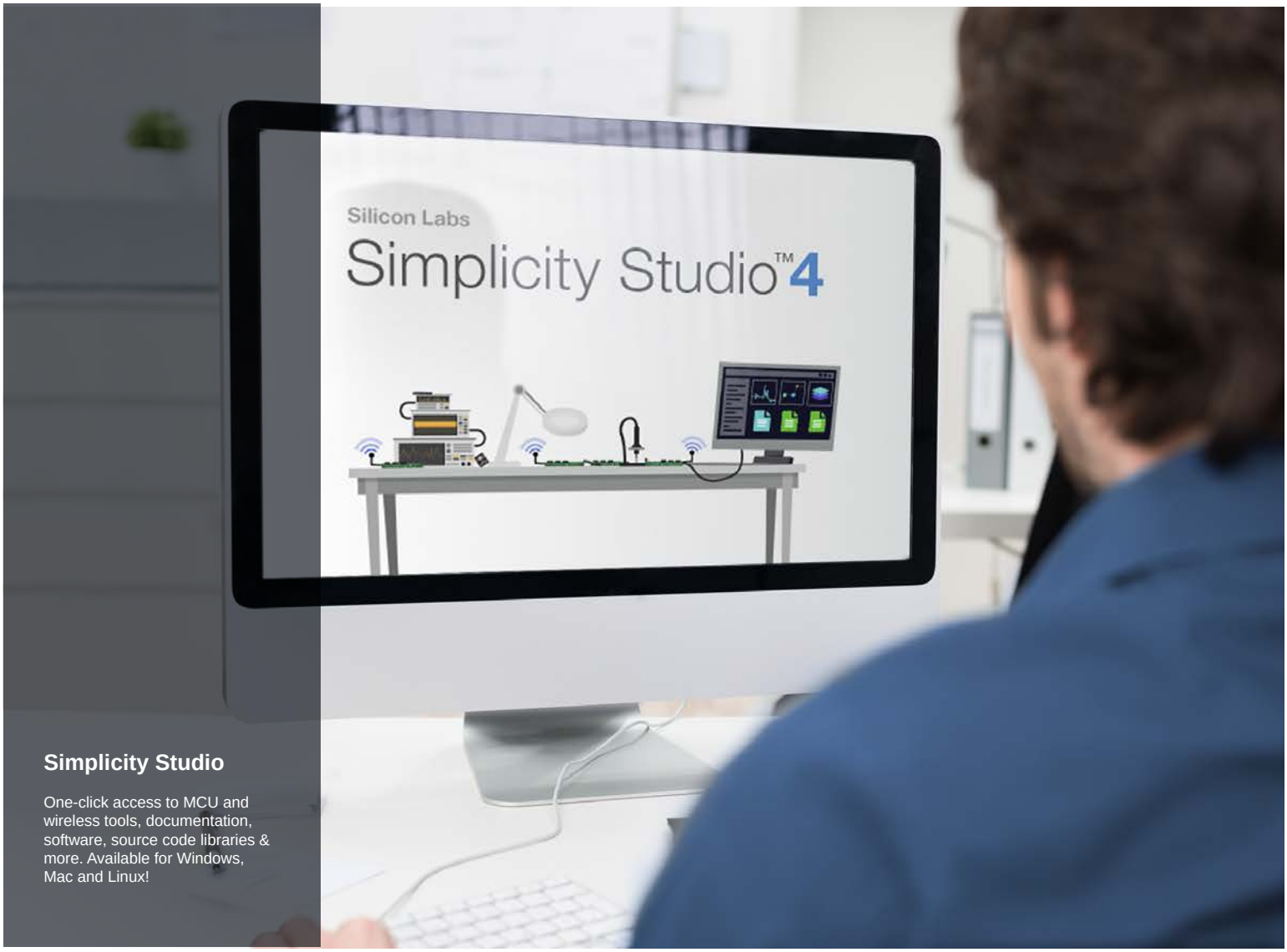
**Note:** This datasheet revision applies to a product under development. Its characteristics and specifications are subject to change without notice.

- This revision applies the following devices:
  - EFM32HG108
  - EFM32HG110
  - EFM32HG210
  - EFM32HG222
  - EFM32HG308
  - EFM32HG309
  - EFM32HG310
  - EFM32HG321
  - EFM32HG322
  - EFM32HG350
- Corrected EM2 current consumption condition in Electrical Characteristics section.
- Updated GPIO electrical characteristics.
- Updated Max $ESR_{HFXO}$ value for Crystal Frequency of 25 MHz.
- Updated LFRCO plots.
- Updated HFRCO table and plots.
- Updated ADC table and temp sensor plot.
- Added DMA current in Digital Peripherals section.
- Updated block diagram.
- For QFN24 and QFN32 packages, updated package dimensions table.
- Corrected leadframe type to matte-Sn.

**Revision 0.20**

December 11th, 2014

- This revision applies the following devices:
  - EFM32HG108
  - EFM32HG110
  - EFM32HG210
  - EFM32HG222
  - EFM32HG308
  - EFM32HG309
  - EFM32HG310
  - EFM32HG321
  - EFM32HG322
  - EFM32HG350
- Preliminary Release.

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