Ordering number : ENA1777A

ECH8661

Power MOSFET

30V, 7A, 24mΩ, −30V, −5.5A, 39mΩ, Complementary Dual ECH8

ON Semiconductor®

http://onsemi.com

Features

- ON-resistance Nch: $R_{DS}(on)1$=18mΩ(typ.), Pch: ON-resistance $R_{DS}(on)1$=30mΩ(typ.)
- The ECH8661 incorporates an N-channel MOSFET and a P-channel MOSFET that feature low ON-resistance and high-speed switching , thereby enablimg high-density mounting
- 4V drive
- Halogen free compliance
- Protection diode in

Specifications

Absolute Maximum Ratings at Ta=25°C

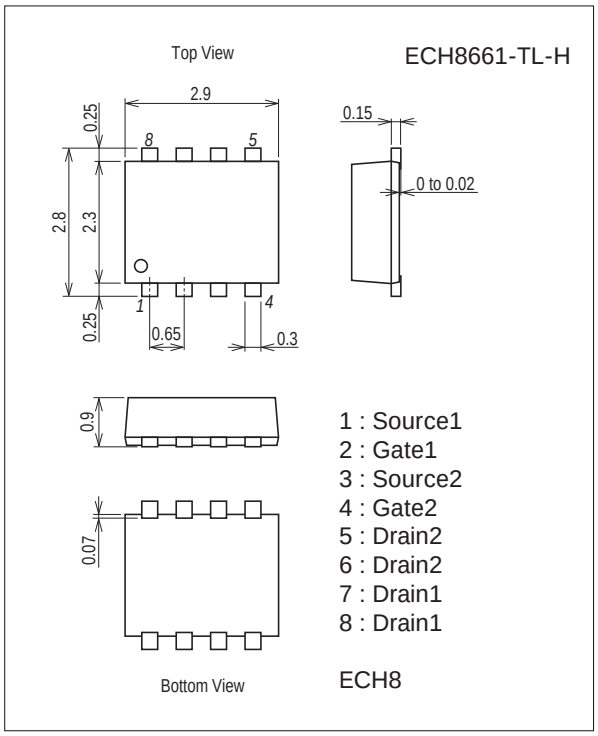
Parameter	Symbol	Conditions	N-channel	P-channel	Unit
Drain-to-Source Voltage	V_{DSS}		30	−30	V
Gate-to-Source Voltage	V_{GSS}		±20	±20	V
Drain Current (DC)	I_D		7	−5.5	A
Drain Current (Pulse)	I_{DP}	PW≤10μs, duty cycle≤1%	40	−40	A
Allowable Power Dissipation	P_D	When mounted on ceramic substrate (900mm²×0.8mm) 1unit	1.3		W
Total Dissipation	P_T	When mounted on ceramic substrate (900mm²×0.8mm)	1.5		W
Channel Temperature	Tch		150		°C
Storage Temperature	Tstg		−55 to +150		°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Package Dimensions

unit : mm (typ)

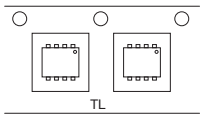
7011A-001



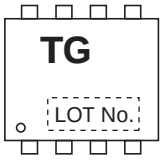
Product & Package Information

- Package : ECH8
- JEITA, JEDEC : -
- Minimum Packing Quantity : 3,000 pcs./reel

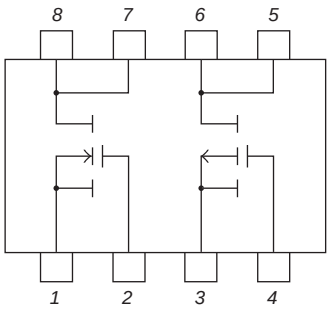
Packing Type : TL



Marking



Electrical Connection



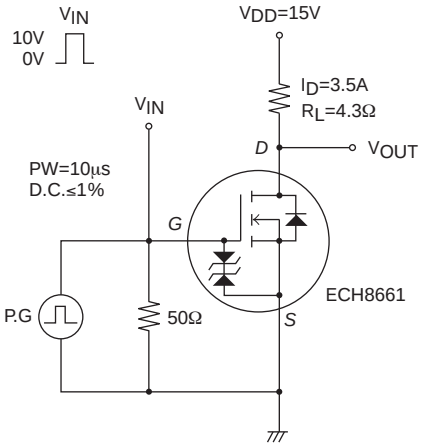
Semiconductor Components Industries, LLC, 2013

Electrical Characteristics at Ta=25°C

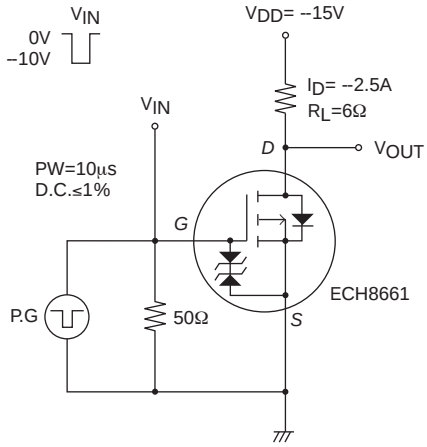
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[N-channel]						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=1mA, V_{GS}=0V	30			V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=30V, V_{GS}=0V			1	μA
Gate-to-Source Leakage Current	I_{GSS}	V_{GS}=±16V, V_{DS}=0V			±10	μA
Cutoff Voltage	V_{GS}(off)	V_{DS}=10V, I_D=1mA	1.2		2.6	V
Forward Transfer Admittance	| yfs |	V_{DS}=10V, I_D=3.5A		3.7		S
Static Drain-to-Source On-State Resistance	R_{DS}(on)1	I_D=3.5A, V_{GS}=10V		18	24	mΩ
	R_{DS}(on)2	I_D=2A, V_{GS}=4.5V		29	41	mΩ
	R_{DS}(on)3	I_D=2A, V_{GS}=4V		39	55	mΩ
Input Capacitance	Ciss	V_{DS}=10V, f=1MHz		710		pF
Output Capacitance	Coss	V_{DS}=10V, f=1MHz		120		pF
Reverse Transfer Capacitance	Crss	V_{DS}=10V, f=1MHz		72		pF
Turn-ON Delay Time	t_d(on)	See specified Test Circuit.		10		ns
Rise Time	t_r			25		ns
Turn-OFF Delay Time	t_d(off)			43		ns
Fall Time	t_f			25		ns
Total Gate Charge	Qg	V_{DS}=15V, V_{GS}=10V, I_D=7A		11.8		nC
Gate-to-Source Charge	Qgs			2.4		nC
Gate-to-Drain “Miller” Charge	Qgd			2.0		nC
Diode Forward Voltage	V_{SD}	I_S=7A, V_{GS}=0V		0.79	1.2	V
[P-channel]						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=−1mA, V_{GS}=0V	−30			V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=−30V, V_{GS}=0V			−1	μA
Gate-to-Source Leakage Current	I_{GSS}	V_{GS}=±16V, V_{DS}=0V			±10	μA
Cutoff Voltage	V_{GS}(off)	V_{DS}=−10V, I_D=−1mA	−1.2		−2.6	V
Forward Transfer Admittance	| yfs |	V_{DS}=−10V, I_D=−2.5A		5.2		S
Static Drain-to-Source On-State Resistance	R_{DS}(on)1	I_D=−2.5A, V_{GS}=−10V		30	39	mΩ
	R_{DS}(on)2	I_D=−1.5A, V_{GS}=−4.5V		55	77	mΩ
	R_{DS}(on)3	I_D=−1.5A, V_{GS}=−4V		58	82	mΩ
Input Capacitance	Ciss	V_{DS}=−10V, f=1MHz		600		pF
Output Capacitance	Coss			145		pF
Reverse Transfer Capacitance	Crss			110		pF
Turn-ON Delay Time	t_d(on)	See specified Test Circuit.		7.2		ns
Rise Time	t_r			23		ns
Turn-OFF Delay Time	t_d(off)			63		ns
Fall Time	t_f			42		ns
Total Gate Charge	Qg	V_{DS}=−15V, V_{GS}=−10V, I_D=−5.5A		13		nC
Gate-to-Source Charge	Qgs			1.8		nC
Gate-to-Drain “Miller” Charge	Qgd			3.2		nC
Diode Forward Voltage	V_{SD}	I_S=−5.5A, V_{GS}=0V		−0.82	−1.2	V

Switching Time Test Circuit

[N-channel]

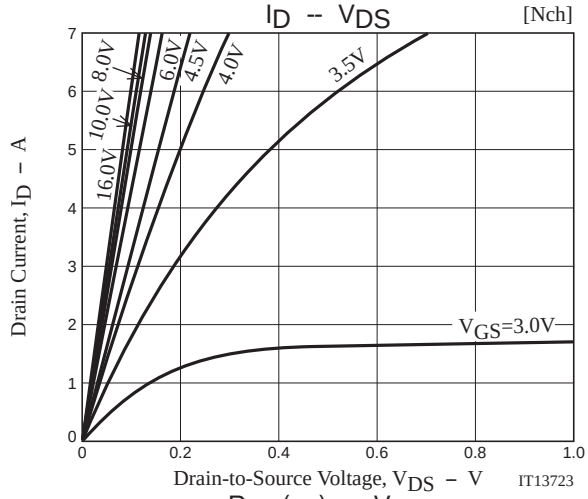


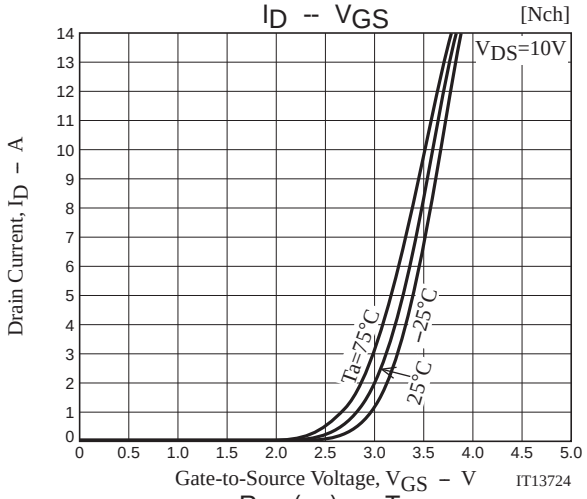
[P-channel]

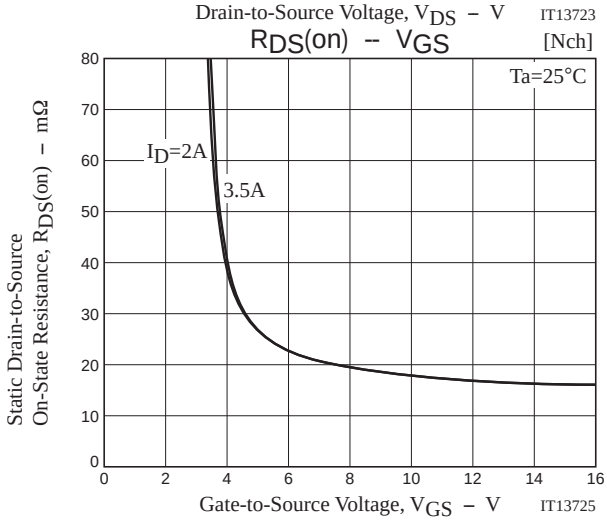


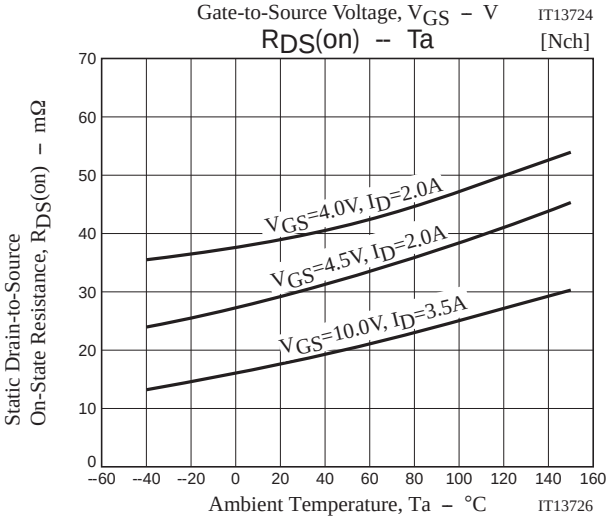
Ordering Information

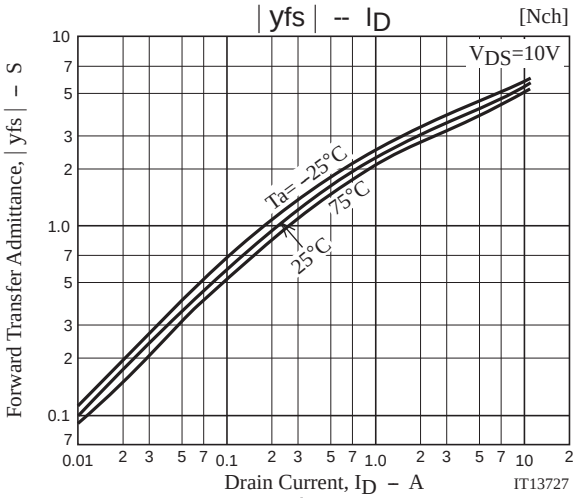
Device	Package	Shipping	memo
ECH8661-TL-H	ECH8	3,000pcs./reel	Pb Free and Halogen Free

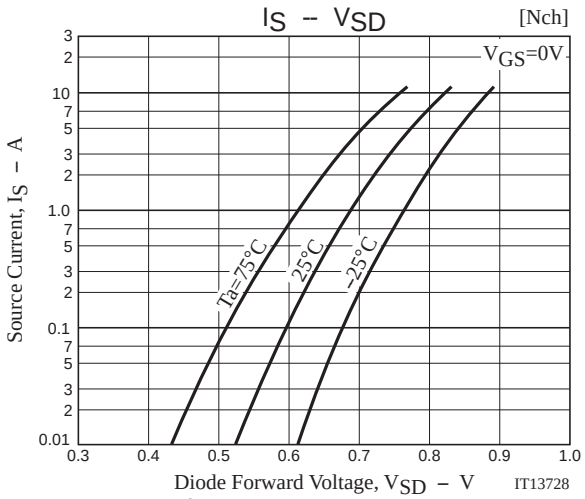


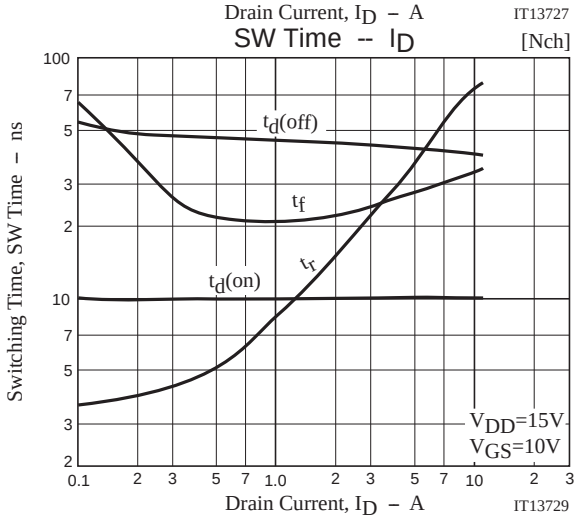


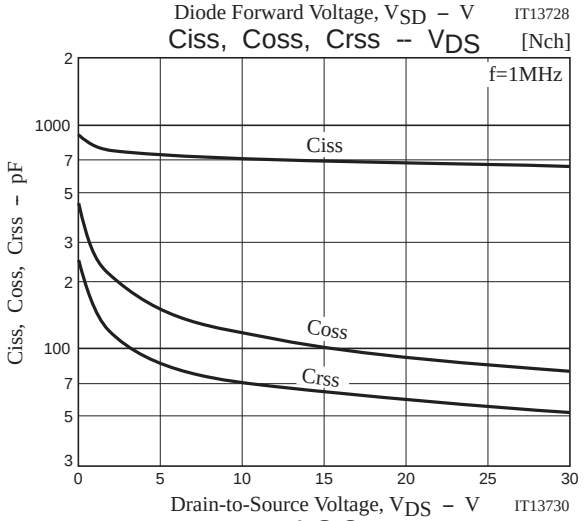


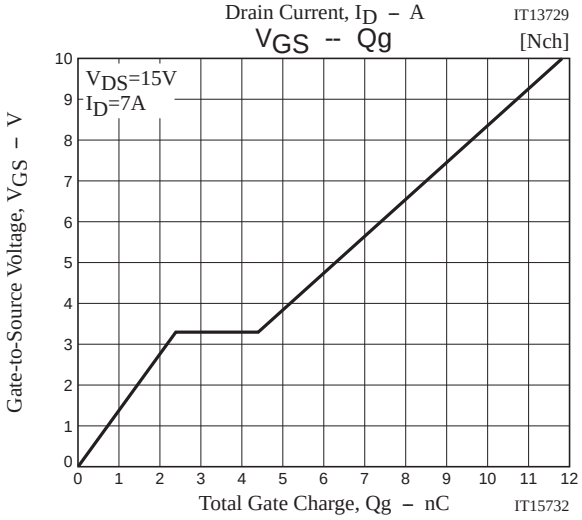


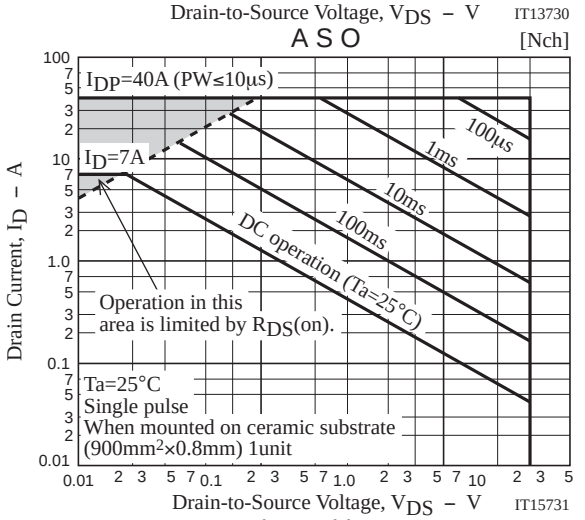

| yfs | -- ID
[Nch]
VDS=10V
Ta= –25°C
75°C
25°C
Forward Transfer Admittance, | yfs | – S
Drain Current, ID – A
IT13727

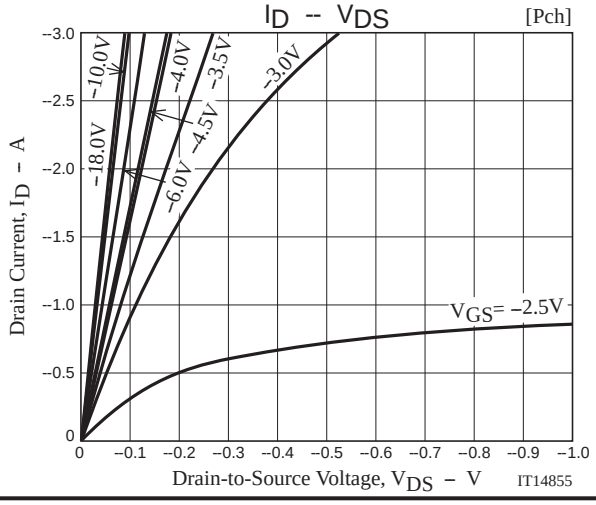

IS -- VSD
[Nch]
VGS=0V
Ta=75°C
25°C
–25°C
Source Current, IS – A
Diode Forward Voltage, VSD – V
IT13728

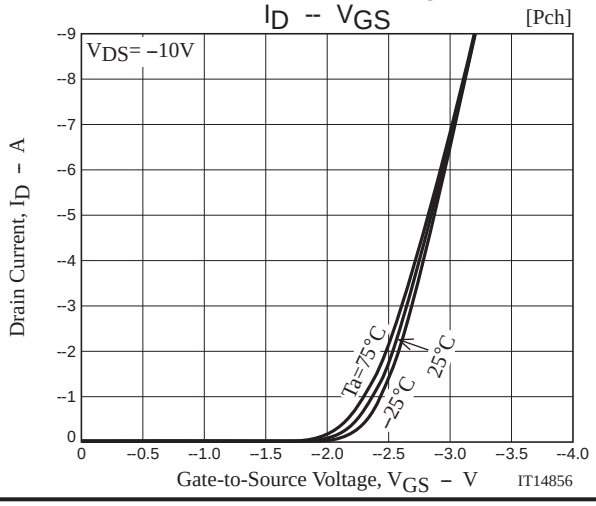

SW Time -- ID
[Nch]
td(off)
tf
tr
td(on)
VDD=15V
VGS=10V
Switching Time, SW Time – ns
Drain Current, ID – A
IT13729

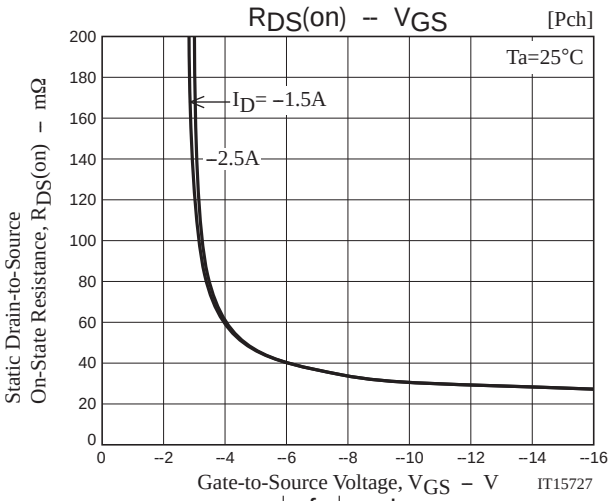

Ciss, Coss, Crss -- VDS
[Nch]
f=1MHz
Ciss
Coss
Crss
Ciss, Coss, Crss – pF
Drain-to-Source Voltage, VDS – V
IT13730

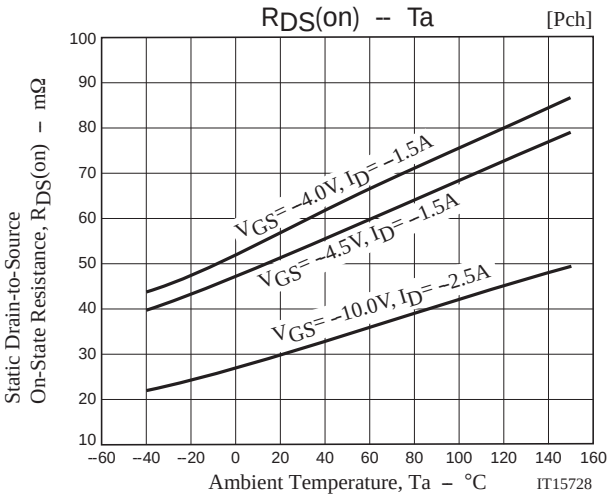

VGS -- Qg
[Nch]
VDS=15V
ID=7A
Gate-to-Source Voltage, VGS – V
Total Gate Charge, Qg – nC
IT15732

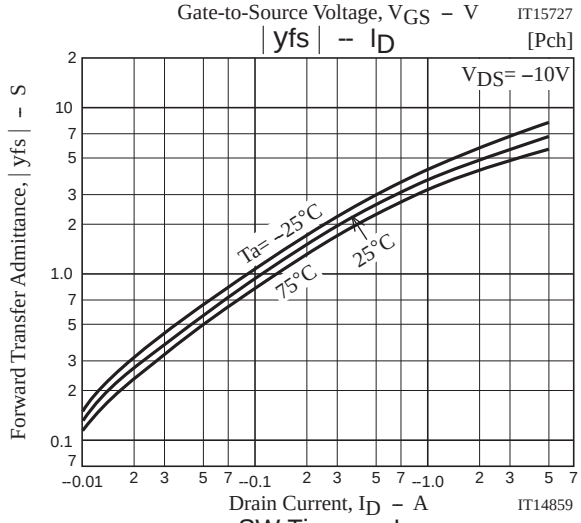

A S O
[Nch]
IDP=40A (PW≤10μs)
ID=7A
100μs
1ms
10ms
100ms
DC operation (Ta=25°C)
Operation in this
area is limited by RDS(on).
Ta=25°C
Single pulse
When mounted on ceramic substrate
(900mm²×0.8mm) 1unit
Drain Current, ID – A
Drain-to-Source Voltage, VDS – V
IT15731

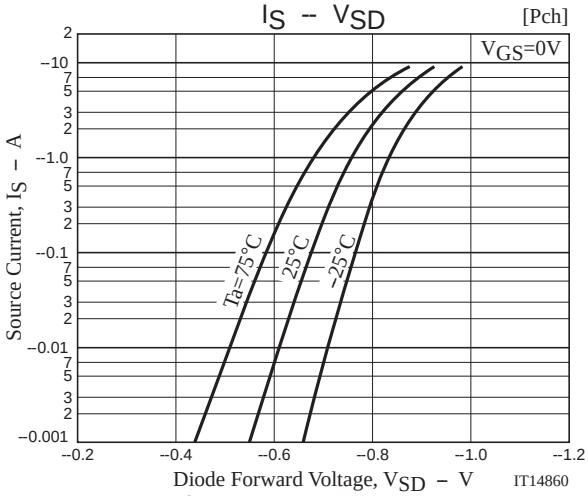

ID -- VDS
[Pch]
–10.0V
–4.0V
–3.5V
–3.0V
–18.0V
–4.5V
–6.0V
VGS= –2.5V
Drain Current, ID – A
Drain-to-Source Voltage, VDS – V
IT14855

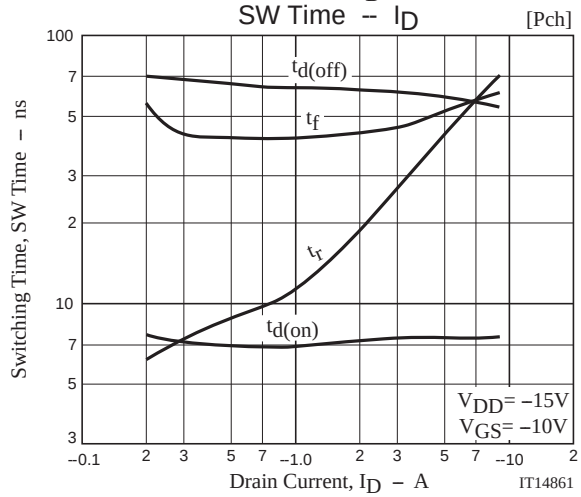

ID -- VGS
[Pch]
VDS= –10V
Ta=75°C
25°C
–25°C
Drain Current, ID – A
Gate-to-Source Voltage, VGS – V
IT14856

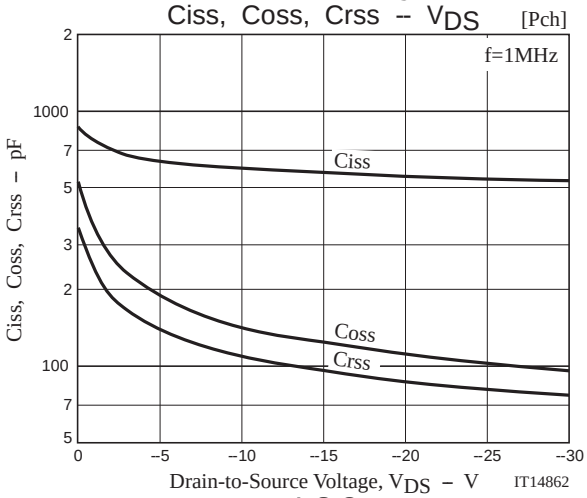

RDS(on) -- VGS
[Pch]
Ta=25°C
ID= –1.5A
–2.5A
Static Drain-to-Source On-State Resistance, RDS(on) – mΩ
Gate-to-Source Voltage, VGS – V
IT15727

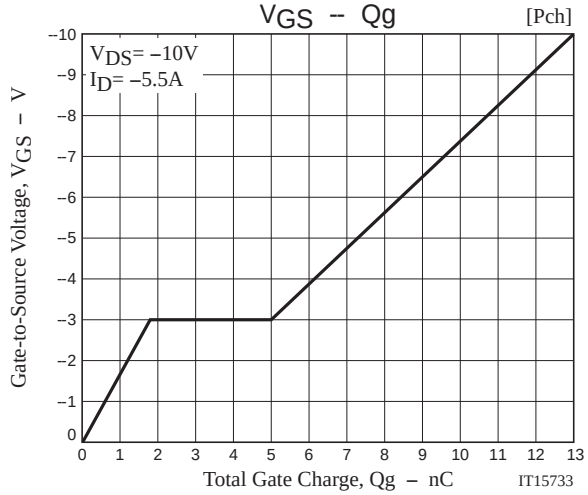

RDS(on) -- Ta
[Pch]
VGS= –4.0V, ID= –1.5A
VGS= –4.5V, ID= –1.5A
VGS= –10.0V, ID= –2.5A
Static Drain-to-Source On-State Resistance, RDS(on) – mΩ
Ambient Temperature, Ta – °C
IT15728

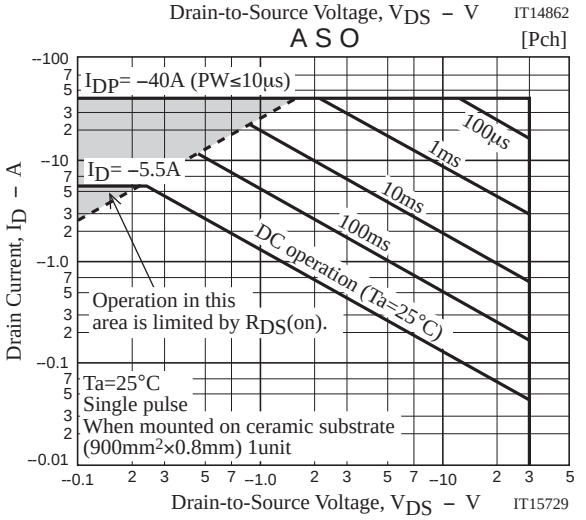

| yfs | -- ID
[Pch]
VDS= –10V
Ta= –25°C
25°C
75°C
Forward Transfer Admittance, | yfs | – S
Drain Current, ID – A
IT14859

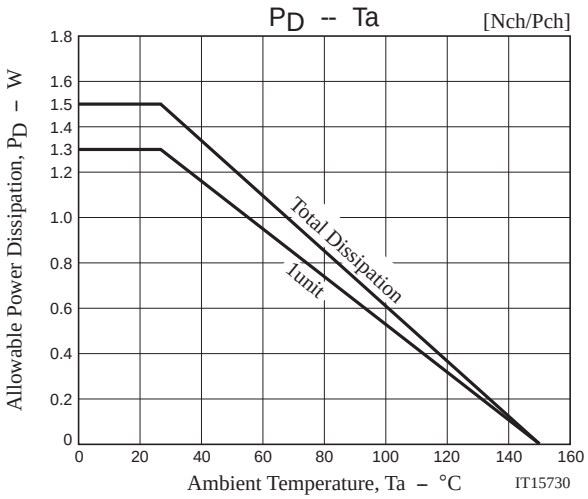

IS -- VSD
[Pch]
VGS=0V
Ta=75°C
25°C
–25°C
Source Current, IS – A
Diode Forward Voltage, VSD – V
IT14860


SW Time -- ID
[Pch]
td(off)
tf
tr
td(on)
VDD= –15V
VGS= –10V
Switching Time, SW Time – ns
Drain Current, ID – A
IT14861


Ciss, Coss, Crss -- VDS
[Pch]
f=1MHz
Ciss
Coss
Crss
Ciss, Coss, Crss – pF
Drain-to-Source Voltage, VDS – V
IT14862


VGS -- Qg
[Pch]
VDS= –10V
ID= –5.5A
Gate-to-Source Voltage, VGS – V
Total Gate Charge, Qg – nC
IT15733


A S O
[Pch]
IDP= –40A (PW≤10μs)
ID= –5.5A
100μs
1ms
10ms
100ms
DC operation (Ta=25°C)
Operation in this area is limited by RDS(on).
Ta=25°C
Single pulse
When mounted on ceramic substrate (900mm²×0.8mm) 1unit
Drain Current, ID – A
Drain-to-Source Voltage, VDS – V
IT15729


PD -- Ta
[Nch/Pch]
Allowable Power Dissipation, PD – W
1.8
1.6
1.5
1.4
1.3
1.2
1.0
0.8
0.6
0.4
0.2
0
0
20
40
60
80
100
120
140
160
Total Dissipation
1unit
Ambient Temperature, Ta – °C
IT15730

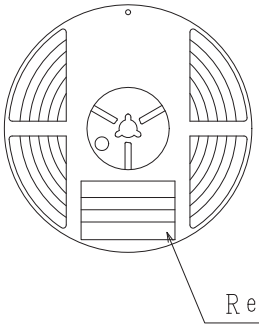
Embossed Taping Specification

ECH8661-TL-H

1. Packing Format

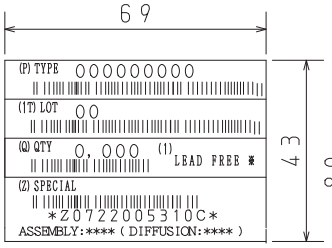
Package Name	Carrier Tape Type	Maximum Number of devices contained (pcs)			Packing format	
		Reel	Inner box	Outer box	Inner BOX (C-1)	Outer BOX (A-7)
ECH8	CPH6	3,000	15,000	90,000	5 reels contained Dimensions:mm(external) 183×72×185	6 inner boxes contained Dimensions:mm(external) 440×195×210

Packing method



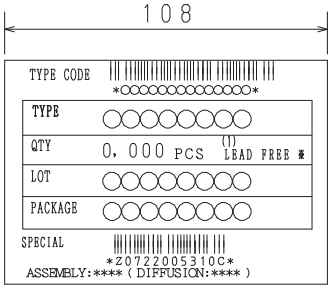
Reel label, Inner box label

(unit:mm)



Outer box label

It is a label at the time of factory shipments. The form of a label may change in physical distribution process.



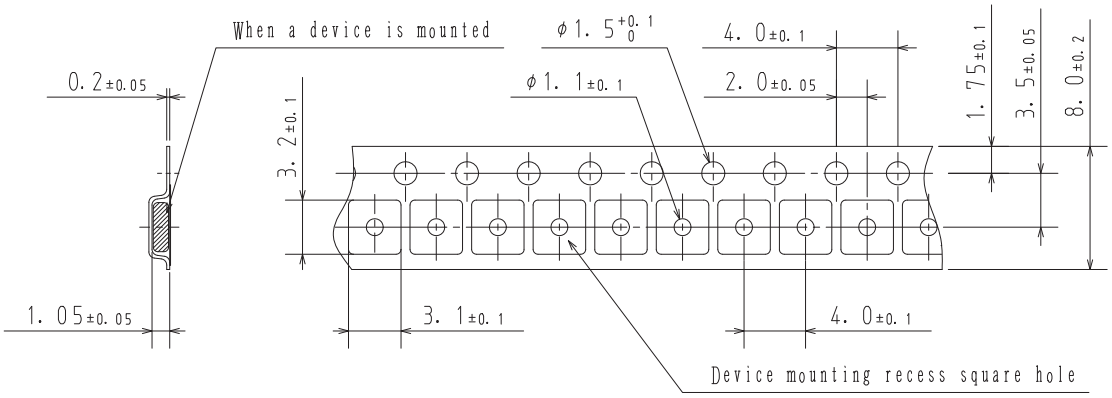
NOTE (1)

The LEAD FREE ※ description shows that the surface treatment of the terminal is lead free.

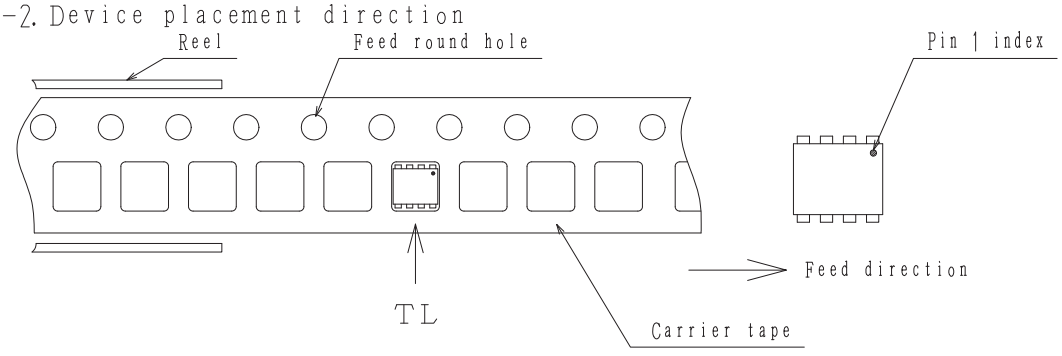
Label	JEITA Phase
LEAD FREE 3	JEITA Phase 3A
LEAD FREE 4	JEITA Phase 3

2. Taping configuration

2-1. Carrier tape size (unit:mm)



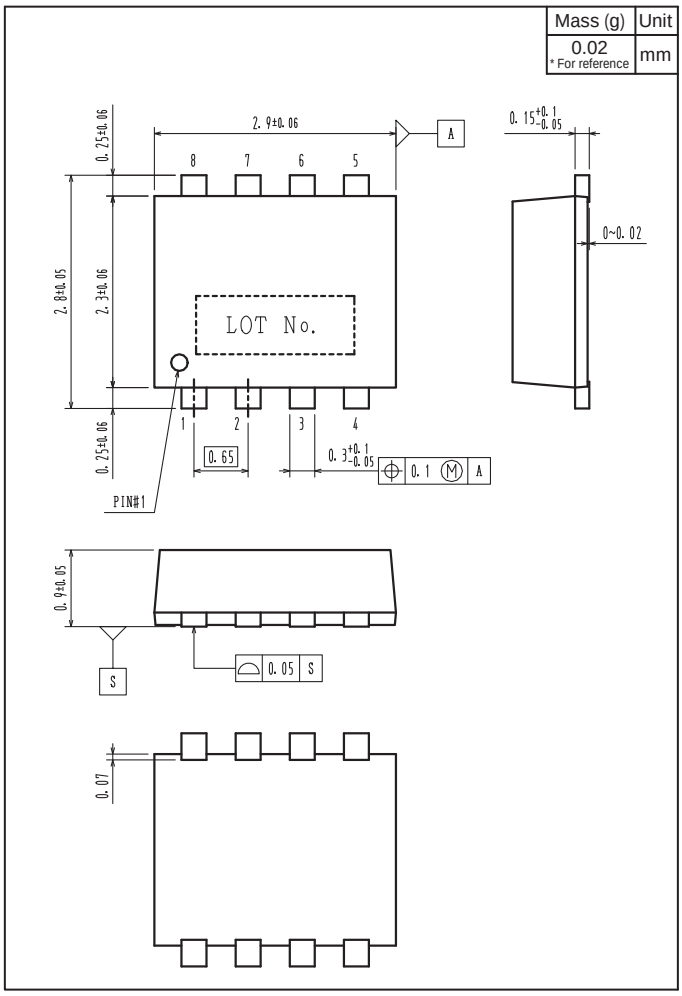
2-2. Device placement direction



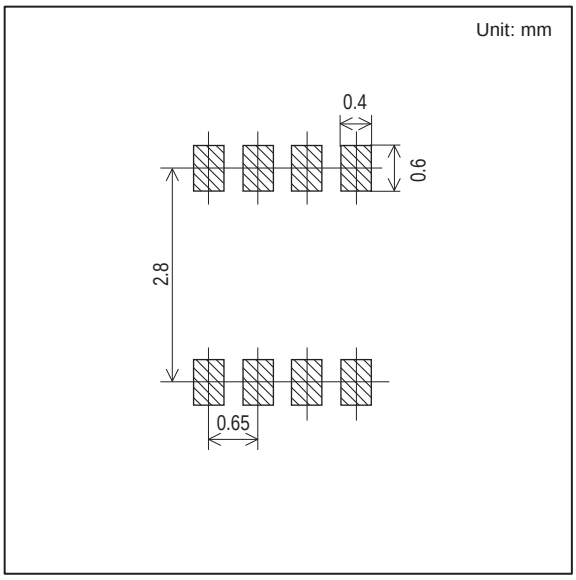
Those with pin 1 index on the feed hole side·····TL

Outline Drawing

ECH8661-TL-H



Land Pattern Example



Note on usage : Since the ECH8661 is a MOSFET product, please avoid using this device in the vicinity of highly charged objects.

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