Ordering number : ENA1358B

ECH8660

Power MOSFET

30V, 4.5A, 59mΩ, −30V, −4.5A, 59mΩ, Complementary Dual ECH8

ON Semiconductor®

http://onsemi.com

Features

- The ECH8660 incorporates an N-channel MOSFET and a P-channel MOSFET that feature low ON-resistance and high-speed switching , thereby enablimg high-density mounting
- 4V drive
- Halogen free compliance

Specifications

Absolute Maximum Ratings at Ta=25°C

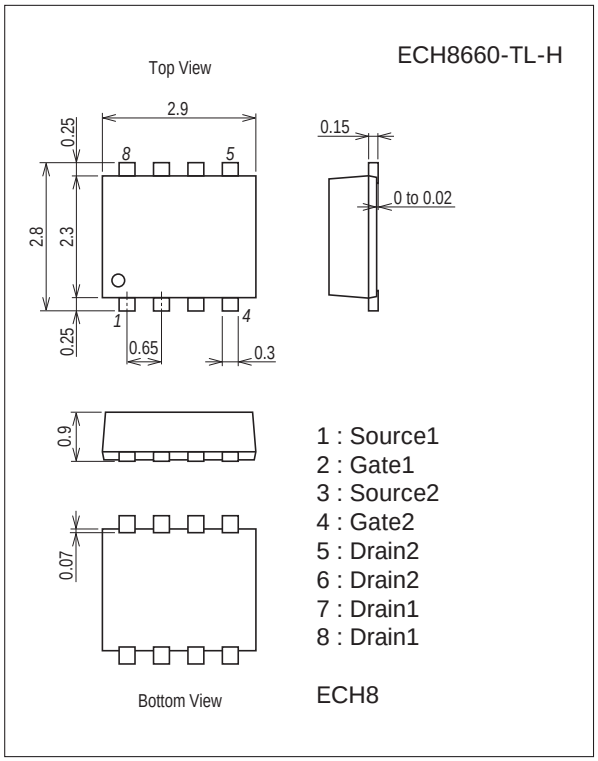
Parameter	Symbol	Conditions	N-channel	P-channel	Unit
Drain-to-Source Voltage	V_{DSS}		30	−30	V
Gate-to-Source Voltage	V_{GSS}		±20	±20	V
Drain Current (DC)	I_D		4.5	−4.5	A
Drain Current (Pulse)	I_{DP}	PW≤10μs, duty cycle≤1%	30	−30	A
Allowable Power Dissipation	P_D	When mounted on ceramic substrate (1200mm²×0.8mm) 1unit	1.3		W
Total Dissipation	P_T	When mounted on ceramic substrate (1200mm²×0.8mm)	1.5		W
Channel Temperature	Tch		150		°C
Storage Temperature	Tstg		−55 to +150		°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Package Dimensions

unit : mm (typ)

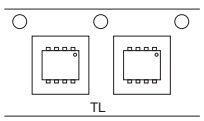
7011A-001



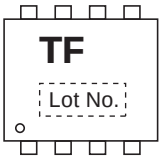
Product & Package Information

- Package : ECH8
- JEITA, JEDEC : -
- Minimum Packing Quantity : 3,000 pcs./reel

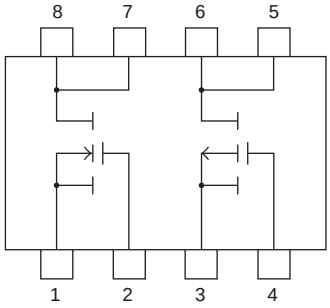
Packing Type : TL



Marking



Electrical Connection

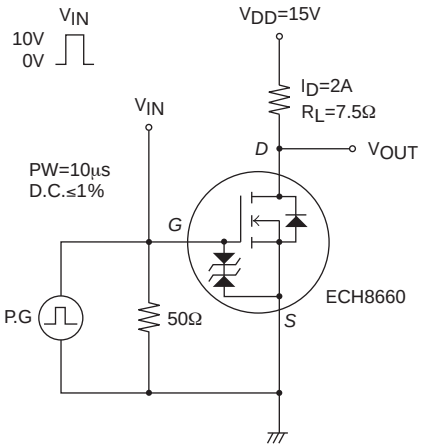


Electrical Characteristics at Ta=25°C

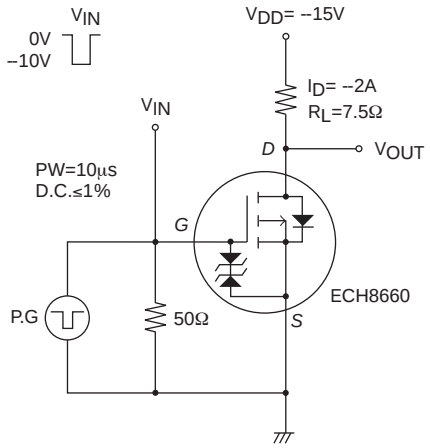
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[N-channel]						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=1mA, V_{GS}=0V	30			V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=30V, V_{GS}=0V			1	μA
Gate-to-Source Leakage Current	I_{GSS}	V_{GS}=±16V, V_{DS}=0V			±10	μA
Cutoff Voltage	V_{GS}(off)	V_{DS}=10V, I_D=1mA	1.2		2.6	V
Forward Transfer Admittance	| yfs |	V_{DS}=10V, I_D=2A	1	1.66		S
Static Drain-to-Source On-State Resistance	R_{DS}(on)1	I_D=2A, V_{GS}=10V		45	59	mΩ
	R_{DS}(on)2	I_D=1A, V_{GS}=4.5V		85	119	mΩ
	R_{DS}(on)3	I_D=1A, V_{GS}=4V		110	155	mΩ
Input Capacitance	Ciss	V_{DS}=10V, f=1MHz		240		pF
Output Capacitance	Coss	V_{DS}=10V, f=1MHz		45		pF
Reverse Transfer Capacitance	Crss	V_{DS}=10V, f=1MHz		30		pF
Turn-ON Delay Time	t_d(on)	See specified Test Circuit.		6.2		ns
Rise Time	t_r	See specified Test Circuit.		11		ns
Turn-OFF Delay Time	t_d(off)	See specified Test Circuit.		17		ns
Fall Time	t_f	See specified Test Circuit.		7.5		ns
Total Gate Charge	Qg	V_{DS}=10V, V_{GS}=10V, I_D=4.5A		4.4		nC
Gate-to-Source Charge	Qgs	V_{DS}=10V, V_{GS}=10V, I_D=4.5A		1.1		nC
Gate-to-Drain “Miller” Charge	Qgd	V_{DS}=10V, V_{GS}=10V, I_D=4.5A		0.64		nC
Diode Forward Voltage	V_{SD}	I_S=4.5A, V_{GS}=0V		0.84	1.2	V
[P-channel]						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=−1mA, V_{GS}=0V	−30			V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=−30V, V_{GS}=0V			−1	μA
Gate-to-Source Leakage Current	I_{GSS}	V_{GS}=±16V, V_{DS}=0V			±10	μA
Cutoff Voltage	V_{GS}(off)	V_{DS}=−10V, I_D=−1mA	−1.2		−2.3	V
Forward Transfer Admittance	| yfs |	V_{DS}=−10V, I_D=−2A	2.5	4.2		S
Static Drain-to-Source On-State Resistance	R_{DS}(on)1	I_D=−2A, V_{GS}=−10V		45	59	mΩ
	R_{DS}(on)2	I_D=−1A, V_{GS}=−4.5V		71	100	mΩ
	R_{DS}(on)3	I_D=−1A, V_{GS}=−4V		82	115	mΩ
Input Capacitance	Ciss	V_{DS}=−10V, f=1MHz		430		pF
Output Capacitance	Coss	V_{DS}=−10V, f=1MHz		105		pF
Reverse Transfer Capacitance	Crss	V_{DS}=−10V, f=1MHz		75		pF
Turn-ON Delay Time	t_d(on)	See specified Test Circuit.		7.5		ns
Rise Time	t_r	See specified Test Circuit.		26		ns
Turn-OFF Delay Time	t_d(off)	See specified Test Circuit.		45		ns
Fall Time	t_f	See specified Test Circuit.		35		ns
Total Gate Charge	Qg	V_{DS}=−10V, V_{GS}=−10V, I_D=−4.5A		10		nC
Gate-to-Source Charge	Qgs	V_{DS}=−10V, V_{GS}=−10V, I_D=−4.5A		2.0		nC
Gate-to-Drain “Miller” Charge	Qgd	V_{DS}=−10V, V_{GS}=−10V, I_D=−4.5A		2.5		nC
Diode Forward Voltage	V_{SD}	I_S=−4.5A, V_{GS}=0V		−0.85	−1.2	V

Switching Time Test Circuit

[N-channel]

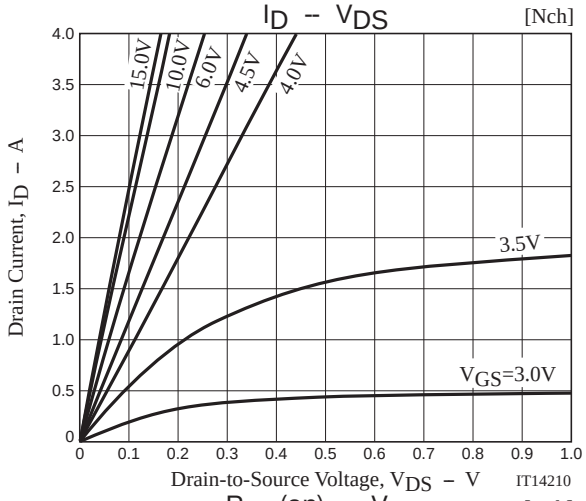


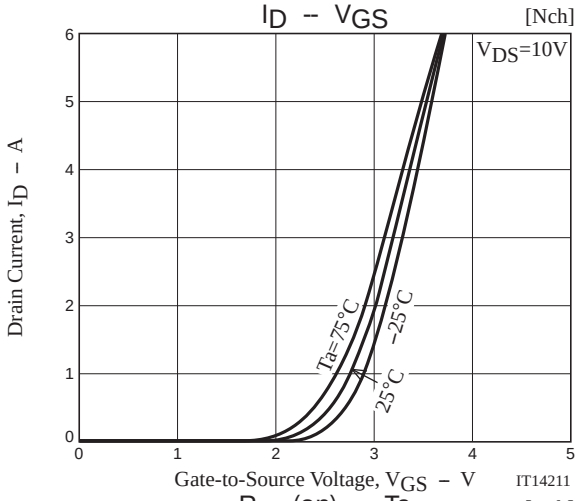
[P-channel]

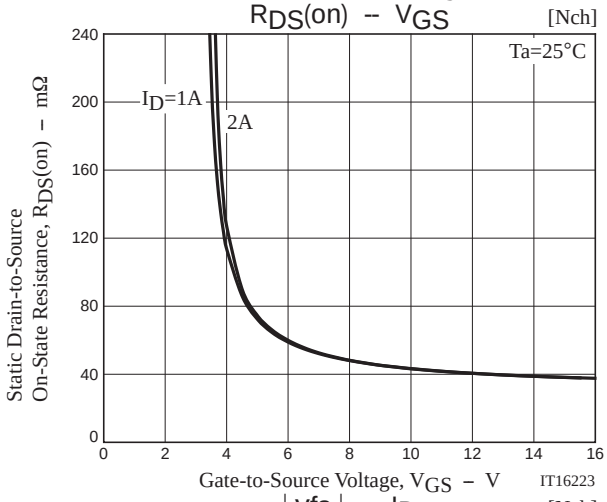


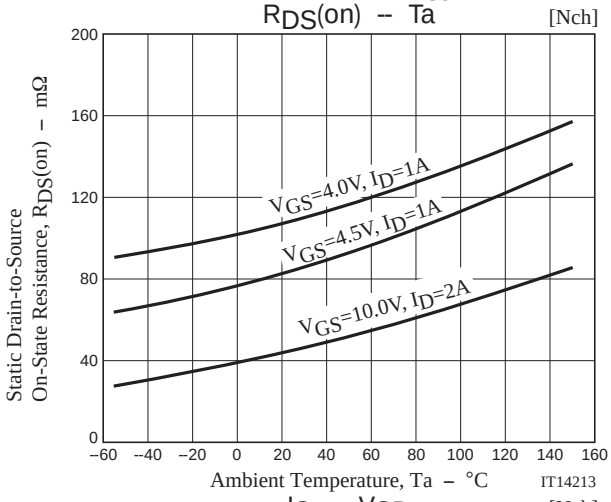
Ordering Information

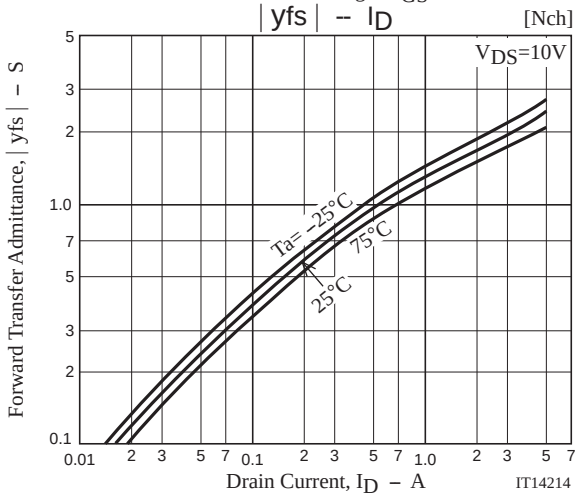
Device	Package	Shipping	memo
ECH8660-TL-H	ECH8	3,000pcs./reel	Pb-Free and Halogen Free

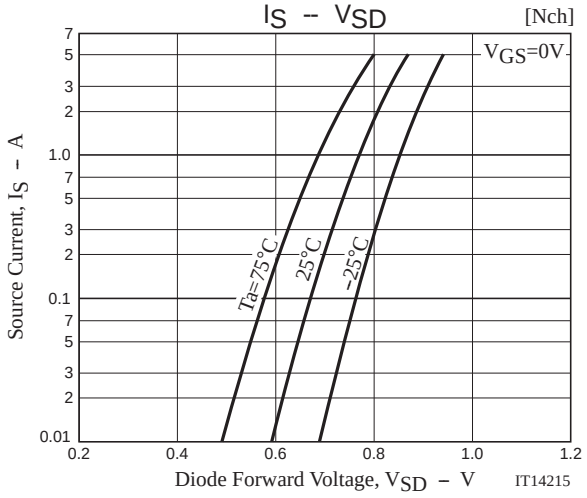


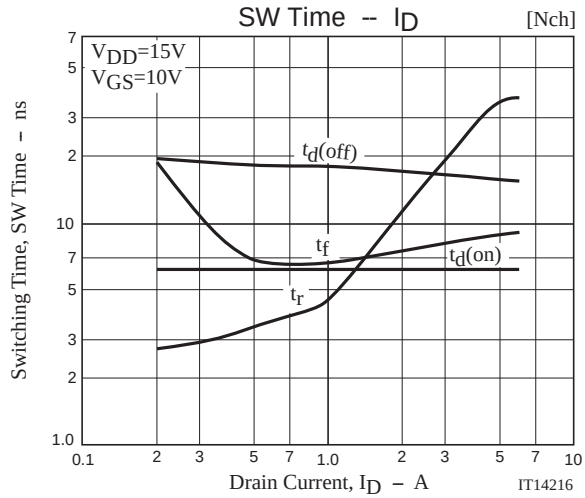


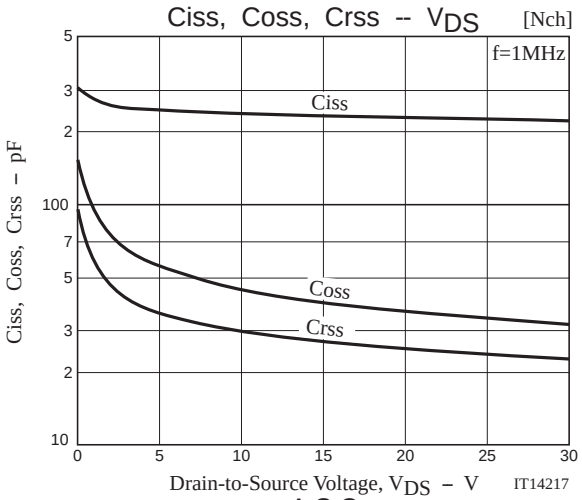


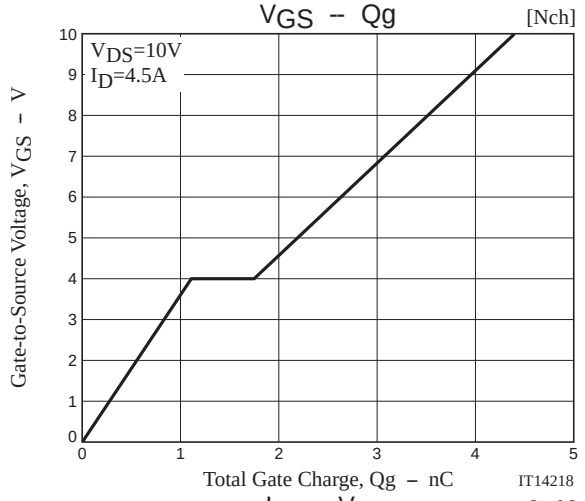


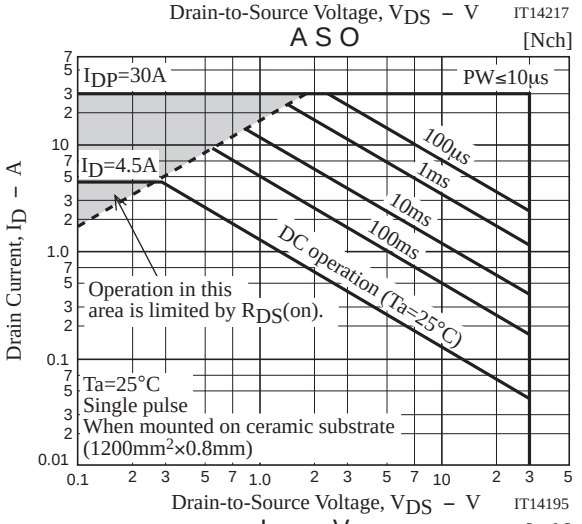


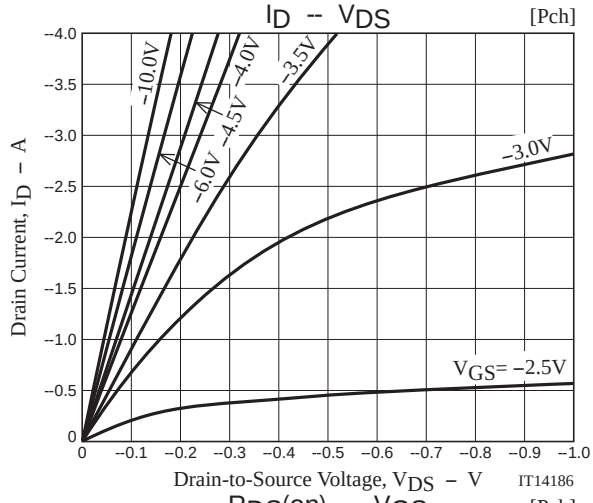


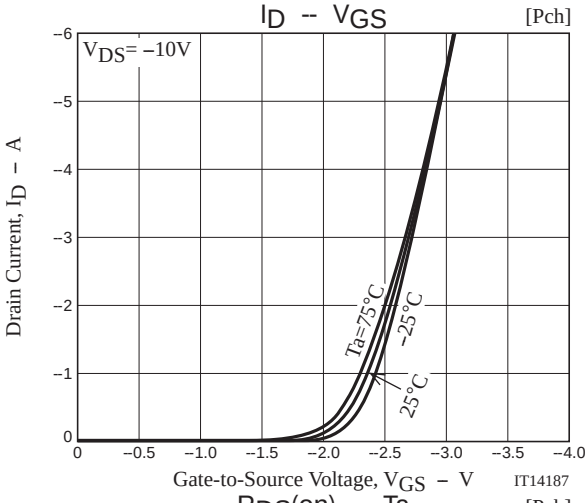

SW Time -- ID
[Nch]
VDD=15V
VGS=10V
td(off)
tf
td(on)
tr
Switching Time, SW Time – ns
Drain Current, ID – A
IT14216

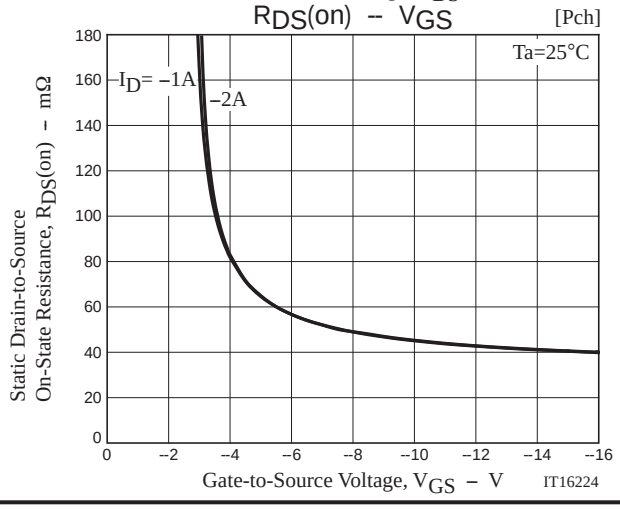

Ciss, Coss, Crss -- VDS
[Nch]
f=1MHz
Ciss
Coss
Crss
Ciss, Coss, Crss – pF
Drain-to-Source Voltage, VDS – V
IT14217

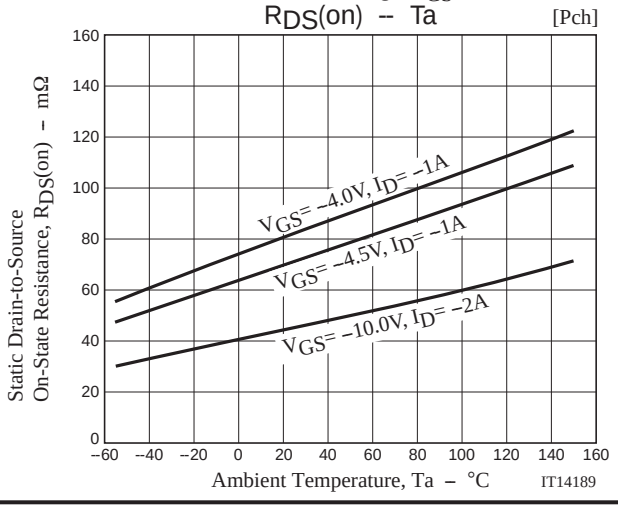

VGS -- Qg
[Nch]
VDS=10V
ID=4.5A
Gate-to-Source Voltage, VGS – V
Total Gate Charge, Qg – nC
IT14218

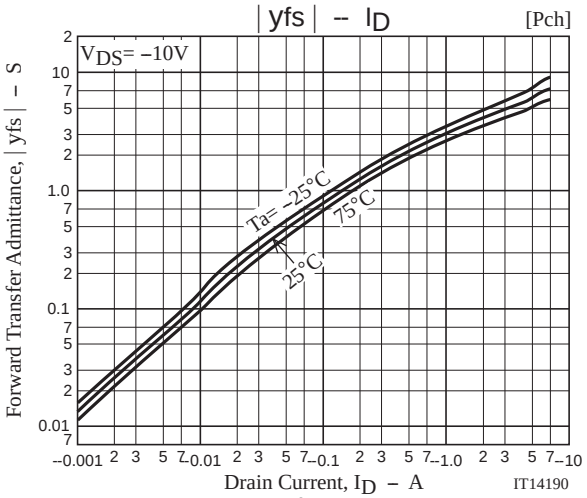

A S O
[Nch]
IDP=30A
PW≤10μs
ID=4.5A
100μs
1ms
10ms
100ms
DC operation (Ta=25°C)
Operation in this
area is limited by RDS(on).
Ta=25°C
Single pulse
When mounted on ceramic substrate
(1200mm2×0.8mm)
Drain Current, ID – A
Drain-to-Source Voltage, VDS – V
IT14195

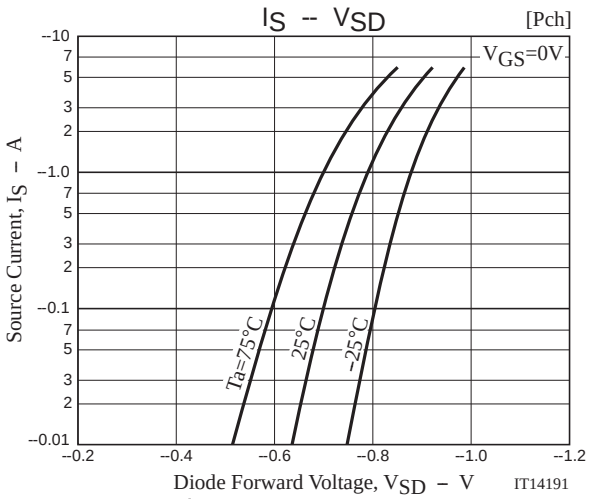

ID -- VDS
[Pch]
–10.0V
–6.0V
–4.5V
–4.0V
–3.5V
–3.0V
VGS= –2.5V
Drain Current, ID – A
Drain-to-Source Voltage, VDS – V
IT14186

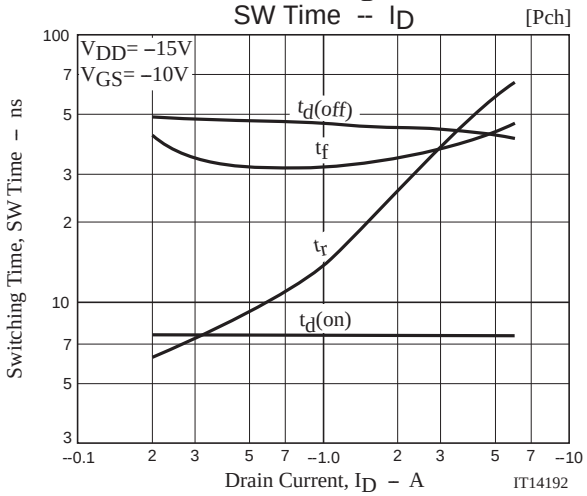

ID -- VGS
[Pch]
VDS= –10V
Ta=75°C
25°C
–25°C
Drain Current, ID – A
Gate-to-Source Voltage, VGS – V
IT14187

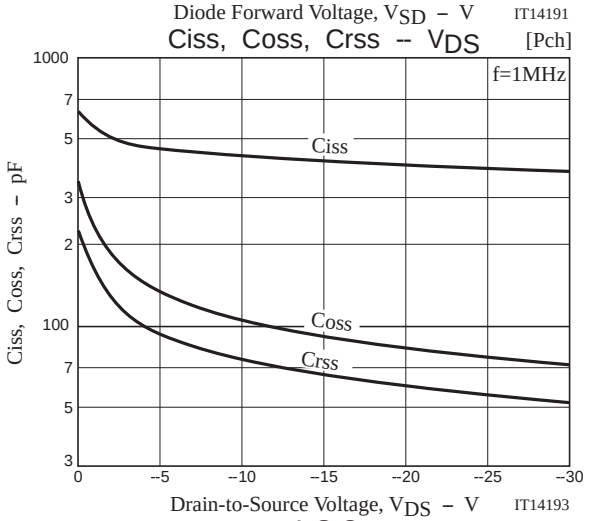

RDS(on) -- VGS
[Pch]
Ta=25°C
ID= –1A
–2A
Static Drain-to-Source
On-State Resistance, RDS(on) – mΩ
Gate-to-Source Voltage, VGS – V
IT16224

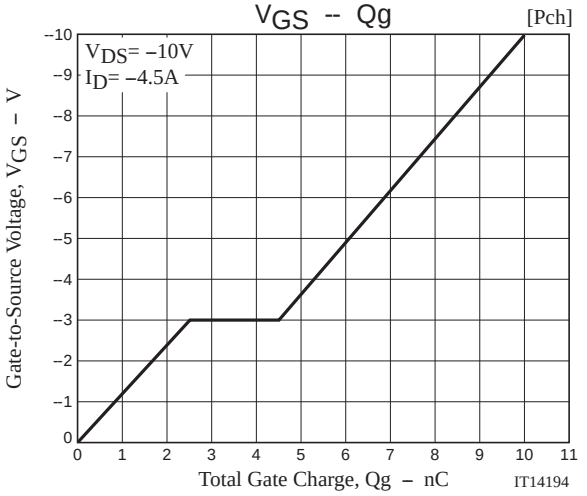

RDS(on) -- Ta
[Pch]
VGS= –4.0V, ID= –1A
VGS= –4.5V, ID= –1A
VGS= –10.0V, ID= –2A
Static Drain-to-Source
On-State Resistance, RDS(on) – mΩ
Ambient Temperature, Ta – °C
IT14189

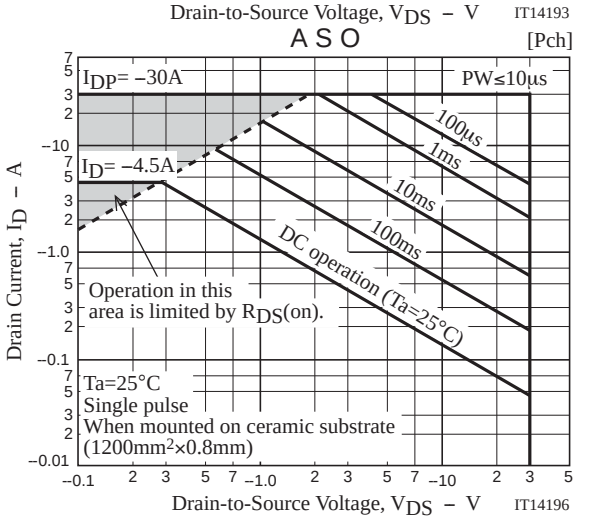

| yfs | -- ID
[Pch]
VDS= −10V
Ta= −25°C
75°C
25°C
Forward Transfer Admittance, | yfs | − S
Drain Current, ID − A
IT14190

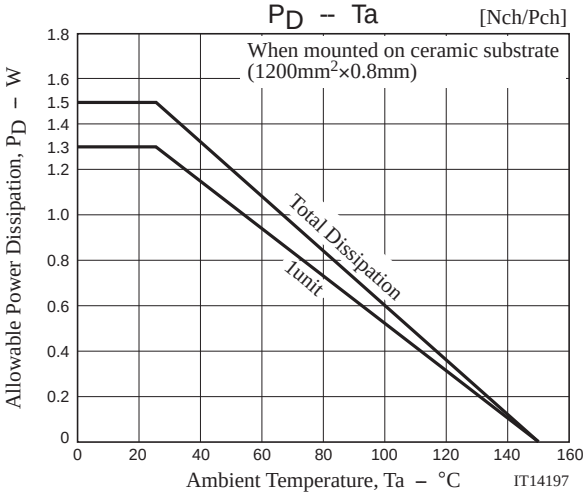

IS -- VSD
[Pch]
VGS=0V
Ta=75°C
25°C
−25°C
Source Current, IS − A
Diode Forward Voltage, VSD − V
IT14191


SW Time -- ID
[Pch]
VDD= −15V
VGS= −10V
td(off)
tf
tr
td(on)
Switching Time, SW Time − ns
Drain Current, ID − A
IT14192


Ciss, Coss, Crss -- VDS
[Pch]
f=1MHz
Ciss
Coss
Crss
Ciss, Coss, Crss − pF
Drain-to-Source Voltage, VDS − V
IT14193


VGS -- Qg
[Pch]
VDS= −10V
ID= −4.5A
Gate-to-Source Voltage, VGS − V
Total Gate Charge, Qg − nC
IT14194


A S O
[Pch]
IDP= −30A
PW≤10μs
100μs
1ms
10ms
100ms
DC operation (Ta=25°C)
ID= −4.5A
Operation in this
area is limited by RDS(on).
Ta=25°C
Single pulse
When mounted on ceramic substrate
(1200mm2×0.8mm)
Drain Current, ID − A
Drain-to-Source Voltage, VDS − V
IT14196


PD -- Ta
[Nch/Pch]
When mounted on ceramic substrate
(1200mm2×0.8mm)
Total Dissipation
1unit
Allowable Power Dissipation, PD − W
Ambient Temperature, Ta − °C
IT14197

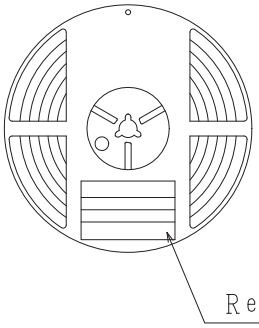
Embossed Taping Specification

ECH8660-TL-H

1. Packing Format

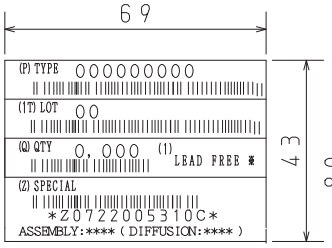
Package Name	Carrier Tape Type	Maximum Number of devices contained (pcs)			Packing format	
		Reel	Inner box	Outer box	Inner BOX (C-1)	Outer BOX (A-7)
ECH8	CPH6	3,000	15,000	90,000	5 reels contained Dimensions:mm(external) 183×72×185	6 inner boxes contained Dimensions:mm(external) 440×195×210

Packing method



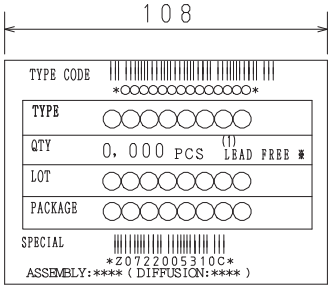
Reel label, Inner box label

(unit:mm)



Outer box label

It is a label at the time of factory shipments. The form of a label may change in physical distribution process.



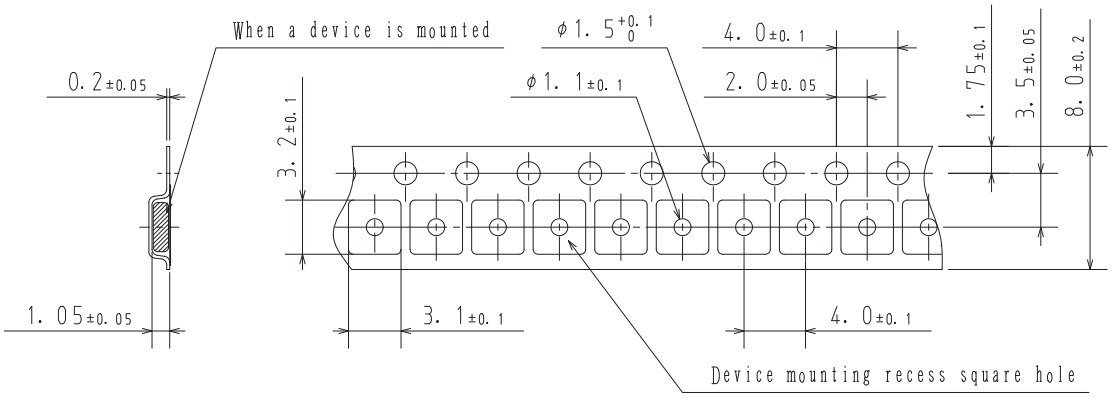
NOTE (1)

The LEAD FREE ※ description shows that the surface treatment of the terminal is lead free.

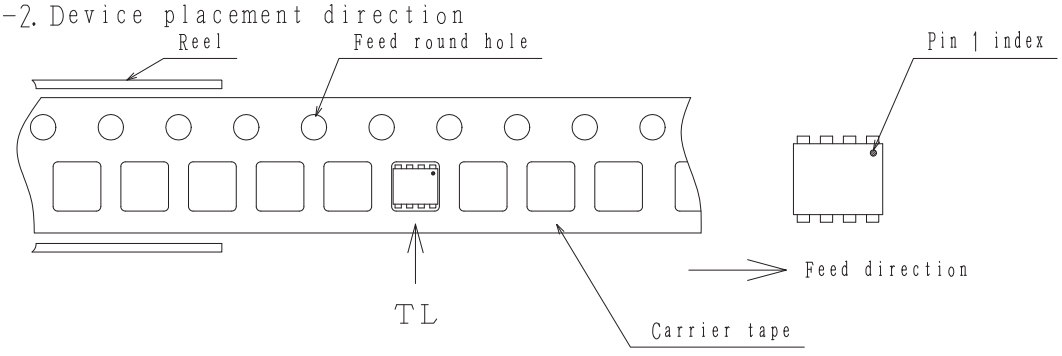
Label	JEITA Phase
LEAD FREE 3	JEITA Phase 3A
LEAD FREE 4	JEITA Phase 3

2. Taping configuration

2-1. Carrier tape size (unit:mm)



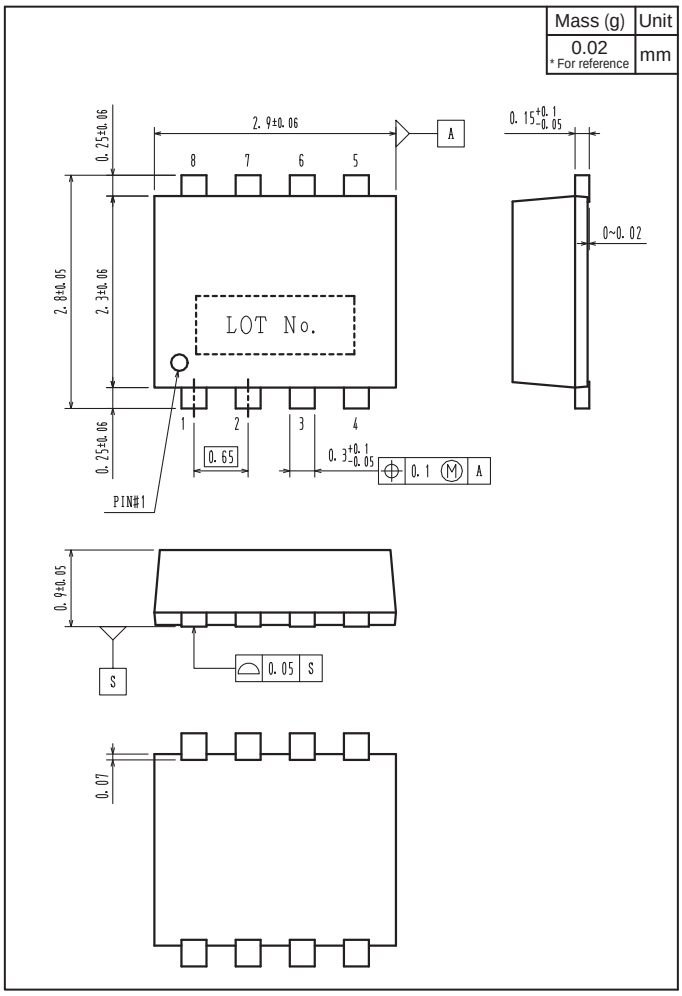
2-2. Device placement direction



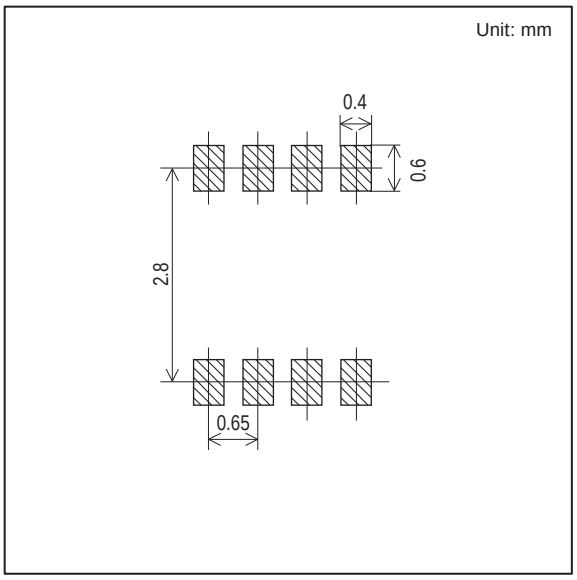
Those with pin 1 index on the feed hole side·····TL

Outline Drawing

ECH8660-TL-H



Land Pattern Example



Note on usage : Since the ECH8660 is a MOSFET product, please avoid using this device in the vicinity of highly charged objects.

ON Semiconductor and the ON logo are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.