ELPIDA

DATA SHEET

1GB Unbuffered DDR3 SDRAM DIMM

EBJ10EE8BAWA (128M words × 72 bits, 1 Rank)

Specifications

- Density: 1GB
- Organization
  - 128M words × 72 bits, 1 rank
- Mounting 9 pieces of 1G bits DDR3 SDRAM sealed in FBGA
- Package: 240-pin socket type dual in line memory module (DIMM)
  - PCB height: 30.0mm
  - Lead pitch: 1.0mm
  - Lead-free (RoHS compliant)
- Power supply: VDD = 1.5V ± 0.075V
- Data rate: 1333Mbps/1066Mbps/800Mbps (max.)
- Eight internal banks for concurrent operation (components)
- Interface: SSTL_15
- Burst lengths (BL): 8 and 4 with Burst Chop (BC)
- /CAS Latency (CL): 6, 7, 8, 9
- /CAS write latency (CWL): 5, 6, 7
- Precharge: auto precharge option for each burst access
- Refresh: auto-refresh, self-refresh
- Refresh cycles
  - Average refresh period
    7.8µs at 0°C ≤ TC ≤ +85°C
    3.9µs at +85°C < TC ≤ +95°C
- Operating case temperature range
  - TC = 0°C to +95°C

Features

- Double-data-rate architecture; two data transfers per clock cycle
- The high-speed data transfer is realized by the 8 bits prefetch pipelined architecture
- Bi-directional differential data strobe (DQS and /DQS) is transmitted/received with data for capturing data at the receiver
- DQS is edge-aligned with data for READs; center-aligned with data for WRITEs
- Differential clock inputs (CK and /CK)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Data mask (DM) for write data
- Posted /CAS by programmable additive latency for better command and data bus efficiency
- On-Die-Termination (ODT) for better signal quality
  - Synchronous ODT
  - Dynamic ODT
  - Asynchronous ODT
- Multi Purpose Register (MPR) for temperature read out
- ZQ calibration for DQ drive and ODT
- Programmable Partial Array Self-Refresh (PASR)
- /RESET pin for Power-up sequence and reset function
- SRT range:
  - Normal/extended
  - Auto/manual self-refresh
- Programmable Output driver impedance control
- Class B temperature sensor functionality with EEPROM

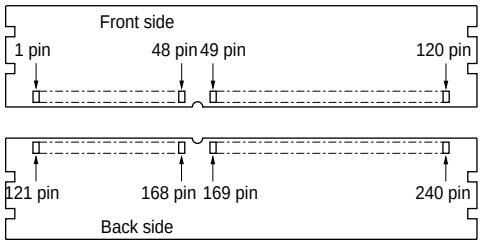
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Ordering Information

Part number	Data rate Mbps (max.)	Component JEDEC speed bin (CL-tRCD-tRP)	Package	Contact pad	Mounted devices
EBJ10EE8BAWA-DJ-E	1333	DDR3-1333H (9-9-9)	240-pin DIMM (lead-free)	Gold	EDJ1108BABG-DG-E EDJ1108BABG-DJ-E
EBJ10EE8BAWA-AE-E	1066	DDR3-1066F (7-7-7)			EDJ1108BABG-DG-E EDJ1108BABG-DJ-E EDJ1108BABG-AC-E EDJ1108BABG-AE-E
EBJ10EE8BAWA-8C-E	800	DDR3-800E (6-6-6)			EDJ1108BABG-DG-E EDJ1108BABG-DJ-E EDJ1108BABG-AC-E EDJ1108BABG-AE-E EDJ1108BABG-AG-E EDJ1108BABG-8A-E EDJ1108BABG-8C-E

Pin Configurations



Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	VREFDQ	61	A2	121	VSS	181	A1
2	VSS	62	VDD	122	DQ4	182	VDD
3	DQ0	63	NC	123	DQ5	183	VDD
4	DQ1	64	NC	124	VSS	184	CK0
5	VSS	65	VDD	125	DM0	185	/CK0
6	/DQS0	66	VDD	126	NC	186	VDD
7	DQS0	67	VREFCA	127	VSS	187	/EVENT
8	VSS	68	NC	128	DQ6	188	A0
9	DQ2	69	VDD	129	DQ7	189	VDD
10	DQ3	70	A10(AP)	130	VSS	190	BA1
11	VSS	71	BA0	131	DQ12	191	VDD
12	DQ8	72	VDD	132	DQ13	192	/RAS
13	DQ9	73	/WE	133	VSS	193	/CS0
14	VSS	74	/CAS	134	DM1	194	VDD
15	/DQS1	75	VDD	135	NC	195	ODT0
16	DQS1	76	NC	136	VSS	196	A13
17	VSS	77	NC	137	DQ14	197	VDD
18	DQ10	78	VDD	138	DQ15	198	NC
19	DQ11	79	NC	139	VSS	199	VSS
20	VSS	80	VSS	140	DQ20	200	DQ36
21	DQ16	81	DQ32	141	DQ21	201	DQ37
22	DQ17	82	DQ33	142	VSS	202	VSS
23	VSS	83	VSS	143	DM2	203	DM4
24	/DQS2	84	/DQS4	144	NC	204	NC
25	DQS2	85	DQS4	145	VSS	205	VSS
26	VSS	86	VSS	146	DQ22	206	DQ38
27	DQ18	87	DQ34	147	DQ23	207	DQ39
28	DQ19	88	DQ35	148	VSS	208	VSS
29	VSS	89	VSS	149	DQ28	209	DQ44
30	DQ24	90	DQ40	150	DQ29	210	DQ45
31	DQ25	91	DQ41	151	VSS	211	VSS
32	VSS	92	VSS	152	DM3	212	DM5
33	/DQS3	93	/DQS5	153	NC	213	NC
34	DQS3	94	DQS5	154	VSS	214	VSS
35	VSS	95	VSS	155	DQ30	215	DQ46
36	DQ26	96	DQ42	156	DQ31	216	DQ47

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
37	DQ27	97	DQ43	157	VSS	217	VSS
38	VSS	98	VSS	158	CB4	218	DQ52
39	CB0	99	DQ48	159	CB5	219	DQ53
40	CB1	100	DQ49	160	VSS	220	VSS
41	VSS	101	VSS	161	DM8	221	DM6
42	/DQS8	102	/DQS6	162	NC	222	NC
43	DQS8	103	DQS6	163	VSS	223	VSS
44	VSS	104	VSS	164	CB6	224	DQ54
45	CB2	105	DQ50	165	CB7	225	DQ55
46	CB3	106	DQ51	166	VSS	226	VSS
47	VSS	107	VSS	167	NC	227	DQ60
48	NC	108	DQ56	168	/RESET	228	DQ61
49	NC	109	DQ57	169	NC	229	VSS
50	CKE0	110	VSS	170	VDD	230	DM7
51	VDD	111	/DQS7	171	NC	231	NC
52	BA2	112	DQS7	172	NC	232	VSS
53	NC	113	VSS	173	VDD	233	DQ62
54	VDD	114	DQ58	174	A12	234	DQ63
55	A11	115	DQ59	175	A9	235	VSS
56	A7	116	VSS	176	VDD	236	VDDSPD
57	VDD	117	SA0	177	A8	237	SA1
58	A5	118	SCL	178	A6	238	SDA
59	A4	119	SA2	179	VDD	239	VSS
60	VDD	120	VTT	180	A3	240	VTT

Pin Description

Pin name	Function
A0 to A13	Address input Row address A0 to A13 Column address A0 to A9
A10 (AP)	Auto precharge
A12 (/BC)	Burst chop
BA0, BA1, BA2	Bank select address
DQ0 to DQ63	Data input/output
CB0 to CB7	Check bit (Data input/output)
/RAS	Row address strobe command
/CAS	Column address strobe command
/WE	Write enable
/CS0	Chip select
CKE0	Clock enable
CK0	Clock input
/CK0	Differential clock input
DQS0 to DQS8, /DQS0 to /DQS8	Input and output data strobe
DM0 to DM8	Input mask
SCL	Clock input for serial PD
SDA	Data input/output for serial PD
SA0, SA1, SA2	Serial address input
VDD	Power for internal circuit
VDDSPD	Power for serial EEPROM
VREFCA	Reference voltage for CA
VREFDQ	Reference voltage for DQ
VSS	Ground
VTT	I/O termination supply for SDRAM
/RESET	Set DRAM to known state
ODT0	ODT control
/EVENT	Temperature event pin
NC	No connection

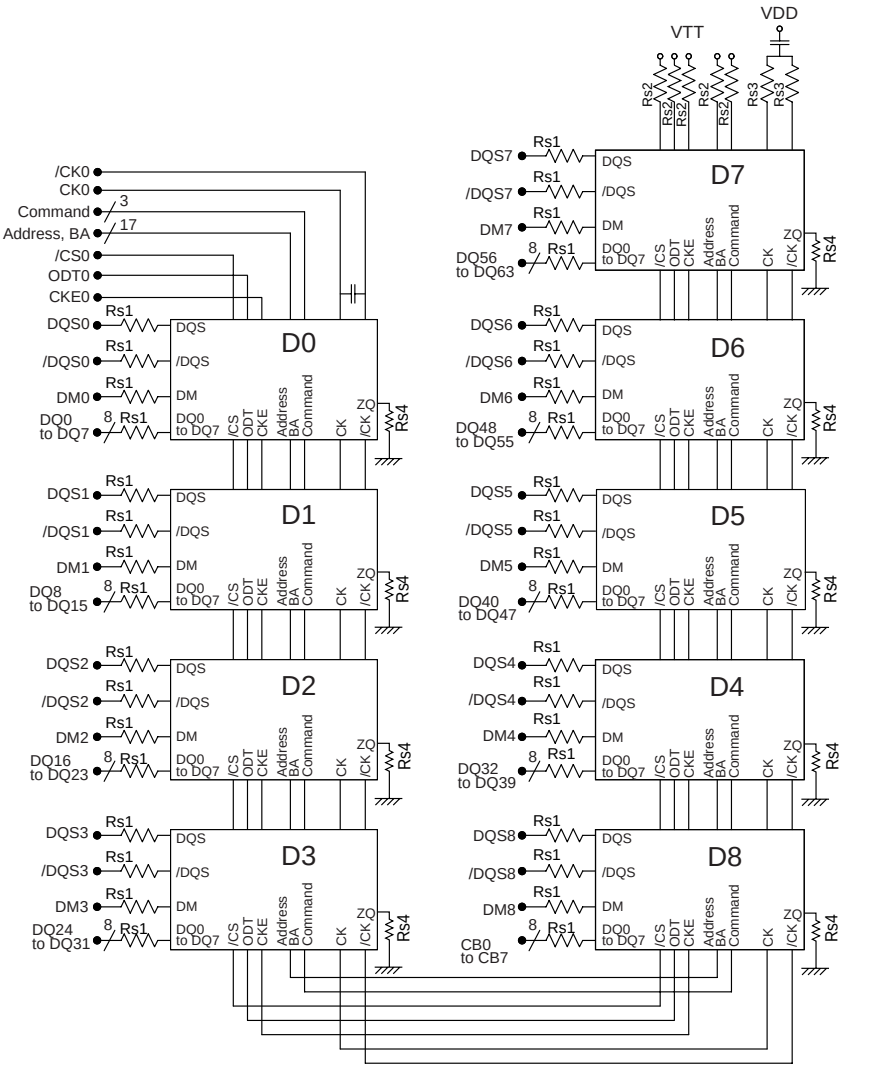
Serial PD Matrix

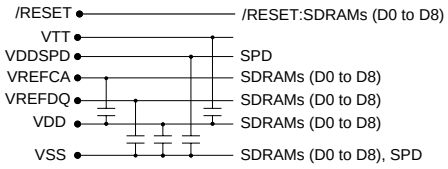
Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
0	Number of serial PD bytes written/SPD device size/CRC coverage	1	0	0	1	0	0	1	0	92H	176/256/0-116
1	SPD revision	0	0	0	1	0	0	0	0	10H	Revision 1.0
2	Key byte/DRAM device type	0	0	0	0	1	0	1	1	0BH	DDR3 SDRAM
3	Key byte/module type	0	0	0	0	0	0	1	0	02H	Unbuffered
4	SDRAM density and banks	0	0	0	0	0	0	1	0	02H	1G bits, 8 banks
5	SDRAM addressing	0	0	0	1	0	0	0	1	11H	14 rows, 10 columns
6	Module nominal voltage, VDD	0	0	0	0	0	0	0	0	00H	1.5V
7	Module organization	0	0	0	0	0	0	0	1	01H	1 rank/×8 bits
8	Module memory bus width	0	0	0	0	1	0	1	1	0BH	72 bits/ECC
9	Fine timebase (FTB) dividend/divisor	0	1	0	1	0	0	1	0	52H	5/2
10	Medium timebase (MTB) dividend	0	0	0	0	0	0	0	1	01H	1
11	Medium timebase (MTB) divisor	0	0	0	0	1	0	0	0	08H	8
12	SDRAM minimum cycle time (tCK (min.)) -DJ	0	0	0	0	1	1	0	0	0CH	1.5ns
	-AE	0	0	0	0	1	1	1	1	0FH	1.875ns
	-8C	0	0	0	1	0	1	0	0	14H	2.5ns
13	Reserved	0	0	0	0	0	0	0	0	00H	—
14	SDRAM /CAS latencies supported, LSB -DJ	0	0	1	1	1	1	0	0	3CH	CL = 6, 7, 8, 9
	-AE	0	0	0	1	1	1	0	0	1CH	CL = 6, 7, 8
	-8C	0	0	0	0	0	1	0	0	04H	CL = 6
15	SDRAM /CAS latencies supported, MSB	0	0	0	0	0	0	0	0	00H	—
16	SDRAM minimum /CAS latencies time (tAA (min.)) -DJ, -AE	0	1	1	0	1	0	0	1	69H	13.125ns
	-8C	0	1	1	1	1	0	0	0	78H	15ns
17	SDRAM write recovery time (tWR)	0	1	1	1	1	0	0	0	78H	15ns
18	SDRAM minimum /RAS to /CAS delay (tRCD) -DJ, -AE	0	1	1	0	1	0	0	1	69H	13.125ns
	-8C	0	1	1	1	1	0	0	0	78H	15ns
19	SDRAM minimum row active to row active delay (tRRD) -DJ	0	0	1	1	0	0	0	0	30H	6ns
	-AE	0	0	1	1	1	1	0	0	3CH	7.5ns
	-8C	0	1	0	1	0	0	0	0	50H	10ns
20	SDRAM minimum row precharge time (tRP) -DJ, -AE	0	1	1	0	1	0	0	1	69H	13.125ns
	-8C	0	1	1	1	1	0	0	0	78H	15ns
21	SDRAM upper nibbles for tRAS and tRC	0	0	0	1	0	0	0	1	11H	

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
22	SDRAM minimum active to precharge time (tRAS), LSB DJ	0	0	1	0	0	0	0	0	20H	36ns
	-AE, -8C	0	0	1	0	1	1	0	0	2CH	37.5ns
23	SDRAM minimum active to active /auto-refresh time (tRC), LSB -DJ	1	0	0	0	1	1	0	0	8CH	49.5ns
	-AE	1	0	0	1	0	1	0	1	95H	50.625ns
	-8C	1	0	1	0	0	1	0	0	A4H	52.5ns
24	SDRAM minimum refresh recovery time delay (tRFC), LSB	0	1	1	1	0	0	0	0	70H	110ns
25	SDRAM minimum refresh recovery time delay (tRFC), MSB	0	0	0	0	0	0	1	1	03H	110ns
26	SDRAM minimum internal write to read command delay (tWTR)	0	0	1	1	1	1	0	0	3CH	7.5ns
27	SDRAM minimum internal read to precharge command delay (tRTP)	0	0	1	1	1	1	0	0	3CH	7.5ns
28	Upper nibble for tFAW -DJ	0	0	0	0	0	0	0	0	00H	
	-AE, -8C	0	0	0	0	0	0	0	1	01H	
29	Minimum four activate window delay time (tFAW) -DJ	1	1	1	1	0	0	0	0	F0H	30ns
	-AE	0	0	1	0	1	1	0	0	2CH	37.5ns
	-8C	0	1	0	0	0	0	0	0	40H	40ns
30	SDRAM output drivers supported	1	0	0	0	0	0	1	1	83H	DLL-off/RZQ/6, 7
31	SDRAM refresh options	1	0	0	0	0	0	0	1	81H	PASR/2X refresh at +85C° to +95C°
32	Module thermal sensor	1	0	0	0	0	0	0	0	80H	Incorporated
33	SDRAM device type	0	0	0	0	0	0	0	0	00H	Standard
34 to 59	Reserved	0	0	0	0	0	0	0	0	00H	—
60	Module nominal height	0	0	0	0	1	1	1	1	0FH	29 < height ≤ 30mm
61	Module maximum thickness	0	0	0	0	0	0	0	1	01H	
62	Reference raw card used	0	0	0	0	0	0	1	1	03H	Raw Card D
63	Address mapping from edge connecter to DRAM	0	0	0	0	0	0	0	0	00H	Standard
64 to 116	Module specific section	0	0	0	0	0	0	0	0	00H	—
117	Module ID: manufacturer's JEDEC ID code, LSB	0	0	0	0	0	0	1	0	02H	Elpida Memory
118	Module ID: manufacturer's JEDEC ID code, MSB	1	1	1	1	1	1	1	0	FEH	Elpida Memory
119	Module ID: manufacturing location	×	×	×	×	×	×	×	×	××	
120	Module ID: manufacturing date	×	×	×	×	×	×	×	×	××	Year code (BCD)
121	Module ID: manufacturing date	×	×	×	×	×	×	×	×	××	Week code (BCD)
122 to 125	Module ID: module serial number	×	×	×	×	×	×	×	×	××	
126	Cyclical redundancy code (CRC) -DJ	0	0	1	1	0	0	1	1	33H	
	-AE	0	0	0	0	0	1	1	0	06H	
	-8C	1	0	0	1	1	1	1	0	9EH	

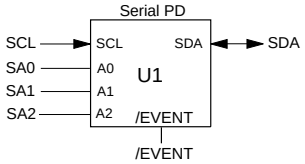
Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
127	Cyclical redundancy code (CRC) -DJ	1	1	1	0	1	1	1	0	EEH	
	-AE	1	1	1	1	1	1	1	1	FFH	
	-8C	1	0	1	0	0	1	1	0	A6H	
128	Module part number	0	1	0	0	0	1	0	1	45H	E
129	Module part number	0	1	0	0	0	0	1	0	42H	B
130	Module part number	0	1	0	0	1	0	1	0	4AH	J
131	Module part number	0	0	1	1	0	0	0	1	31H	1
132	Module part number	0	0	1	1	0	0	0	0	30H	0
133	Module part number	0	1	0	0	0	1	0	1	45H	E
134	Module part number	0	1	0	0	0	1	0	1	45H	E
135	Module part number	0	0	1	1	1	0	0	0	38H	8
136	Module part number	0	1	0	0	0	0	1	0	42H	B
137	Module part number	0	1	0	0	0	0	0	1	41H	A
138	Module part number	0	1	0	1	0	1	1	1	57H	W
139	Module part number	0	1	0	0	0	0	0	1	41H	A
140	Module part number	0	0	1	0	1	1	0	1	2DH	—
141	Module part number -DJ	0	1	0	0	0	1	0	0	44H	D
	-AE	0	1	0	0	0	0	0	1	41H	A
	-8C	0	0	1	1	1	0	0	0	38H	8
142	Module part number -DJ	0	1	0	0	1	0	1	0	4AH	J
	-AE	0	1	0	0	0	1	0	1	45H	E
	-8C	0	1	0	0	0	0	1	1	43H	C
143	Module part number	0	0	1	0	1	1	0	1	2DH	—
144	Module part number	0	1	0	0	0	1	0	1	45H	E
145	Module part number	0	0	1	0	0	0	0	0	20H	(Space)
146	Module revision code	0	0	1	1	0	0	0	0	30H	Initial
147	Module revision code	0	0	1	0	0	0	0	0	20H	(Space)
148	SDRAM manufacturer’s JEDEC ID code, LSB	0	0	0	0	0	0	1	0	02H	Elpida Memory
149	SDRAM manufacturer’s JEDEC ID code, MSB	1	1	1	1	1	1	1	0	FEH	Elpida Memory
150 to 175	Manufacturer's specific data	0	0	0	0	0	0	0	0	00H	
176 to 255	Open for customer use										

Block Diagram

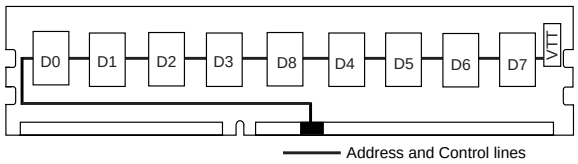




Notes :
1. DQ wiring may be changed within a byte.
2. DQ, DQS, /DQS, ODT, DM, CKE, /CS relationships must be maintained as shown.



* D0 to D8: 1G bits DDR3 SDRAM
Address, BA: A0 to A13, BA0 to BA2
Command: /RAS, /CAS, /WE
U1: 256 bytes EEPROM
Rs1: 15Ω
Rs2: 39Ω
Rs3: 36Ω
Rs4: 240Ω



Electrical Specifications

- All voltages are referenced to VSS (GND).

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Notes
Power supply voltage	VDD	–0.4 to +1.975	V	1, 3, 4
Input voltage	VIN	–0.4 to +1.975	V	1, 4
Output voltage	VOUT	–0.4 to +1.975	V	1, 4
Reference voltage	VREFCA	–0.4 to 0.6 × VDD	V	3, 4
Reference voltage for DQ	VREFDQ	–0.4 to 0.6 × VDDQ	V	3, 4
Storage temperature	Tstg	–55 to +100	°C	1, 2, 4
Power dissipation	PD	9	W	
Short circuit output current	IOUT	50	mA	1, 4

Notes: 1. Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. Storage temperature is the case surface temperature on the center/top side of the DRAM.
3. VDD and VDDQ must be within 300mV of each other at all times; and VREF must be not greater than 0.6 × VDDQ, When VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.
4. DDR3 SDRAM component specification.

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Operating Temperature Condition

Parameter	Symbol	Rating	Unit	Notes
Operating case temperature	TC	0 to +95	°C	1, 2, 3

Notes: 1. Operating temperature is the case surface temperature on the center/top side of the DRAM.

2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0°C to +85°C under all operating conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between +85°C and +95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
   a) Refresh commands must be doubled in frequency, therefore reducing the refresh interval tREFI to 3.9µs. (This double refresh requirement may not apply for some devices.)
   b) If Self-refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 bit [A6, A7] = [0, 1]) or enable the optional Auto Self-Refresh mode (MR2 bit [A6, A7] = [1, 0]).

Recommended DC Operating Conditions (TC = 0°C to +85°C)

Parameter	Symbol	min.	typ.	max.	Unit	Notes
Supply voltage	VDD, VDDQ	1.425	1.5	1.575	V	1, 2, 3
	VSS	0	0	0	V	1
	VDDSPD	3.0	3.3	3.6	V	
Input reference voltage	VREFCA (DC)	0.49 × VDDQ	0.50 × VDDQ	0.51 × VDDQ	V	1, 4, 5
Input reference voltage for DQ	VREFDQ (DC)	0.49 × VDDQ	0.50 × VDDQ	0.51 × VDDQ	V	1, 4, 5
Termination voltage	VTT	VDDQ/2 – TBD	TBD	VDDQ/2 + TBD	V	

Notes: 1. DDR3 SDRAM component specification.

2. Under all conditions VDDQ must be less than or equal to VDD.
3. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
4. The AC peak noise on VREF may not allow VREF to deviate from VREF(DC) by more than ±1% VDD (for reference: approx ±15 mV).
5. For reference: approx. VDD/2 ± 15 mV.

DC Characteristics 1 (TC = 0°C to +85°C, VDD = 1.5V ± 0.075V, VSS = 0V)

Parameter	Symbol	Data rate (Mbps)	max.	Unit	Notes
Operating current (ACT-PRE)	IDD0	1333	1080	mA	
		1066	990		
		800	900		
Operating current (ACT-READ-PRE)	IDD1	1333	1260	mA	
		1066	1125		
		800	1035		
Precharge power-down standby current	IDD2PF	1333	360	mA	Fast PD Exit
		1066	315		
		800	270		
	IDD2PS	1333	126	mA	Slow PD Exit
		1066	117		
		800	108		
Precharge quiet standby current	IDD2Q	1333	630	mA	
		1066	540		
		800	450		
Precharge standby current	IDD2N	1333	675	mA	
		1066	585		
		800	495		
Active power-down current (Always fast exit)	IDD3P	1333	405	mA	
		1066	360		
		800	315		
Active standby current	IDD3N	1333	765	mA	
		1066	675		
		800	585		
Operating current (Burst read operating)	IDD4R	1333	1980	mA	
		1066	1620		
		800	1260		
Operating current (Burst write operating)	IDD4W	1333	2160	mA	
		1066	1800		
		800	1440		
Burst refresh current	IDD5B	1333	3015	mA	
		1066	2835		
		800	2655		
All bank interleave read current	IDD7R	1333	3105	mA	
		1066	2565		
		800	2340		

Self-Refresh Current (TC = 0°C to +85°C, VDD = 1.5V ± 0.075V)

Parameter	Symbol	max.	Unit	Notes
Self-refresh current normal temperature range	IDD6	90	mA	
Self-refresh current extended temperature range	IDD6ET	162	mA	
Auto self-refresh current	IDD6TC	162	mA	

AC Timing for IDD Test Conditions

For purposes of IDD testing, the following parameters are to be utilized.

	DDR3-1333	DDR3-1066	DDR3-800	
Parameter	9-9-9	7-7-7	6-6-6	Unit
CL (IDD)	9	7	6	tCK
tCK min.(IDD)	1.5	1.875	2.5	ns
tRCD min. (IDD)	13.5	13.13	15	ns
tRC min. (IDD)	49.5	50.63	52.5	ns
tRAS min.(IDD)	36	37.5	37.5	ns
tRP min. (IDD)	13.5	13.13	15	ns
tFAW (IDD)	30	37.5	40	ns
tRRD (IDD)	6.0	7.5	10	ns
tRFC (IDD)	110	110	110	ns

DC Characteristics 2 (TC = 0°C to +85°C, VDD, VDDQ = 1.5V ± 0.075V)

(DDR3 SDRAM Component Specification)

Parameter	Symbol	Value	Unit	Notes
Input leakage current	$\|I_{LI}\|$	2	µA	VDD ≥ VIN ≥ VSS
Output leakage current	$\|I_{LO}\|$	5	µA	DDQ ≥ VOUT ≥ VSS

Pin Functions

CK, /CK (input pin)

CK and /CK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of /CK. Output (read) data is referenced to the crossings of CK and /CK (both directions of crossing).

/CS (input pin)

All commands are masked when /CS is registered high. /CS provides for external rank selection on systems with multiple ranks. /CS is considered part of the command code.

/RAS, /CAS, and /WE (input pins)

/RAS, /CAS and /WE (along with /CS) define the command being entered.

A0 to A13 (input pins)

Provided the row address for active commands and the column address for read/write commands to select one location out of the memory array in the respective bank. (A10(AP) and A12(/BC) have additional functions, see below) The address inputs also provide the op-code during mode register set commands.

[Address Pins Table]

Address (A0 to A13)		
Row address (RA)	Column address (CA)	Notes
AX0 to AX13	AY0 to AY9	

A10(AP) (input pin)

A10 is sampled during read/write commands to determine whether auto-precharge should be performed to the accessed bank after the read/write operation. (high: auto-precharge; low: no auto-precharge)

A10 is sampled during a precharge command to determine whether the precharge applies to one bank (A10 = low) or all banks (A10 = high). If only one bank is to be precharged, the bank is selected by bank addresses (BA).

A12 (/BC) (input pin)

A12 is sampled during read and write commands to determine if burst chop (on-the-fly) will be performed.

(A12 = high: no burst chop, A12 = low: burst chopped.)

BA0 to BA2 (input pins)

BA0, BA1 and BA2 define to which bank an active, read, write or precharge command is being applied. BA0 and BA1 also determine if a mode register is to be accessed during a MRS cycle.

[Bank Select Signal Table]

	BA0	BA1	BA2
Bank 0	L	L	L
Bank 1	H	L	L
Bank 2	L	H	L
Bank 3	H	H	L
Bank 4	L	L	H
Bank 5	H	L	H
Bank 6	L	H	H
Bank 7	H	H	H

Remark: H: VIH. L: VIL.

CKE (input pin)

CKE high activates, and CKE low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE low provides precharge power-down and self-refresh operation (all banks idle), or active power-down (row active in any bank). CKE is asynchronous for self-refresh exit. After VREF has become stable during the power-on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper self-refresh entry and exit, VREF must be maintained to this input. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, /CK, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self-refresh.

DQ and CB (input and output pins)

Bi-directional data bus.

DQS and /DQS (input and output pin)

Output with read data, input with write data. Edge-aligned with read data, centered in write data.
The data strobe DQS is paired with differential signals /DQS to provide differential pair signaling to the system during READs and WRITEs.

ODT (input pins)

ODT (registered high) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to each DQ, DQS, /DQS, DM. The ODT pin will be ignored if the mode register (MR1) is programmed to disable ODT.

DM (input pins)

DM is the reference signal of the data input mask function. DMs are sampled at the cross point of DQS and /DQS.

VDD (power supply pins)

1.5V is applied. (VDD is for the internal circuit.)

VDDSPD (power supply pin)

3.3V is applied (For serial EEPROM).

VSS (power supply pin)

Ground is connected.

VTT (power supply pin)

I/O termination supply for SDRAM.

VREFDQ (power supply)

Reference voltage for DQ.

VREFCA (power supply)

Reference voltage for CA.

/RESET (input pin)

/RESET is negative active signal (active low) and is referred to GND.

/EVENT (output pin)

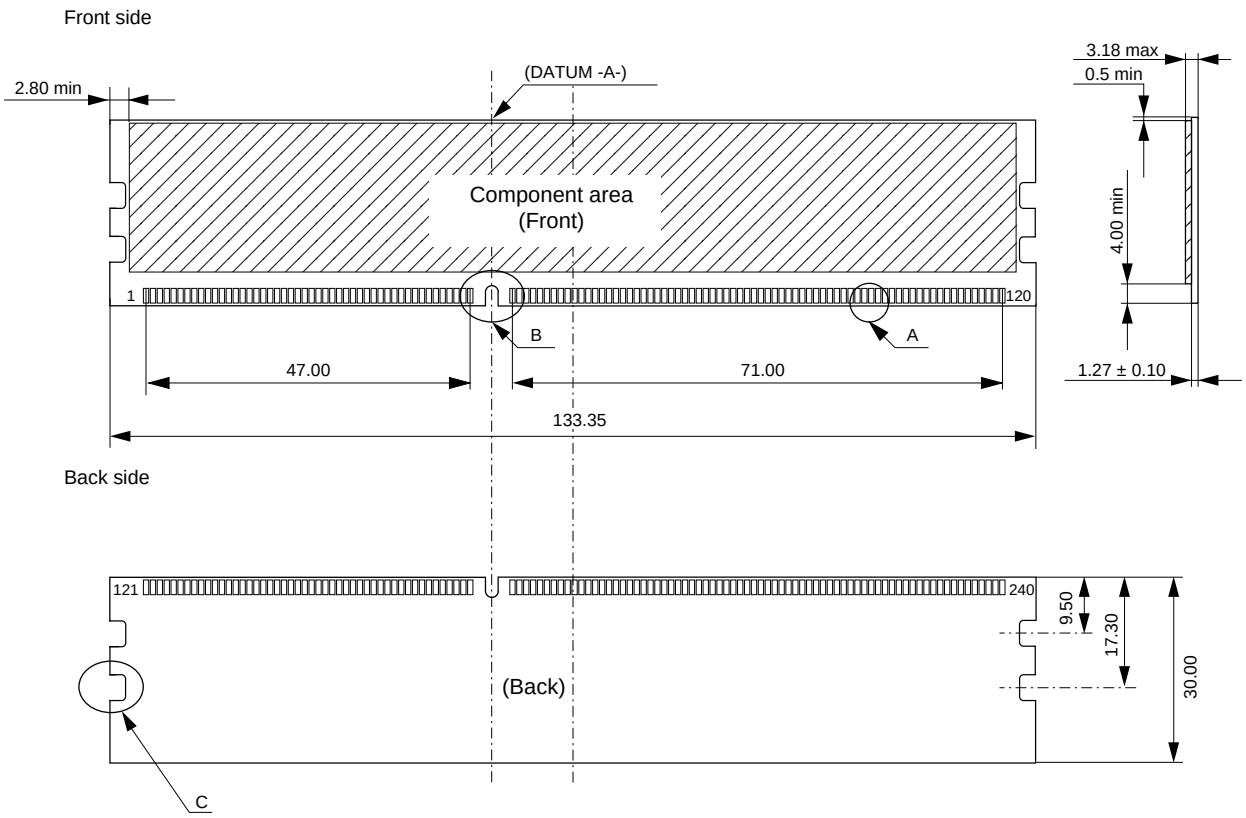
Temperature alert output.

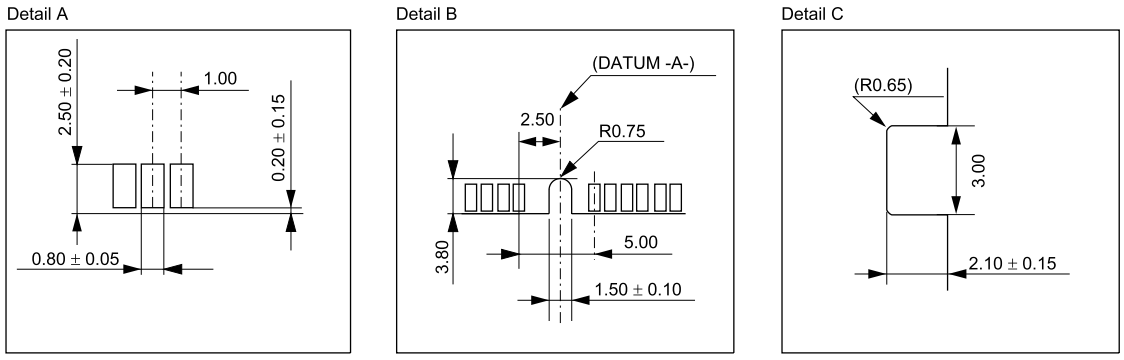
Detailed Operation Part, Electrical Characteristics and Timing Waveforms

Refer to the EDJ1108BABG, EDJ1116BABG datasheet (E1248E).

Physical Outline

Unit: mm





ECA-TS2-0193-03

CAUTION FOR HANDLING MEMORY MODULES

When handling or inserting memory modules, be sure not to touch any components on the modules, such as the memory ICs, chip capacitors and chip resistors. It is necessary to avoid undue mechanical stress on these components to prevent damaging them.
In particular, do not push module cover or drop the modules in order to protect from mechanical defects, which would be electrical defects.

When re-packing memory modules, be sure the modules are not touching each other.
Modules in contact with other modules may cause excessive mechanical stress, which may damage the modules.

MDE0202

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

CME0107

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[Usage environment]

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2) Usage in exposure to direct sunlight or the outdoors, or in dusty places.
3) Usage involving exposure to significant amounts of corrosive gas, including sea air, CL_2, H_2S, NH_3, SO_2, and NO_X.
4) Usage in environments with static electricity, or strong electromagnetic waves or radiation.
5) Usage in places where dew forms.
6) Usage in environments with mechanical vibration, impact, or stress.
7) Usage near heating elements, igniters, or flammable items.

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