FEATURES

- HIGH OUTPUT POWER CAPABILITY
- SINGLE SUPPLY (+7.5V to +24V)
- THD+N < 0.05% @ 1W, 8Ω
- HIGH EFFICIENCY, > 90% @ 4Ω, 20W
- LOW QUIESCENT CURRENT, 13mA
- LOW NOISE (190μV typ.)
- POP ELIMINATION AT STARTUP AND SHUTDOWN
- BUILT-IN THERMAL PROTECTION
- INTEGRATED SHORT CIRCUIT PROTECTION
- 180mΩ MOSFET SWITCHES
- MUTE / STANDBY MODE
- SMALL SMD PACKAGE IS BOTH LEAD-FREE (Pb) AND GREEN

APPLICATIONS

- TELEVISIONS
- HOME AUDIO MINI-SYSTEMS
- FLAT PANEL MONITORS
- MULTIMEDIA SPEAKERS
- SURROUND SOUND DVD SYSTEMS

1.0 GENERAL DESCRIPTION

The ATA-120 Class-D Audio Amplifier is a fully integrated monolithic audio amplifier that can provide audio power up to 20 watts @ 10% THD into a 4Ω speaker.

The ATA-120 incorporates a single ended output structure with built-in short circuit and overtemperature protection. This low noise, high performance device delivers the excellent audio quality of a class A/B amplifier while still achieving class-D efficiency greater than 90%.

ORDERING INFORMATION:

Part Number *	Package	Temperature
ATA-120	SOIC8	-40°C to + 85°C
EB-120	Evaluation Board for the ATA-120	

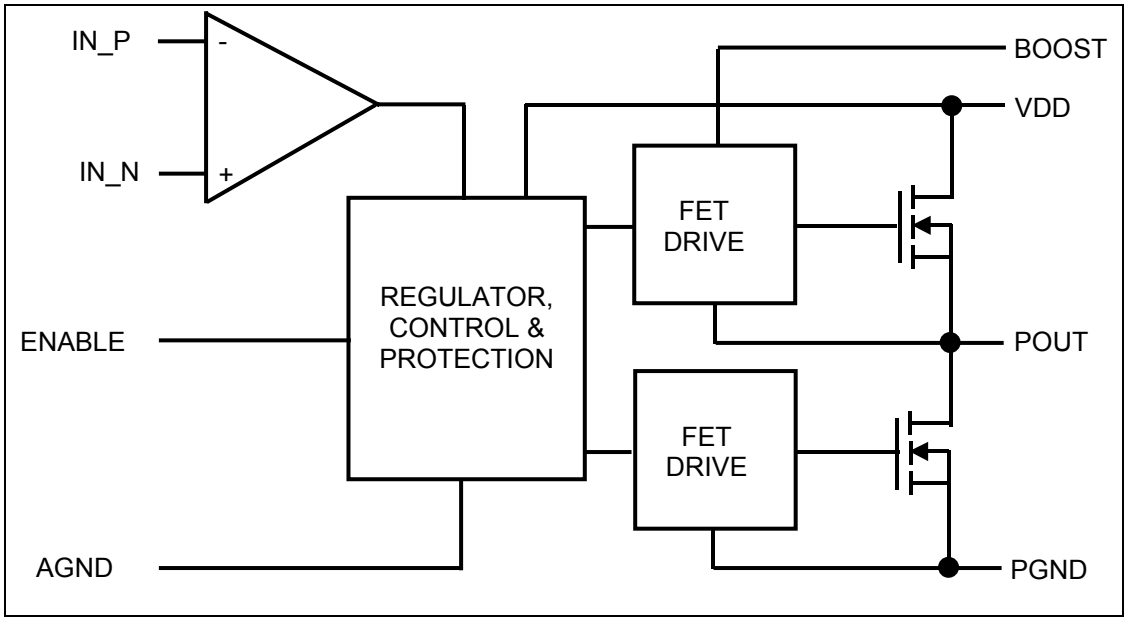


Figure 1 - Block Diagram

Absolute Maximum Ratings [Note 1]

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{DD}	Supply Voltage			26	V
V_{BOOST}	Bootstrap Voltage	V_{OUT}-0.3		V_{OUT}+6.5	V
V_{ENABLE}	Enable Voltage	-0.3		6.0	V
V_{OUT}	Output Switch	-1		VDD+1	V
V_{IN_P}	Positive Input	-1		VDD+1	V
V_{IN_N}	Negative Input	-1		VDD+1	V
-	Analog GND to Power GND	-0.3		0.3	V
T_j	Junction Temperature			150	°C
T_{LEADS}	Lead Temperature			260	°C
T_S	Storage Temperature	-65		150	°C

Note 1 – Operation above maximum ratings may damage the device.

1.1 Recommended Operating Conditions [Note 2]

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{DD}	Supply Voltage	7.5		24	V
T_A	Operating Temperature	-40		85	°C

Note 2 - Performance not guaranteed beyond recommended operating conditions.

1.2 Thermal Characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
θ_{J-A}	Thermal Resistance, Junction to Ambient		105		°C/W
θ_{J-C}	Thermal Resistance, Junction to Case [Note 3]		50		°C/W

Note 3 – Solder pins directly to large copper surface areas to improve device cooling.

1.3 Electrical Characteristics [Note 4]

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Supply Current						
I_{STBY}	Standby Current	V_{ENABLE} = 0		130		µA
I_Q	Quiescent Current			13		mA
Output Drivers						
R_{DS-ON}	Output MOSFET on Resistance	Sourcing and Sinking		0.18		Ω
I_{SC}	Short Circuit Current	Sourcing and Sinking	3	5		A
Inputs						
V_{IN}	IN_P, IN_N Input Common Mode Voltage Range		0	$\frac{VDD}{2}$	VDD-1.5	V
I_{IN}	IN_P, IN_N Input Current			1	5	µA
V_{ENABLE}	Enable Threshold Voltage	Rising signal voltage		1.4	2.0	V
		Falling signal voltage	0.4	1.2		
I_{ENABLE}	Enable Input Current	V_{ENABLE} = 5V		1		µA
Thermal Shutdown						
T_{SD}	Thermal Shutdown Trip Point	T_J Rising		150		°C
T_{SD-HYS}	Thermal Shutdown Hysteresis			30		°C

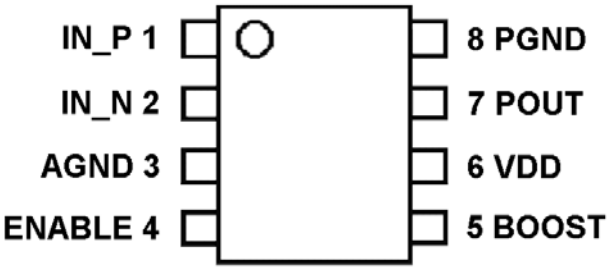
Note 4 – Performance based on circuit in Figure 3, V_{DD} = 24V, V_{ENABLE} = 5V, T_A = 25°C

1.4 Typical Operating Characteristics [Note 5]

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
P_{OUT}	Power Output	THD+N = 10%, 4Ω Load		20		W
		THD+N = 10%, 8Ω Load		10		W
THD+N	Total Harmonic Distortion Plus Noise	P_{OUT} = 1 W, 4Ω Load		0.1		%
		P_{OUT} = 1 W, 8Ω Load		0.05		%
η	Efficiency	P_{OUT} = 20 W, 4Ω Load		90		%
		P_{OUT} = 10 W, 8Ω Load		93		%
BW	Maximum Power Bandwidth			20		KHz
DNR	Dynamic Range	A-Weighted		91		dB
SNR	Signal to Noise Ratio	A-Weighted, relative to 15W		92		dB
	Noise Floor	A-Weighted		190		µV
PSR	Power Supply Rejection			47		dB

Note 5 – Performance based on circuit of Figure 3, V_{DD} = 24V, V_{ENABLE} = 5V, f = 1 KHz, T_A = 25°C

2.0 PIN DESCRIPTION



Pin No.	Pin Name	Pin Function
1	IN_P	**Amplifier Positive Input**. IN_P is the positive side of the differential input to the amplifier. Use a resistive voltage divider to set the voltage at IN_P to V_{DD}/2. See Figure 3.
2	IN_N	**Amplifier Negative Input**. IN_N is the negative side of the differential input to the amplifier. Drive the input signal and close the feedback loop at IN_N. See Figure 3.
3	AGND	**Analog Ground**. Signal input ground. Connect AGND to PGND at one single point.
4	ENABLE	**Enable Input**. Set ENABLE high to turn-on the amplifier; set it low to turn it off.
5	BOOST	**High-Side MOSFET Bootstrap Input**. A capacitor from BOOST to POUT supplies the gate drive current to the high-side of the MOSFET. Connect a 0.47µF capacitor from POUT to BOOST. Place a 6.2V zener diode from BOOST to POUT to prevent overstressing the internal circuitry.
6	VDD	**Power Supply Input**. VDD is the drain of the high-side MOSFET switch and supplies the power to both the output stage and the ATA-120 internal control circuitry. In addition to the main bulk capacitor, bypass VDD to PGND with a 1µF X7R capacitor placed close to the IC's V_{DD} (pin 6) and P_{GND} (pin 8).
7	POUT	**Switched Power Output**. POUT is the output of the ATA-120. Connect the L-C filter between POUT and the output blocking capacitor. See Figure 3.
8	PGND	**Power Ground**. Power stage ground. Connect PGND to AGND at one single point.

3.0 Functional Description

The ATA-120 is a single-ended Class-D audio amplifier that converts analog audio input signals into PWM pulses. The pulses drive an internal high current output stage and, when filtered through an external L-C filter, reproduce the input signal across the load. Because of the switching Class-D output stage, power dissipation in the amplifier is drastically reduced compared to Class A, Class B or Class A/B amplifiers while maintaining high fidelity and low distortion.

The amplifier uses a differential input to the modulator. IN_P is the positive input and IN_N is the negative input. The common mode voltage of the input is set to half the DC power supply input voltage ($V_{DD}/2$) through the resistive voltage divider formed by R2 and R5. The input capacitor C3 couples the AC input signal into the amplifier while blocking the DC component.

The output driver stage uses two 180 mΩ N-channel MOSFETs to deliver the pulses to the L-C output filter which in turn drives the load. When the output switches low, the bootstrap capacitor, C9, which is located between POUT and BOOST, is charged from VDD through internal circuitry inside the ATA-120. The gate of the upper MOSFET is driven from this voltage (higher than VDD but clamped to safe levels by zener diode D2).

3.1 Pop Elimination

The DC-blocking capacitor, C38, allows only AC current to pass to the output load (speaker). To insure that the amplifier properly passes low frequency signals, the time constant of $C38*R_{LOAD}$ needs to be long. Typically the C11 capacitor charges over a long time period and would normally result in turn-on and/or turn-off “pops”. The ATA-120, however, includes internal circuitry that eliminates the turn-on and turn-off pops associated with this charging of the AC coupling capacitor.

3.2 Short Circuit/Overload Protection

The ATA-120 has internal overload and short circuit protection. The currents in both the high-side and low-side MOSFETs are internally measured and if the current exceeds the 5A (typical) short circuit current limit on either MOSFET, both MOSFETs are placed in an open condition. After the short circuit condition is removed, the ATA-120 restarts with the same power up sequence that is used for normal starting to prevent a pop from occurring.

3.3 Mute/Enable Function

The ENABLE input is an active high enable control. To enable the device, drive ENABLE with a 2.0V or greater voltage. To disable the amplifier, drive it below 0.4V. While the device is disabled, the VDD operating current is less than 130µA and the output MOSFETs are turned off. The ATA-120 requires approximately 500ms from the time that ENABLE is asserted (driven high) to when the amplifier arrives at normal operation.

4.0 Power Output

Figure 2 shows the full-scale sine-wave output power as a function of Power Supply Voltage for 2, 3, 4, 6, and 8 Ohm loads. Output power is constrained for higher impedance loads by the maximum voltage limit of the ATA-120 and by the over-current protection limit for lower impedance loads. The minimum threshold for the over-current protection circuit is 3.0A (at 25 ºC) but the typical threshold is 5.0A. Solid lines depict typical output power capability of the ATA-120. Dashed lines depict the output power capability constrained to the minimum current specification of for the ATA-120. The output power curves assume proper thermal management of the power device's internal dissipation. Since The IC's thermal path is predominantly through the leadframe to the PC Board copper foil, a sufficient copper area must be connected to each lead in order to facilitate proper cooling.

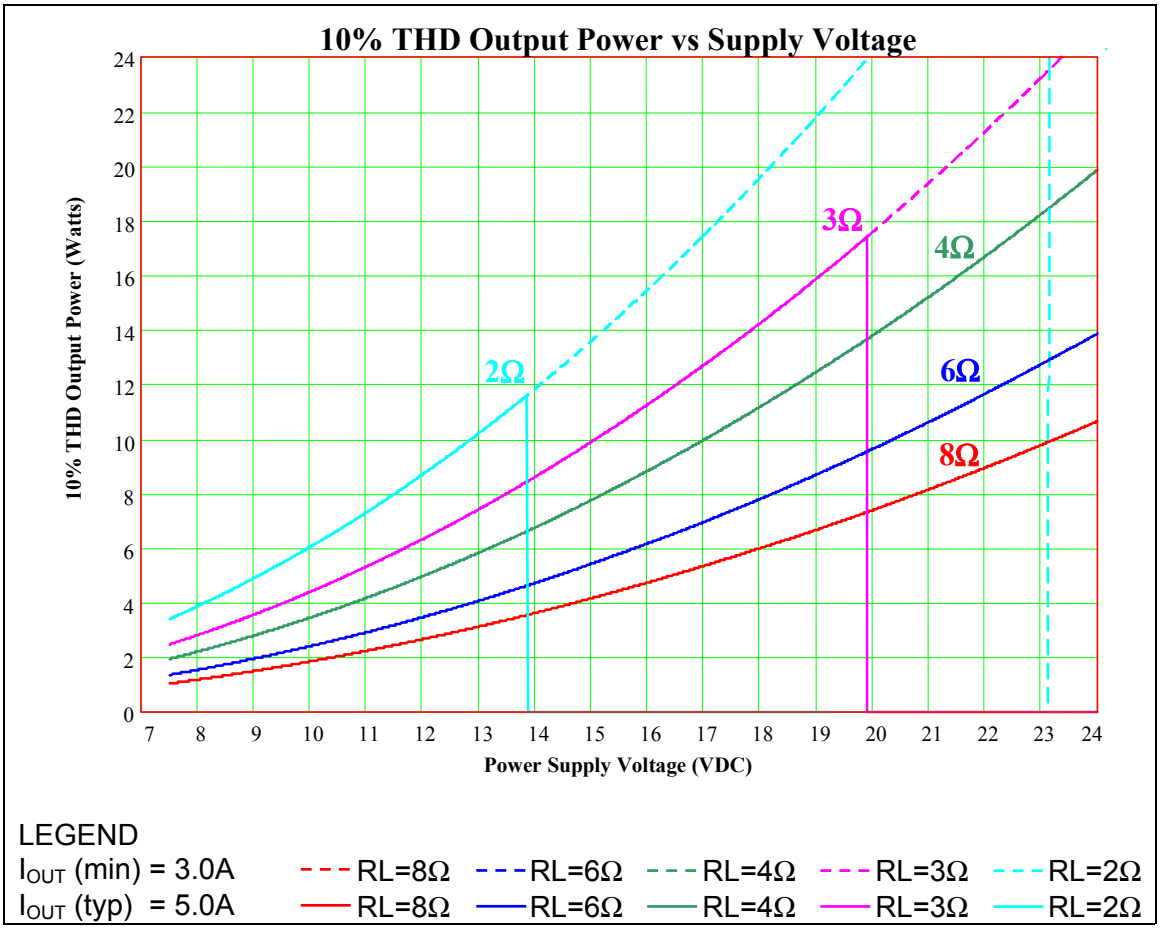


Figure 2 – 10% THD Power Output vs. Power Supply Voltage

Note 6 : Sine-wave output power (<1% THD) is approximately 23% Lower.

5.0 Application Information

The ATA-120 uses a minimum number of external components to complete a Class-D audio amplifier. The application circuit of Figure 3 matches the component identifiers used in this section. It is optimized for both a 24V power supply and a 1.5V RMS maximum input signal and should be suitable for most applications. If this circuit does not correspond to the requirements of the required application, the following sections show how to customize the amplifier circuitry.

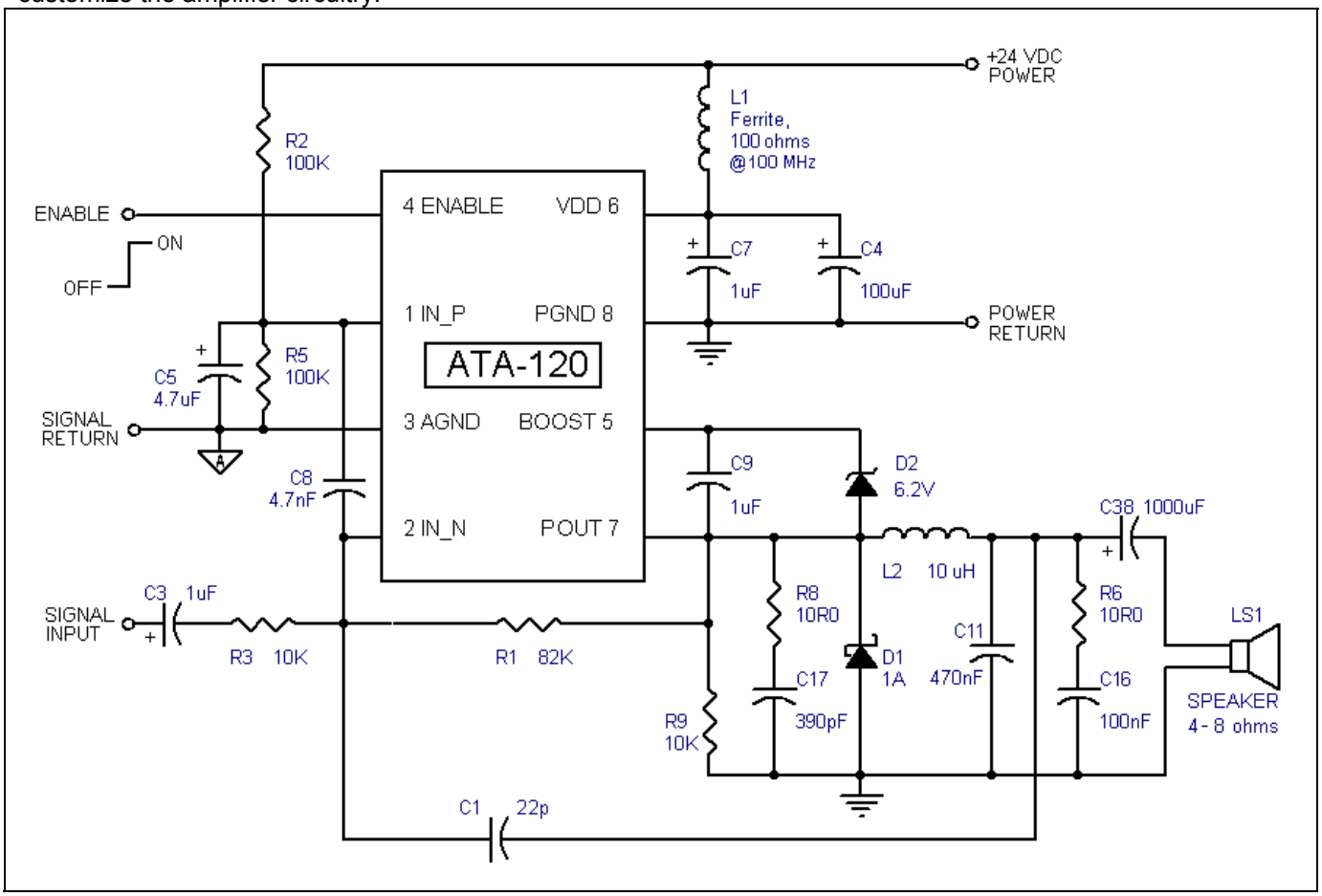


Figure 3 - Typical 20W Audio Amplifier Circuit

5.1 Setting the Voltage Gain

The amplifier voltage gain is set by the combination of R1 and R3. The voltage gain sets the output voltage power for a given input signal voltage and is set by the following equation:

$$A_V = -\frac{R_1}{R_3}$$ *Equation 1*

The maximum output voltage is limited by the power supply. To achieve the maximum power out of the ATA-120 amplifier, set the gain such that the maximum AC input signal results in the maximum output voltage swing.

The maximum output voltage swing is $\pm V_{DD}/2$. For a given input signal voltage, where $V_{IN}(pk)$ is the peak input voltage, the maximum voltage gain is

$$A_{V(\max)} = \frac{V_{DD}}{2 \times V_{IN(pk)}} \qquad \textit{Equation 2}$$

This voltage gain setting results in the peak output voltage approaching it's maximum for the maximum input signal. In some cases the amplifier may be required to overdrive slightly, allowing the THD to increase at high power levels, and thus a higher gain than $A_{V\,(max)}$ may be required.

5.2 Setting the Switching Frequency

The zero-signal switching frequency is a function of V_{DD}, the capacitor C_8 and the feedback resistor R_1. Lower switching frequencies result in more inductor ripple, causing more quiescent output voltage ripple, increasing the output noise and distortion. Higher switching frequencies result in more power loss. The optimum frequency is between 600-700 kHz. Use the following steps, along with Figure 4, to select the appropriate timing capacitor, C_{INT} that will result in a recommended operating frequency of approximately 700 kHz:

1. Choose the Power supply voltage (V_{DD}) based on output power requirements and the selected speaker impedance.
2. Determine the voltage gain required to drive the amplifier to full output power.

$$\text{Gain} = \frac{V_{DD}}{2 \times V_{IN\text{-}RMS} \times \sqrt{2}} \qquad \textit{Equation 3}$$

3. The intersection of the V_{DD} and Gain lines in Figure 4 will determine the C_{INT} capacitor value.
4. Set the value of R_1 to the required gain times R_3 (fixed at 10KΩ).

5.2.1 EXAMPLE 1:

The reference design of Figure 3 uses a 1.0 V_{RMS} input signal to drive a 4Ω speaker to 15 watts of sine wave output (~20 watts @ 10% THD) using a 24 VDC power supply.

5. Select 24 V on the V_{DD} scale (red line).
6. The required gain is:

$$\text{Gain} = \frac{24V}{2 \times V_{IN} \times \sqrt{2}} = 8.5\ \text{V/V} \qquad \textit{Equation 4}$$

3. Since we used a more common 82KΩ feedback resistor in the design, we'll follow the 8.2 V/V line (red line) across on the gain scale in the graph.
   Find where it intersects the voltage line.
   Choose the closest capacitor line, C_{INT} = 4.7 nF.
4. Multiply the voltage gain (not 8.5 but 8.2 based on the pre-selected resistor) by R3 (fixed at 10KΩ) to get the proper value of the R_1 gain-setting resistor, 82K.

5.2.2 EXAMPLE 2:

A design with a 0.5 VRMS input signal is required to drive a 2Ω speaker to 9 watts of sine wave output (12 watts @ 10% THD) using a 14 VDC power supply.

1. Select 14 V on the V_{DD} scale (blue line).
2. The required gain is:

$$\text{Gain} = \frac{14V}{2 \times V_{IN} \times \sqrt{2}} = 9.9\ \text{V/V}\,. \qquad \textit{Equation 5}$$

3. Follow this value (blue line) across on the gain scale in the graph.
   Find where it intersects the voltage line.
   Choose the closest capacitor line, C_{INT} = 1.8 nF.

4. Multiply the voltage gain (9.9) by R3 (fixed at 10KΩ) to get the value of the R_1 gain-setting resistor, 99K.

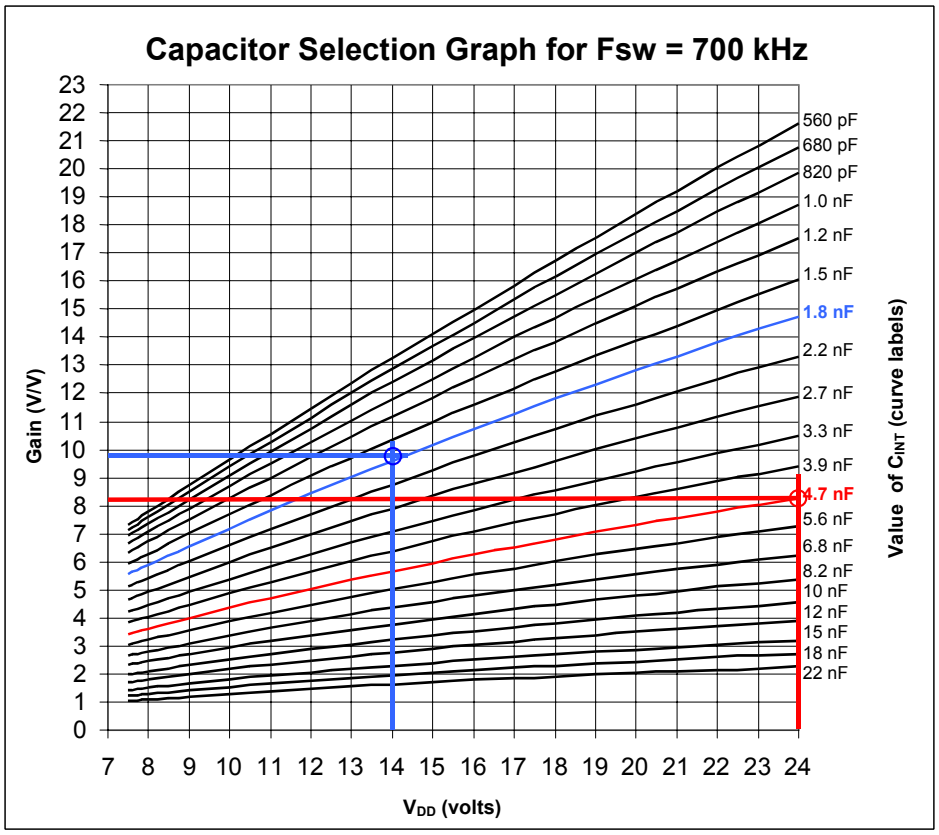


Figure 4 – Determining the Timing Capacitor, C_{INT}

5.3 Choosing the output L-C Filter

The Inductor-Capacitor (L-C) filter converts the pulse train at POUT to the output voltage that drives the speaker. The characteristic frequency of the L-C filter (f_0) needs to be high enough to allow high frequency audio to pass to the output, yet low enough to filter out high frequency products of the pulses from POUT. The characteristic frequency of the L-C filter is:

$$f_0 = \frac{1}{2\pi\sqrt{L2 \times C11}}$$ *Equation 6*

For the circuit of Figure 3, typical values for the L-C filter are 10µH for the inductor (L2) and 470nF for the capacitor (C11) resulting in a characteristic frequency of 73 kHz.

The voltage ripple at the output is approximated by the equation:

$$V_{RIPPLE} \approx V_{DD} \times \left[\frac{f_0}{f_{sw}}\right]$$ *Equation 7*

The quality factor (Q) of the L-C filter is important. If this is too low, passband frequency may be rolled off, if this is too high, then peaking may occur at high signal frequencies reducing the passband flatness. The circuit Q is set by the speaker load resistance (typically 4Ω or 8Ω) and both the L and C as illustrated by the following equation:

$$Q = \frac{R_{LOAD}}{2 \times \pi \times f_0 \times L2} = R_{LOAD} \times \sqrt{\frac{C11}{L2}}$$ *Equation 8*

where f_0 is the characteristic frequency in Hz. The use of an L-C filter with a Q between 0.7 and 1 gives the smoothest performance.

The actual output ripple and noise is affected by the type of inductor and capacitor used in the L-C filter. Use a film capacitor for C11 and an inductor for L2 with sufficient power handling capability to supply the output current to the load. The inductor should exhibit soft saturation characteristics. If the inductor exhibits hard saturation, it should operate well below the saturation current. Gapped ferrite, MPP, Powdered Iron, or similar type toroidal cores are recommended. If open or shielded bobbin ferrite cores are used for multi-channel designs, make sure that the start windings of each inductor line up (all starts going toward POUT pin, or all starts going toward the output) to prevent crosstalk or other channel-to-channel interference.

5.4 Output Coupling Capacitor

The combination of the coupling capacitor, C38, and the load resistance results in a first-order high-pass filter. The capacitor, C38, serves to block DC voltages and thus passes only the amplified AC signal from the L-C filter to the load. The value of C38 should be selected such that the output corner frequency (f_{OUT}) is at or below the lowest required audio frequency. The output corner frequency, f_{OUT}, (-3dB point) can be approximated as:

$$f_{OUT} = \frac{1}{2 \times \pi \times R_{LOAD} \times C38}$$ *Equation 9*

The output coupling capacitor carries the full load current, so a low ESR capacitor type should be chosen such that its ripple current rating is greater than the maximum AC load current. Low ESR aluminum electrolytic capacitors are recommended.

5.5 Input Coupling Capacitor

The input coupling capacitor, C3, is used to pass only the AC signal at the input. In a typical system application, the source input signal is typically centered around the circuit ground, while the ATA-120 input is at half the power supply voltage ($V_{DD}/2$). The input coupling capacitor transmits the AC signal from the source to the ATA-120 while blocking the DC voltage. Choose an input coupling capacitor such that the corner frequency (f_{IN}) is less than the passband frequency. The corner frequency is:

$$f_{IN} = \frac{1}{2 \times \pi \times R3 \times C3}$$ *Equation 10*

5.6 Power Source

For maximum output power, the amplifier circuit requires a regulated external power source to supply the power to the amplifier. The higher the power supply voltage, the more power can be delivered to a given load resistance. However, if the power source voltage exceeds the maximum operating voltage of 26V, the ATA-120 could sustain damage. The power supply rejection of the ATA-120 is good, however noise at the power supply can get to the output, so care must be taken to minimize power supply noise within the pass-band frequencies. Bypass the power supply with a large capacitor (typically aluminum electrolytic) along with a smaller 1µF ceramic capacitor at the ATA-120 V_{DD} supply pins.

5.7 Circuit Layout

The circuit layout is critical for optimum performance and low output distortion and noise. Place the following components as close to the ATA-120 as possible:

Power supply bypass, C7. C7 carries the transient current for the switching input stage. To prevent overstressing of the ATA-120 and excessive noise at the output, place the power supply bypass capacitor as close to pins 6 (VDD) and 8 (PGND) as possible.

Output Catch Diode, D1. D1 caries the current over the dead-time while both MOSFET switches are off. Place D1 between pins 7 (POUT) and 8 (PGND) to prevent the voltage at POUT from swinging excessively below ground.

Input Modulator Capacitor, C8. C8 is used to set the amplifier switching frequency and is typically on the order of a few nanofarads. Place C8 as close to the differential input pins (1 and 2) as possible to reduce distortion and noise.

Reference Bypass Capacitor C5. C5 filters the ½ V_{DD} reference voltage at the IN_P input (pin 1). Place C5 as close to IN_P as possible to improve power supply rejection and reduce distortion and noise at the output.

Use two separate ground planes, analog ground (AGND) and power ground (PGND), and connect the 2 grounds together at a single point to prevent noise injection into the amplifier input to reduce distortion. Power components (C4, C7, C9 and D1 and the speaker return) connect to the power ground. The front-end analog components (C5, R5, and the input signal ground) connect to the analog ground.

Place the input and feedback resistors R3 and R1 as close to the IN_N input as possible. Make sure that any traces carrying the switching node (POUT) voltage are separated far from any input signal traces. If multiple amplifiers are used on a single board, make sure that each channel is physically separated to prevent crosstalk. If it is required to run the POUT trace near the input, shield the input with a ground plane between the traces. Make sure that all inductors used on a single circuit board have the same orientation.

If multiple channels are used on a single board, make sure that the power supply is routed from the source to each channel individually, not serially. This prevents channel-to-channel coupling through the power supply input.

5.8 Electro-Magnetic Interference (EMI) Considerations

Due to the switching nature of the Class-D amplifier, care must be taken to minimize the effects of electromagnetic interference from the amplifier. However, with proper component selection and careful attention to circuit layout, the effects of the EMI due to the amplifier switching can be minimized.

The power inductors are a potential source of radiated emissions. For the best EMI performance, use toroidal inductors, since the magnetic field is well contained inside the core. However toroidal inductors can be expensive to wind. For a more economical solution, use shielded gapped ferrite or shielded ferrite bobbin core inductors. These inductors typically do not contain the field as well toroidal inductors, but usually can achieve a better balance of good EMI performance with low cost.

The size of high-current loops that carry rapidly changing currents needs to be minimized. To do this, make sure that the V_{DD} bypass capacitor (C7) is as close to the ATA-120 as possible.

Nodes that carry rapidly changing voltage, such as POUT, need to be made as small as possible. If sensitive traces run near a trace connected to POUT, place a ground shield between the traces.

6.0 Performance Measurements

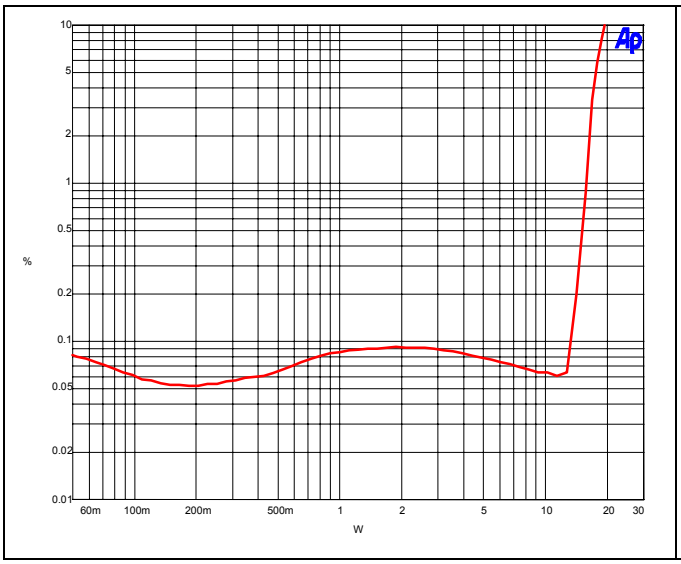


Figure 5 - THD+N vs. P_{OUT} @ 4Ω (1kHz)

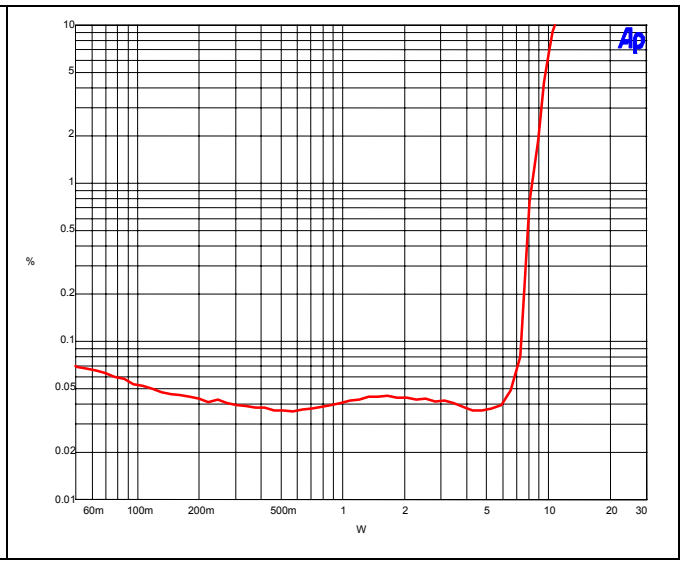


Figure 6 – THD+N vs. P_{OUT} @ 8Ω (1kHz)

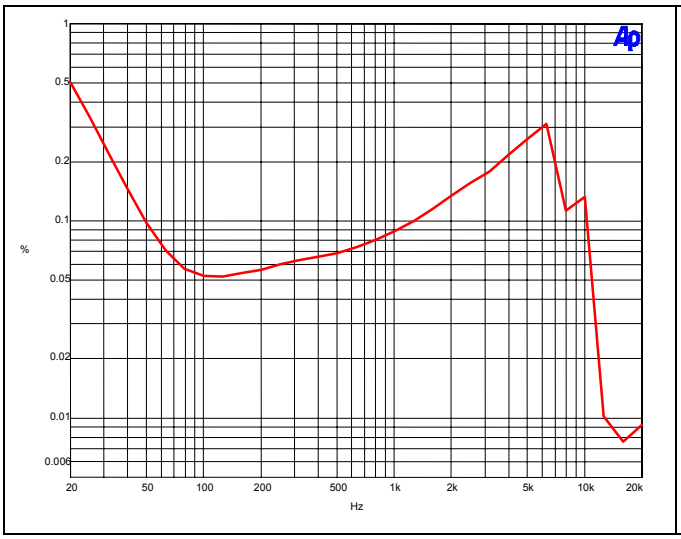


Figure 7 – THD+N vs. Frequency @ 4Ω (1W)

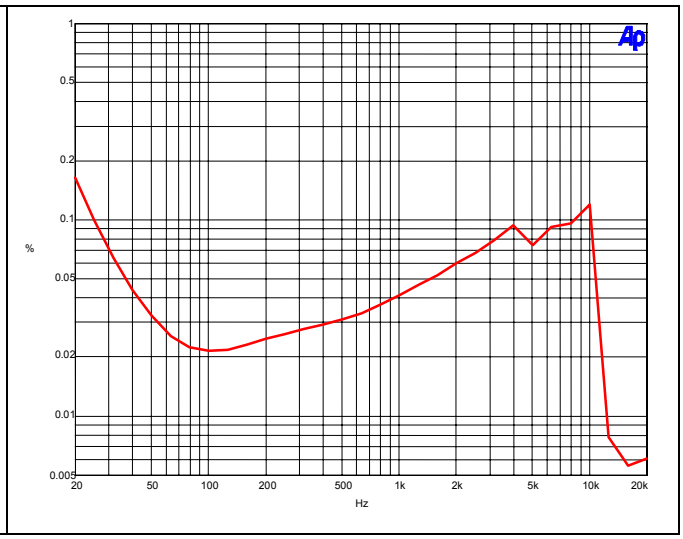


Figure 8 - THD+N vs. Frequency @ 8Ω (1W)

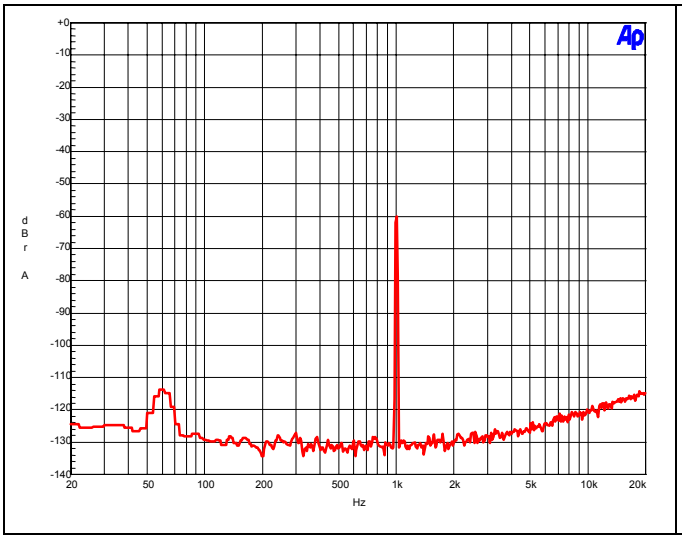


Figure 9 – FFT Noise Floor 190µV (A-weighted, Typical, A_V = 8.2)

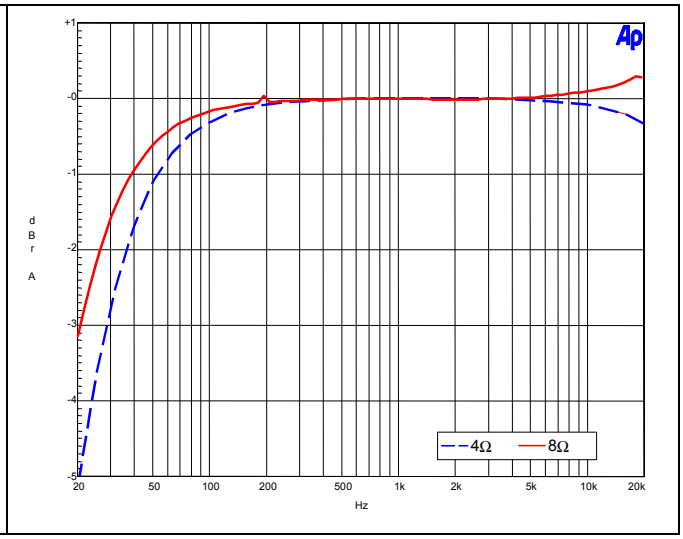


Figure 10 – Frequency Response using 2200uF coupling capacitor, (A_V = 8.2, Ref = 2 Vrms, Dotted (Blue)=4Ω, Solid (Red)=8Ω)

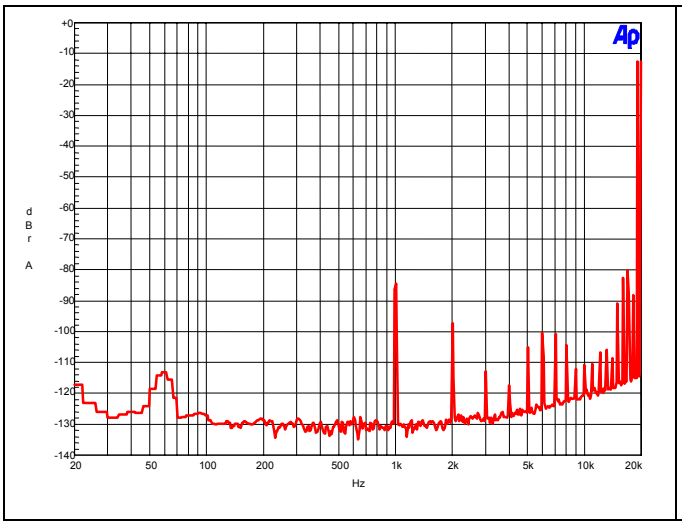


Figure 11 – IHF-IMD (1W)

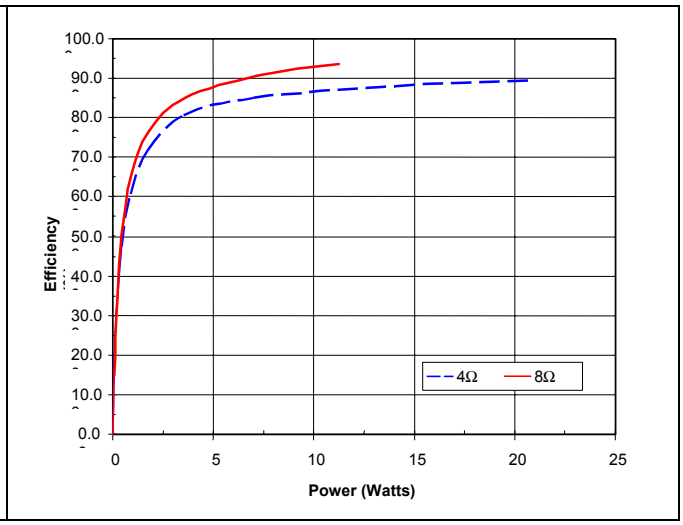
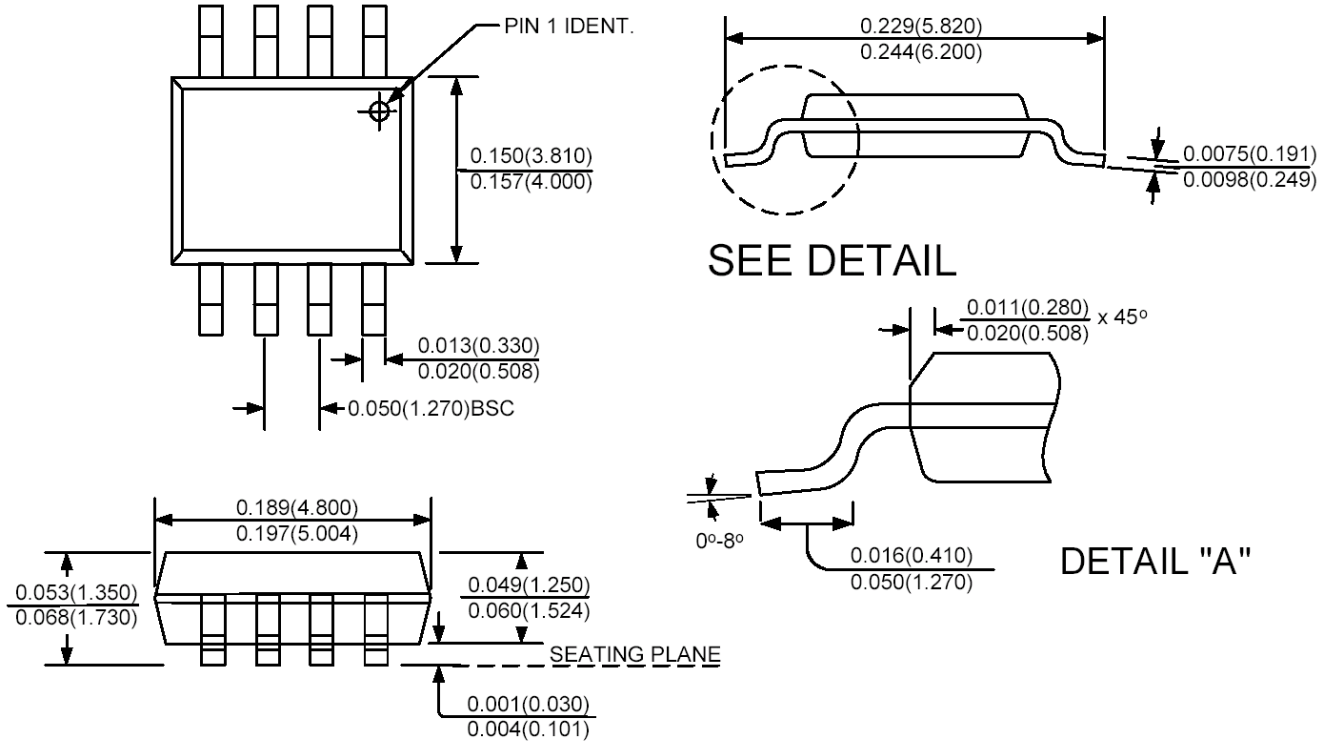


Figure 12 – Efficiency vs P_{OUT}

PACKAGE OUTLINE

SOIC8



Note: Dimensions are in inches (mm).

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