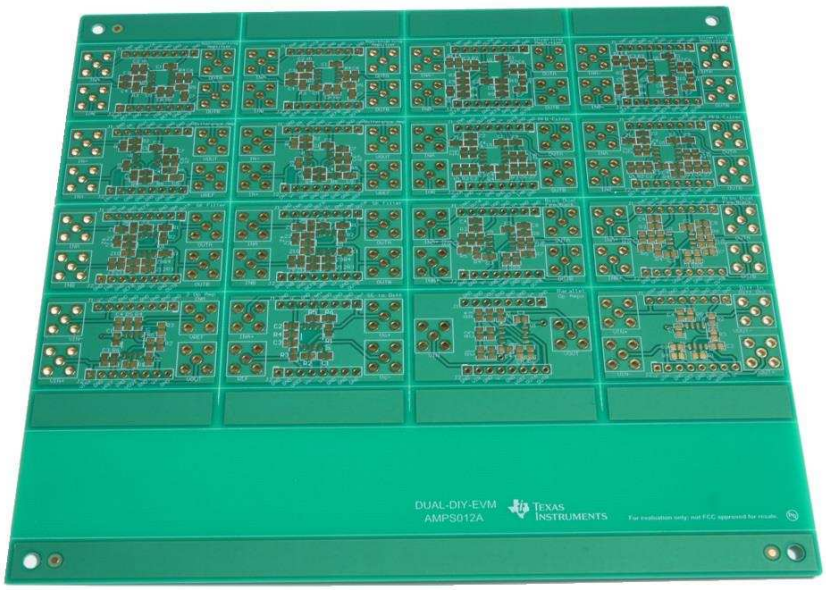
DUAL-DIYAMP-EVM



This user's guide contains support documentation for the DUAL-DIYAMP Evaluation Module (EVM). Included is a description of how to set up and configure the EVM, printed circuit board (PCB) layout, schematic, and bill of materials (BOM) of the DUAL-DIYAMP-EVM.

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1 Introduction

The DUAL-DIYAMP-EVM is an EVM developed for dual package op amps to give users the ability to easily evaluate amplifier circuits. This “break apart” EVM has several popular op-amp configurations including amplifiers, filters, stability compensation, and other signal conditioning circuits that require two amplifiers. The EVM is designed for 0805 and 0603 package size surface mount components enabling easy prototyping. This board gives the user the ability to build anything from a simple amplifier to complex signal chains by combining different configurations.

1.1 DUAL-DIYAMP-EVM Kit Contents

Table 1 details the contents included in the DUAL-DIYAMP-EVM kit.

Table 1. DUAL-DIYAMP-EVM Kit Contents

Item	Description	Quantity
DUAL-DIYAMP-EVM	PCB	1
Header Strip	100-mil (2.54 mm) spacing, 32 position, through hole	2

1.2 Features

The EVM has the following features:

- Multiple circuit configurations
- Breadboard compatible
- Schematic provided in silk screen on the PCB
- Multiple connector options for the input and output connections: SMA, test point, and wires.

1.3 List of Circuits on EVM

The EVM has the following circuits:

- Non-inverting amplifier
- Inverting amplifier
- Difference amplifier with reference buffer
- Multiple feedback active filter
- Sallen-Key filter
- Riso with dual feedback
- Two op amp instrumentation amplifier
- Single-ended input to differential output
- Parallel op amps
- Differential input to differential output

2 Hardware Setup

Assembly of the DUAL-DIYAMP-EVM involves identifying and breaking out the desired circuit configuration from the EVM, soldering the components, header strip, and input and output connections. This section presents the details of these procedures.

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2.1 EVM Circuit Locations

Figure 1 and Table 2 map the location of each circuit configuration on the EVM. Figure 1 labels each circuit configuration with a letter ranging from A to J. Table 2 matches the circuit configuration to a letter in Figure 1 and also provides the name of each individual circuit written in silk screen on the EVM.

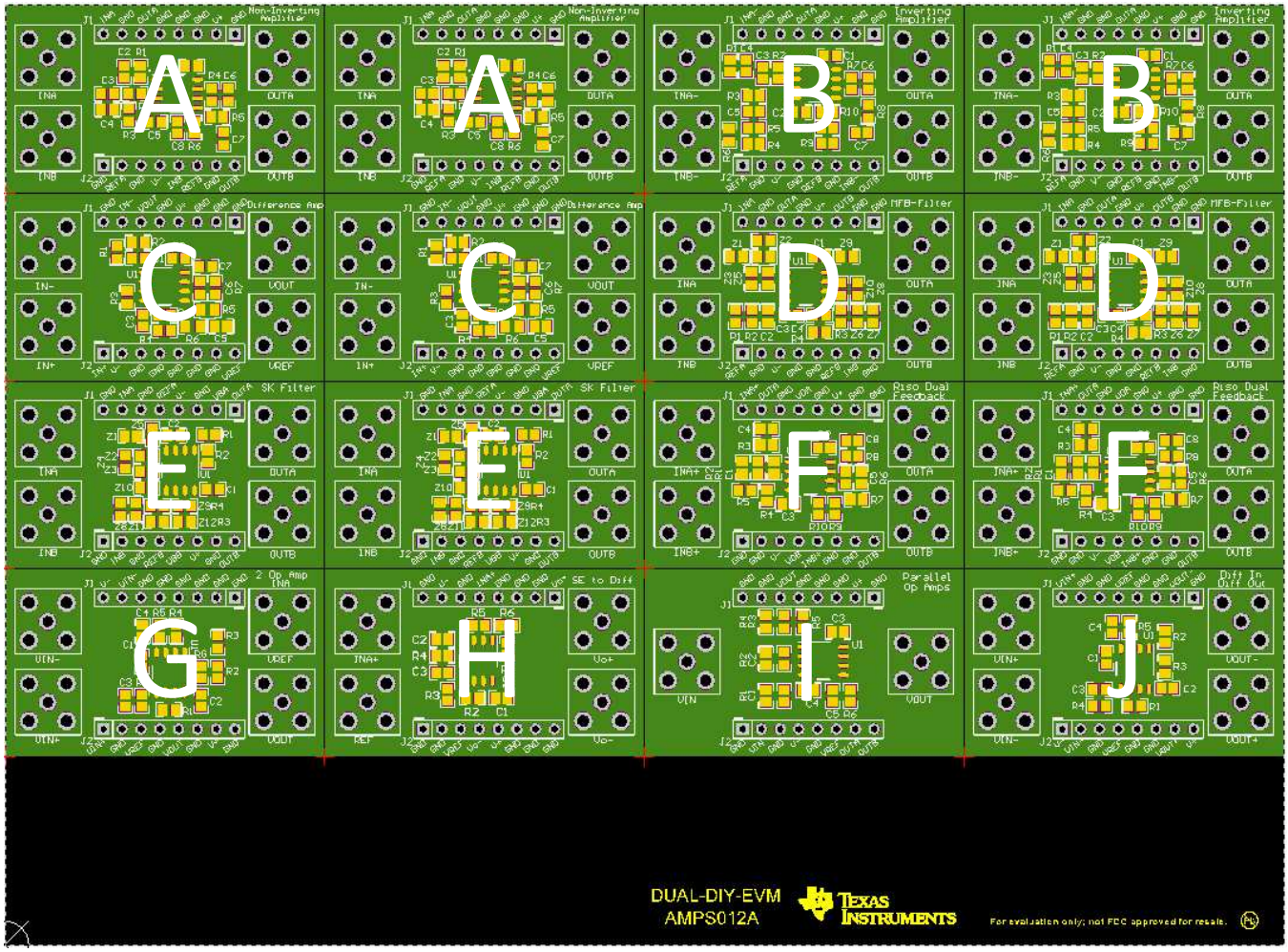


Figure 1. Circuit Configuration Location

Table 2. Circuit Configuration Location Legend

Circuit Name	Silk Screen Label	Letter in Figure 1
Non-inverting amplifier	Non-inverting Amplifier	A
Inverting amplifier	Inverting Amplifier	B
Difference amplifier with reference buffer	Difference Amp	C
Multiple feedback filter	MFB - Filter	D
Sallen-Key filter	SK Filter	E
Riso with dual feedback	Riso Dual Feedback	F
Two op amp instrumentation amplifier	2 Op Amp INA	G
Single-ended input to differential output	SE to Diff	H
Parallel op amps	Parallel Op Amps	I
Differential input to differential output	Diff In Diff Out	J

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2.2 EVM Assembly Instructions

This section has step-by-step instructions on how to assemble a circuit configuration from the EVM.

1. Choose the desired circuit configuration. See Section 2.1 for the location of each circuit configuration.
2. Gently flex the PCB panel at the score lines to separate the desired circuit configuration from the EVM.

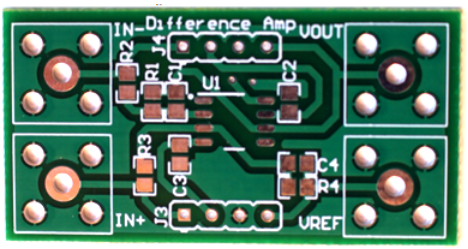


Figure 2. Detach Desired Circuit Configuration

3. Solder device and surface mount passive components to the separated PCB.

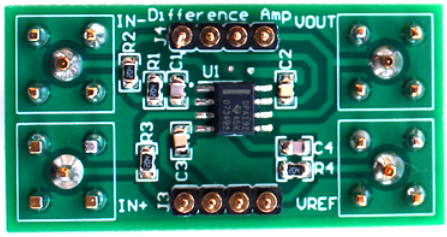


Figure 3. Detach Configuration With Attached IC and Passive Components

4. Use long-nose pliers to break header strips, provided in the EVM kit, into 8-position lengths.

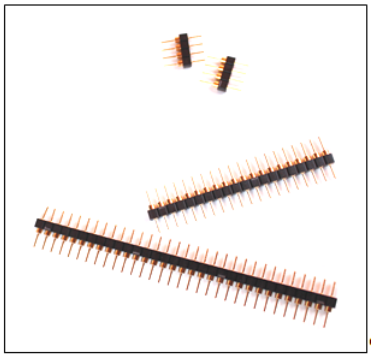


Figure 4. Terminal Strip (TS-132-G-AA) Broken Into 4-Pin Lengths

5. Insert header strips into a spare DIP socket as shown in Figure 5.

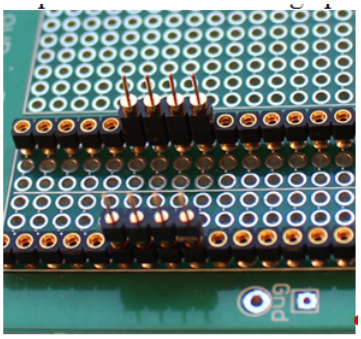


Figure 5. 4-Pin Length Terminal Strips Inserted in DIP Socket

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6. Position separated PCB over pins and solder the connections. Carefully remove from the DIP socket.

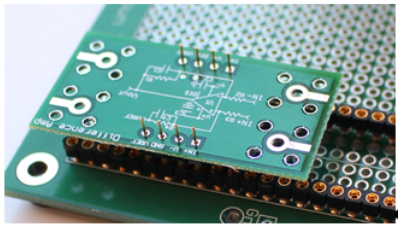


Figure 6. Detached Board Configuration Position Over Terminal Pins

7. Attach SMA connectors, test points, or wires to the inputs and outputs of the separated PCB.

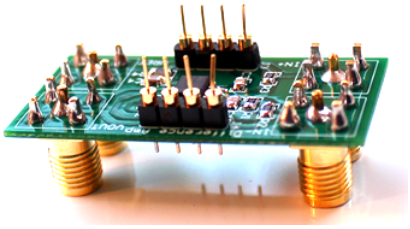


Figure 7. Fully-Assembled Circuit Configuration From DIYAMP-SOIC-EVM

3 Schematic and PCB Layout

This section provides the schematic and PCB layout of each circuit configuration provided on the EVM.

3.1 Schematic PCB Drawing

Each circuit board has the schematic of the circuit in silk screen located on the back of the PCB for easy reference. Figure 8 displays an example of a schematic on the back of the PCB.

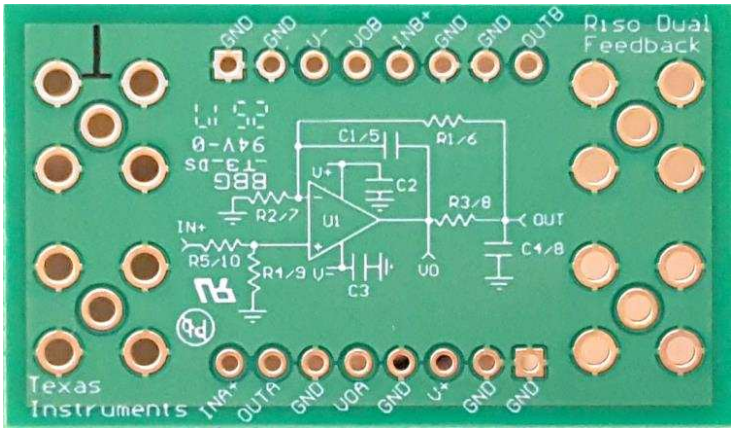


Figure 8. Silk Screen Schematic

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3.2 Non-Inverting Amplifier

Figure 9 displays the schematic for the non-inverting amplifier circuit configuration.

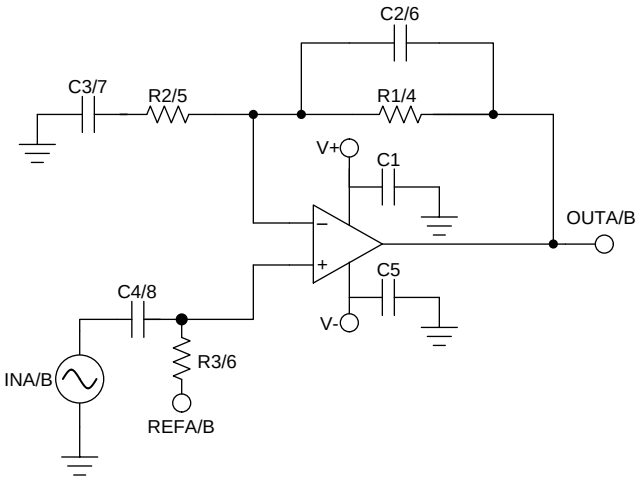


Figure 9. Non-Inverting Amplifier Schematic

The non-inverting amplifier circuit configuration takes an input signal that is applied directly to the high impedance non-inverting input and outputs a signal that is the same polarity as the input signal. The feedback network for this topology is R1, R2, C2, and C3 for channel A and R4, R5, C6, and C7 for channel B.

There are multiple ways to configure the non-inverting amplifier circuit configuration. The following cases show the two primary use-case configurations for this circuit.

Case 1: Standard non-inverting circuit

This circuit can be configured into a standard non-inverting circuit by shorting C4/8 and C3/7 with a 0-Ω resistor and leaving R3/6 unpopulated.

Equation 1 displays the transfer function of the non-inverting amplifier circuit configuration shown in Figure 9.

$$\text{OUTA / B} = \left(1 + \frac{R_{1/4}}{R_{2/5}}\right)\text{INA / B} \quad (1)$$

where

- $C_{4/8}$ is shorted with a 0-Ω resistor
- $C_{3/7}$ is shorted with a 0-Ω resistor
- $R_{3/6}$ is unpopulated

Capacitor C2 for channel A and C6 for channel B provide the option to filter the output. The cutoff frequency of the filter can be calculated using Equation 2.

$$f_c = \frac{1}{2 \times \pi \times R_{1/4} \times C_{2/6}} \quad (2)$$

Case 2: AC-coupled, non-inverting amplifier configuration

This circuit board can be configured as an ac-coupled, non-inverting circuit by populating C4/8 and C3/7 with capacitors and populating R3/6 with resistors. Test points REFA for channel A and REFB for channel B are used to set the dc biasing of the circuit. The dc bias voltage is typically set to one half of the supply voltage of the amplifier.

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Populating C4/8 with capacitors ac couples the input of the circuit. The corner frequency of the high-pass filter created by C4/8 and R3/6 is calculated in Equation 3:

$$f_c = \frac{1}{2 \times \pi \times C_{4/8} \times R_{3/6}} \quad (3)$$

Similarly, capacitor C3/7 creates a high-pass filter with R2/5. The corner frequency of the high-pass filter created by C3/7 and R2/5 is calculated in Equation 4.

$$f_c = \frac{1}{2 \times \pi \times C_{3/7} \times R_{2/5}} \quad (4)$$

Figure 10 displays the PCB layout of the top layer of the non-inverting amplifier circuit configuration.

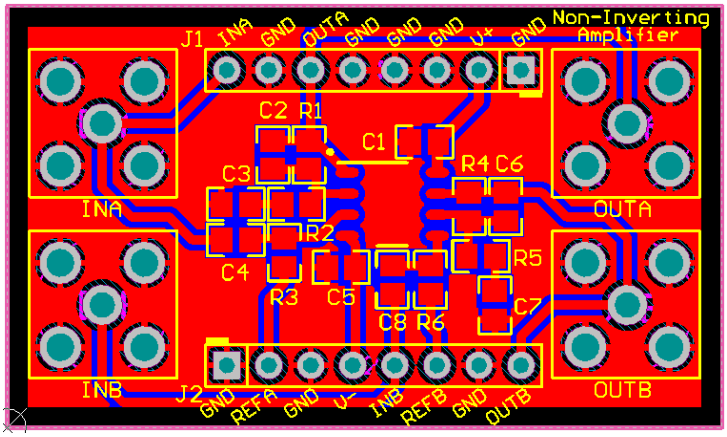


Figure 10. Non-Inverting Amplifier Top Layer PCB Layout

3.3 Inverting Amplifier

Figure 11 shows the schematic for the inverting amplifier circuit configuration.

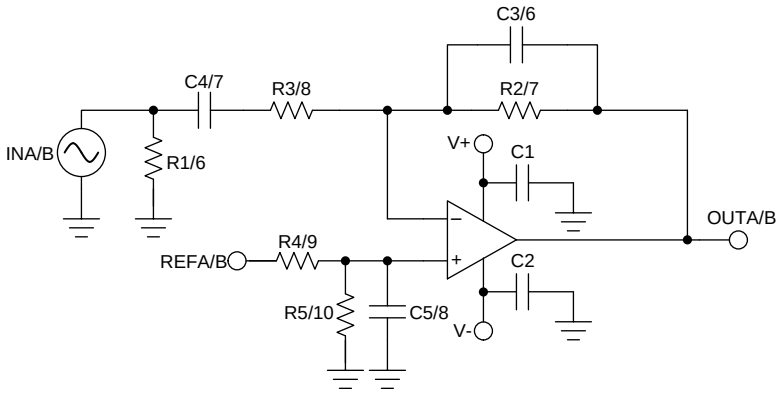


Figure 11. Inverting Amplifier Schematic

The inverting amplifier configuration takes an input signal and outputs a signal that is the opposite polarity as the input signal. The benefit of this topology is that it avoids common mode limitations. The ratio of the resistors in the feedback network will determine the amount of gain the input signal will be amplified by.

The inverting amplifier circuit configuration provides the option to ac couple the input, filter the output, and bias the output of the amplifier to a desired value.

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Equation 5 displays the dc transfer function of the inverting amplifier circuit configuration.

$$OUTA/B = \left(-\frac{R_{2/7}}{R_{3/8}}\right)INA/B + \left(\frac{R_{5/10}}{R_{4/9}+R_{5/10}}\right)\left(1+\frac{R_{2/7}}{R_{3/8}}\right)REFA/B$$

where

- $C_{4/7}$ is shorted with a 0-Ω resistor (5)

Capacitor C4 for channel A and C7 for channel B provide the option to ac couple the input of the circuit. Equation 6 displays the dc transfer function of the ac-coupled inverting amplifier circuit configuration.

$$OUTA/B = \left(\frac{R_{5/10}}{R_{4/9}+R_{5/10}}\right)REFA/B$$

where

- The input is ac coupled with $C_{4/7}$ (6)

Equation 7 calculates the cut-off frequency of the high-pass filter.

$$f_{c_highpass} = \frac{1}{2\times\pi\times C_{4/7}\times R_{3/8}} \quad (7)$$

Capacitors C3 and C6 provide the option to filter the output. Equation 8 calculates the cut-off frequency of the filter.

$$f_{c_OUT} = \frac{1}{2\times\pi\times C_{3/6}\times R_{2/7}} \quad (8)$$

Capacitor C5 for channel A and C8 for channel B provide the option to filter noise introduced from the reference voltage, REFA/B. Equation 9 calculates the cutoff frequency of the filter.

$$f_{c_REF} = \frac{1}{2\times\pi\times C_{5/8}\times R_{4/9}\,//\,R_{5/10}} \quad (9)$$

Figure 12 displays the PCB layout of the top layer of the inverting amplifier circuit configuration.

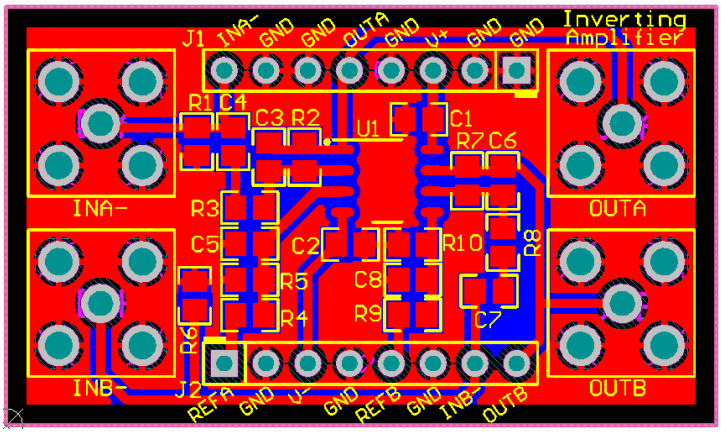


Figure 12. Inverting Amplifier Top Layer PCB Layout

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3.4 Difference Amplifier With Reference Buffer

Figure 13 shows the schematic for the difference amplifier with reference buffer circuit configuration.

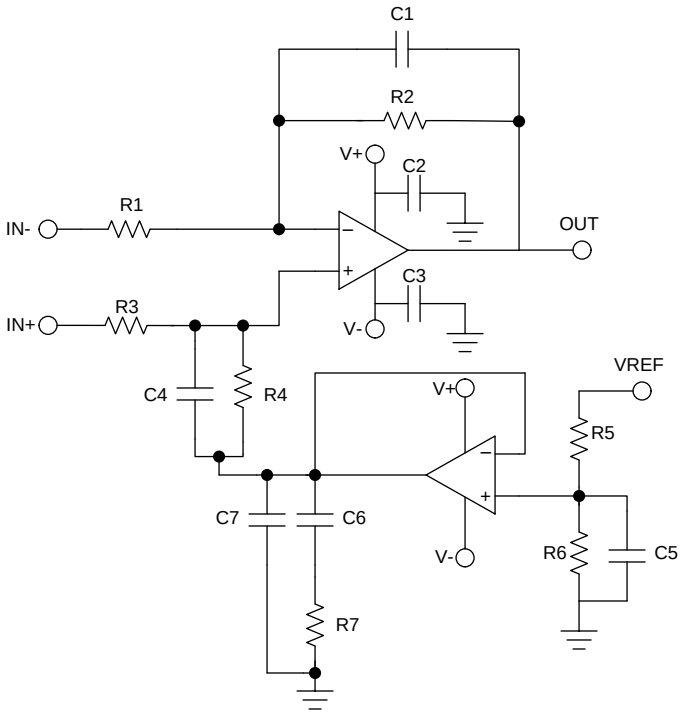


Figure 13. Difference Amplifier with Reference Buffer Schematic

The difference amplifier utilizes both inverting and non-inverting inputs and produces an output that is dependent on the difference between the inputs. The gain of the difference amplifier is dependent on the ratio of R2 to R1 (and subsequently R4 to R3). The reference buffer in the circuit buffers the reference voltage to maintain the common mode rejection of the difference amplifier.

Equation 10 displays the transfer function of the difference amplifier with reference buffer circuit configuration.

$$V_{out} = \left(\frac{R_4}{R_3 + R_4}\right)\left(1 + \frac{R_2}{R_1}\right)(IN+) + \left(\frac{R_3}{R_3 + R_4}\right)\left(\frac{R_6}{R_5 + R_6}\right)\left(1 + \frac{R_1}{R_2}\right)Vref - \frac{R_2}{R_1}(IN-) \quad (10)$$

If $R_1 = R_3$ and $R_2 = R_4$, Equation 10 simplifies to Equation 11:

$$V_{out} = \frac{R_2}{R_1}\left(V_{IN+} - V_{IN-}\right) + \left(\frac{R_6}{R_5 + R_6}\right)V_{ref} \quad (11)$$

Capacitors C1 and C4 provide the option to filter the output of the amplifier. Equation 12 calculates the cut-off frequency of the filter.

$$f_c = \frac{1}{2 \times \pi \times R_2 \times C_1} \quad (12)$$

where

- $R_1 = R_3$
- $R_2 = R_4$
- $C_1 = C_4$

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Figure 14 displays the PCB layout of the top layer of the difference amplifier with reference buffer circuit configuration.

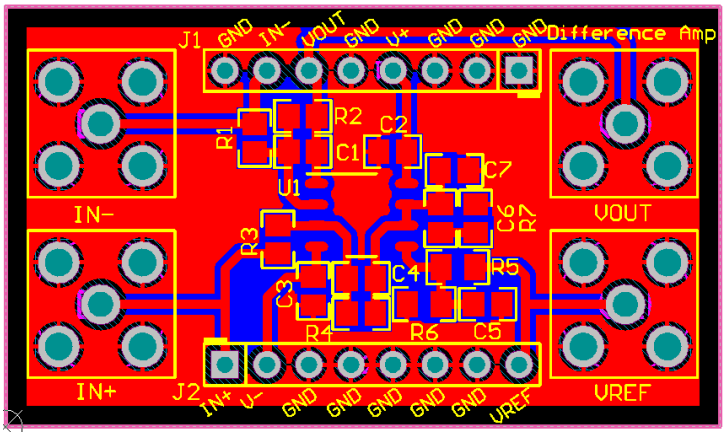


Figure 14. Difference Amplifier with Reference Buffer Top Layer PCB Layout

3.5 Multiple Feedback Active Filter

Figure 15 shows the schematic for the multiple feedback (MFB) active filter circuit configuration.

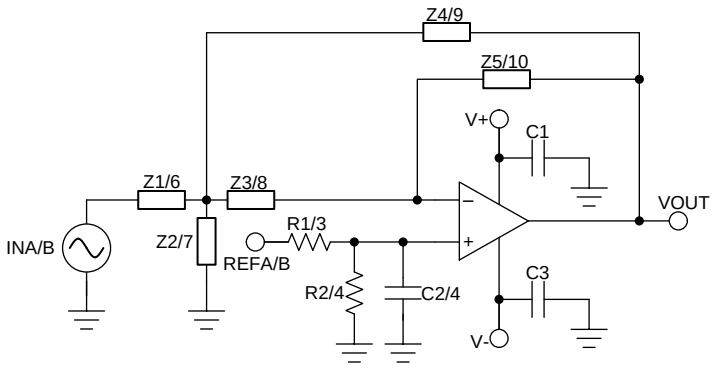


Figure 15. Multiple Feedback Active Filter Schematic

The MFB topology (sometimes called infinite gain or Rauch) is often preferred due to low sensitivity to component variation. The MFB topology creates an inverting second-order stage.

The MFB filter circuit can be configured as a low-pass filter, high-pass filter, or band-pass filter based on the component selection of Z1/6 through Z5/10. Table 3 displays the type of passive component that should be chosen for Z1/6 through Z5/10 for each filter configuration.

Table 3. MFB Filter Type Component Selection

Pass-Band Filter Type	Type of Component (Z1/6)	Type of Component (Z2/7)	Type of Component (Z3/8)	Type of Component (Z4/9)	Type of Component (Z5/10)
Low Pass	R1/6	C2/7	R3/8	R4/9	C5/10
High Pass	C1/6	R2/7	C3/8	C4/9	R5/10
Band Pass	R1/6	R2/7	C3/8	C4/9	R5/10

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For additional guidance in designing a filter, download FilterPro™ active filter design software.

Capacitor C2 for channel A and C4 for channel B provide the option to filter noise that may be introduced from the REFA/B. Equation 13 calculates the cut-off frequency due to C2/4.

$$f_{c_REF} = \frac{1}{2 \times \pi \times C_{2/4} \times R_{1/3} \,//\, R_{2/4}} \tag{13}$$

Figure 16 displays the PCB layout of the top layer of the multiple feedback active filter circuit configuration.

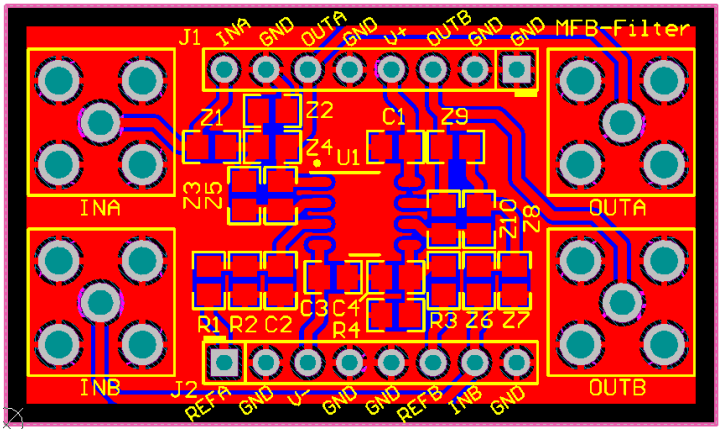


Figure 16. Multiple Feedback Active Filter Top Layer PCB Layout

3.6 Sallen-Key Filter

Figure 17 displays the schematic for the Sallen-Key active filter circuit configuration.

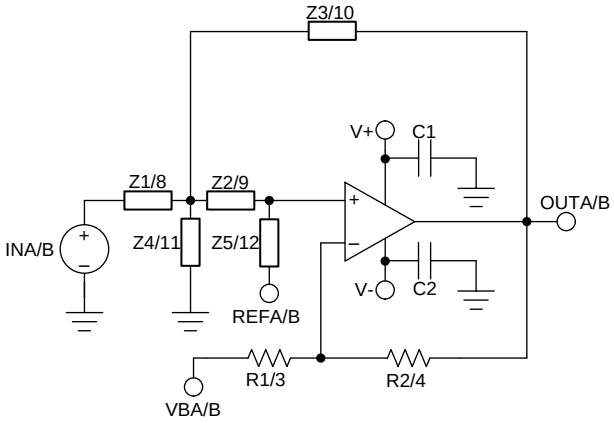


Figure 17. Sallen-Key Active Filter Schematic

The Sallen-Key filter is one of the most commonly applied active filter topologies. The Sallen-Key filter can be configured as a low-pass filter, high-pass filter, or band-pass filter based on the component selection of Z1/8 through Z5/12. Table 4 displays the type of passive components that should be chosen for Z1/8 through Z5/12 for each filter configuration.

Table 4. Sallen-Key Filter Component Type Selection

Pass-Band Filter Type	Type of Component (Z1/8)	Type of Component (Z2/9)	Type of Component (Z3/10)	Type of Component (Z4/11)	Type of Component (Z5/12)
Low Pass	R1/8	R2/9	C3/10	Not Populated	C5/12
High Pass	C1/8	C2/9	R3/10	Not Populated	R5/12
Band Pass	R1/8	C2/9	R3/10	C4/11	R5/12

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For guidance in designing a filter, download the FilterPro™ active filter design software.

Figure 18 displays the PCB layout of the top layer of the multiple feedback active filter circuit configuration.

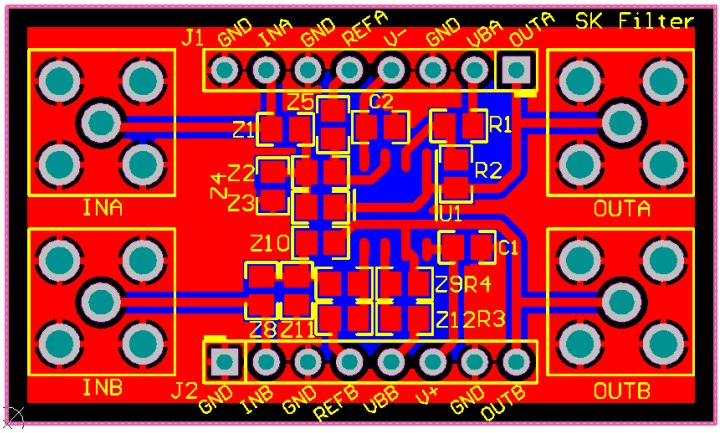


Figure 18. Sallen-Key Active Filter PCB Layout

3.7 Riso With Dual-Feedback

Figure 19 displays the schematic for the Riso with dual-feedback circuit configuration.

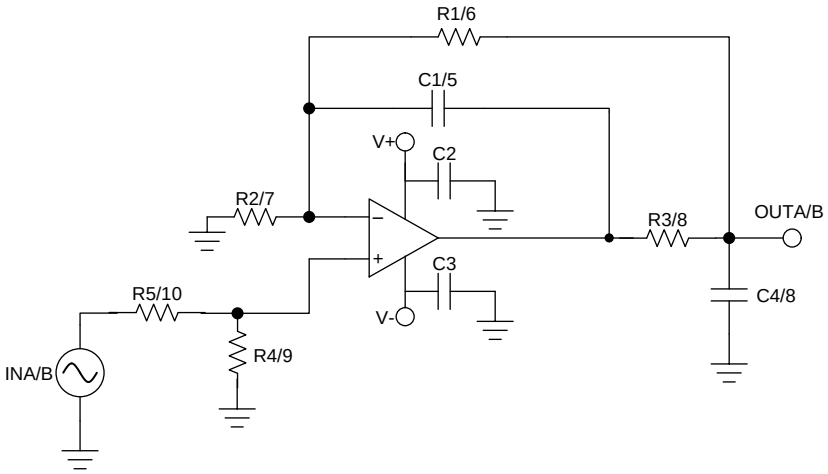


Figure 19. Riso With Dual-Feedback Schematic

Equation 14 calculates the dc gain of the Riso with dual-feedback circuit configuration.

$$OUTA/B = \left(\frac{R_{4/9}}{R_{5/10} + R_{4/9}}\right)\left(1 + \frac{R_{1/6}}{R_{2/7}}\right) INA/B \quad (14)$$

This capacitive load (C4/8) compensation technique uses an isolation resistor (R3/8) to compensate the circuit by adding a zero to cancel the pole from the output impedance and capacitive load. Refer to the *TI Precision Labs - Op Amps: Stability 5* video for detailed information on this technique.

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Figure 20 displays the PCB layout of the top layer of the Riso with dual-feedback circuit configuration.

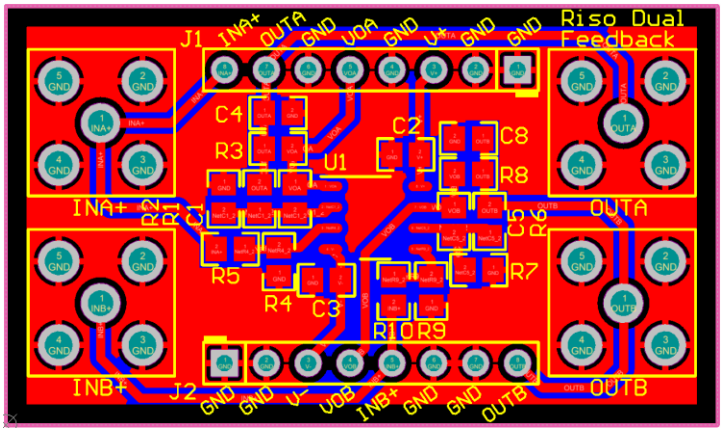


Figure 20. Riso With Dual-Feedback PCB Layout

3.8 Two Op-Amp Instrumentation Amplifier

Figure 21 displays the schematic for the two op-amp instrumentation amplifier circuit configuration.

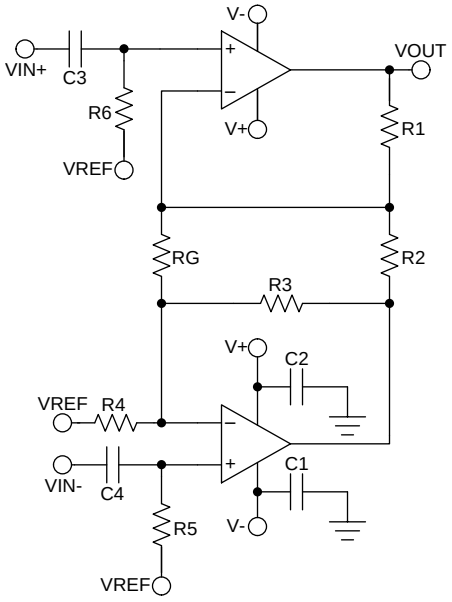


Figure 21. Two Op-Amp Instrumentation Amplifier Schematic

The two op-amp instrumentation amplifier takes a differential input and outputs a single-ended signal. This circuit configuration provides a high-impedance input to sources interfacing with this circuit. While the two op-amp instrumentation amplifier does not provide as high of common mode rejection ration (CMRR) as the three op-amp instrumentation amplifier topology, the two op-amp instrumentation requires only two op amps, thereby reducing cost.

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Equation 15 calculates the transfer function of the two op-amp instrumentation amplifier shown in Figure 21.

$$VOUT = ((VIN+) - (VIN-))\left(1 + \frac{R_1}{R_2} + \frac{2R_1}{R_G}\right) + VREF \quad (15)$$

where

- $R_1 = R_4$
- $R_2 = R_3$

Capacitors C3 and C4 provide the option to ac couple the input. Equation 16 calculates the cut-off frequency of the high-pass filter.

$$f_c = \frac{1}{2 \times \pi \times C_3 \times R_6} \quad (16)$$

where

- $C_3 = C_4$
- $R_6 = R_5$

Figure 22 displays the PCB layout of the top layer of the two op-amp instrumentation amplifier circuit configuration.

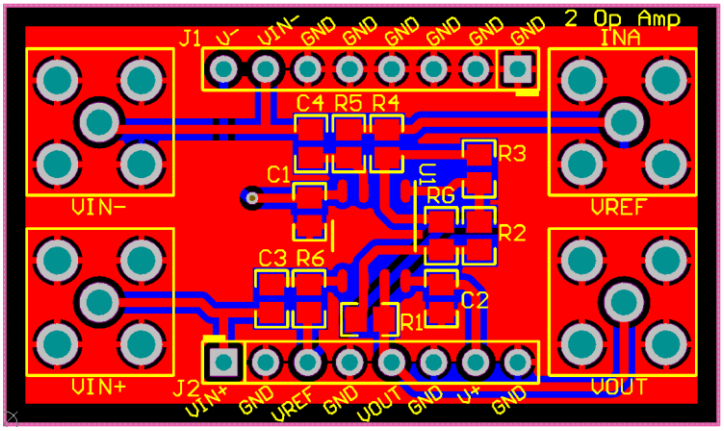


Figure 22. Two Op-Amp Instrumentation Amplifier Top Layer PCB Layout

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3.9 Single-Ended Input to Differential Output

Figure 23 displays the schematic for the single-ended input to differential output circuit configuration.

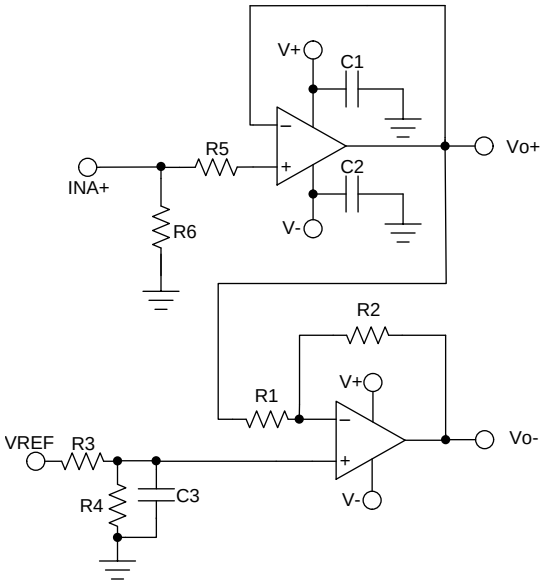


Figure 23. Single-Ended Input to Differential Output Schematic

The single-ended input to differential output circuit is used to convert a single-ended input to a differential output.

Equation 17 displays the transfer function of the single-ended input to differential output circuit configuration.

$$V_{OUT} = (V_o +) - (V_o -) = \left(1 + \frac{R_2}{R_1}\right)(INA +) + \left(\frac{R_4}{R_3 + R_4}\right)\left(1 + \frac{R_2}{R_1}\right)VREF \quad (17)$$

Capacitor C3 provides the option to filter noise introduced from the reference voltage (VREF). Equation 18 calculates the cut-off frequency of the filter.

$$f_c = \frac{1}{2 \times \pi \times C_3 \times R_3 \,/\, /R_4} \quad (18)$$

Figure 24 displays the PCB layout of the top layer of the single-ended input to differential output circuit configuration.

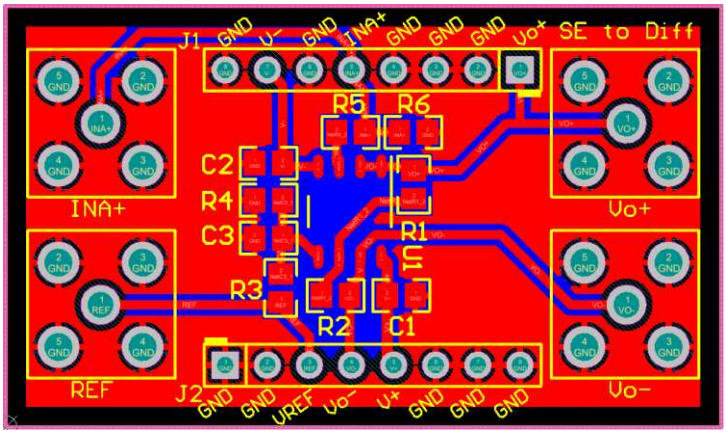


Figure 24. Single-Ended Input to Differential Output Top Layer PCB Layout

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3.10 Parallel Op Amps

Figure 25 displays the schematic of the parallel op-amp circuit configuration.

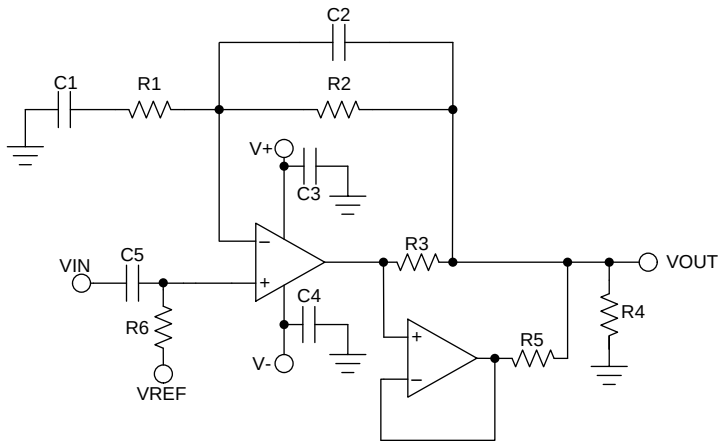


Figure 25. Parallel Op Amp Schematic

Parallel op amps are used to increase the maximum current supplied to a load. Placing two op amps in parallel doubles the maximum current into the load compared to using a single amplifier. This circuit is useful for applications that require driving low impedance loads or applications that require more current supplied into a load than a single op amp can typically supply.

There are multiple ways to configure the non-inverting amplifier circuit configuration. The following cases show the two primary use-case configurations for this circuit.

Case 1: Standard non-inverting configuration

This circuit can be configured into a standard non-inverting circuit by shorting C1 and C5 with a 0-Ω resistor and leaving R6 unpopulated.

Equation 19 displays the transfer function of the non-inverting amplifier circuit configuration shown in Figure 25.

$$VOUT = \left(1 + \frac{R_2}{R_1}\right) VIN \tag{19}$$

where

- C_1 is shorted with a 0-Ω resistor
- C_5 is shorted with a 0-Ω resistor
- R_6 is unpopulated

Capacitor C2 provides the option to filter the output. Equation 20 calculates the cut-off frequency of the filter.

$$f_c = \frac{1}{2 \times \pi \times R_2 \times C_2} \tag{20}$$

Case 2: AC-coupled non-inverting amplifier configuration

This circuit can be configured into an ac-coupled, non-inverting circuit by populating C1 and C5 with capacitors and R6 with a resistor. Test point VREF is used to set the dc biasing of the circuit. The dc biasing is typically set to one half of the supply voltage of the amplifier.

Populating C5 ac couples the input of the circuit. Equation 21 calculates the corner frequency of the high-pass filter created by C5 and R6.

$$f_c = \frac{1}{2 \times \pi \times R_6 \times C_5} \tag{21}$$

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Similarly, capacitor C1 creates a high-pass filter with R1. Equation 22 calculates the corner frequency of the high-pass filter created by C1 and R1.

$$f_c = \frac{1}{2 \times \pi \times R_1 \times C_1} \quad (22)$$

Figure 26 displays the PCB layout of the top layer of the parallel op amp circuit configuration.

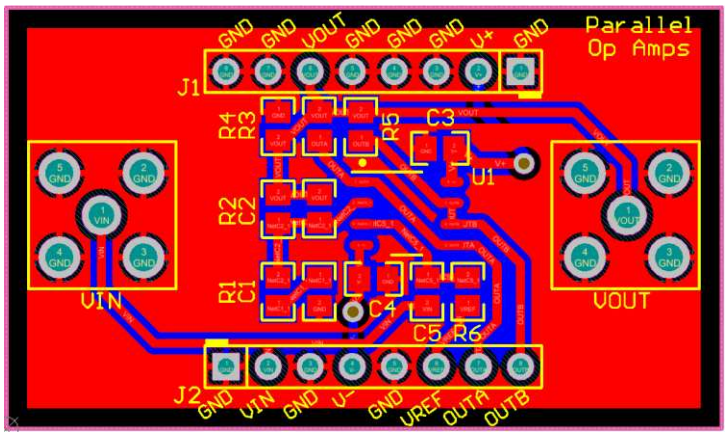


Figure 26. Parallel Op-Amp Top Layer PCB Layout

3.11 Differential Input to Differential Output

Figure 27 displays the schematic for the differential input to differential output circuit configuration.

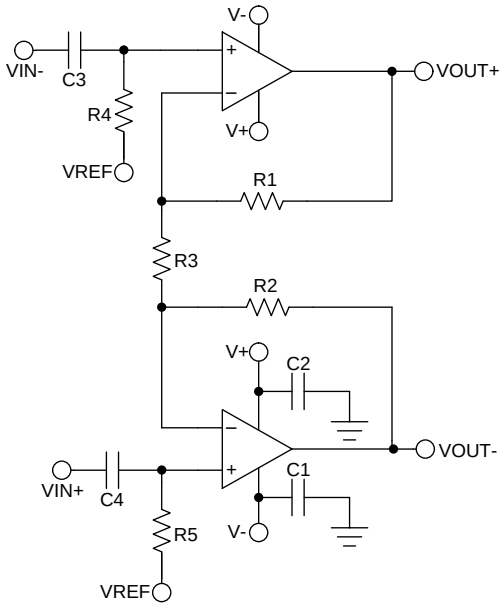


Figure 27. Differential Input to Differential Output Schematic

The differential input to differential output circuit configuration is used to condition a differential signal, such as gain or attenuation, and still maintain the signal as differential.

Equation 23 calculates the transfer function of the differential input to differential output circuit configuration shown in Figure 27.

$$VOUT = ((VOUT+) - (VOUT-)) = ((VIN+) - (VIN-)) \left(1 + \frac{R_1 + R_2}{R_3}\right) \quad (23)$$

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Capacitors C3 and C4 provide the option to ac couple the input to the circuit. Equation 24 calculates the corner frequency of the high-pass filter created by C3 and R4 and C4 and R5.

$$f_c = \frac{1}{2 \times \pi \times R_4 \times C_3} \quad (24)$$

where

- $C_3 = C_4$
- $R_4 = R_5$

Test point VREF is used to set the dc biasing of the circuit which is typically set to one half of the supply voltage.

Figure 28 displays the PCB layout of the top layer of the differential input to differential output circuit configuration.

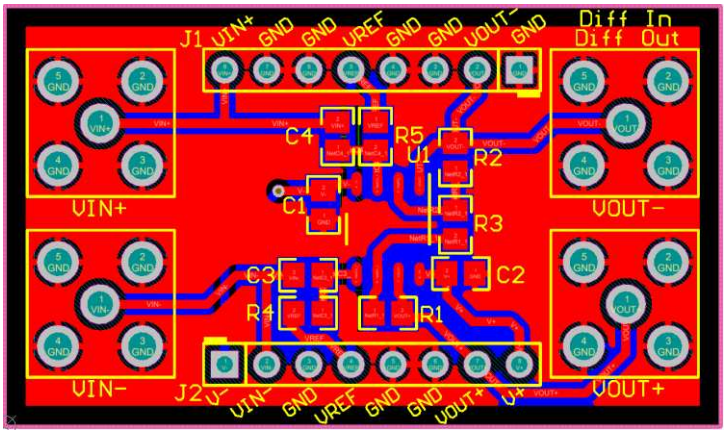


Figure 28. Differential Input to Differential Output Top Layer PCB Layout

4 Connections

This section provides a description for each connection available on the EVM.

4.1 Inputs and Outputs

The input and output connection slots were designed to fit the following connections: vertical SMA, horizontal SMA, wires, or through-hole test points. Examples of these four connectors are shown in this section.

The SMA recommended for this board is TE Connectivity part number 5-1814400-1. Figure 29 shows SMA vertical connectors attached to both the input and output terminal.

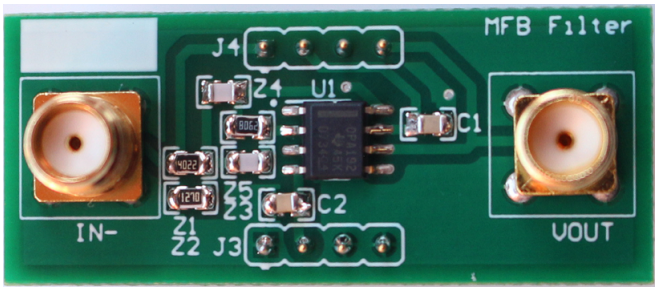


Figure 29. SMA Vertical Connectors

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Figure 30 shows SMA horizontal connectors attached to the input signal terminal.

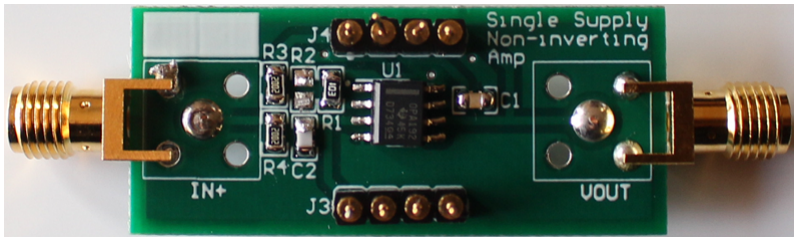


Figure 30. SMA Horizontal Connectors

Figure 31 shows a wire attached to the input and output terminal.

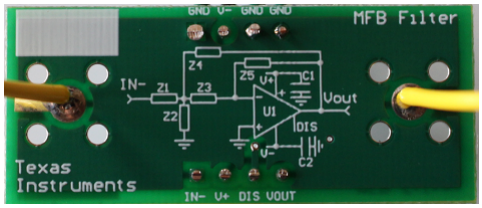


Figure 31. Wire Connections

Figure 32 shows a through-hole test point connector attached to the output and Vref terminal.

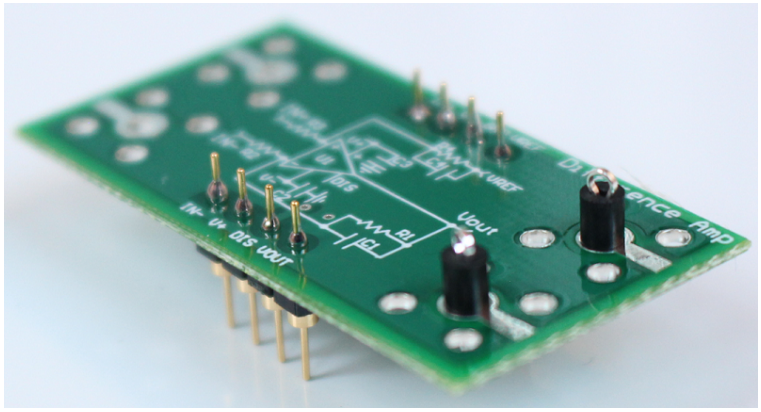


Figure 32. Through-Hole Test Points

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The input and output connections can also be accessed from the header strip. The input connections for channel A and channel B are labeled INA and INB, respectively. The output connections for channel A and channel B are labeled OUTA and OUTB, respectively. An example highlighting the input and output is shown in Figure 33.

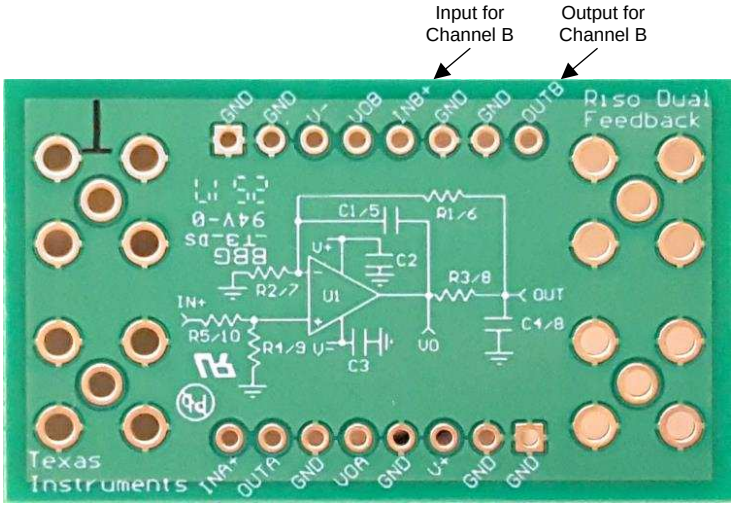


Figure 33. Input and Output Labeled as INA, INB and OUTA and OUTB

Depending on the circuit, only one input and output may be available. In that case the input and output is labeled Vin and Vout, respectively.

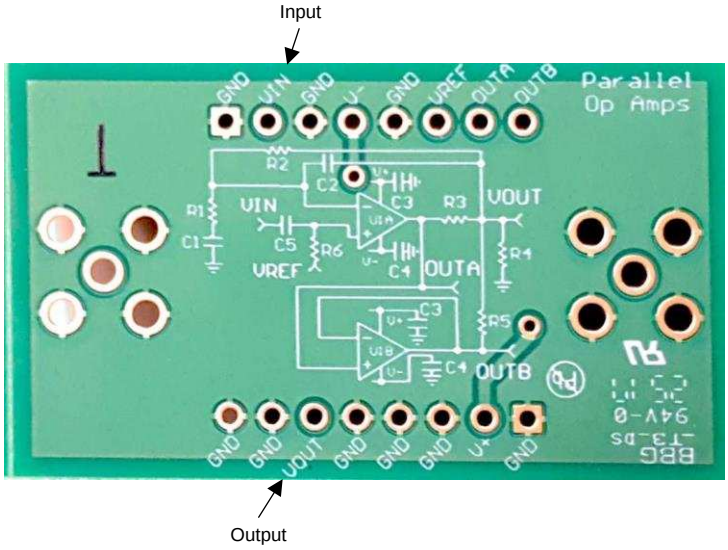


Figure 34. Input and Output Labeled as Vin and Vout

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4.2 Power

Power can only be applied using the header pins located at the top and bottom of the PCB. The positive power supply is labeled V+, the negative power supply is labeled V-, and ground is labeled GND. As an alternative, wires can be used in place of the header strips to power the board directly. Figure 35 shows an all-wire assembly.

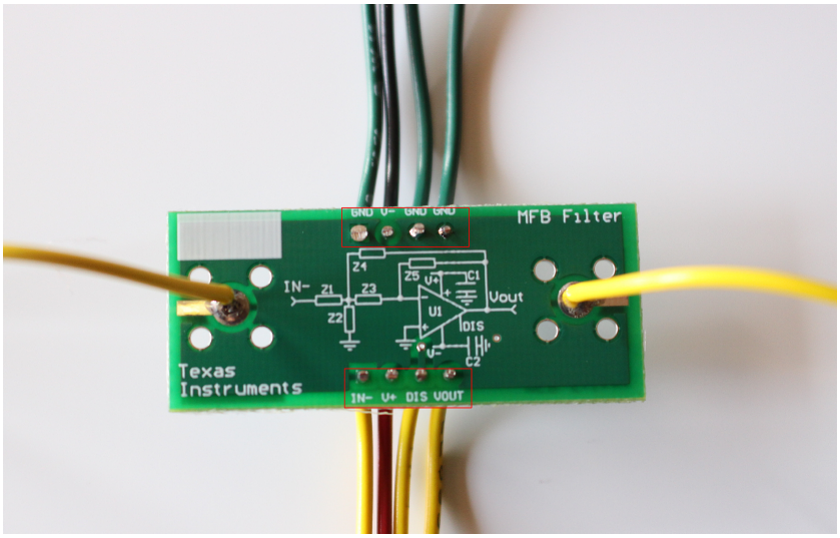


Figure 35. Wire Alternative for Terminal Area

5 Bill of Materials and References

This section lists the bill of materials and reference documents.

5.1 Bill of Materials

Table 5 displays the EVM bill of materials.

Table 5. DUAL-DIYAMP-EVM Bill of Materials

Designator	Qty	Description	Part Number	Manufacturer
PCB	1	Printed-circuit board	AMPS012	Any
J1, J2	2	Header, 2.54 mm, 32x1, Gold, TH	TS-132-G-AA	Samtec

5.2 References

The following reference documents are available on www.ti.com:

1. *Comparator with Hysteresis Reference Design* (TIDU020)
2. TI Precision Labs Training https://training.ti.com/ti-precision-labs-op-amps
3. *Analysis of the Sallen-Key Architecture*(SLOA024)
4. *AC Coupled, Single-Supply, Inverting and Non-inverting Amplifier Reference Design* (TIDU871)
5. FilterPro Design Tool

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      FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

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      CAUTION

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FCC Interference Statement for Class B EVM devices

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- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

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Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

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2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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