DSPI_FIFO

Serial Peripheral Interface
Master/Slave with FIFO
ver 1.07

OVERVIEW

The DSPI_FIFO is a fully configurable SPI master/slave device, which allows user to configure polarity and phase of serial clock signal SCK.

The DSPI_FIFO allows the microcontroller to communicate with serial peripheral devices. It is also capable of interprocessor communications in a multi-master system. A serial clock line (SCK) synchronizes shifting and sampling of the information on the two independent serial data lines. DSPI_FIFO data are simultaneously transmitted and received.

The DSPI_FIFO is a technology independent design that can be implemented in a variety of process technologies.

The DSPI_FIFO system is flexible enough to interface directly with numerous standard product peripherals from several manufacturers. The system can be configured as a master or a slave device. Data rates as high as CLK/8. Clock control logic allows a selection of clock polarity and a choice of two fundamentally different clocking protocols to accommodate most available synchronous serial peripheral devices. When the SPI is configured as a master, software selects one of eight different bit rates for the serial clock.

The DSPI_FIFO automatically drive selected by SSCR (Slave Select Control Register) slave select outputs (SS7O – SS0O), and address SPI slave device to exchange serially shifted data. Error-detection logic is included to support interprocessor communications. A write-collision detector indicates when an attempt is made to write data to the serial shift register while a transfer is in progress. A multiple-master mode-fault detector automatically disables DSPI_FIFO output drivers if more than one SPI devices simultaneously attempts to become bus master.

The DSPI_FIFO supports two DMA modes: single transfer and multi-transfer. These modes allow DSPI_FIFO to interface to higher performance DMA units, which can interleave their transfers between CPU cycles or execute multiple byte transfers.

DSPI_FIFO is **fully customizable**, which means it is delivered in the exact configuration to meet users' requirements. *There is no need to pay extra for not used features and wasted silicon.* It includes **fully automated testbench** with **complete set of tests** allowing easy package validation at each stage of SoC design flow.

APPLICATIONS

- Embedded microprocessor boards
- Consumer and professional audio/video
- Home and automotive radio
- Digital multimeters

All trademarks mentioned in this document
are trademarks of their respective owners.

http://www.DigitalCoreDesign.com
http://www.dcd.pl

Copyright 1999-2007 DCD – Digital Core Design. All Rights Reserved.

KEY FEATURES

- SPI Master
  - *Master and Multi-master operations*
  - *Two modes of operation: SPI mode and FIFO mode*
  - *8 SPI slave select lines*
  - *System error detection*
    - *Mode fault error*
    - *Write collision error*
  - *Interrupt generation*
  - *Supports speeds up 1/8 of system clock*
  - *Bit rates generated 1/8 - 1/1024 of system clock.*
  - *Four transfer formats supported*
  - *Simple interface allows easy connection to microcontrollers*
- SPI Slave
  - *Slave operation*
  - *Two modes of operation: SPI mode and FIFO mode*
  - *System error detection*
  - *Interrupt generation*
  - *Supports speeds up ¼ of system clock*
  - *Simple interface allows easy connection to microcontrollers*
  - *Four transfer formats supported*
- Two DMA Modes allows single and multi-transfer
- In the FIFO mode transmitter and receiver are each buffered with 16/64 byte FIFO's to reduce the number of interrupts presented to the CPU
- **Optional** FIFO size extension to **128, 256 or 512 Bytes**
- Fully synthesizable, static synchronous design with no internal tri-states

CONFIGURATION

The following parameters of the DSPI_FIFO core can be easy adjusted to requirements of dedicated application and technology. Configuration of the core can be prepared by effortless changing appropriate constants in package file. There is no need to change any parts of the code.

• FIFO Control logic	-	enable - disable
• FIFO size	-	standard 16/64 - large up to 512
• SLAVE SELECT SETUP TIME	-	Number of CLK periods of SSO low before SPI starts transmission
• SLAVE SELECT HIGH TIME	-	Number of CLK periods of SSO High between two consecutive master transmissions.
• SLAVE SELECT HOLD TIME	-	Number of CLK periods of SSO low after end of SPI master transmission

DELIVERABLES

- Source code:
  - ◊ VHDL Source Code or/and
  - ◊ VERILOG Source Code or/and
  - ◊ Encrypted, or plain text EDIF netlist
- VHDL & VERILOG test bench environment
  - ◊ Active-HDL automatic simulation macros
  - ◊ ModelSim automatic simulation macros
  - ◊ Tests with reference responses
- Technical documentation
  - ◊ Installation notes
  - ◊ HDL core specification
  - ◊ Datasheet
- Synthesis scripts
- Example application
- Technical support
  - ◊ IP Core implementation support
  - ◊ 3 months maintenance
    - Delivery the IP Core updates, minor and major versions changes
    - Delivery the documentation updates
    - Phone & email support

All trademarks mentioned in this document
are trademarks of their respective owners.

Copyright 1999-2007 DCD – Digital Core Design. All Rights Reserved.

LICENSING

Comprehensible and clearly defined licensing methods without royalty fees make using of IP Core easy and simply.

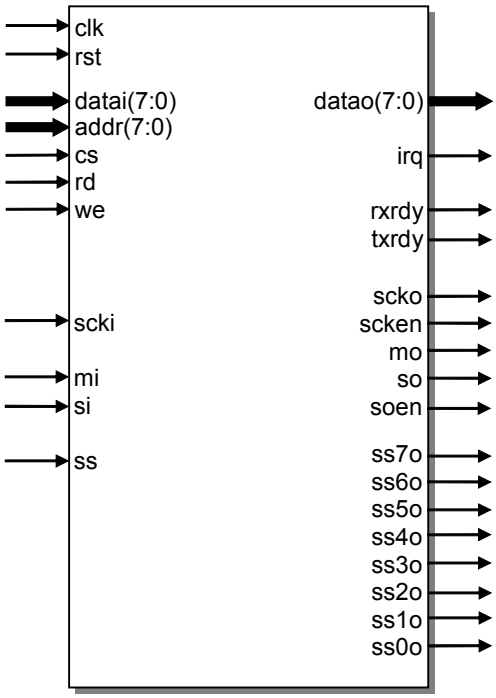
Single Design license allows use IP Core in single FPGA bitstream and ASIC implementation.

Unlimited Designs, *One Year* licenses allow use IP Core in unlimited number of FPGA bitstreams and ASIC implementations.

In all cases number of IP Core instantiations within a design, and number of manufactured chips are unlimited. There is no time restriction except *One Year* license where time of use is limited to 12 months.

- Single Design license for
  - *VHDL, Verilog source code called HDL Source*
  - *Encrypted, or plain text EDIF called Netlist*
- One Year license for
  - *Encrypted Netlist only*
- Unlimited Designs license for
  - *HDL Source*
  - *Netlist*
- Upgrade from
  - *HDL Source to Netlist*
  - *Single Design to Unlimited Designs*

SYMBOL



PINS DESCRIPTION

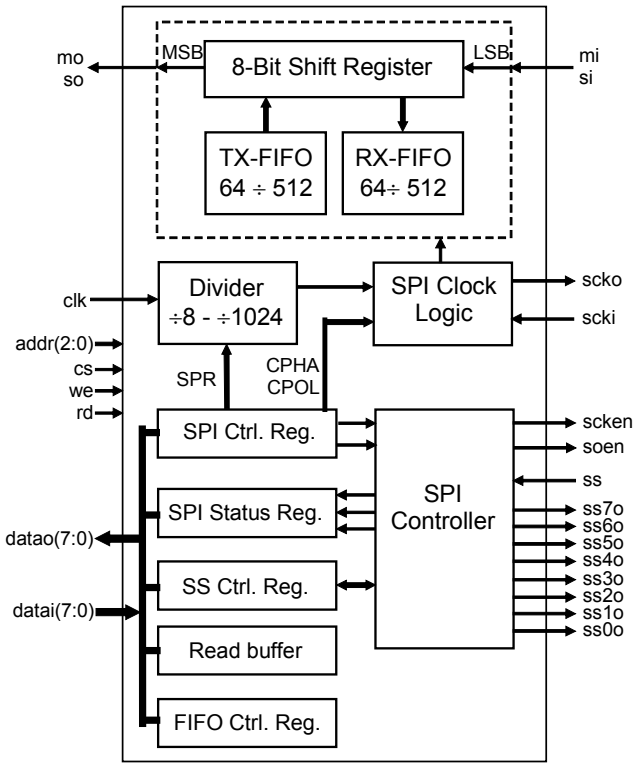
PIN	TYPE	DESCRIPTION
clk	input	Global clock
rst	input	Global reset
datai(7:0)	input	Data bus input
addr(1:0)	input	Processor address lines
cs	input	Chip select
rd	input	Processor read strobe
we	input	Processor write strobe
scki	input	SPI clock input
mi	input	Master serial data input
si	input	Slave serial data input
ss	input	Slave select
datao(7:0)	output	Data bus output
irq	output	Interrupt request
txrdy	output	Transmitter ready output
rxrdy	output	Receiver ready output
scko	output	SPI clock output
scken	output	SPI clock output enable
mo	output	Master serial data output
so	output	Slave serial data output
soen	output	Slave output enable
ss7o-ss0o	output	Slave select outputs

All trademarks mentioned in this document are trademarks of their respective owners.

Copyright 1999-2007 DCD – Digital Core Design. All Rights Reserved.

BLOCK DIAGRAM

Shift register and Read Data Buffer – it is a central element in the SPI system. The system is single buffered in the transmit direction and double buffered in the receive direction. This fact means new data for transmission cannot be written to the shifter until the previous transaction is complete; however, received data is transferred into a parallel read data buffer so the shifter is free to accept a second serial character. As long as the first character is read out of the read data buffer before the next serial character is ready to be transferred, no overrun condition will occur. When an SPI transfer occurs, an 8-bit character is shifted out on data pin while a different 8-bit character is simultaneously shifted in a second data pin. Another way to view this transfer is that an 8-bit shift register in the master and another 8-bit shift register in the slave are connected as a circular 16-bit shift register. When a transfer occurs, this distributed shift register is shifted eight bit positions; thus, the characters in the master and slave are effectively exchanged.



Receiver FIFO - The Rx FIFO can be 64 (128, 256, 512) levels deep, it receives data until the number of bytes in the FIFO equals the selected interrupt trigger level. At that time if interrupt is enabled, the DSPI_FIFO will issue an interrupt to the CPU. The Rx FIFO will continue to store bytes until it is full, and will not accept any next byte. Any more data entering the Rx shift register will set the Overrun Error flag.

Transmitter FIFO - the Tx portion of the DSPI_FIFO transmits data through SO/MO as soon as the CPU loads a byte into the Tx FIFO in Master mode. In Slave mode the transmission is started after correct edge of the SCK signal. The DSPI_FIFO will prevent loads to the Tx FIFO if it currently holds 64 (128, 256, 512) characters (depending on SFCR(5) bit value and selected FIFO size). Loading to the Tx FIFO again will be enabled as soon as the next character is transferred to the Tx shift register. These capabilities account for the largely autonomous operation of the Tx

Control Register may be read or written at any time, is used to configure the DSPI_FIFO System. This register controls the mode of transmission (Master, Slave), polarity and phase of SPI Clock and transmission speed.

Status Register (SPSR) is read only register contains flags indicating the completion of transfer or occurrence of system errors. All flags are set automatically when the corresponding event occur and cleared by software sequence.

Slave Select Control Register configures which slave select output should be driven while SPI master transfer. Contents of SSCR register is automatically assigned on SS7O-SS0O pins when DSPI_FIFO master transmission starts.

SPI Clock Logic - Software can select any of four combinations of serial clock (SCK) phase and polarity using two bits in the SPI control register (SPCR). The clock polarity is specified by the CPOL control bit, which selects an active high or active low clock and has no significant effect on the transfer format. The clock phase (CPHA) control bit selects one of two fundamentally different transfer formats. The clock phase and polarity should be identical for the master SPI device and the communicating slave device. In some cases, the phase and polarity are changed between transfers to allow a master device to communicate with peripheral slaves having different requirements. The flexibility of the SPI system on the

All trademarks mentioned in this document
are trademarks of their respective owners.

Copyright 1999-2007 DCD – Digital Core Design. All Rights Reserved.

DSPI_FIFO allows direct interface to almost any existing synchronous serial peripheral.

SPI Controller manages the Master/Slave operation and controls the transmission. The SPI Controller manages the transmission speed and format (Phase and polarity). Controller is also responsible for generating of interrupt request and detection of transmission errors.

PERFORMANCE

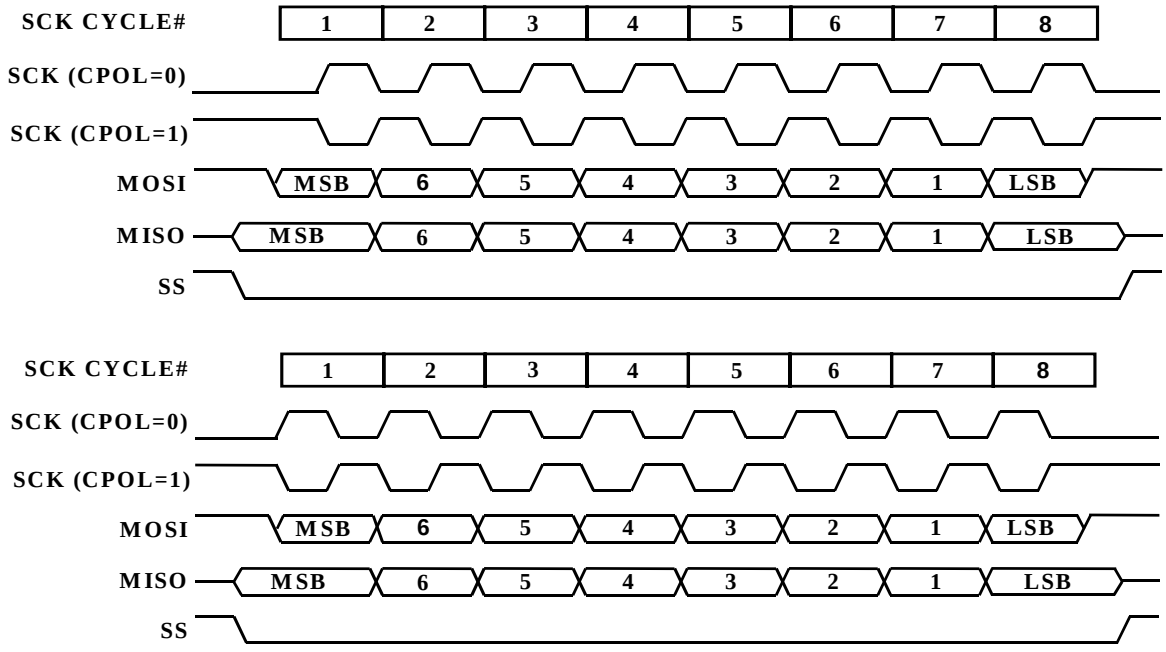
The following table gives a survey about the Core performance in the ALTERA® devices after Place & Route (all key features have been included):

Device	Speed grade	Logic Cells	F_{max}
CYCLONE	-6	324	171 MHz
CYCLONE2	-6	314	197 MHz
STRATIX	-5	324	206 MHz
STRATIX2	-3	273	313 MHz
STRATIXGX	-5	324	210 MHz
APEX2A	-7	370	178 MHz
APEX20KC	-7	369	152 MHz
APEX20KE	-1	369	115 MHz
APEX20K	-1	369	94 MHz
ACEX1K	-1	369	103 MHz
FLEX10KE	-1	369	103 MHz

Core performance in ALTERA® devices

Transfer Formats

Software can select any of four combinations of serial clock (SCK) phase and polarity using two bits in the SPI control register (SPCR). The clock polarity is specified by the CPOL control bit, which selects an active high or active low clock and has no significant effect on the transfer format. The clock phase (CPHA) control bit selects one of two fundamentally different transfer formats. The clock phase and polarity should be identical for the master SPI device and the communicating slave device. In some cases, the phase and polarity are changed between transfers to allow a master device to communicate with peripheral slaves having different requirements. The flexibility of the SPI system on the DSPI_FIFO allows direct interface to almost any existing synchronous serial peripheral.



All trademarks mentioned in this document are trademarks of their respective owners.

Copyright 1999-2007 DCD – Digital Core Design. All Rights Reserved.

CONTACTS

For any modification or special request please contact to Digital Core Design or local distributors.

Headquarters:

Wroclawska 94

41-902 Bytom, POLAND

e-mail: info@dcd.pl

tel. : +48 32 282 82 66

fax : +48 32 282 74 37

Distributors:

Please check http://www.dcd.pl/apartn.php

All trademarks mentioned in this document are trademarks of their respective owners.

http://www.DigitalCoreDesign.com
http://www.dcd.pl

Copyright 1999-2007 DCD – Digital Core Design. All Rights Reserved.