

General Description

The DSC612RL3A-010K is a two-output low power MEMS clock generator.

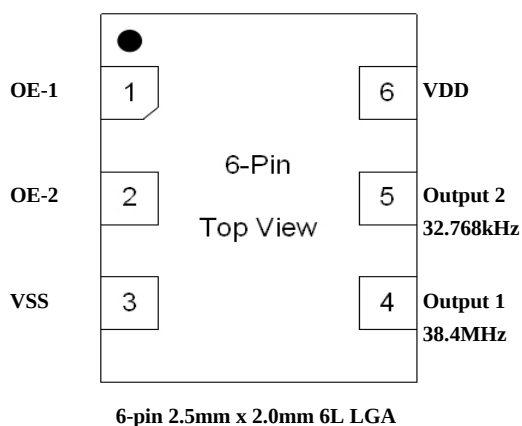
The MEMS based clock generator eliminates the need of external crystal or reference clock.

Refer to [DSC612 master data sheet](#) to read full descriptions.

Features

- Two LVCMOS clock outputs:
38.4MHz, 32.768kHz
- Ultra-small package size: 2.5mm x 2.0mm 6L LGA
- High stability: ± 20 ppm
- Temperature range: -40°C to $+105^{\circ}\text{C}$
- Low power consumption: $\sim 5\text{mA}$ (both outputs active)
- Wide supply voltage range: 1.71V -3.63V VDD
- Excellent shock and vibration immunity
- High reliability
- Lead free and RoHS compliant
- AEC-Q100 automotive grade available

Pin Configuration and Description



Pin Number	Pin Name	Pin Type	Pin Description
1	OE-1	I	Output Enable H = Output Active L = Output Disabled (High Impedance)
2	OE-2	I	Output Enable H = Output Active L = Output Disabled (High Impedance)
3	VSS	Power	Power Supply Ground
4	Output 1	O	38.4MHz LVCMOS Clock Output Controlled by Pin 1 (OE-1)
5	Output 2	O	32.768kHz LVCMOS Clock Output Controlled by Pin 2 (OE-2)
6	VDD	Power	Power Supply

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Ordering Information

Ordering Part Number	Temperature Range	High Stability	Shipping	Package
DSC612RL3A-010K	-40°C to +105°C	±20ppm	Tube	2.5mm x 2.0mm 6L LGA
DSC612RL3A-010KT	-40°C to +105°C	±20ppm	Tape and Reel	2.5mm x 2.0mm 6L LGA

Devices are Green and RoHS compliant. Sample material may have only a partial top mark.

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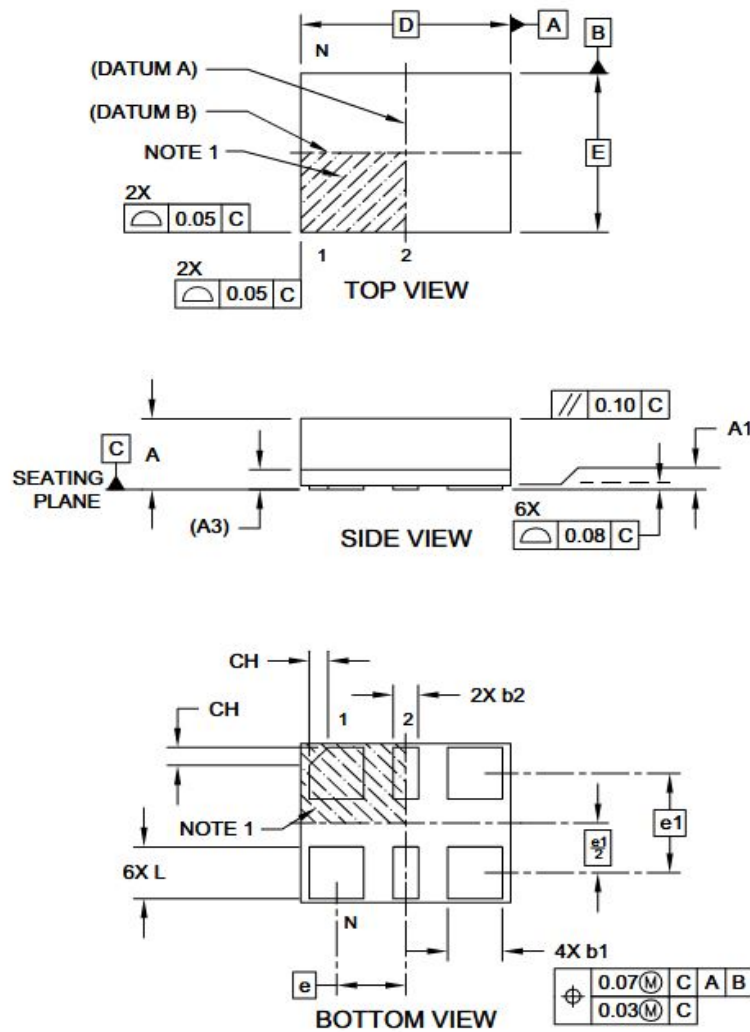
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6-Lead 2.5 mm x 2.0 mm VFLGA Package Outline and Recommended Land Pattern

6-Lead Very Thin Fine Pitch Land Grid Array (AWA) - 2.5x2.0 mm Body [VFLGA]

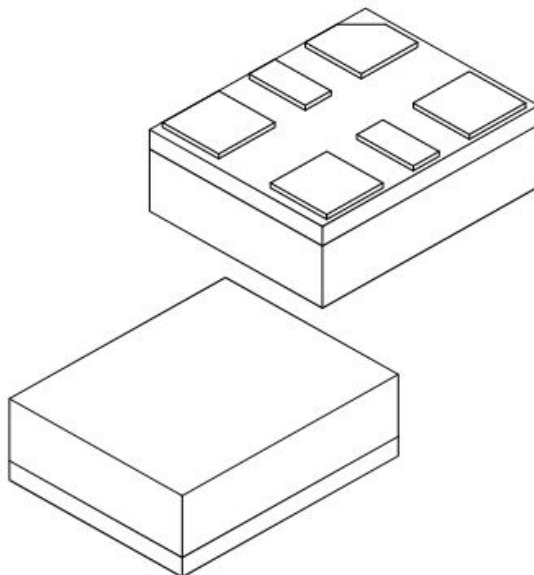
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



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6-Lead Very Thin Fine Pitch Land Grid Array (AWA) - 2.5x2.0 mm Body [VFLGA]

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Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Terminals	N	6		
Terminal Pitch	e	0.825 BSC		
Terminal Pitch	e1	1.25 BSC		
Overall Height	A	0.79	0.84	0.89
Standoff	A1	0.00	0.02	0.05
Substrate Thickness (with Terminals)	A3	0.20 REF		
Overall Length	D	2.50 BSC		
Overall Width	E	2.00 BSC		
Terminal Width	b1	0.60	0.65	0.70
Terminal Width	b2	0.25	0.30	0.35
Terminal Length	L	0.60	0.65	0.70
Terminal 1 Index Chamfer	CH	-	0.225	-

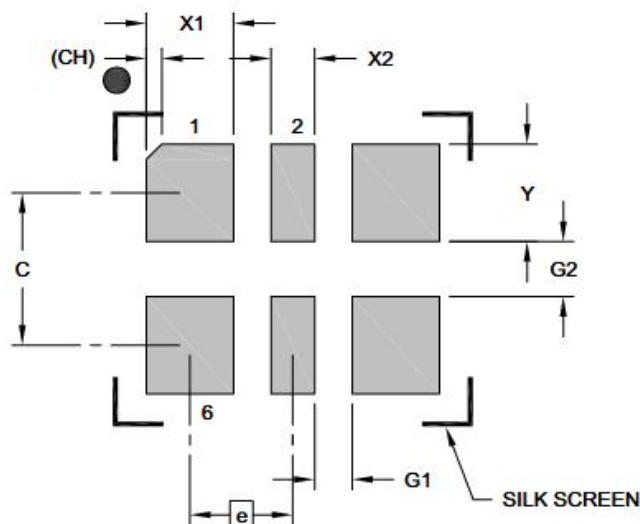
Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

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6-Lead Very Thin Fine Pitch Land Grid Array (AWA) - 2.5x2.0 mm Body [VFLGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

**RECOMMENDED LAND PATTERN**

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E		0.825 BSC	
Contact Spacing	C		1.25 BSC	
Contact Width (X4)	X1			0.70
Contact Width (X2)	X2			0.35
Contact Pad Length (X6)	Y			0.80
Space Between Contacts (X4)	G1	0.30		
Space Between Contacts (X3)	G2	0.45		
Contact 1 Index Chamfer	CH		0.13 X 45° REF	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-3204A